APPENDIX D

2200MVP SIGNAL RUN LIST

Signal	Source DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
$\overline{AB_1}$	REG						D_1		D_1
$\overline{AB_2}$	REG						4_1		5_1
$\overline{AB_3}$	REG						6_1		6_1
$\overline{AB_4}$	REG						E_1		E_1
$\overline{AB_5}$	REG						7_1		F_1
$\overline{AB_6}$	REG						T_3		6_3
$\overline{AB_7}$	REG						16_3		7_3
$\overline{AB_8}$	REG						17_3		8_3
A Bus Ø	REG		S_2			Y_2	B_3		
A Bus 1	REG		14_2			20_2	3_3		
A Bus 2	REG		R_2			X_2	A_3		
A Bus 3	REG		13_2			B_3	2_3		
A Bus 4	REG		P_2			18_2	Z_2		
A Bus 5	REG		M_2			17_2	20_2		
A Bus 6	REG		K_2			U_2	U_2		
A Bus 7	REG		14_1			6_2	D_2		
$\overline{ABS}$	REG						8_1		J_1
ALUCLK	ALU					W_2	W_2		
$\overline{B}$	ST			V_2	U_2				
B Bus Ø			Z_2			L_3	10_3		
B Bus 1			21_2			K_3	K_3		
B Bus 2			20_2			9_3	9_3		
B Bus 3			18_2			J_3	J_3		
B Bus 4			V_2			8_3	8_3		
B Bus 5			U_2			7_3	7_3		
B Bus 6			16_2			5_3	D_3		
B Bus 7			15_2			4_3	4_3		
$\overline{BLK-CA}$	ALU					10_2	10_2		
BRANCH	ALU			9_2		5_2			
CØ	ALU					16_2	16_2		
C1	ALU					S_2	S_2		
C2	ALU					R_2	R_2		
C3	ALU					12_2	12_2		
C4	ALU					11_2	11_2		

Signal	Source DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
C5	ALU					M_2	M_2		
C6	ALU					K_2	K_2		
C7	ALU					H_2	H_2		
CA	ALU					8_2	8_2		
CA Ø	IC	10_2	7_2	6_2					
CA 1	IC	P_2	H_2	H_2					
CA 2	IC	L_2	6_2	5_2					
CA 3	IC	11_2	9_2	7_2					
CA 4	IC	M_2	F_2	F_2					
CA 5	IC	9_2	5_2	4_2					
CA 6	IC	20_2	11_2	12_2					
CA 7	IC	V_2	L_2	M_2					
CA 8	IC	X_2	N_2	P_2					
CA 9	IC	19_2	10_2	11_2					
CA 10	IC	21_2		13_2					
CA 11	IC	W_2		N_2					
C Bus Ø					18_2		17_2		
C Bus 1					15_2		15_2		
C Bus 2					14_2		14_2		
C Bus 3					13_2		13_2		
C Bus 4					P_2		P_2		
C Bus 5					N_2		N_2		
C Bus 6					L_2		L_2		
C Bus 7					J_2		J_2		
$\overline{\text{CBS}}$	REG						20_3		5_3
CDI_{0-23}									
CDO Ø	CM	20_3	L_3		L_3				
CDO 1	CM	19_3	K_3		H_3				
CDO 2	CM	18_3	J_3		F_3				
CDO 3	CM	M_3	E_3		E_3				
CDO 4	CM	L_3	D_3		D_3				
CDO 5	CM	10_3	3_3		C_3				
CDO 6	CM	C_2	E_2		D_2				
CDO 7	CM	B_2	D_2		4_2				
CDO 8	CM	A_2	C_2		B_2				

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
CDO 9	CM		10_1	1_2		A_2				
CDO 10	CM		K_1	A_2		R_1				
CDO 11	CM		J_1	N_1		P_1				
CDO 12	CM		X_3	11_3		16_3				
CDO 13	CM		W_3	7_3		10_3				
CDO 14	CM		V_3	6_3		21_2				
CDO 15	CM		N_3	5_3		20_2				
CDO 16	CM		11_3	4_3				5_3		
CDO 17	CM		K_3	C_3		Y_2		Y_2		
CDO 18	CM		3_2	4_2		E_1		L_1		
CDO 19	CM		2_2	3_2		F_2		F_2		
CDO 20	CM		1_2	2_2		6_2		6_2		
CDO 21	CM		L_1	B_2		E_2		E_2		
CDO 22	CM		9_1	R_1		5_2		5_2		
CDO 23	CM		8_1	13_1				1_2		
$\overline{CE}$	ALU	11_1	U_2				T_2			
CEN	ALU						9_2	9_2		
$\overline{CIO}$	ST					5_1		5_1		
CNTD	IC				10_1	10_1				
$\overline{CPB}$	REG							19_3		4_3
DI Ø	ALU	16_3					16_3			
DI 1	ALU	17_3					17_3			
DI 2	ALU	S_3					R_3			
DI 3	ALU	T_3					S_3			
DI 4	ALU	U_3					19_3			
DI 5	ALU	15_3					15_3			
DI 6	ALU	14_3					14_3			
DI 7	ALU	P_3					P_3			
DI 8	ALU	13_3					13_3			
DI 9	MB	13_1					16_3			
DI 10	MB	P_1					17_3			
DI 11	MB	12_1					R_3			
DI 12	MB	6_1					S_3			
DI 13	MB	5_1					19_3			

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
DI 14	MB	E_1					15_3			
DI 15	MB	F_1					14_3			
DI 16	MB	4_1					P_3			
DI 17	MB	D_1					13_3			
$\overline{\text{DMPI}}$	REG				2_2			2_2		
DMS 1	ST	10_3				20_3				
DMS 2	ST	10_3				X_3				
DO Ø	DM	19_3		T_3						
DO 1	DM	20_3		U_3						
DO 2	DM	V_3		17_3						
DO 3	DM	W_3		18_3						
DO 4	DM	18_3		S_3						
DO 5	DM	X_3		19_3						
DO 6	DM	11_3		9_3						
DO 7	DM	M_3		H_3						
DO 8	DM	12_3		10_3						
DO 9	DM	M_1		11_1						
DO 10	DM	L_1		10_1						
DO 11	DM	10_1		L_1						
DO 12	DM	H_1		7_1						
DO 13	DM	8_1		J_1						
DO 14	DM	J_1		8_1						
DO 15	DM	K_1		9_1						
DO 16	DM	7_1		H_1						
DO 17	DM	9_1		K_1						
$\overline{\text{HALT}}$	I/O							K_1		K_1
$\overline{\text{IB 1}}$	I/O							P_1		15_1
$\overline{\text{IB 2}}$	I/O							B_2		S_1
$\overline{\text{IB 3}}$	I/O							4_2		14_1
$\overline{\text{IB 4}}$	I/O							12_1		R_1
$\overline{\text{IB 5}}$	I/O							C_2		N_1
$\overline{\text{IB 6}}$	I/O							11_1		P_1
$\overline{\text{IB 7}}$	I/O							A_2		L_1
$\overline{\text{IB 8}}$	I/O							M_1		M_1
$\overline{\text{IB 9}}$	I/O							10_1		2_3

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
$\overline{\text{IBS}}$	I/O							F_3		1_3
ICC Ø	IC				14_3	14_3				
ICC 1	IC				15_3	15_3				
ICC 2	IC				13_3	13_3				
ICC 3	IC				B_3	A_3				
ICC 4	IC				R_3	R_3				
ICC 5	IC				P_3	P_3				
ICC 6	IC				N_3	N_3				
ICC 7	IC				12_3	12_3				
ICC 8	IC				K_3	K_3				
ICC 9	IC				9_3	9_3				
ICC 10	IC				J_3	J_3				
ICC 11	IC				8_3	8_3				
ICC 12	IC				5_3	5_3				
ICC 13	IC				4_3	4_3				
ICC 14	IC				3_3	3_3				
ICC 15	IC				2_3	2_3				
I/O CLK	ALU						11_3			L_3
$\overline{\text{LHPC}}$	IC				11_1	11_1				
$\overline{\text{LLPC}}$	IC				M_1	M_1				
LOP	ST			T_2	U_2	T_2		T_2		
$\overline{\text{LPI}}$	ST				9_1	9_1	9_1			
$\overline{\text{MARCLK}}$	ALU	R_3		14_3	H_3		F_3			
$\overline{\text{MS 1}}$	IC		18_2		E_2					
$\overline{\text{MS 2}}$	IC		T_2		D_2					
$\overline{\text{MS 3}}$	IC		17_2		C_2					
$\overline{\text{MS 4}}$	IC		18_2		17_2					
$\overline{\text{MS 5}}$	IC		T_2		T_2					
$\overline{\text{MS 6}}$	IC		17_2		16_2					
$\overline{\text{OB1}}$	REG		1_3					6_3		A_3
$\overline{\text{OB2}}$	REG		Z_2					11_3		B_3
$\overline{\text{OB3}}$	REG		R_1					M_3		C_3
$\overline{\text{OB4}}$	REG		12_1					12_3		D_3

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
$\overline{OB5}$	REG		11_1					14_3		J_3
$\overline{OB6}$	REG		6_1					13_3		H_3
$\overline{OB7}$	REG		5_1					P_3		F_3
$\overline{OB8}$	REG		4_1					N_3		E_3
$\overline{OBS}$	REG							H_1		H_1
PCCC	IC				8_1	8_1				
PECM	MC			17_2	18_2	16_2				
PEDM	MC			J_2	3_2			3_2		
PH Ø	ST	9_3	M_1			19_3	20_3			
PH 1	ST	8_3	F_1			22_2	3_3			
PH 2	ST	K_3	E_1			W_3	X_3			
PH 3	ST	J_3	D_1			18_3	E_3			
PH 4	ST	F_3	T_3			W_2	2_3			
PH 5	ST	C_3	S_3			11_2	14_2			
PH 6	ST	5_3	R_3			R_2	Z_2			
PH 7	ST		2_3			M_2	L_2			
PINC	IC				K_1	K_1				
PL Ø	ST		16_3	R_3		T_3	T_3			
PL 1	ST	6_3	15_3			S_2	V_2			
PL 2	ST	D_3	14_3			12_2	15_2			
PL 3	ST	2_3	B_3			9_2	N_2			
PL 4	ST	14_1	A_3			1_2	F_2			
PL 5	ST	A_3	22_2			7_2	J_2			
PL 6	ST	B_3	P_1			10_2	P_2			
PL 7	ST	H_3	N_1			X_2	A_3			
POR	PSR				W_2	V_2		V_2	E_1	
$\overline{PRMS}$	PSR		E_3						B_1	3_3
RØ	MC			P_3			1_3	1_3		
R1	MC			13_3			22_2	22_2		
R2	MC			16_3	16_3		18_3	18_3		
R3	MC			15_3	T_3		V_3	V_3		
R4	MC			Y_2	Z_2		M_3	S_3		
R5	MC			1_3	E_3		N_3	15_3		
R6	MC			22_2	1_3		21_2	21_2		

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
R7	MC			A_3	D_3		C_3	C_3		
R8	MC			2_3	F_3			E_3		
R9	MC			19_2	20_2			18_2		
R10	MC			X_2	Y_2			X_2		
R11	MC			N_3	L_3			L_3		
R12	MC			20_3	18_3					
R13	MC			X_3	19_3					
R14	MC			W_3	W_3		W_3	W_3		
R15	MC			V_3	U_3		U_3	U_3		
R16	MC			F_3	6_3	6_3	6_3			
R17	MC			M_3	10_3					
R18	MC			4_1	4_1		4_1			
R19	MC			12_3			12_3			
R20	MC			5_1	5_1		5_1			
R21	MC			E_1	E_1		E_1			
R22	MC			D_1	D_1		D_1			
RA Ø	IC	E_3			J_2					
RA 1	IC	7_3			K_2					
RA 2	IC	3_3			8_2					
RA 3	IC	R_1			10_2					
RA 4	IC	1_3			14_2					
RA 5	IC	4_3			R_2					
$\overline{R}$/B	I/O							X_3		K_3
$\overline{REF}$	ALU	L_3	Y_2		B_2		B_2			
REFCLK	IC				15_2		13_2			
$\overline{RESET}$	PSR				S_2				D_1	
$\overline{ROMS}$	IC			W_2	X_2		11_1			
$\overline{R}$/W1	MC	N_3		B_3						
$\overline{R}$/W2	MC	N_1		12_2						
$\overline{R}$/W (CM)	IC		K_2		F_1					
SØ	ST				7_3	7_3				
S1	ST				11_3	11_3				
S2	ST				M_3	M_3				
S3	ST				S_3	S_3				

Signal	Source DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
S4	ST			17_3	17_3				
S5	ST			V_3	V_3				
S6	ST			A_3	Z_2				
S7	ST			C_3	B_3				
$\overline{SB}$	ST			19_2	17_2				
SH0	REG					7_2	7_2		
$\overline{SR}$	ST			21_2	19_2	19_2			
$\overline{T1}$	ALU			14_1	14_1	14_1	14_1		
$\overline{T2}$	ALU				12_1	12_1		F_1	
$\overline{T3}$	ALU		P_1	N_2	N_1	N_1	N_1		
$\overline{T4}$	ALU		M_1	P_1	4_1	P_1			
$\overline{T5}$	ALU			1_2		1_2			
$\overline{T6}$	ALU		F_1		F_1	F_1	F_1		
$\overline{T7}$	ALU			12_1		M_1			
$\overline{T8}$	ALU			A_2		A_2			
$\overline{T9}$	ALU	4_2			2_2	2_2			
$\overline{T10}$	ALU				C_2	C_2			
$\overline{T11}$	ALU				3_2	3_2			
$\overline{T12}$	ALU			13_1	13_1	13_1	13_1		
$\overline{T13}$	ALU					4_2			
$\overline{T14}$	ALU					D_2			
$\overline{T15}$	ALU					E_2			
$\overline{T16}$	ALU			R_1		R_1	R_1		
$\overline{TAP}$	ST			H_1	H_1				
$\overline{TCMDR}$	ALU		6_1		J_1	J_1	J_1		
$\overline{TSP}$	ST			7_1	7_1				
XOP	ST		12_1	L_1	L_1				
$\overline{XPA}$	ST			6_1	6_1				

Signal	Source	DM	CM	MC	IC	ST	ALU	REG	PSR	I/O
+5VR1	PSR			2_1				2_1	8_1	2_1
				B_1				B_1	J_1	B_1
				21_3				21_3		14_3
				Y_3				Y_3		R_3
+5VR2	PSR	2_1	2_1		2_1	2_1	2_1		10_1	
		B_1	B_1		B_1	B_1	B_1		L_1	
		21_3	21_3		21_3	21_3	21_3			
		Y_3	Y_3		Y_3	Y_3	Y_3			
-5VR	PSR	3_1	3_1	3_1	3_1	3_1	3_1	3_1	15_1	
		C_1	C_1	C_1	C_1	C_1	C_1	C_1	S_1	
+12VR	PSR	15_1	15_1	15_1	15_1	15_1	15_1	15_1	11_1	15_3
		S_1	S_1	S_1	S_1	S_1	S_1	S_1	M_1	S_3
-12VR	PSR								12_1	12_3
									N_1	N_3
$\pm$0V		1_1	1_1	1_1	1_1	1_1	1_1	1_1	13_1	3_1
		A_1	A_1	A_1	A_1	A_1	A_1	A_1	P_1	C_1
		22_3	22_3	22_3	22_3	22_3	22_3	22_3	14_1	13_3
		Z_3	Z_3	Z_3	Z_3	Z_3	Z_3	Z_3	R_1	P_3
				8_3						