03-0026- 1

Customer Engineering Division

MICROPROCESSOR MANUAL OF MASS STORAGE DEVICES

WANG

Customer Engineering Division

MICROPROCESSOR MANUAL OF MASS STORAGE DEVICES

WANG LABORATORIES, INC.
836 NORTH STREET, TEWKSBURY MASSACHUSETTS 01876 TEL (617) 851-4111 TWX 710 343-6769 TELEX 94-7421

TABLE OF CONTENTS

1. INTRODUCTION

This manual contains technical information concerning the microprocessors of Model 30, 40, 60 and 70 Disk Drives and is to be used as the basic text for future microprocessors. As new microprocessors are designed for new products, addenda to this manual will be published containing the theory of operation of both the software and hardware portions of the new microprocessor.

Presently, October, 1975, the manual consists of Sections 2 and 3. Section 2 is titled the "Model 2270 Microprocessor" and contains descriptions of the basic components of the microprocessor, an explanation of the instruction set (software), a theory of operation (hardware), schematic drawings and a troubleshooting section.

Section 3 contains hardware descriptions of all the boards used in the microprocessors of the 30, 40 and 60 disk drives. This section was written with the assumption that Section 2 has been read.

2. MODEL 2270 MICROPROCESSOR

2.1 MODEL 2270 SIMPLIFIED THEORY OF OPERATION

Being similar to most general purpose microprocessors, a typical Wang Labs' disk microprocessor is comprised of the following elements (Refer to Figure 1):

A Read-Only-Memory (ROM); used to control all disk microprocessor operations.

A Random-Access-Memory (RAM); normally used as a transitional working register.

An Arithmetic/Logic Unit (ALU)

Two general purpose registers: The *A* register, and the *K* register.

Two Status registers; ST_0 and ST_1, actually control indicators which sense and set various disk and disk microprocessor conditions.

The 6718 or 7018 board contains the entire microprocessor logic for the WCS and Model 2270 disks. Figure 1 shows the simplified block diagram for the 6718/7018 board.

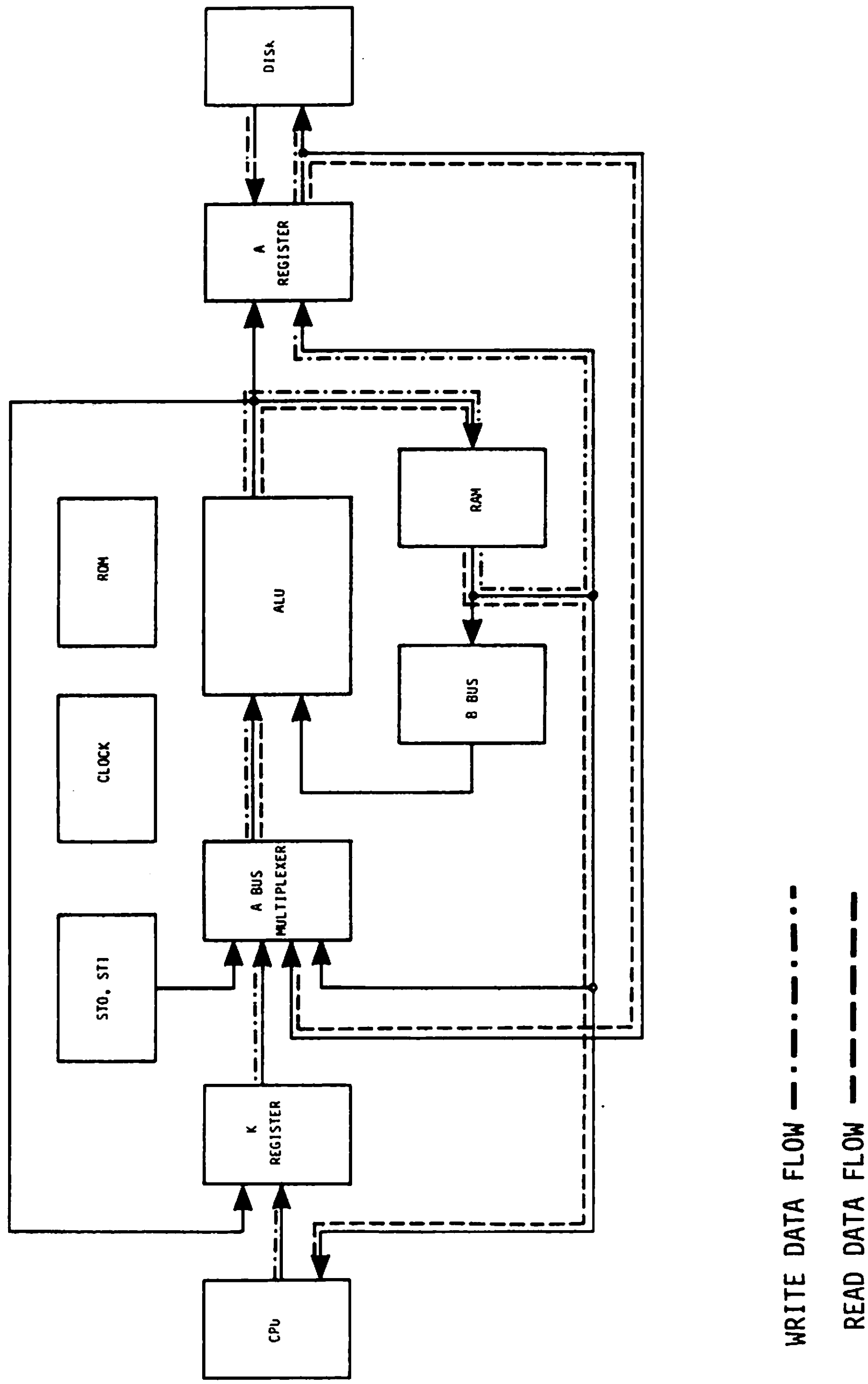


FIGURE 1 SIMPLIFIED BLOCK DIAGRAM

Read/Write Data Flow

When data is written on the disk (refer to Figure 1), data is strobed into the K register from the CPU and clocked into the A bus multiplexer. The output of the multiplexer is applied to the ALU and sent to the RAM. The RAM outputs the data to the A register which sends the data to be written to the disk.

When data is read from the disk, it is applied to the A register, the A bus multiplexer and on to the ALU. The ALU applies the data to the RAM and finally to the CPU.

The extra lines shown in Figure 1 are not used during a read/write sequence but are used for data manipulation and housekeeping functions before, during and after the read/write sequence.

2.1.1 *READ ONLY MEMORY*

The ROM is the heart of the microprocessor and contains the microprogram for the microprocessor. The 6718 utilizes four INTEL 1702A Programmable Read Only Memory (PROM) Integrated Circuits and the 7018 is capable of using four PROMs or two EA4000 ROM Integrated Circuits. Each PROM contains a 256 x 8 bit matrix and the EA a 512 x 8 matrix.

Since a ROM Instruction requires 16 bits, two PROMs are simultaneously selected to provide a 16 bit output. With this configuration, the total ROM capacity is 512 bytes or steps. See Figure 2.

The steps in the ROM are expressed in hexadecimal notation. Steps 0000_{16} to $00FF_{16}$ (0-255) utilize L111 and L113 while steps 0100_{16} to $01FF_{16}$ (256-511) utilize L112 and L114. The ROM is addressed by an instruction counter (IC) which normally increments the ROM one step after an instruction has been decoded and performed. Nine bits are applied to the ROM from the IC; IC_{7-0} provide the addressing and IC_8 and $\overline{IC}_8$ are used for chip select. The IC can cause the ROM to branch from the increment operation to any address by a *branch* instruction.

The 16 bit ROM output, RI_{15} - RI_0, is latched into D-latches and becomes bits R_{15} - R_0.

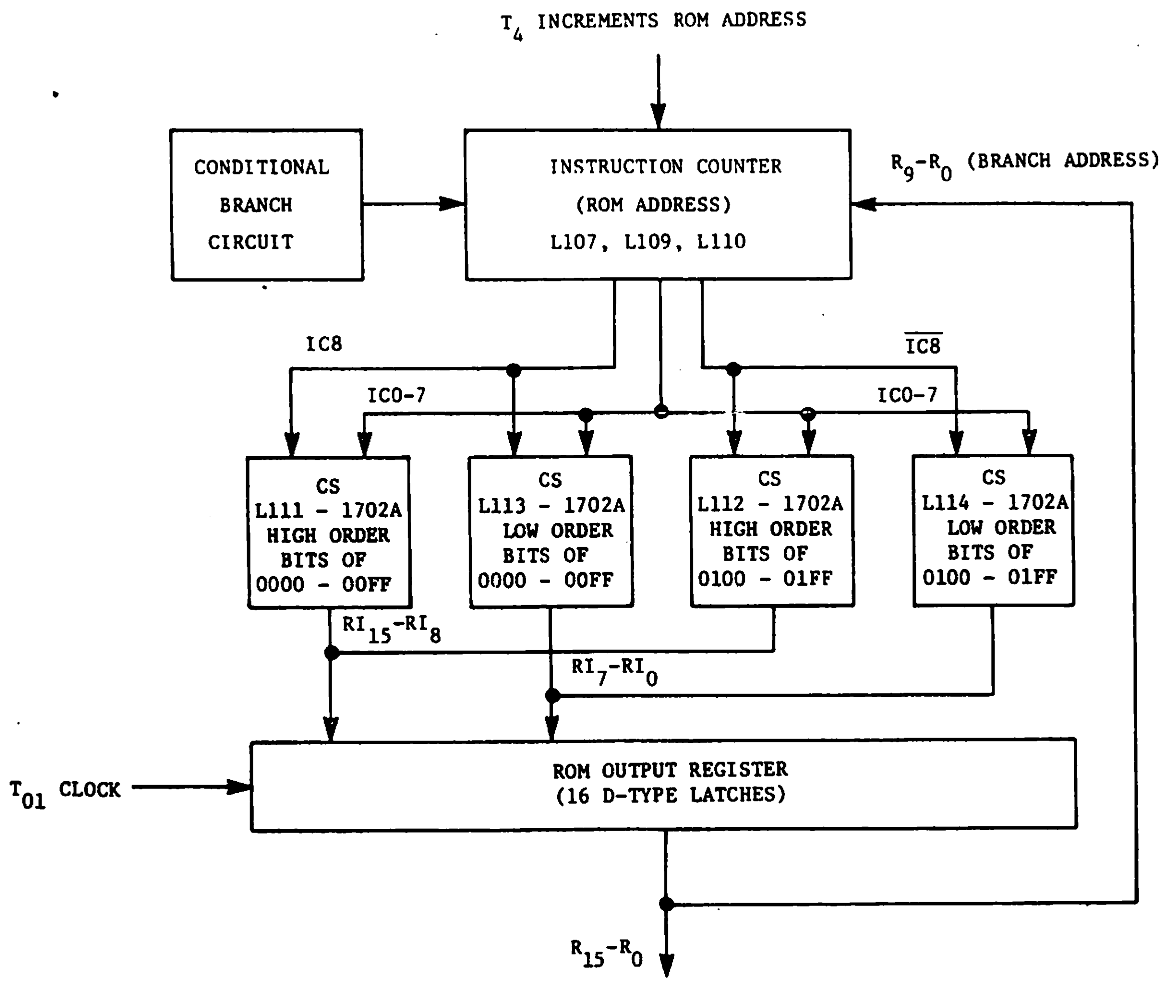


FIGURE 2 READ ONLY MEMORY

2.1.2 *RANDOM ACCESS MEMORY*

The RAM consists of four 2101-1 Integrated Circuits with a capacity of 256 x 4 bits resulting in a total storage capacity of 512 bytes. See Figure 3. The RAM address counter addresses the RAM with AD_8 - AD_0 bits and can increment, decrement or preset the RAM to any address. Information can only be loaded into the RAM from the ALU, C_7 - C_0, but the output can be transferred to the A register, ALU or the CPU. The ROM is divided into two sections: Locations $8C00_{16}$ - $8CFF_{16}$ (these are locations 0-255 - the reason for this notation will be explained later) are used for the read/write buffer and various locations between $8D00_{16}$ - $8DFF_{16}$ (256-511) are used as a work buffer. Refer to the RAM allocation chart below.

RAM ALLOCATION

LOCATION	DESCRIPTION
8C00 - 8CFF	Read/write buffer
8D0F	Zero sent to the 2200
8D10	2200 Address byte #1
8D11	2200 Address byte #2
8D12	2200 Address byte #3
8D20	Header byte #1 (track from disk)
8D21	Header byte #2 (sector from disk)
8D25	Disk track #1 (track currently under head)
8D26	Disk track #2 (track currently under head)
8D27	Disk track #3 (track currently under head)
8D30	Error count
8D31	Internal status
8D32	Address sent to 2200
8D33	Format retries
8DD4 - 8DE7	20 Bytes of zeroes
8DE8	03 Byte
8DE9	Header byte #1 (track desired)
8DEA	Header byte #2 (sector desired)
8DEB - 8DFE	20 Bytes of zeroes
8DFF	03 Byte

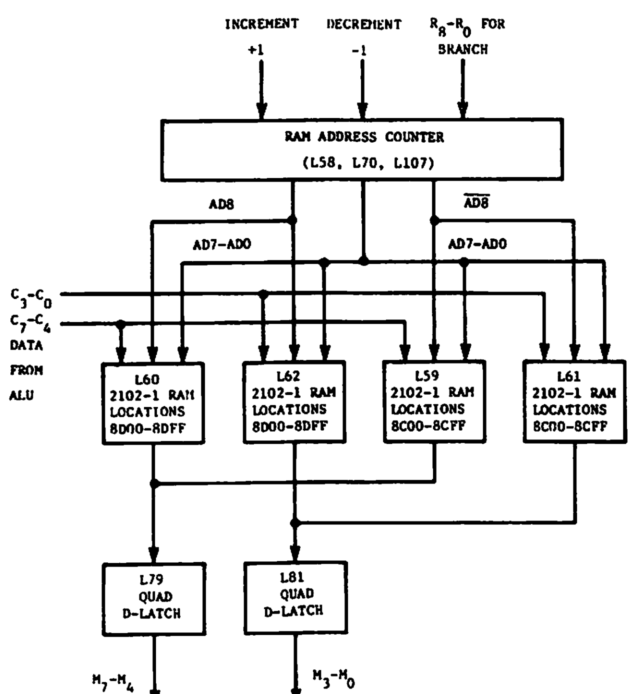


FIGURE 3 RANDOM ACCESS MEMORY

2.1.3 *ARITHMETIC/LOGIC UNIT*

Two 74181 integrated circuits, designed to perform specific arithmetic or logical operations, as directed by the ROM Microinstruction sequence, comprise the ALU.

This ALU responds to sixteen instructions. Basic ALU inputs consist of the A bus, the B bus, a Carry-In bit, and a function select code decoded from the ROM.

The A bus is the output of a multiplexer, incorporating the A register, the K register, and Status registers St_0 or ST_1 as selectable inputs.

The B bus is the output of a two-part register, incorporating the eight low order ROM bits (R_7 - R_0), or the eight bit RAM output (M_7 - M_0).

The ALU output is the C bus (C_7 - C_0); data on this bus can be stored in the A register, K register, RAM, or can be transferred to the status registers ST_0 or ST_1. Again, ALU manipulations are directed by the ROM instruction set.

2.1.4 *REGISTER STRUCTURE*

1) K Register:

The general purpose K register stores data from either the controlling CPU (KS_7 - KS_0), or from the disk microprocessor ALU (C_7 - C_0); i.e., whichever source is selected by the ROM for input to the K register.

When commanded by the ROM, the contents of the K register is transferred to the ALU.

2) A Register:

The general purpose A register stores data from (1) the disk microprocessor RAM (M_7 - M_0), which is data to be written on the disk, (2) the disk data (a READ), (3) the cyclic redundancy check (CRC) circuitry (verifies disk data accuracy), and (4) the ALU (C_7 - C_0). The contents of the A register may be used by the ALU, or may be used as a transitional register for each data byte written on the disk.

3) Status Registers (ST_0, ST_1):

Status register ST_0 reports eight disk/CPU conditions to the disk microprocessor, as follows:

Word Ready ST0-1 (Bit 1) - The 4th bit of a four-bit binary counter, used to indicate when each byte is ready to be transferred from disk to RAM, via the A register and ALU (WRITE). Word Ready is also used to indicate when each byte is ready to be transferred from RAM to disk via the A register.

Address Bit 8 ST0-2 (Bit 2) - The 9th (highest order) RAM address bit; (2^9 = 512 byte addresses).

10 ms Delay ST0-3 (Bit 3) - The output of an integrated circuit (active for 10 ms). This delay is used to allow time for proper disk access.

File Inoperable ST0-4 (Bit 4) - The output of a data safety circuit which indicates when data integrity could be jeopardized by a variety of disk conditions, such as R/W heads not being loaded, drive door open, etc. File Inoperable may be thought of as a Shugart Disk Ready/Not Ready indicator.

CAX ST0-5 (Bit 5) - Made up of IOB terms IOB_1 and IOB_3. CAX distinguishes a select address from a data transfer operation.

Calculator Input Strobe ST0-6 (Bit 6) - A strobe from 2200 to disk microprocessor which must accompany each address or data byte from the 2200 to the K register. This status bit indicates that one byte is ready to be transferred from the K register to RAM via the ALU.

Disk #3 ST0-7 (Bit 7) - A select line which, when active, indicates that selection of disk #3 is desired.

Calculator Busy ST0-8 (Bit 8) - The Ready/Busy indicator from the 2200 CPU I/O controller board.

These bits are sampled by the ALU via the A Bus inputs when ROM bits R_9 and $R_8 = 10_B$ ($R_9 = 1$; $R_8 = 0$).

Status register ST_1 reports five disk/disk microprocessor conditions back to the microprocessor as follows:

Sector Bits 0-3 ST1-1 through 4 (Bits 1, 2, 3, 4) - These bits contain the current sector address under the disk drive read/write head. This address is the output of a binary counter, and is monitored as such.

Sector Mark Pulse ST1-5 (Bit 5) - This bit is ultimately the Sector Mark pulse ($\overline{SCM}$) from the disk. (One pulse for each sector on the disk). It is used to denote the beginning of each sector.

Track ØØ ST1-6 (Bit 6) - A line from the Disk Drive which indicates when the R/W head is positioned at track zero (the outer most track).

Carry ST1-7 (Bit 7) - This is the carry bit for arithmetic operations. It is gated to the ALU for ROM microinstructions specifying carry, and receives that resultant carry.

Head Load ST1-8 (Bit 8) - A signal indicating to the microprocessor that one of the 3 Disk Drive R/W heads have been loaded.

These bits are sampled by the ALU via the B Bus inputs when ROM bits R_9 and $R_8 = 11_2$.

2.2 THE INSTRUCTION SET - HARDWARE CONTROL VIA SOFTWARE

2.2.1 *GENERAL*

Control is implemented via 16-bit ROM instructions, as explained in Section 2.1.1. This 16-bit output (bits $R_{15} - R_0$) is distributed throughout the disk microprocessor, and is subsequently decoded as instructions to perform specific logic operations and data manipulations.

ROM output is formatted such that type of operation, registers involved, destination of resultant data, information source(s), and other control factors are defined by a single 16-bit instruction. The assembled sequence of "microinstructions" is referred to as the *microprogram* for the peripheral's microprocessor.

There are 24 basic instructions in the 2270 instruction set with each instruction having variables resulting in literally thousands of unique instructions available for data manipulation. The microprocessor hardware is designed so that it can execute every instruction with the end result predictable in every case.

Each of the instructions are comprised of two parts: the *operation code* and the *operand*. The operation code is defined as a portion of a computer instruction that indicates which action is to be performed by the computer. ROM bits $R_{15} - R_8$ are used as the operation code. Operand is defined as any one of the quantities entering into or arising from an operation. ROM bits $R_7 - R_0$ comprise the operand.

Operation code bits indicate the following, depending on which instruction category (to be explained later) is applicable:

1) Function to be performed.

2) Register (A, K, ST_0, ST_1) used in performing this function.

3) Whether to increment/decrement RAM address, or allow current RAM address to remain unchanged.

4) Selection of destination for resultant information (function performed). That is, store these results either in a register (A, K, ST_0, ST_1) or back into the current RAM location.

5) Whether high order bits (7-4) or low order bits (3-0) of the register designated (A, K, ST_0, ST_1) will be used for comparisons involved in conditional branch instructions.

Operand code bits indicate the following (again depending on which instruction category is applicable):

1) Use operand (via microprocessor ALU B Bus) as mask bits, along with bits (via microprocessor ALU A Bus) from a register (A, K, ST_0, ST_1) designated by ROM bits R_8 and R_9.

2) Use operand bits R_7 - R_4 as a mask for 4-bit Conditional Branch instructions.

3) Use operand bits R_3 - R_0 or R_7 - R_0 as a destination branch address for Conditional Branch instructions.

4) Use operand bits R_7 - R_0 plus operation code bit R_8 as a destination address for Unconditional Branch instructions.

5) Use operand bits R_7 - R_0 plus operation code bit R_8 as a new RAM address to be preset via Load Auxiliary instruction in the WCS microprogram.

2.2.2 *INSTRUCTION CATEGORIES*

The 2270 microprocessor instruction set can be arranged into five major categories.

1) Register Instructions:

An operation using 8 bits of RAM output ($M_7 - M_0$) contained at the current RAM address, and 8 bits contained in a register (A, K, ST_0, ST_1) designated by ROM bits R_9 and R_8. The results of such instructions are either stored into the current RAM location or stored back into the register designated by ROM bits R_9 and R_8. The RAM address can be incremented, decremented or remain unchanged by bits R_{11} and R_{10}.

There are eight register instructions as explained below:

INSTRUCTION	EXPLANATION
NOOP	No operation. Used as a filler command and has no effect but to cause the ROM address to increment.
B to M	B to memory. Transfers contents of B (buffer register A, K, STØ or ST1) to memory and causes RAM address to increment, decrement or remain unchanged.
M to B	Memory to B. Transfers contents of memory to B (buffer register A, K, STØ or ST1) and causes RAM address to increment, decrement or remain unchanged.
Add wo/carry	Binary add without carry bit. A binary add of the contents of B (buffer register A, K, STØ or ST1) and RAM with result to RAM or B and causes RAM address to increment, decrement or remain unchanged.
OR	Logical OR function. ORs the contents of B (buffer register A, K, STØ or ST1) with RAM with result to RAM or B and causes RAM address to increment, decrement or remain unchanged.

XOR	Exclusive OR function. Same as OR function except contents of B and RAM are exclusive ORed.
Add w/carry	Binary add with carry bit. Same as add without carry instruction.
AND	Logical AND function. ANDs the contents of B (buffer register A, K, STØ or ST1) with contents of RAM with result to RAM or B and causes RAM address to increment, decrement or remain unchanged.

2) Immediate Instructions:

An operation using 8 bits of ROM output (R_7 - R_0) contained at the current ROM address, and 8 bits contained in a register (A, K, ST_0, ST_1) designated by ROM bits R_8 and R_9. The results of such instructions are stored back into the designated register (R_8, R_9).

There are four immediate instructions as explained below:

INSTRUCTION	EXPLANATION
OR Immediate	Logical OR function. The contents of a register (A, K, STØ or ST1) are ORed with the eight least significant bits of ROM with the result stored back into the register.
XOR Immediate	Exclusive OR function. Same as OR Immediate except contents are exclusive ORed.
Add w/carry Imm.	Binary add with carry bit. The binary add w/carry bit of a register (A, K, STØ or ST1) with the eight least significant bits of ROM with the result stored back into the register.

AND Immediate	Logical AND function. Same as OR Immediate except contents are ANDed.

3) Branch Instructions:

These instructions are divided into two categories: *conditional branch* and *unconditional branch*. The conditional branch instructions allow from 0 to $\pm$ 15 microprogram step jumps; or, from 0 to $\pm$ 255 microprogram step jumps (depending on which conditional branch instruction is performed). The unconditional branch instructions causes a jump to *any* step within the microprocessor's microprogram.

There are eight branch instructions as explained below:

INSTRUCTION	EXPLANATION
Br if Reg. = 0	Branch if register = 0. Conditional branch to step indicated by the eight least significant bits of ROM if register (A, K, STØ or ST1) equals zero. Maximum number of steps is $\pm$255.
Br. if Reg. $\neq$ 0	Branch if register $\neq$ 0. Same as above if register does not equal zero.
Br. if True L,H	Branch if True Low or Branch if True High. Conditional branch to step indicated by ROM bits R_3 - R_0 if the 4 least significant bits (Low) or the 4 most significant bits (High) of register (A, K, STØ or ST1) equal any corresponding true ROM bits R_7 - R_4. Maximum number of branch steps is $\pm$15.
Br. if False L,H	Branch if False Low or Branch if False High. Conditional branch to step indicated by ROM bits R_3 - R_0 if the 4 LSB (Low) or the 4 MSB (High) of register (A, K, STØ or ST1) equal any corresponding false ROM bits R_7 - R_4. Maximum number of branch steps is $\pm$15.

Br. if = Mask	Branch if equal to Mask. Conditional branch to step indicated by ROM bits $R_3 - R_0$ if either the 4 LSB or 4 MSB (selected by a bit of the instruction code) of a register (A, K, STØ or ST1) equal the mask of ROM bits $R_7 - R_4$. Maximum # of branch steps is ± 15.
Br. if ≠ Mask	Branch if not equal to Mask. Same as above if register does not equal mask.
UB to steps 0-255	Unconditional Branch to steps 0-255. In the form of HEX 88YY, causes the microprogram to branch to the address contained in YY to one of the first 256 steps of the microprogram (steps 0-255).
UB to steps 256-511	Unconditional Branch to steps 256-511. In the form of HEX 89YY, causes the microprogram to branch to the address contained in YY to one of the second 256 steps of the microprogram (steps 256-511).

4) RAM Address Instructions:

These two instructions allow the ROM outputs $R_8 - R_0$ to preset the RAM address.

INSTRUCTION	EXPLANATION
Load Aux. (0-255)	Load Auxiliary. Enables the ROM bits $R_8 - R_0$ to preset the RAM to any address between 0-255 (the data buffer). The instruction takes the form of HEX 8CXX where XX is the RAM address.
Load Aux. (256-511)	Load Auxiliary. Enables the ROM bits $R_8 - R_0$ to preset the RAM to any address between 256 and 511 (the work buffer). The instruction takes the form of 8DXX where XX is the RAM address.

5) Control Instructions:

Control instructions initiate disk functions such as disk head movement, read, write, format, etc. These instructions are decoded directly from ROM outputs to peripheral interfacing hardware in the microprocessor. The ALU is not involved in these instructions.

There are 14 control functions used in the 2270:

INSTRUCTION	EXPLANATION
Control 1	Takes the form of HEX ECXX where
	EC01 - Turn on read gate (RDG)
	EC02 - Turn on write gate (WTG)
	EC04 - Turn on busy signal (BSY)
	EC08 - Format (FMT)
	EC10 - Head direction Select (HD DIR)
	EC20 - Preset CRC (PRC)
	EC40 - Head step (HD ST)
	EC80 - Head load (HD LD)
Control 2	Takes the form of HEX FCXX where
	FC01 - Select drive #3
	FC02 - Select drive #2
	FC04 - Select drive #1
	FC08 - Clear file inop. (FIR)
	FC10 - Strobe to 2200
	FC20 - 10 ms delay
	FC40 - Not used
	FC80 - Not used

2.2.3 *INSTRUCTION SET SUMMARY*

2.2.3.1 Introduction

Tables 1, 2 and 3 summarize the 24 instructions. Table 1 lists all the instructions and is divided into three major columns. The first column labeled "instruction category" contains the instruction names arranged by category as explained in Section 2.2.2. The second major column is labeled "operation code bits" and lists in binary the eight most significant bits of ROM output. This is the first half of any instruction, the operation code. The third major column is labeled "operand code bits" and lists in binary the eight least significant bits of ROM output. This is the second half of any instruction, the operand.

Referring to the second major column, it is noted that ROM bits R_{15}-R_{12} are fixed ones and zeroes for the register instructions but that bits R_{11}-R_8 may vary. The I/D heading under ROM bits R_{11} and R_{10} indicates increment or decrement of RAM address depending upon the status of these two bits.

It is at this point that Table 2 is required; Table 2 is an expansion of all the abbreviations used in Table 1. Referring to Table 2, the I/D bits are expanded into the four possible configurations. For example, if I/D bits R_{11} and R_{10} are a one and zero respectively for a register instruction, the result of the operation is stored in RAM and the RAM address is decremented one location.

Again referring back to Table 1, the last two bits of the operation code (bits R_9 and R_8) determine what register is to be used in the operation. This column is headed by "REG." which is an abbreviation for register. Observing Table 2, the two bits decode one of the four registers. For example, if ROM bits R_9 and R_8 are both low during a register instruction, the A register is the selected register.

Table 3 allows the reader to disregard Tables 1 and 2 since Table 3 is a breakdown of all the instructions in hexadecimal form. For example, if a 1700_{16} code is encountered in the program, the reader would be forced to convert the hexadecimal code to binary (0001011100000000), refer to Table 1 for the type of instruction, and finally to Table 2 to determine the register used and whether or not the RAM address is incremented or decremented. However, by utilizing Table 3, the reader can instantly determine that a 1700_{16} code is a B to M instruction involving register ST1 and incrementing the RAM address.

TABLE 1

2270 MICROPROCESSOR INSTRUCTION SET

	OPERATION CODE BITS-(R_{15}-R_8)								OPERAND CODE BITS-(R_7-R_0)
INSTRUCTION CATEGORY	15	14	13	12	11	10	9	8	7 6 5 4 3 2 1 0
REGISTER INSTRUCTIONS	INSTRUCTION CODE				I/D		REG.		OPERAND
NO-OP	0	0	0	0	ID	ID	B		Not Used
B to Memory	0	0	0	1	ID	ID	B		Not Used
Memory to B	0	0	1	0	ID	ID	B		Not Used
Binary ADD wo/carry	0	0	1	1	ID	ID	B		Not Used
OR	0	1	0	0	ID	ID	B		Not Used
XOR - Exclusive OR	0	1	0	1	ID	ID	B		Not Used
Binary ADD with carry	0	1	1	0	ID	ID	B		Not Used
AND	0	1	1	1	ID	ID	B		Not Used
IMMEDIATE INSTRUCTIONS	INSTRUCTION CODE						REG.		IMMEDIATE OPERAND (B BUS)
OR Immediate	1	1	0	0	1	0	B		I I I I I I I I
XOR Immediate	1	1	0	1	1	0	B		I I I I I I I I
Binary ADD w/carry Immed	1	1	1	0	1	0	B		I I I I I I I I
AND Immediate	1	1	1	1	1	0	B		I I I I I I I I
BRANCH INSTRUCTIONS (Conditional; 8 bit)	INSTRUCTION CODE						REG.		BRANCH ADDRESS (B BUS)
Branch if Register = 0	1	1	0	0	1	1	B		Y Y Y Y Y Y Y Y
Branch if Register ≠ 0	1	1	0	1	1	1	B		Y Y Y Y Y Y Y Y
MASK BRANCH INSTRUCTIONS (Conditional; 4 bit)	INSTRUCTION CODE					H/L	REG.		MASK BRANCH ADDRESS
Branch IF True	1	0	1	0	0	S	B		M M M M Y Y Y Y
Branch IF False	1	0	1	1	0	S	B		M M M M Y Y Y Y
Branch IF = Mask	1	0	0	0	0	S	B		M M M M Y Y Y Y
Branch IF ≠ Mask	1	0	0	1	0	S	B		M M M M Y Y Y Y
UNCONDITIONAL BRANCH	INSTRUCTION CODE								BRANCH ADDRESS
TO STEPS 0-255 (0000-00FF)	1	0	0	0	1	0	0	0	Y Y Y Y Y Y Y Y
TO STEPS 256-511 (0100-01FF)	1	0	0	0	1	0	0	1	Y Y Y Y Y Y Y Y
RAM ADDRESS INSTRUCTIONS	INSTRUCTION CODE								RAM ADDRESS LOADED
LOAD AUX (DATA BUFFER)	1	0	0	0	1	1	0	0	X X X X X X X X
LOAD AUX (WORK BUFFER)	1	0	0	0	1	1	0	1	X X X X X X X X
CONTROL INSTRUCTIONS	INSTRUCTION CODE								CONTROL OPERAND
Control 1	1	1	1	0	1	1	0	0	Z Z Z Z Z Z Z Z
Control 2	1	1	1	1	1	1	0	0	Z Z Z Z Z Z Z Z

TABLE 2

EXPLANATION OF LETTER DESIGNATIONS

FOR INSTRUCTION SET BITS

I/D = Increment/decrement of RAM Address

- 00 = Result to original RAM address; no increment or decrement
- 01 = Result to original RAM address then increment (+1)
- 10 = Result to original RAM address then decrement (-1)
- 11 = Result to selected register(B) and increment RAM address

REG. = Selected register

- 00 = A register
- 01 = K register
- 10 = Status Reg. 0
- 11 = Status Reg. 1

I = Immediate Operand (R_0 - R_7 Mask)

M = Mask; a unique configuration of binary bits.

Y = Branch Address

S = High order or Low order 4-bits for MASK Branch Instruction.

- 0 = Low order (Bits 0 - 3)
- 1 = High order (Bits 4 - 7)

X = New R. A. M. Address for LOAD Aux

Z = Control Operand

Control 1 ($ECZZ_{16}$):

- EC01 - Turn on Read Gate; RDG - (CNTRL1 AND R_0)
- EC02 - Turn on Write Gate; WTG - (CNTRL1 AND R_1)
- EC04 - Turn on Busy Signal; BSY - (CNTRL1 AND R_2)
- EC08 - Not used - (CNTRL1 AND R_3)
- EC10 - Head Direction Select; HD DIR - (CNTRL1 AND R_4)
- EC20 - PRC - (CNTRL1 AND R_5)
- EC40 - Head Step; HD ST - (CNTRL1 AND R_6)
- EC80 - Head Load; HD LD - (CNTRL1 AND R_7)

Control 2 ($FCZZ_{16}$)

FC01 - Select Drive #3 - (CNTRL2 AND R_0)

FC02 - Select Drive #2 - (CNTRL2 AND R_1)

FC04 - Select Drive #1 - (CNTRL2 AND R_2)

FC08 - Clear File Inop.; FIR - (CNTRL2 AND R_3)

FC10 - Strobe to 2200 - (CNTRL2 AND R_4)

FC20 - 10 ms. Delay - (CNTRL2 AND R_5)

FC40 - Not used - (CNTRL2 AND R_6)

FC80 - Not used - (CNTRL2 AND R_7)

TABLE 3

EXPANDED BREAKDOWN OF

MICROPROCESSOR OPERATION CODES

B To M

	A	K	St0	St1	
1.					
	1000	1100	1200	1300	No RAM I/D
	1400	1500	1600	1700	AD + 1
	1800	1900	1A00	1B00	AD - 1

M To B

	A	K	St0	St1	
2.					
	2000	2100	2200	2300	No RAM I/D
	2400	2500	2600	2700	AD + 1
	2800	2900	2A00	2B00	AD - 1

Add Without Carry (RAM)

	A	K	St0	St1	
3.					
	3000	3100	3200	3300	No RAM I/D
	3400	3500	3600	3700	AD + 1
	3800	3900	3A00	3B00	AD - 1
	3C00	3D00	3E00	3F00	AD + 1 Result to B

OR (RAM)

4.	A	K	St0	St1	
	4000	4100	4200	4300	No RAM I/D
	4400	4500	4600	4700	AD + 1
	4800	4900	4A00	4B00	AD - 1
	4C00	4D00	4E00	4F00	AD + 1 Result to B

Exclusive OR (RAM)

5.	A	K	St0	St1	
	5000	5100	5200	5300	No RAM I/D
	5400	5500	5600	5700	AD + 1
	5800	5900	5A00	5B00	AD - 1
	5C00	5D00	5E00	5F00	AD + 1 Result to B

Add With Carry (RAM)

6.	A	K	St0	St1	
	6000	6100	6200	6300	No RAM I/D
	6400	6500	6600	6700	AD + 1
	6800	6900	6A00	6B00	AD - 1
	6C00	6D00	6E00	6F00	AD + 1 Result to B

AND (RAM)

7.	A	K	St0	St1	
	7000	7100	7200	7300	No RAM I/D
	7400	7500	7600	7700	AD + 1
	7800	7900	7A00	7B00	AD - 1
	7C00	7D00	7E00	7F00	AD + 1 Result to B

8. OR Immediate

C8II	C9II	CAII	CBII

9. Exclusive OR Immediate

D8II	D9II	DAII	DBII

10. Add With Carry Immediate

E8II	E9II	EAII	EBII

11. AND Immediate

F8II	F9II	FAII	FBII

Branch Commands

12.

A	K	St0	St1		
80MY	81MY	82MY	83MY	= Mask L	
84MY	85MY	86MY	87MY	= Mask H	
90MY	91MY	92MY	93MY	≠ Mask L	
94MY	95MY	96MY	97MY	≠ Mask H	Can only branch
A0MY	A1MY	A2MY	A3MY	True L	within a ±15 step
A4MY	A5MY	A6MY	A7MY	True H	area.
B0MY	B1MY	B2MY	B3MY	False L	
B4MY	B5MY	B6MY	B7MY	False H	
CCYY	CDYY	CEYY	CFYY	= 0	Can branch within
DCYY	DDYY	DEYY	DFYY	≠ 0	a ±255 step area.

13. Unconditional Branch = 88YY steps 0 - 255 in microprogram
89YY steps 256-511 in microprogram

14. Load Auxiliary = 8CXX - RAM 0 - 255 (DATA BUFFER)
8DXX - RAM 256-511 (WORK BUFFER)

15. Control 1 = ECZZ (See Table 2)
Control 2 = FCZZ (See Table 2)

2.2.3.2 Instruction Set Examples

1) Register Instructions

The following two examples are typical of Register Instruction decoding:

EXAMPLE: $10XX_{16}$ (B to M)

	HEX 1				HEX 0				n/a				n/a			
Binary Value	0	0	0	1	0	0	0	0	X	X	X	X	X	X	X	X
	R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

Where: 0 = low ($\pm$0V)
1 = high (+5V)
X = don't care

In the above register instruction, R_{15} - R_{12} identify a Register-to-Memory command (sometimes referred to as B-to-M, in notation form). ROM bits R_{11} and R_{10} indicate that RAM address will not be incremented and that the contents of the A register (designated by ROM bits $R_{9,8} = 00_2$) will be stored at the current RAM location. ROM bits R_7 - R_0 are not used in register instructions. The above information can be verified by using Tables 1 and 2. However, by referring to Table 3, the $10XX_{16}$ code is immediately recognized as a B to M with the A register and no RAM increment or decrement.

EXAMPLE: $65XX_{16}$ (Add with Carry)

	HEX 6				HEX 5				n/a				n/a			
Binary Value	0	1	1	0	0	1	0	1	X	X	X	X	X	X	X	X
	R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

For this instruction, R_{15} - R_{12} designate that a Binary Add with Carry will be performed between the 8 bits at the current RAM location, and the 8-bit contents of the register designated by ROM bits R_9, R_8. In this case, R_9 and $R_8 = 01_2$, designating the 8-bit K register. The Binary Add with Carry is performed, and R_{11} and R_{10} indicate that the result is stored at the current RAM location and then the RAM address is incremented. Referring to Table 3, the 65XX code is decoded as an Add with Carry instruction involving the K register and incrementing the RAM address.

Generally speaking, a *Register* instruction is an operation performed between an eight bit register (A, K, ST_0, ST_1) designated by R_9, R_8 and the eight bits stored at the current *RAM* address.

2) Immediate Instructions

The following example is typical of Immediate Instruction decoding:

EXAMPLE: $F8AA_{16}$ (AND Immediate)

	HEX F				HEX 8				HEX A				HEX A			
Binary Value	1	1	1	1	1	0	0	0	1	0	1	0	1	0	1	0
	R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

All Immediate Instructions are performed using the 8 bits contained in a register (A, K, ST_0, ST_1) designated by R_9 and R_8, and the 8-bit mask presented in R_7 - R_0. The results of Immediate Instructions are transferred back to the designated register (A, K, ST_0, ST_1).

For the example Immediate Instruction F8AA, ROM bits R_{15} - R_{10} designate an AND IMMEDIATE operation. The result of this AND IMMEDIATE is stored back into designated register A (R_9, R_8 = 00_2). This can be verified by using Table 3.

The 8-bit mask present in bits R_7 - R_0 (10101010) are the bits that are ANDed in the ALU with the present contents of RAM.

As an example, if the RAM contains a bit configuration of 11110000 and this AND Immediate is executed, the final result in the A register would be a bit configuration of 10100000 (10101010 ANDed with 11110000 = 10100000).

3) Branch Instructions

The various Branch instructions are explained individually:

First, there are eight *4-bit* Branch instructions; they cause a branch from 0 to $\pm$ 15 steps from the current microprogram step if a specified condition is met. These eight 4-bit instructions belong to the *conditional* category of Branch instructions.

Four ROM bits (R_3 - R_0) determine the Branch address; therefore, there are 16 (2^4) unique combinations of those binary bits possible. Thus (for example) if the current ROM address is 0000_{16}, and the Branch address specified by R_3 - R_0 is 1111_2, a jump of +15 steps is performed, branching the microprogram to ROM address $000F_{16}$. Conversely, if the current ROM address is $000F_{16}$, and the Branch address specified by R_3 - R_0 is 0000_2, a jump of -15 steps is performed, branching the microprogram to ROM address 0000_{16}. These 4-bit conditional branch instructions compare the contents of a register designated by R_9 and R_8 to a mask presented by bits R_7 - R_4. If the conditions of the branch are *met*, branch to a step (ROM address) designated by R_3 - R_0 is made. If the conditions of the branch are *not* met, the microprogram continues sequentially to the next step in that routine.

Since these instructions can only compare four bits of a register specified by R_9 and R_8 with the four mask bits (R_7 - R_4), either the four high order bits or the four low order bits of the designated register is specified by ROM bit R_{10}. If R_{10} = high, or logical "one", compare bits 7-4 of the designated register with mask bits R_7 - R_4; if R_{10} = low, or logical "zero", compare bits 3-0 of the designated register with mask bits R_7 - R_4.

The following examples are typical of each four bit conditional branch instruction.

EXAMPLE: $805A_{16}$ (Br A = ML)

									MASK				BRANCH			
	HEX 8				HEX 0				HEX 5				HEX A			
Binary Value	1	0	0	0	0	0	0	0	0	1	0	1	1	0	1	0
	R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

COMPARE

Contents of A Register:	X	X	X	X	0	1	0	1	x = irrelevant value
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
	High Order				Low Order				

This instruction causes a branch by changing the current set up of IC_7 - IC_0. Actually, the only bits of ROM address that change from the current address are IC_{0-3}. This ROM address modification takes place only if the *low* order bits of the A register (A_3 - A_0) are identical to the mask presented in R_7 - R_4. With the A register in the state indicated above, the condition sought is met and a branch is performed.

If the current ROM step (address) was:

Binary: 0 0 0 0 0 1 1 1

HEX 0 7

The new address would be:

Binary: 0 0 0 0 1 0 1 0

HEX 0 A

Since the new address $= 010_{10}$ $(=A_{16})$

And the previous address $= 07_{10}$ $(=7_{16})$

Subtract -

Branch to address 0A (a jump of +3) occurs when specified conditions are met.

The above example microinstruction, 805A, is a typical "Branch if A = Mask Low" conditional branch in the microprocessor.

EXAMPLE: 8426_{16} (Br. A = MH)

MASK (HEX 2) BRANCH (HEX 6)

	HEX 8				HEX 4				HEX 2				HEX 6			
Binary Value	1	0	0	0	0	1	0	0	0	0	1	0	0	1	1	0
	R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

COMPARE

x = irrelevant value

Contents of A register:	0	0	1	0	X	X	X	X
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

This instruction causes a branch to the ROM address designated by $R_3 - R_0$ if the *high* order bits of the A register $(A_7 - A_4)$ are equal to the mask presented in $R_7 - R_4$. Again, the specified condition is met and the branch is performed. The ROM address is changed in the same manner as the previous $805A_{16}$ example.

The example microinstruction 8426 is a typical "Branch if = Mask High" conditional branch in the microprocessor.

EXAMPLE: $A0CF_{16}$ (Br A = TL)

MASK BRANCH

	HEX A				HEX 0				HEX C				HEX F			
Binary Value	1	0	1	0	0	0	0	0	1	1	0	0	1	1	1	1
	R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

x = irrelevant value								
	X	X	X	X	1	1	X	X
	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

This instruction causes a branch only if the configuration of TRUE (ON; logic '1') bits presented in the R_7 - R_4 mask match the configuration of TRUE (ON; logic '1'; high) bits contained in the four low order bits (3-0) of a register designated by ROM bits R_8 and R_9. ROM bits R_{15} - R_{11} designate *Branch if True;* bit R_{10} (=0) designates four low order bits of the register selected by R_8 and R_9, which in this case is the A register.

Generally speaking, this is called a *Branch if True Low* (Branch if A register low order TRUE bits match R_7 - R_4 TRUE bits). If any one of the TRUE mask bits R_7 - R_4) do not match up to a corresponding true bit in A_3 - A_0, no branch occurs.

ROM address is modified for branch in the same manner as the previous $805A_{16}$ example.

Since only TRUE *mask* bits are being compared, any other TRUE bits in the *selected register* not corresponding to TRUE bits in the mask are ignored.

If "Branch IF True High" is the instruction, the four high order bits of the A register would be used to compare with the TRUE mask bits presented in R_7 - R_4.

EXAMPLE: $B03F_{16}$ (A = FL)

HEX B				HEX 0				HEX 3 (MASK)				HEX F (BRANCH)			
1	0	1	1	0	0	0	0	0	0	1	1	1	1	1	1
R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

Contents of A Register:

X	X	X	X	0	0	X	X
A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0

X = irrelevant value

This instruction causes a branch if the configuration of false (low; 0) bits presented in the R_7 - R_4 FALSE mask bits (bits R_7 and R_6 in this case) match up to corresponding low order FALSE bits in the A register (A_3 and A_2 in this case).

A "Branch IF False High" instruction follows the same format as the above example. The only difference being that the FALSE high order bits of the selected register (the A register in this example) would be compared.

The two remaining conditional branch instructions have the capability to branch 0 to $\pm$ 255 steps from the current step in the microprogram. This is achieved by changing IC_7 - IC_0. Unlike the 4 bit conditional branch instructions which actually can modify only the four low order ROM address bits (IC_3 - IC_0), all 8 ROM address bits can be changed to the address contained in bits R_7 - R_0. These instructions cause a branch only if all eight bits of the register designated by R_9 and R_8 are either =0 or ≠0.

These two instructions are as follows:

BRANCH IF REGISTER =0: 1 1 0 0 1 B B Y Y Y Y Y Y Y Y

BRANCH IF REGISTER ≠0: 1 1 0 1 1 B B Y Y Y Y Y Y Y Y

where B = selected register

EXAMPLE: $DD2C_{16}$ (Branch IF Reg ≠ 0)

HEX D				HEX D				HEX 2				HEX C			
1	1	0	1	1	1	0	1	0	0	1	0	1	1	0	0
R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

The example causes a branch from the current step, to step 002C or 012C, (depending on whether the current step lies within steps 0000 - 00FF or within 0100 - 01FF) if register K ('B' = 01) is any value other than zero.

The last Branch Instruction category is the *Unconditional Branch*. These instructions cause a direct branch to *any* step in the microprogram, subject to *no* conditions.

These two instructions are as follows:

UNCONDITIONAL BRANCH 88YY
(to 0000 thru 00FF) 1 0 0 0 1 0 0 0 Y Y Y Y Y Y Y Y

UNCONDITIONAL BRANCH 89YY
(to 0100 thru 01FF) 1 0 0 0 1 0 0 1 Y Y Y Y Y Y Y Y

EXAMPLE: $89C5_{16}$ (UB)

HEX 8				HEX 9				HEX C				HEX 5			
1	0	0	0	1	0	0	1	1	1	0	0	0	1	0	1
R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

This example causes a direct branch to step 01C5 in the microprogram without meeting any logic conditions.

4) Ram Address Instructions

Load auxiliary instructions unconditionally preset a RAM address specified by R_7 - R_0 (AD_7 - AD_0), using R_8 (AD_8) as a chip enable.

The LOAD AUXILIARY instructions are as follows:

LOAD AUXILIARY 8CXX
(DATA BUFFER): 1 0 0 0 1 1 0 0 X X X X X X X X

LOAD AUXILIARY 8DXX
(WORK BUFFER): 1 0 0 0 1 1 0 1 X X X X X X X X
Where X = new RAM address bits.

EXAMPLE: $8D20_{16}$ (Load Auxiliary; Work Buffer)

HEX 8				HEX D				HEX 2				HEX 0			
1	0	0	0	1	1	0	1	0	0	1	0	0	0	0	0
R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

This example presets RAM address to 20_{16}; bit R_8 = 1 selects the Work Buffer RAM integrated circuits. Location 20 in the Work Buffer is the location for storage of the track header byte read from each disk sector. $8CXX_{16}$ presets to any location within the R/W Data Buffer in RAM.

5) Control Instructions

Control instructions are used to perform operations external to the microprocessor, such as sending a strobe to the 2200 CPU, or loading a R/W head in a Shugart disk drive.

The Control instructions are as follows:

CONTROL 1 1 1 1 0 1 1 0 0 Z Z Z Z Z Z Z Z ECZZ
CONTROL 2 1 1 1 1 1 1 0 0 Z Z Z Z Z Z Z Z FCZZ

EXAMPLE: $FC10_{16}$ (Control 2)

HEX F				HEX C				HEX 1				HEX 0			
1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0
R_{15}	R_{14}	R_{13}	R_{12}	R_{11}	R_{10}	R_9	R_8	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0

This instruction causes one strobe and one byte of data input to be sent to the CPU, as specified by the Control Operand 10_{16}.

2.2.3.3 Typical Microprogram

The following microprogram is the prime routine for the WCS microprocessor. The prime routine consisting of 27 steps is initiated whenever the disk unit is turned on, the RESET key on the 2200 is depressed or the format button is depressed. Refer to text at end of program for a more detailed explanation of some of the actions that occur in the program.

SAMPLE MICROPROGRAM: WCS PRIME ROUTINE

STEP (IN HEX)	HEX CODE	INSTRUCTION	COMMENT
0000	FC04	CNTRL 2/04	Select Disk #1
0001	F800	A AND IMM	Clear A Register (Immediate Operand = 0's).
0002	8D00	Load Auxiliary	Select RAM address ØØ in the Work Buffer.
0003	1400	A to M(+1)	Take zeroes in A register and transfer to current RAM location then increment (+1) to next RAM address. This clears locations 00-FF of the Work Register.

0004	A223	BOTL	(Branch to 0003 IF STO-2 (AD_8) is ON). This causes a loop which increments and clears each RAM location in the *work buffer* (256-511) per step 0003 comments.
0005	1400	A to M(+1)	Same as step 0003 except clear *data buffer* (RAM locations 0-255). Note that when RAM address =111111111, adding (incrementing) RAM address brings the clear operation to RAM location 000000000 (MSB carry not used)
0006	B2D5	BOFL	(Branch to step 0005 IF STO-2 (AD_8) is OFF). This causes a loop similar to steps 0003 and 0004. Per comments for step 0005 the RAM data buffer is cleared.
0007	C803	A OR IMM	Immediate Operand = HEX 03; therefore, HEX 03 is transferred to the A register.
0008	8DE8	LOAD AUXILIARY	RAM address is preset to location $E8_{16}$ (or 488_{10}) which is the 1st HEX 03 byte for disk sector format.
0009	1000	A to M(N)	Transfer HEX 03 to current RAM location (Work Buffer, step 488_{10}). No change (N) in RAM address.

000A	8DFF	LOAD AUXILIARY	RAM address is preset to location FF_{16} (or 511_{10}) which is the HEX 03 byte for disk sector Write operations; this is also the second HEX 03 in sector format.
000B	1000	A to M(N)	HEX 03 (per comments for step 000A) transferred to RAM work buffer location 511_{10}.
000C	A74E	B1TH	Branch to step 000E IF bit 7 (carry) is ON, indicating that Format Button has been depressed.
000D	88C8	U.B.	Assuming FORMAT has not been initiated, unconditionally branch to step 00C8 to continue PRIME routine.
00C8	FB00	ST1 AND IMM	Immediate Operand $=00_{16}$ to clear carry.
00C9	EC00	CNTRL1	Clear Busy indicator to CPU.
00CA	FC00	CNTRL2	Clear Disk Select.
00CB	8C00	LOAD AUXILIARY	R/W data buffer.
00CC	F800	A AND IMM	Clear A register.
00CD	8D30	LOAD AUXILIARY	Location of Error Count.
00CE	1400	A to M(+1)	Clear Error Count.
00CF	1400	A to M(+1)	Clear Status.

00D0	1400	A to M(+1)	Clear Format Retry Count.
00D1	1400	A to M(+1)	Clear loc. 33_{16} in work buffer.
00D2	1400	A to M(+1)	Clear spare loc. in work buffer.
00D3	8D0F	LOAD AUXILIARY	Location of ØØ byte to be sent to CPU.
00D4	A624	BOTH	Branch to step 00D4 IF bit 6 of ST_0 is ON. (Look for 2200 strobe).

The comments provide a basic explanation of what the instruction does, however the reasons are not always evident. This paragraph helps explain the reasons behind the steps executed in a prime routine.

STEP	REASON
0000	Disk #1 is always selected. It is assumed that disk #1 will be used.
0001	Clears the A register. A clearing process has now begun to set all pertinent registers to zero.
0002	Selects location 00 of the RAM's work buffer area. The next instruction will start a routine that will clear the 256 locations in the RAM.
0003	Takes the zeroes from the A register and transfers them to location 00 of the RAM then increments RAM address.
0004	Branch Ø = TL. Branch to step 0003 if STO-2 is on (AD8). The 23 of the code A223 indicates a mask of 2 and a branch to 3. The AD8 is always turned on by a Load Aux. command and this was done in step 0002. L99-3 turns on AD8 during a Load Aux. to the work buffer. This branch command causes a loop between steps 3 and 4 to clear the 256 locations per step 3 comment.

0005 Same as step 0003 except clear *data buffer* (RAM locations 0-255). Note that when RAM address = 111111111, adding (incrementing) RAM address brings the clear operation to RAM location 000000000 (MSB carry not used).

0006 (Branch to step 0005 IF bit 2 of ST_0 (AD_8) is OFF). This causes a loop similar to steps 0003 and 0004. Per comments for step 0005 the RAM data buffer is cleared.

0007 The value HEX 03 is transferred to the empty A register by an OR Immediate. (The 03 is used when formatting a disk; this code is written in every sector as an aid in locating data on a write and read.)

0008 The RAM address is preset to location 8DE8 (488) which is the first HEX 03 byte for disk sector format.

0009 Transfers the 03 to the present RAM location without increment or decrement.

000A The RAM address is preset to location 8DFF (511) which is the 03 byte for disk write; this is also the second 03 in sector format.

000B Same as step 0009 but location 8DFF (511).

000C Branch to step 000E if bit 7 of ST1 register is on (the carry bit). The carry bit has several uses, one of which is being a flag to indicate that the format button was depressed. If the carry bit is on, the program branches to step 0190 to continue the format routine, otherwise continue.

000D Assuming format has not been initiated, unconditionally branch to step 00C8 to continue prime routine.

00C8 00D2	When the microprogram was first written, steps C8 and C9 contained the operations that steps D3 and D4 now contain; however, due to necessary modifications in the microprogram, codes were added to steps C8 through D2 for use in another routine. Consequently, the unconditional branch to C8 from 0D was never changed to read "branch to D3." Therefore steps C8 through D2 are executed during a prime routine but are not necessary.
00D3	This Load Aux. presets the RAM address to location 8D0F preparing to receive a strobe from the 2200.
00D4	Branch to step 00D4 (branch on itself) until the 2200 strobe bit is sensed by ST0-6.

2.2.4 *MODEL 2270 MICROPROGRAM*

This section contains the complete Model 2270 microprogram with flow charts. To aid in following the Format, Write and Read routines, these routines are listed in abbreviated form below.

FORMAT - WITH HEAD UNLOADED

1) Prime routine 0000-000C.
2) Format 000E.
3) 100 ms delay 0190-0198.
4) Select disk #1 000F-0010.
5) Load head with 50 ms delay 0017-001D.
6) Clear file inop. 0011-0012.
7) Br. to 0015 if no error 0012.
8) Br. to 001F if carry on 0015.
9) Move head to track 0 001F-0025.
10) Find requested sector 0027-0031.
11) Write format 0033-0041.
12) Checking and incrementing sectors 0043-004A.

13) When sector 15 is formatted, increment track #0046.

14) Checking and incrementing tracks 004D–0057.

15) When entire disk is formatted branch to 0058 from 0032.

16) Read header bytes and store in RAM 0058-0070.

17) Read routine for format 0075-0088.

18) Check CRC 0089-008D.

19) Check sector count for format read 008F-0096.

20) Check track count and step head 0097-00A2.

21) When finished reading format, branch to 0000 from 009E.

22) Prime routine 0000–000C.

23) No format 000D.

24) Prime continued 00C8–00D4.

WRITE-WITH HEAD UNLOADED AND OVER TRACK ZERO

1) Prime 0000–000C.

2) No format 000D.

3) Prime continued 00C8–00D4.

4) Three initial address bytes from CPU 00D4–00DE.

5) Check for illegal address 00DF–00E6.

6) Track and sector conversion 00EA–0107.

7) Select desired disk from conversion 0108–0110.

8) Clear file inop. 0010.

9) Load head, 50 ms delay 0017-001E.

10) Clear file inop. 0011-0012.

11) Load head, 50 ms delay 0015-0016.

12) Load head and select appropriate track address 0111-011D.

13) Step head to desired track 0125-013B.

14) Head moved previously? Possible retry 013C–0140.

15) Answer last address byte 0143-0147.

16) Data from CPU (write) 014C–0154.

17) Accept LRC byte from CPU 0155–0158.

18) Find requested hardware sector 0028–0032.

19) Read header bytes and store in RAM 0058–0063.

20) Compare header bytes with requested address 0064-0074.

21) Write routine 017B-018D.

22) First and last (error) strobe to CPU 00C4-00C7.

23) Prime continued preparing for first strobe of any operation 00C8-00D4.

READ-WITH HEAD LOADED AND NOT ON TRACK ZERO

1) Prime 0000-000C.

2) No format 000D.

3) Prime continued 00C8-00D3.

4) Three initial address bytes from CPU 00D4-00DE.

5) Check for illegal address 00DF-00E9.

6) Track and sector conversion 00EA-001F.

7) Select desired disk from conversion 0108-0110.

8) Clear file inop. 0010-0012.

9) Load head, 50 ms delay 0015-0016.

10) Load head and select appropriate track address 0111-0120.

11) Move head to track zero 0021-0026.

12) Step head to desired track 0126-0135.

13) Head moved previously? Possible retry 013C-0140.

14) Answer last address byte 0143-014B.

15) Accept LRC byte from CPU 0157-0158.

16) Find requested sector 0028-0032.

17) Read header bytes and store in RAM 0058-0063.

18) Compare header bytes with requested address 0064-0073.

19) Read routine 0075-0088.

20) Check CRC 0089-008E.

21) RAM location 0F contains a 00 byte? 0159-0163.

22) Send data and LRC on read 0164-016D.

23) Prime continued preparing for first strobe on any operation 00C8-00D4.

MODEL: 2270 MICROPROGRAM

BOARD: 6718 or 7018

PROMS: L111 378-0452R1

L113 378-0453R1

L112 378-0454R1

L114 378-0455R1

REMARKS:
1. L113 contains the low order bits of steps 0000-00FF.
2. L111 contains the high order bits of steps 0000-00FF.
3. L114 contains the low order bits of steps 0100-01FF.
4. L112 contains the high order bits of steps 0100-01FF.

	STEP	MICROCODE	INSTRUCTION	COMMENT
PRIME	0000	FC04	CNTRL-2	Sel. Disk 1
	0001	F800	A and IM	Clr A Reg
	0002	8D00	LA	M to 256
	0003	1400	A to M(+1)	Clr 256 - 511
	0004	A223	BOTL	Br AD8 ON
	0005	1400	A to M(+1)	Clr 0 - 255
	0006	B2D5	BOFL	Br AD8 OFF
	0007	C803	A or IM	03 to A Reg.
	0008	8DE8	LA	M to 488
	0009	1000	A to M(N)	03 to 488
	000A	8DFF	LA	M to 511
	000B	1000	A to M(N)	2nd 03 to 511
	000C	A74E	BITH	Br Carry On
NO FMT	000D	88C8	UB	Br to Beg.
FMT	000E	8990	UB	Br 100ms Delay
FILE INOP CLEAR	000F	FC04	CNTRL-2	Sel. Disk 1
	0010	B777	BIFH	Br Hd. Unloaded
	0011	EC80	CNTRL-1	Head Load
	0012	FC0B	CNTRL-2	Clear File,Sel. 2 & 3
	0013	A285	BOTL	Br STO Bit 4 On (FIO)
	0014	899B	UB	Br to Fmt Retry
LOAD HEAD WITH 50 MS DELAY	0015	A74F	BITH	Br Carry On
	0016	8911	UB	Br to R/W
	0017	EC80	CNTRL-1	Load Head
	0018	F900	K and IM	Clr K Reg.
	0019	FC23	CNTRL-2	Start 10 ms
	001A	A24A	BOTL	Br 10 ms On
	001B	E901	K add IM	Add 1 to K Reg
	001C	9159	BR K $\neq$ ML	BR $\neq$ 50 ms
	001D	A741	BITH	Br Carry On
	001E	8811	UB	Br to R/W

MOVE HEAD TO TRACK 0	001F	FC23	CNTRL-2	Start 10 ms
	0020	A240	BOTL	Br 10 ms On
	0021	B7D5	BIFH	BR = Track 0
	0022	EC90	CNTRL-1	Set Dir.
	0023	ECD0	CNTRL-1	Step$\rightarrow$Track 0
	0024	881F	UB	Br to Zero Hd
	0025	A747	BITH	Br Carry On
	0026	8926	UB	Br to R/W
FIND REQUESTED HARDWARE SECTOR	0027	C980	K or IM	*
	0028	8D50	LA	Sctr Count Loc.
	0029	A719	BITH	BR SM ON
	002A	B7EA	BIFH	BR SM OFF
	002B	1300	STI to M(N)	Sect. Loc. To M
	002C	2000	M To A(N)	Sect. Loc. to A
	002D	F80F	A and Im	Mask High Order
	002E	8DEA	LA	Sect. Requested
	002F	5C00	A $\oplus$ M(+1)	XOR SECTOR
	0030	DC28	BR A $\neq$ 0	Br $\neq$ SECTOR
	0031	A743	BITH	Br Carry On
	0032	8858	UB	Br To R/W
FORMAT WRITE	0033	B572	BKFH	BR To RD Format
	0034	8DD4	LA	WT FMT
	0035	ECA6	CNTRL-1	WTG ON
	0036	ECA6	CNTRL-1	PRC
	0037	F900	K and IM	Clr K Reg
	0038	E901	K add IM	Add 1 to K
	0039	DD38	BR K $\neq$ 0	BR $\neq$ 819.2us
	003A	ECA6	CNTRL-1	PRC
	003B	A22B	BOTL	BR AD8 ON
	003C	B2DC	BOFL	BR AD8 OFF
	003D	E901	K add IM	Add 1 to K
	003E	B5DD	BKFH	BR $\neq$ 103.4us
	003F	F900	K and IM	Clr K
	0040	ECA4	CNTRL-1	Stop Write
	0041	A283	BOTL	Br No Error
KEEPS CHECKING & INCREMENTING SECTORS (FMT WRITE)	0042	880F	UB	Br to Retry
	0043	8DEA	LA	Sec Loc.
	0044	2000	M to A(N)	Sec Loc. to A
	0045	D80F	A $\oplus$ IM	
	0046	800D	BR A = ML	BR = SCTR 15
	0047	2000	M to A(N)	Sector to A Reg
	0048	E801	A add IM	Add 1 to SECTOR
	0049	1000	A to M(N)	Next Sector to M
	004A	8827	UB	B Wrt Next Sec.
KEEPS CHECKING CYLINDERS AND STEPS HEAD DURING FORMAT WRITE	004B	0000	NOOP	Not Used
	004C	0000	NOOP	Not Used
	004D	1800	A to M(-1)	Sector 0 to M
	004E	2000	M to A(N)	Cyl add to A
	004F	E801	A add IM	Cyl add +1
	0050	A446	BATH	Br Cyl = 64
	0051	1000	A to M(N)	Next Cyl to M
	0052	ECC4	CNTRL-1	Step$\rightarrow$76
	0053	FC23	CNTRL-2	Start 10 ms
	0054	A244	BOTL	Br 10 ms On
	0055	8827	UB	B Wrt Next Sctr.
	0056	90D1	BR A $\neq$ ML	Br Cyl $\neq$ 77
	0057	8828	UB	Br Rd. Next Sctr.

*Set 80 bit to indicate write

READ HEADER BYTES AND STORE IN RAM	0058	8D20	LA	Cyl. Byte Loc.
	0059	F900	K and IM	Clr K Reg.
	005A	E901	K add IM	Add 1 to K
	005B	956A	Br K ≠ MH	Br ≠ 307.2us
	005C	EC95	CNTRL-1	RDG On
	005D	ECB5	CNTRL-1	PRC On
	005E	A21E	BOTL	BR WR = 1
	005F	1400	A to M(+1)	Cyl. Byte to M
	0060	B2E0	BOFL	BR WR = 0
	0061	1400	A to M(+1)	Sec. Byte to M
	0062	ECB5	CNTRL-1	PRC
	0063	8D20	LA	Cyl. Byte
COMPARE HEADER BYTES WITH REQUESTED ADDRESS	0064	2100	M to K(N)	Cyl. Loc. to K
	0065	8DE9	LA	Track Address
	0066	5D00	K ⊕ M(+1)	1 See footnote
	0067	DDA3	BR K ≠ 0	Track Error
	0068	2100	M to K(N)	Sec. to K Reg.
	0069	8D21	LA	Sector Byte
	006A	5D00	K ⊕ M(+1)	2 See footnote
	006B	DDA8	BR K ≠ 0	Sector Error
	006C	8D31	LA	Status Loc.
	006D	C980	K or IM	CRC Error
	006E	4900	K or M(-1)	CRC ER to M
	006F	F900	K and IM	Clr K
	0070	A745	BITH	Br Carry On
	0071	8D10	LA	1st Add Byte
	0072	2100	M to K(N)	1st byte to K
	0073	B5B5	BKFH	BR If Read
	0074	897B	UB	Br to Write
READ ROUTINE - INCLUDES FORMAT (READ HIGH ORDER 1ST)	0075	F900	K and IM	Clr K Reg.
	0076	8C00	LA	Data Buffer
	0077	E901	K add IM	Add 1 to K Reg
	0078	95B7	K ≠ MH	Br ≠ 563.2us
	0079	F900	K and IM	Clr K Reg
	007A	ECA5	CNTRL-1	PRC
	007B	A21B	BOTL	BR WR = 1
	007C	1400	A to M(+1)	Data to Mem
	007D	8880	UB	Br Check AD8
	007E	C904	K or IM	
	007F	88C4	UB	Br Send CRC Err
	0080	A225	BOTL	Br AD8 On
	0081	B2E1	BOFL	BR WR = 0
	0082	1400	A to M(+1)	Data to Mem.
	0083	A225	BOTL	Br AD8 On
	0084	887B	UB	Br Wait for WR
	0085	A215	BOTL	B WR = 1 (1st CRC)
	0086	1400	A to M(+1)	
	0087	B2E7	BOFL	B WR = 0 (2nd CRC)
	0088	EC90	CNTRL-1	Stop Read
CHECK CRC	0089	2401	CRC to A(+1)	1st CRC to A
	008A	DCA3	BR A ≠ 0	BR If CRC Err
	008B	2001	CRC to A	2nd CRC to A
	008C	DCA3	BR A ≠ 0	BR If CRC Err
	008D	A74F	BITH	BR Carry On
	008E	8959	UB	B Send Data 2200

1. ⊕ Requested track with track read
2. ⊕ Requested sector with sector read

CHECKS SEC-TOR COUNT FMT READ	008F	8DEA	LA	Sector Loc.
	0090	2000	M to A(N)	Sector to A
	0091	D80F	A ⊕ IM	
	0092	8007	BR A = ML	BR = Sector 15
	0093	2000	M to A(N)	Sector to A
	0094	E801	A add IM	Add 1 to Sect
	0095	1000	A to M(N)	Next Sctr to M
	0096	8828	UB	Look Next Sctr
KEEPS CHECKING CYLINDERS AND STEPS HEAD DURING FORMAT READ	0097	1800	A to M(-1)	
	0098	2000	M to A(N)	Cyl to A Reg.
	0099	E8FF	A add IM	A Reg - 1
	009A	1000	A to M(N)	Next Cyl to M
	009B	D8FF	A ⊕ IM	
	009C	DC9F	BR A ≠ 0	Br to Step HD
	009D	FB00	STI and IM	Clr Carry
	009E	8800	UB	Br to Stop Fmt
	009F	ECD4	CNTRL-1	Step Head
	00A0	FC23	CNTRL-2	ST 10 ms
	00A1	A241	BOTL	Br 10 ms On
	00A2	8828	UB	Look Next Sctr
ERROR ROUTINE	00A3	EC84	CNTRL-1	Stop Read
	00A4	8D31	LA	Status Loc.
	00A5	2000	M to A(N)	Status Loc. To A
	00A6	C808	A or IM	Trk Error Bit
	00A7	1000	A to M(N)	Trk Error To M
	00A8	EC84	CNTRL-1	Stop Read
	00A9	F900	K and IM	Clr K Reg
	00AA	8D30	LA	Err Count
	00AB	2000	M to A(N)	Err Count To A
	00AC	E801	A add IM	Add 1 to Count
	00AD	1400	A to M(+1)	Err Count To M
	00AE	0000	NOOP	Not Used
	00AF	0000	NOOP	Not Used
	00B0	A082	BATL	Br 8 Errors
	00B1	8828	UB	Br Reread Sctr
	00B2	B7B4	BIFH	Br Carry Off
	00B3	899D	UB	BR FMT Retry
	00B4	2000	M to A(N)	Status to A
	00B5	F900	K and IM	Clr K Reg.
	00B6	B478	BAFH	Br Fmt Byte Err
	00B7	887E	UB	CRC Er to 2200
	00B8	A08B	BATL	Br Trk Err
	00B9	C902	K or IM	02 to K
	00BA	88C4	UB	Sect. Err to 2200
	00BB	A419	BATH	Br if HD Moved
	00BC	C810	A or IM	
	00BD	1000	A to M(N)	HD Moved Stat→M
	00BE	8D10	LA	1st Addr. Byte
	00BF	2000	M to A(N)	1st Byte to A
	00C0	C820	A or IM	
	00C1	8911	UB	Br to Zero HD
FIRST AND LAST STROBE TO CPU	00C2	F900	K and IM	Clr K Reg.
	00C3	C9C0	K or IM	Rein Reply
	00C4	8D32	LA	*
	00C5	1100	K to M(N)	
	00C6	B676	BOFH	Wait KBD
	00C7	FC13	CNTRL-2	Strobe to 2200

* Address, error or reinitialize to 2200.

PRIME (CONTINUED) PREPARING FOR FIRST STROBE OF ANY OPERATION	00C8	FB00	STI and IM	Clr Carry
	00C9	EC00	CNTRL-1	Clr Busy
	00CA	FC00	CNTRL-2	Clr Select
	00CB	8C00	LA	Data Buffer
	00CC	F800	A and IM	Clr A Reg.
	00CD	8D30	LA	Error Count
	00CE	1400	A to M(+1)	Clr Err Count
	00CF	1400	A to M(+1)	Clr Status Loc.
	00D0	1400	A to M(+1)	Fmt Retries
	00D1	1400	A to M(+1)	Clr Loc. 33
	00D2	1400	A to M(+1)	Clr Loc. 34
	00D3	8D0F	LA	
3 INITIAL ADDRESS BYTES FROM CPU	00D4	A624	BOTH	Look 2200 Str.
	00D5	B6D5	BOFH	Look End Str.
	00D6	A618	BOTH	Br Not Reint
	00D7	88C2	UB	Br to Reint
	00D8	0400	NOOP (+1)	Mem (+1)
	00D9	1100	K to M(N)	Addr Byte to M
	00DA	E801	A add IM	Add 1 to A
	00DB	B67B	BOFH	Wait KBD
	00DC	FC13	CNTRL-2	Str to 2200
	00DD	A03F	BATL	BR = 3rd Byte
	00DE	88D4	UB	Look Next Byte
CHECK FOR ILLEGAL ADDRESS	00DF	0000	NOOP	Delay
	00E0	0000	NOOP	Delay
	00E1	8D10	LA	1st Addr Byte
	00E2	2400	M to A(+1)	1st Addr Byte→A
	00E3	9007	BR A ≠ ML	Br Ill Addr
	00E4	2400	M to A(+1)	2nd Addr Byte→A
	00E5	9407	BR A ≠ MH	Br Ill Addr
	00E6	B03A	BAFL	BR ≠ Ill Addr
	00E7	F900	K and IM	Clr K Reg
	00E8	C901	K or IM	Hex 01 to K Reg
	00E9	88C4	UB	Ill Addr→2200
TRACK & SECTOR CONVERSION	00EA	F900	K and IM	Clr K Reg
	00EB	B0ED	BAFL	Br 256 Bit Off
	00EC	C910	K or IM	Hex 10 to K Reg
	00ED	B0DF	BAFL	BR 512 Bit Off
	00EE	C920	K or IM	Hex 20 to K Reg
	00EF	2800	M to A(-1)	3rd Addr Byte→A
	00F0	B472	BAFH	Br 128 Bit Off
	00F1	C908	K or IM	Hex 08 to K Reg
	00F2	B4B4	BAFH	Br 64 Bit Off
	00F3	C904	K or IM	Hex 04 to K Reg
	00F4	B4D6	BAFH	Br 32 Bit Off
	00F5	C902	K or IM	Hex 02 to K Reg
	00F6	B4E8	BAFH	Br 16 Bit Off
	00F7	C901	K or IM	Hex 01 to K Reg
	00F8	8DE9	LA	Trk Loc.
	00F9	1500	K to M(+1)	Trk Loc. to M
	00FA	F80F	A and IM	Mask Hi Bits
	00FB	1000	A to M(N)	Sctr Loc→M
	00FC	2100	M to K(N)	Sctr to K
	00FD	F803	A and IM	
	00FE	1000	A to M(N)	
	00FF	6000	A add M(N)	

TRACK & SECTOR CONVERSION (CONT'D)	0100	2000	M to A(N)	
	0101	6000	A add M(N)	
	0102	F800	A and IM	Clr A Reg.
	0103	B1B5	BKFL	
	0104	C801	A or IM	
	0105	B177	BKFL	
	0106	C802	A or IM	
	0107	6000	A add M(N)	Sctr Conv to M
SELECT DESIRED DISK FROM CONVERSION	0108	8D10	LA	1st Add Byte
	0109	2000	M to A(N)	1st Byte to A
	010A	B6BF	BOFH	Br Disk #3
	010B	A41D	BATH	BR Disk #2
	010C	880F	UB	BR Sel Disk #1
	010D	FC02	CNTRL-2	Sel Disk #2
	010E	8810	UB	Br Ck Hdld Fi
	010F	FC01	CNTRL-2	Sel Disk #3
	0110	8810	UB	Br Ck Hdld Fi
LOAD HEAD & SELECT APPROPRIATE TRACK ADDRESS	0111	EC80	CNTRL-1	Load Head
	0112	8DE9	LA	Trk Addr
	0113	2100	M to K(N)	Trk Addr to K
	0114	B6BB	BOFH	Br Disk #3
	0115	A41C	BATH	Br Disk #2
	0116	8D25	LA	D #1 Trk Loc.
	0117	A42E	BATH	Trk Err, Zero HD
	0118	2000	M to A(N)	Trk Loc. to A
	0119	A48D	BATH	Al Rdy Zero HD
	011A	8821	UB	Br to Zero HD
	011B	8921	UB	Br Trk 3 Loc.
	011C	8923	UB	Br Trk 2 Loc.
	011D	8925	UB	
	011E	F800	A and IM	Clr A Reg
	011F	1000	A to M(N)	Set Trk Loc. to 0
	0120	8821	UB	Br to Zero HD
	0121	8D27	LA	Disk #3 Trk Loc.
	0122	8917	UB	
	0123	8D26	LA	Disk #2 Trk Loc.
	0124	8917	UB	
STEP HEAD TO DESIRED TRACK	0125	F87F	A and IM	
	0126	C980	K or IM	
	0127	1100	K to M(N)	
	0128	D87F	A $\oplus$ IM	
	0129	3C00	A ADD M(+1)	
	012A	A74D	BITH	Br Carry On
	012B	D8FF	A $\oplus$ IM	
	012C	8933	UB	
	012D	E801	A ADD IM	Add 1 to A
	012E	EC80	CNTRL-1	Set Dir 77
	012F	ECC0	CNTRL-1	Step Head

STEP HEAD TO DESIRED TRACK (CONTINUED)	0130	FC23	CNTRL-2	Start 10 ms
	0131	A241	BOTL	Br 10 ms
	0132	E8FF	A add I	Subt. 1 From A
	0133	CC39	BR A = 0	
	0134	B7B6	BIFH	Br Carry Off
	0135	892E	UB	
	0136	EC90	CNTRL-1	Set Dir→0
	0137	ECD0	CNTRL-1	Step Head
	0138	8930	UB	
	0139	FB00	STO and IM	C/R Carry
	013A	FC23	CNTRL-2	Start 10 ms
	013B	A24B	BOTL	Br 10 ms On
HEAD MOVED PREVIOUSLY? POSSIBLE RETRY	013C	8D31	LA	Status Loc.
	013D	2000	M to A(N)	Status to A
	013E	0000	NOOP	
	013F	0000	NOOP	
	0140	B4E3	BAFH	Br HD not moved
	0141	8828	UB	Br to R/W
	0142	88C2	UB	BR to Reint
ANSWER LAST ADDRESS BYTE	0143	8D10	LA	1st Add Byte
	0144	2800	M to A(-1)	
	0145	B675	BOFH	Wait KBD
	0146	FC13	CNTRL-2	Str To 2200
	0147	A44C	BATH	Br If Write
	0148	A628	BOTH	Wait 2200 Str
	0149	B6D9	BOFH	Wait End Str
	014A	B6E2	BOFH	Wait KBD
	014B	8957	UB	
	014C	F800	A AND IM	CLR A Reg
DATA FROM CPU (WRITE)	014D	8C00	LA	Data Buffer
	014E	A62E	BOTH	Wait Str
	014F	B6DF	BOFH	Wait End Str
	0150	A612	BOTH	Br Not Reint
	0151	88C2	UB	Br to Reint
	0152	1100	K to M(N)	Data Byte to M
	0153	89C0	UB	Br to Gen LRC
	0154	0000	NOOP	Not Used
ACCEPT LRC BYTE FROM CPU	0155	0000	NOOP	Not Used
	0156	0000	NOOP	Not Used
	0157	EC84	CNTRL-1	Bsy On
	0158	8828	UB	Br to Write
RAM LOCATION OF CONTAINS A 00 BYTE	0159	F900	K and IM	Clr K Reg
	015A	8D10	LA	1st Add Byte
	015B	2800	M to A(-1)	
	015C	B67C	BOFH	Wait KBD
	015D	FC13	CNTRL-2	Str to 2200
	015E	0000	NOOP	Delay
	015F	0000	NOOP	Delay
	0160	0000	NOOP	Delay
	0161	8C00	LA	Data Buffer
	0162	A48E	BATH	Br If compare
	0163	F800	A and IM	Clr A Reg

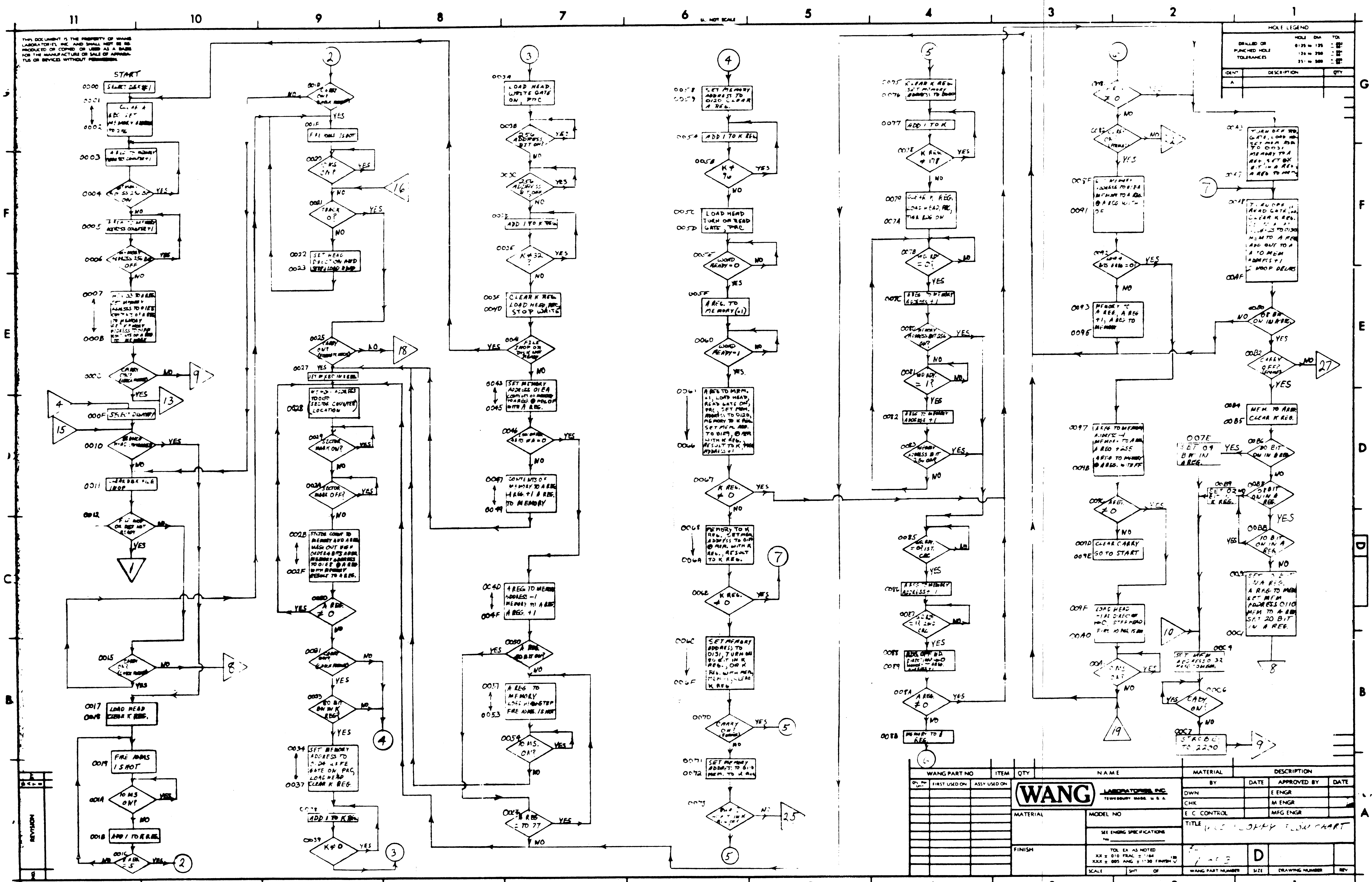
SEND DATA & CRC ON READ	0164	B674	BOFH	Wait KBD
	0165	FC13	CNTRL-2	Str to 2200
	0166	0000	NOOP	Delay
	0167	0000	NOOP	Delay
	0168	6C00	A ADD M(+1)	Generate LRC
	0169	B2D4	BOFL	Br AD8 Off
	016A	1000	A to M(-1)	LRC to Mem
	016B	B67B	BOFH	Wait KBD
	016C	FC13	CNTRL-2	LRC to 2
DATA FROM CPU FOR WRITE COMPARE	016D	88C8	UB	Br to Beg
	016E	A62E	BOTH	Wait 2200 Str
	016F	B6DF	BOFH	Wait End Str
	0170	5D00	K $\oplus$ M(+1)	*
	0171	CD73	BR K = 0	Br Data Compare
	0172	C8FF	A or Im	
	0173	A225	BOTL	Br AD8 On
	0174	896E	UB	Br to Compare
	0175	A625	BOTH	Wait 2200 Str
	0176	B6D6	BOFH	Wait End Str
	0177	8009	BR A = ML	B No Err On Comp
	0178	88E7	UB	Br Send Err
	0179	F900	K and IM	Clr K Reg
	017A	898A	UB	
WRITE ROUTINE (WRITE HIGH ORDER 1ST)	017B	EC84	CNTRL-1	Stop Read
	017C	F800	A and IM	Clr A Reg
	017D	F900	K and IM	Clr K Reg
	017E	E901	K ADD IM	Add 1 to K
	017F	959E	BR K ≠ MH	Br ≠ 460.8us
	0180	8DF9	LA	
	0181	ECA6	CNTRL-1	WTG
	0182	ECA6	CNTRL-1	PRC
	0183	A716	BITH	Br Sm On
	0184	EC80	CNTRL-1	Stop Write
	0185	88E7	UB	Br Send Err
	0186	A223	BOTL	Br AD8 On
	0187	A717	BITH	BR SM ON
	0188	B7E8	BIFH	BR SM OFF
	0189	EC80	CNTRL-1	Stop Write
	018A	B2D5	BOFL	Br AD8 Off
	018B	B275	BOFL	Br Rdy Err
	018C	F900	K and IM	Clr K Reg
	018D	88C4	UB	Last Byte→2200
	018E	0000	NOOP	Not Used
	018F	0000	NOOP	Not Used
100 MS DELAY TO CHECK FORMAT INSTRUCTION LEGITMATE	0190	F800	A and IM	Clr A Reg
	0191	FB00	STI AND IM	Clr Carry
	0192	FC23	CNTRL-2	Start 10 ms
	0193	A243	BOTL	Br 10 ms
	0194	E801	A ADD IM	Add 1 to A
	0195	90A1	BR a ≠ ML	BR ≠ 10 (100 ms)
	0196	A748	BITH	Br Carry On
	0197	8800	UB	Br to Prime
	0198	880F	UB	Br to Fmt

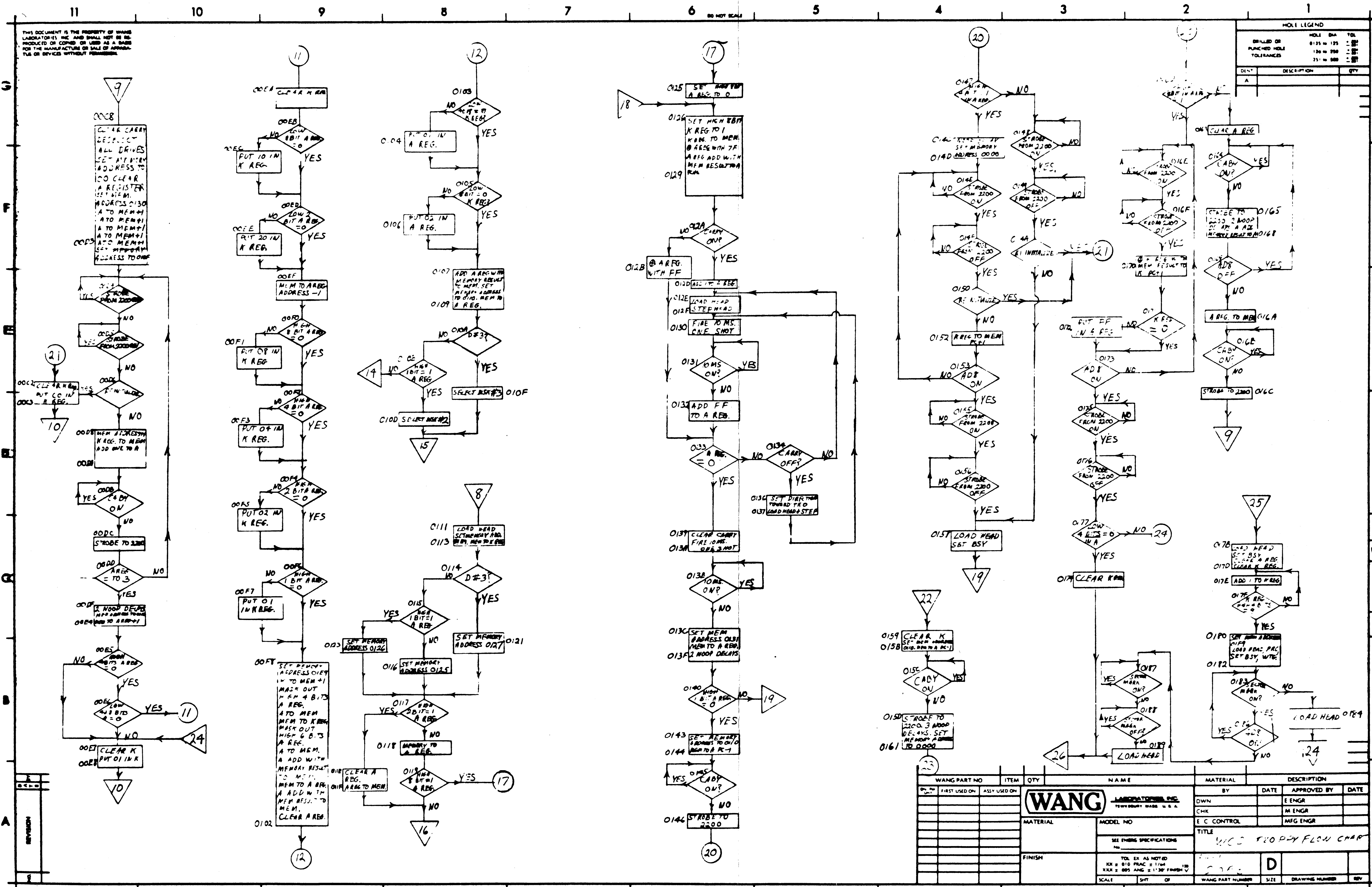
*Data read with data from 2200

COUNT FORMAT RETRIES	0199	0000	NOOP	Not Used
	019A	0000	NOOP	Not Used
	019B	A74D	BITH	Br Carry On
	019C	88E7	UB	Err to 2200
	019D	8D33	LA	Format Retries
	019E	2000	M to A(N)	
	019F	E801	A ADD IM	
	01A0	1000	A to M(N)	Add 1 to A Reg.
	01A1	A043	BATL	Br = 4 Retries
	01A2	89B0	UB	
FLASH FORMAT LIGHT	01A3	F800	A AND IM	Clr A Reg
	01A4	E801	A ADD IM	Add 1 to A
	01A5	FC23	CNTRL-2	START 10 ms
	01A6	A246	BOTL	Br 10 ms On
	01A7	90F4	BR A ≠ ML	Br A ≠ 15 (150 ms)
	01A8	F800	A and IM	Clr A Reg
	01A9	FC00	CNTRL-2	Turn Off D1
	01AA	E801	A ADD IM	Add 1 to A
	01AB	FC23	CNTRL-2	Start 10 ms
	01AC	A24C	BOTL	BR 10 ms On
	01AD	90FA	BR A ≠ ML	Br A ≠ 15 (150 ms)
	01AE	FC04	CNTRL-2	Turn on DK1
	01AF	89A3	UB	
BRANCH TO RETRY FORMAT	01B0	F800	A and IM	Clr A Reg
	01B1	8DE9	LA	Trk Loc.
	01B2	1400	A to M(+1)	Clr Trk
	01B3	1400	A to M(+1)	Clr Sector
	01B4	880F	UB	Br to Retry
	01B5	0000	NOOP	
	01B6	0000	NOOP	
	01B7	0000	NOOP	
	01B8	0000	NOOP	
	01B9	0000	NOOP	
	01BA	0000	NOOP	
	01BB	0000	NOOP	
	01BC	0000	NOOP	
	01BD	0000	NOOP	
	01BE	0000	NOOP	
	01BF	0000	NOOP	
	01C0	6C00	A add M(+1)	Generate LRC
	01C1	A223	BOTL	Br AD8 On
	01C2	894E	UB	Br to Next Byte
	01C3	A623	BOTL	Wait 2200 Str
	01C4	B6D4	BOFH	Wait End of Str
	01C5	8D34	LA	LRC Loc
	01C6	1100	K to M(N)	LRC to M
	01C7	5C00	A $\oplus$ M(+1)	*
	01C8	DCCA	BA ≠ 0	Br LRC Bad
	01C9	8957	UB	Br to Write
	01CA	88E7	UB	Br to Send Error
	01CB	0000	NOOP	
	01CC	0000	NOOP	
	01CD	0000	NOOP	
	01CE	0000	NOOP	
	01CF	0000	NOOP	

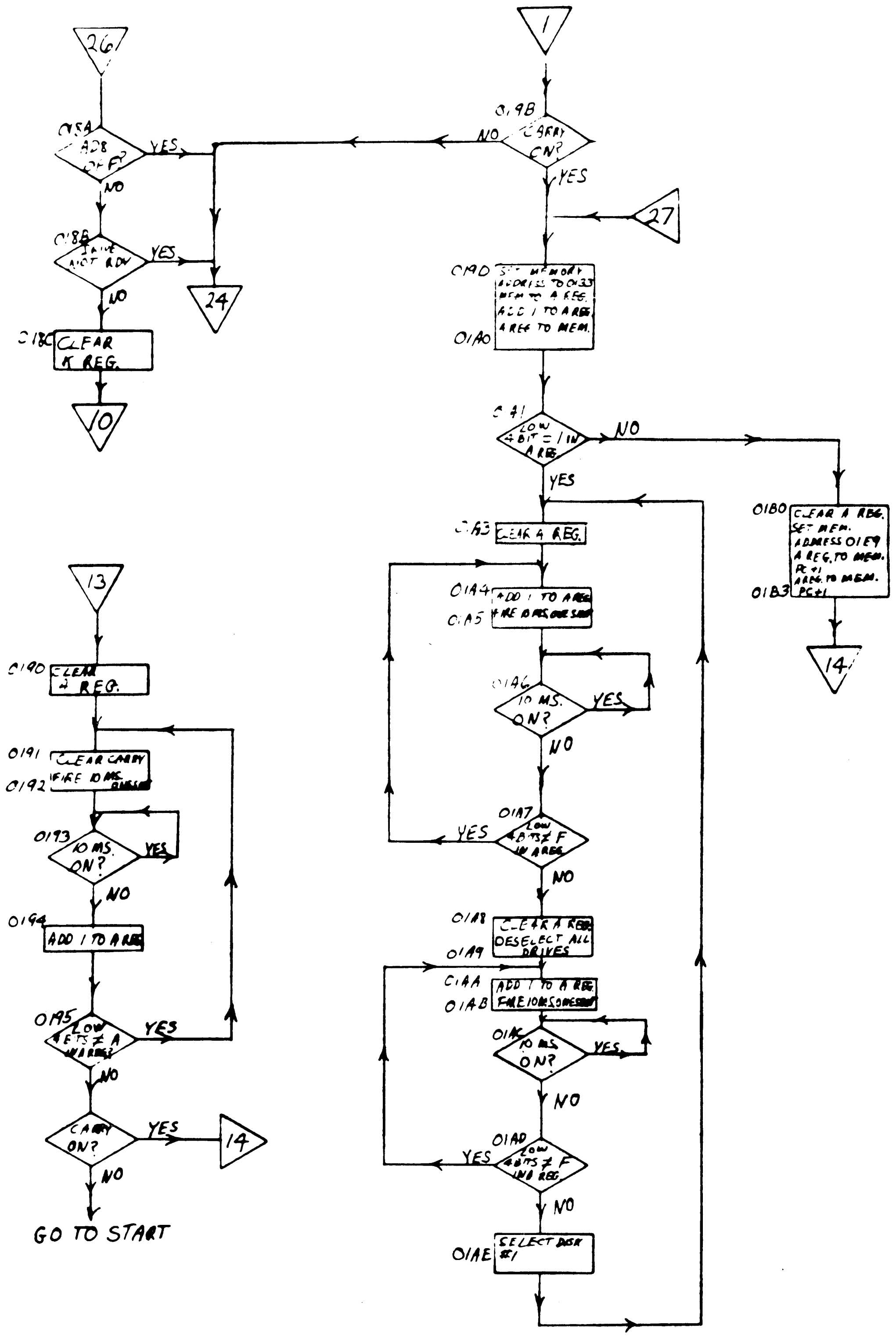
* $\oplus$ LRC byte from 2200 with LRC byte generated.

01D0	EC00	CNTRL-1	Turn Off RDG
01D1	8C00	LA	Mem to 00
01D2	F900	K and IM	Clr K Reg
01D3	F800	A and IM	Clr A Reg
01D4	C955	K or IM	55 to K
01D5	C8AA	A or IM	AA to A
01D6	1000	A to M(N)	AA to M
01D7	5100	K $\oplus$ M(N)	FF in Mem
01D8	2000	M to A(N)	FF to A
01D9	E801	A ADD IM	Add 1 (result 0)
01DA	DCD0	BR A $\neq$ 0	
01DB	7D00	K and M(+1)	Result to K
01DC	9150	BR K $\neq$ ML	BR 1 4-bit $\neq$ 1
01DD	9550	BR K $\neq$ MH	Br 10 40-bit $\neq$ 1
01DE	7100	K and M	A
01DF	4100	K or M	
01E0	2800	M to A(-1)	
01E1	5C00	A $\oplus$ M(+1)	Result to A
01E2	7C00	A and M(+1)	Result to A
01E3	CCE5	BR A = 0	
01E4	89D0	UB	
01E5	E801	A ADD IM	Add 1 to A
01E6	1400	A to M(+1)	
01E7	B2D5	BOFL	Br AD8 Off
01E8	1000	A to M(N)	
01E9	2100	M to K(N)	
01EA	8C00	LA	Mem→0
01EB	5D00	K $\oplus$ M(+1)	Result to K
01EC	911C	BR K $\neq$ ML	B $\neq$ 01
01ED	8C02	LA	
01EE	5100	K $\oplus$ M	Result to M
01EF	2400	M to A(+1)	
01F0	E901	K ADD IM	Add 1 to K
01F1	A224	BOTL	Br AD8 On
01F2	CCEE	BR A = 0	
01F3	89F3	UB	
01F4	FC00	CNTRL-2	Deselect Drives
01F5	FC01	CNTRL-2	Sel Disk 3
01F6	EC80	CNTRL-1	Load HD 3
01F7	FC02	CNTRL-2	Sel Disk 2
01F8	EC80	CNTRL-1	Load HD 2
01F9	FC04	CNTRL-2	Sel Disk 1
01FA	EC80	CNTRL-1	Load HD 1
01FB	B77B	BIFH	Br Sm Off
01FC	A78C	BITH	Br Sm On
01FD	A71D	BITH	Br HD Loaded
01FE	B7EE	BIFH	Br HD Unloaded
01FF	8800	UB	


THIS DOCUMENT IS THE PROPERTY OF WANG LABORATORIES, INC. AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS A BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS OR DEVICES WITHOUT PERMISSION.
START
HOLE LEGEND
LOAD HEAD, WRITE GATE ON, PRC
ADD 1 TO K REG
LOAD HEAD TURN ON READ GATE, PRC
ADD 1 TO K
CLEAR K REG
SET HEAD DIRECTION AND STEP LOAD HEAD
CLEAR K REG LOAD HEAD, PRC STOP WAIT
GO TO START
CLEAR CARRY
LOAD HEAD CLEAR K REG.
FIRE 10MS 1 SHOT
ADD 1 TO K REG.
MEM. TO AREG. CLEAR K REG.
STROBE TO 2200
WANG PART NO
ITEM
QTY
NAME
MATERIAL
DESCRIPTION
FIRST USED ON
ASSY USED ON
WANG LABORATORIES INC. TEWKSBURY MASS. U.S.A.
BY
DATE
APPROVED BY
DWN
CHK
E C CONTROL
E ENGR
M ENGR
MFG ENGR
MODEL NO
SEE ENGRG SPECIFICATIONS No
FINISH
TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30 FINISH
TITLE FLOPPY FLOW CHART
SCALE
SHT OF
WANG PART NUMBER
SIZE D
DRAWING NUMBER
REV
REVISION



THIS DOCUMENT IS THE PROPERTY OF WANG LABORATORIES INC. AND SHALL NOT BE REPRODUCED OR COPIED OR USED AS A BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS OR DEVICES WITHOUT PERMISSION.
HOLE LEGEND
STROBE TO 2200
CLEAR K
PUT 01 IN K
LOAD HEAD
SELECT DSK #3
SELECT DSK #2
SET MEMORY ADDRESS 0126
SET MEMORY ADDRESS 0127
SET MEMORY ADDRESS 0125
FIRE 10 MS. ONE SHOT
ADD FF TO A REG.
CLEAR A REG.
A REG. TO MEM
WANG
LABORATORIES INC.
FLOPPY FLOW CHART



WANG LABORATORIES INC. TEWKSBURY MASS. U.S.A.

TITLE: FLOW CHART

SIZE: D

2.3 HARDWARE OPERATIONAL THEORY

2.3.1 *INTRODUCTION*

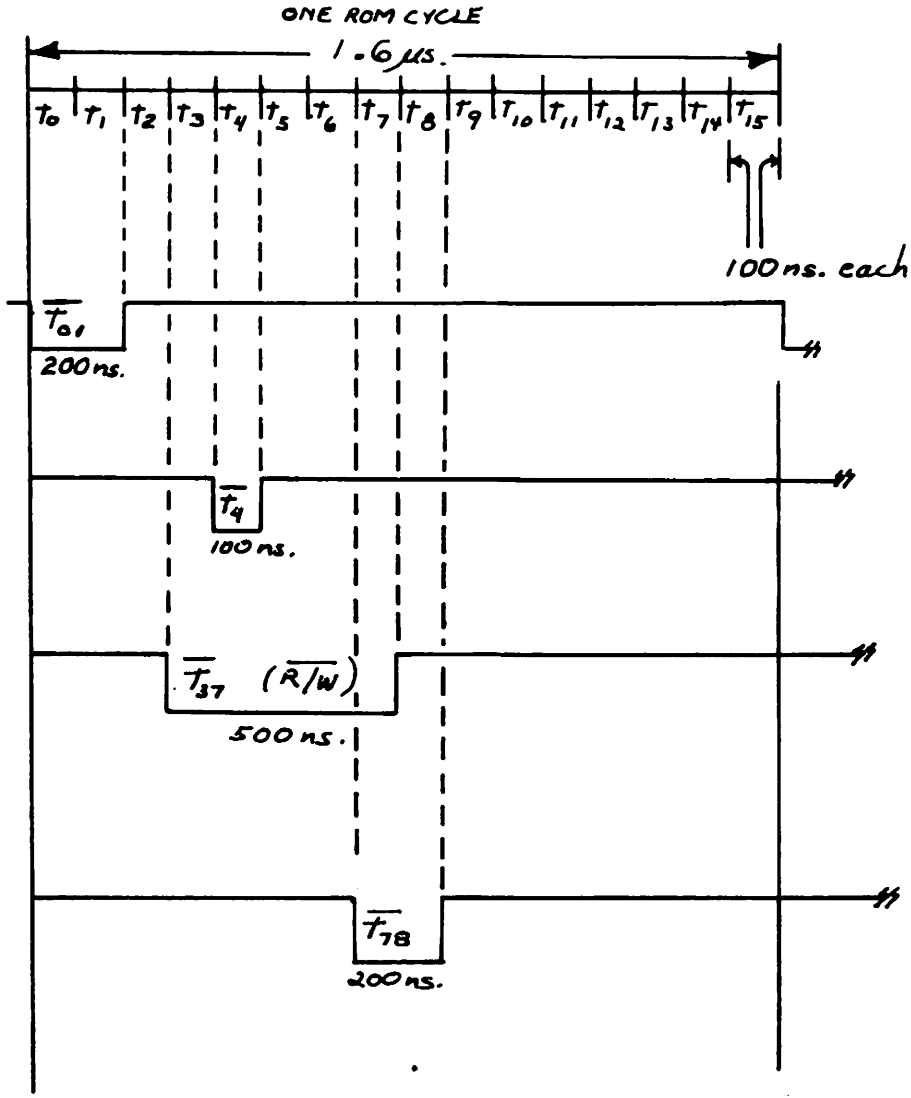
This section is devoted to the explanation of the 6718 microprocessor board. The following areas are explained:

1) Timing
2) Input to microprocessor from CPU
3) Output of microprocessor to disk
4) Input from disk to microprocessor
5) Output from microprocessor to CPU
6) Disk control operations
7) Sector Counter
8) Cyclic Redundancy Check
9) Format Routine

To comprehend the explanation, the reader must refer to the 6718 schematics and the block diagram.

2.3.2 *TIMING*

The master clock generates 16 clock periods each 100 ms in duration labeled T_0 through T_{15} (refer to timing chart below). One complete ROM cycle is 1.6 µs. The cycle begins at T_{01} when a new instruction is clocked into the ROM output register L78-81 and the information stored in RAM is clocked into the memory register L79 and 81. From T_{3-7} the RAM chips are enabled to write if desired. At T_4 the ROM instruction, which was loaded into the output registers at T_{01} is executed. Also during T_4, the new ROM address is loaded, either by incrementing L109 or L110, or by loading a branch address. At T_{78} the memory address is incremented or decremented, if applicable. The next T_{01} starts a new ROM cycle.



2.3.3 *INPUT TO MICROPROCESSOR FROM CPU*

Data from the 2200 enters the microprocessor via the K register (L3 and L6) from here it is loaded into RAM. This is accomplished in the following manner. To begin, R_8 and R_9 select the K register inputs of the A Bus multiplexer (L4, L5, L12, L15) thus presenting the K register contents to the 74181 ALU (L13 and L14). ALUs are capable of performing several logic and arithmetic functions selected by L21 pins 2, 8, 10, 12 and L20 pin 12. The configuration of these pins is dependent on the output of L42 and L50 which decode ROM bits R_{15} - R_{11} to determine the instruction and the ALU function necessary to perform this instruction. In this case the ALU chips will direct the data to its outputs (C_7 - C_0) unprocessed. From here the data is available for storage in the RAM (L59 - L62). Data will be written in a location designated by the address contained in L58, L70, and L107. These can be incremented, decremented, or loaded in block form, thus the ROM can directly control RAM address. To actually write the data, a line designated R/W must be changed; this is done by L47 and L48. L47 and L48, along with L30, L31, L32, L39, L40, L69, make up the ROM instruction decoder. Here is a list of ICs and their function in this decoder:

L32 Pin 7 -	Indicates to send the result to the selected register and increment RAM address.
L32 Pin 5 -	Increment RAM address.
L32 Pin 6 -	Decrement RAM address.
L32 Pin 9 -	Control Command.
L32 Pin 10 -	Immediate Instruction.
L39 Pin 4 -	A register clock.
L39 Pin 5 -	K register clock.
L39 Pin 7 -	Status register 1 clock.
L39 Pin 9 -	Load Auxiliary.
L39 Pin 10 -	Unconditional Branch.
L39 Pin 11 -	Branch if the high order register bits meet the condition.
L39 Pin 12 -	Branch if the low order register bits meet the condition.

With the data in RAM the processor is now ready to accept more data or process present data.

2.3.4 *OUTPUT OF MICROPROCESSOR TO DISK*

Data from the microprocessor makes its way to the disk in the following manner. At T_{01} the data in the current RAM address is loaded into the RAM output register; from here it is available for input to the A register (L66 and L67). With write gate (WTG) on, these inputs to the A register are selected via L37, L38, L54 and L55 and A register clock (ACU), L74 pin 6, loads the first byte of data in the A register. This data is now converted from parallel to serial by L75, L86, L93, L103 and L105 and sent to the disk to be written in the double frequency (2F) format via L95 and L105. After the first byte, the A register is clocked by Word Ready (WDRDY) which occurs every time 8 bits have been converted from parallel to serial.

2.3.5 *INPUT FROM DISK TO MICROPROCESSOR*

Information from the disk is first converted from serial to parallel by L73 and L76. Again WDRDY clocks the data into the A register each time 8 bits have been assembled into a parallel word. From the A register the data must be loaded into RAM. This is accomplished by R_8 and R_9 selecting the A register inputs to the A Bus Multiplexer (L4, L5, L12, L15) thus presenting the data to the ALU (L13 and L14). Again the ROM instruction decoder has put the RAM in a write mode through L47 and L48, and the ALU Function Decoder (L42 and L50) has allowed the data to pass through the ALU unchanged. When this data appears on the C Bus it is immediately stored in the memory location indicated by L58, L70, and L107. Memory address is then incremented and the processor is ready to accept the next byte from the disk.

2.3.6 *OUTPUT FROM MICROPROCESSOR TO CPU*

Once data from the disk is loaded into RAM it is ready to be transferred to the 2200 CPU. This is the path that the transfer follows. Since the RAM is normally in a read mode, the data can be accessed by simply changing the RAM address. This presents data to the RAM output register (L79 and L81); at T_{01} it is loaded, thus a new byte of data can be loaded every ROM cycle (1.6 μs). From the RAM output register the data is buffered through L28 and L29 which are strobed by L43 and L44. Since these are under ROM control, the data transfer between the processor and the 2200 is synchronized. Synchronization is necessary because the processor is faster than the 2200; the processor must wait for the 2200 to become ready which is accomplished in the microprogram. When the 2200 indicates that it is ready to accept another byte, the above process is repeated. This continues until all data is transferred.

2.3.7 *DISK CONTROL OPERATIONS*

All disk operations are controlled by the ROM with two instructions: Control 1 and Control 2. The control commands are listed below with the logic gates that decode them and a short description of each.

CNTRL1 AND R0 L65-2	Turns the Read Gate (RDG) on to enable the processor to read from the disk.
CNTRL1 AND R1 L65-5	Turns the Write Gate (WTG) on to enable the processor to write on the disk.
CNTRL1 AND R2 L65-7	Turns the Processor Busy (BSY) on to inform the CPU that the processor is busy.
CNTRL1 AND R3	NOT USED in 2270.
CNTRL1 AND R4 L65-12	Head Direction Select (HD DIR). A high signal sets the head direction toward track 77 while a low signal sets the head direction to track Ø. This control signal must be used with a disk selected while the head is loaded and in conjunction with head step.
CNTRL1 AND R5 L51-6	PRC. Used as a reset command before a read or write to clear the CRC register and preset logic that will be used for the read/write.
CNTRL1 AND R6 L63-4	Head Step (HDST). This is the output of a one-shot which moves the head one track. A disk must be selected, the head loaded an a direction chosen to properly move the head.
CNTRL1 AND R7 L43-6	Load Head (LDHD). When the head is loaded, a delay of 50 ms must be provided for settling time.
CNTRL2 AND R0 L64-3	Select disk #3 (DK3).
CNTRL2 AND R1 L64-6	Select disk #2 (DK2).
CNTRL2 AND R2 L64-11	Select disk #1 (DK1).
CNTRL2 AND R3 L63-12	File inoperable reset (FIR). Resets the file inoperable condition in the disk that arises when data integrity could be jeopardized as: R/W heads not loaded, drive door open, etc. This condition can be thought of as a ready/busy indicator.

CNTRL2 AND R4 L44-13	Strobe to 2200. Not applicable to this section.
CNTRL2 AND R5 L83-3	10 ms delay. Because of the speed of the ROM cycle, delays are necessary to halt the microprogram while mechanical actions take place. Any number of 10 ms delays can be used to create longer delays.
CNTRL2 AND R6	NOT USED in 2270.
CNTRL2 AND R7	NOT USED in 2270.

2.3.8 *SECTOR COUNTER*

The sector counters consist of L1, L7, L8, L9, L16, L17, L25 and L34. L1 and L8 divide the incoming sector pulses by two and apply their outputs to L7, L17 and L34 which are binary up counters. All of these counters are cleared or reset whenever an index pulse is received from a disk. Multiplexers L16 and L25 are selected so that only the sector count of the selected disk is applied to the ST1 register.

2.3.9 *CYCLIC REDUNDANCY CHECK*

The CRC circuit is comprised of L36, L45, L46 and L53. During a write command, data being written is shifted through the CRC circuitry to develop a unique 16-bit code that is written on the disk in two bytes at the end of the 256 byte data transfer. When the 256 bytes of data are read, the data is shifted through the CRC circuitry and a 16-bit CRC code is stored. This code is then compared with the CRC read from the disk and if the data was read correctly, the two 16-bit codes will be equal. No provision is made to determine if data was correctly written, therefore, if a CRC error develops on a read, it cannot be determined if data was written or read incorrectly.

2.3.10 *FORMAT ROUTINE*

When the format button is depressed, L56 is preset by pin 7. This action turns the carry bit on, which is used as an indicator by the microprogram. $\overline{\text{PF}}$ (prime/format) is generated which resets the ROM IC to step 0000. From this point, the microprogram clears the hardware for the next 12 steps which are also used during a prime routine. The 13th step of the program (step 000C) checks to see whether the carry bit is on or off. Because the carry bit was turned on, the program branches to 0190 and begins a 100 ms delay to determine whether the carry bit was legitimately turned on. If a noise spike generated the format signal, the spike will be cleared by one of the 13 T_4 signals applied to L56-6 during the 13 steps of the prime routine. When the 100 ms delay is completed with the carry bit still on, disk #1 is selected, the head is loaded and stepped to track zero. When the correct sector is found, sector zero, on track zero, the write gate is turned on and the following data is written on the disk from these memory locations:

302 BYTES PER SECTOR

LOCATION	01D4 to 01E7	01E8	01E9	01EA	01EB to 01FE	01FF	0000-00FF	
	20 Bytes 00	03 Byte	Track Address	Sector Address	20 Bytes 00	03 Byte	256 Bytes 00	CRC#1 CRC#2

Twenty bytes of zeroes are written immediately after the sector mark is decoded to allow for the mechanical tolerances of the sector pick-up from drive to drive. A byte of 03 is written and is used as an indicator on a read to allow the logic time to decode the track and sector addresses. The second set of 20 bytes of zeroes is written so that on subsequent read or write commands, the logic has time to determine whether a read or write is to be executed. The second 03 byte is written and used as an indicator that data follows on a read or write. When the second 03 is decoded on a read command, the next 256 bytes (plus 2 bytes of CRC) is read data; on a write command, start writing 256 bytes of data (plus 2 bytes of CRC).

When the processor has written one sector with the above data, the process is repeated for all sectors in the track, then for all tracks on the disk. All 77 available tracks on the disk are formatted even though the processor utilizes only 64. After the 77 tracks are formatted, there is a read format routine (also used during a read) that checks the track and sector addresses along with the CRC codes. This read format routine is done beginning with track 76 and ending with track 0. When the disk has been verified after a complete format routine, there is an unconditional branch to step 0000 where the microprogram does its initializing before cycling on step 00D4 waiting for a 2200 strobe.

2.4 TROUBLESHOOTING PROCEDURES

2.4.1 *INTRODUCTION*

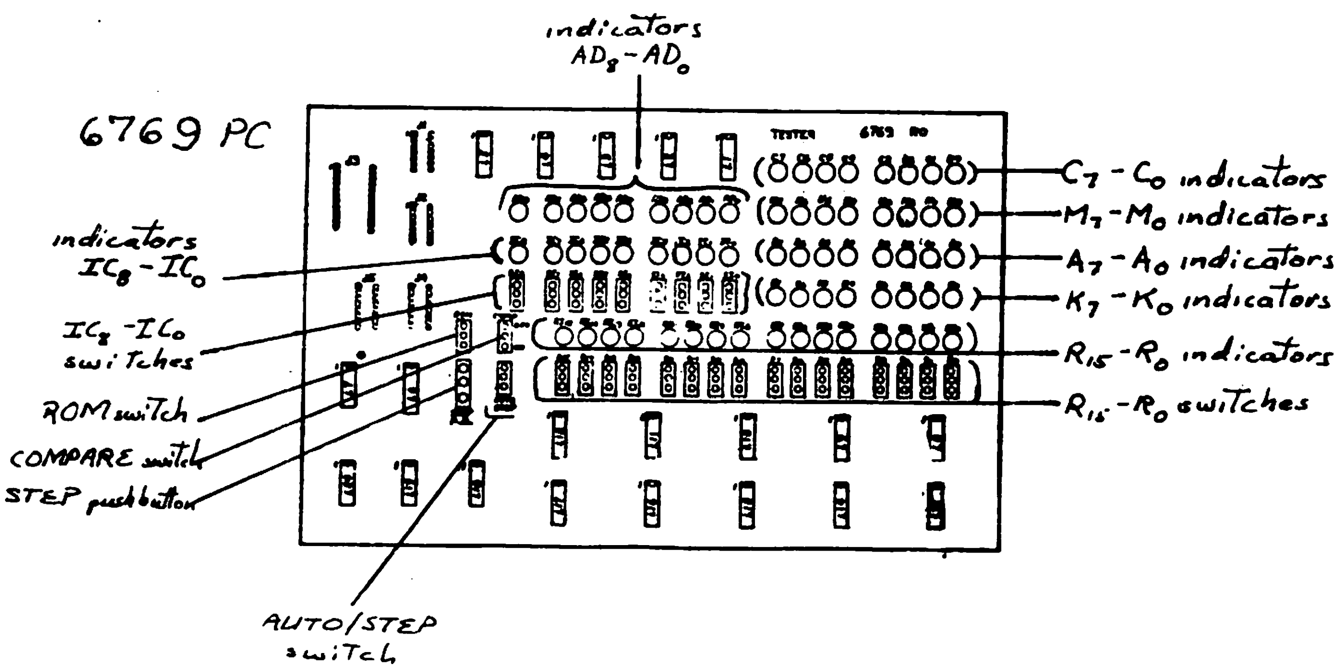
The purpose of these test units is to observe internal microprocessor conditions and to exercise, via manual control, all microprocessor functions.

Two versions of 2270 test units exist: one board for use with the 6718 only (a 6769 tester) and another capable of testing both the 6718 and 7018 (a 7069 tester). The 6769 test board has the test cables for testing the 6718 hard-wired to the 6769. The 7069 has three 36 lead ribbon test cables for testing the 7018 hard-wired to the 7069 and, five IC sockets to connect the test cables to the 6718 board.

Schematic diagrams for the 6769 and 7069 testers are included at the end of this section.

2.4.2 *FAMILIARIZATION WITH PHYSICAL LAYOUT OF TEST UNITS*

Version 1 - 6769 Tester



03-0026-1

Version 2 - 7069 tester

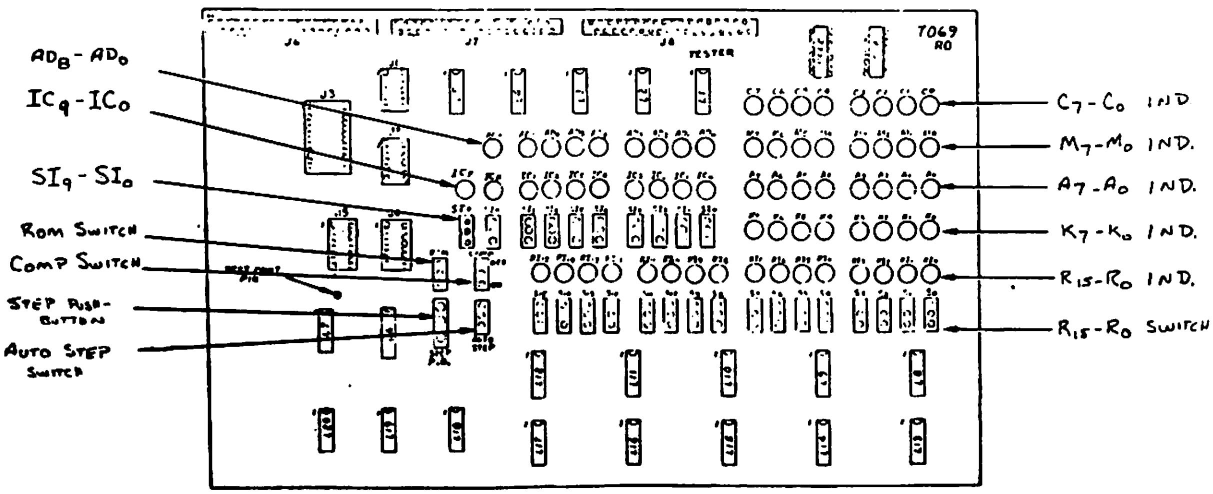


CHART 2.4.1

	ON 6718 PCB	PART #	7069 PCB CONN
CABLE# 1	T.P.s	(None) 16 Lead Ribbon	J5
CABLE# 2	T.P.s	881000	J1
CABLE# 3	T.P.s	860000	J2
CABLE# 4	T.P.s	883000	J3
CABLE# 5	T.P.s	882000	J4
6718 PCB T.P.s		654-1157R	

CHART 2.4.2

7069 PCB	PART #	7018 PCB
J6	220-3013	P9
J7	220-3013	P7
J8	220-3013	P8

NOTE:

Pin 1 of each test cable fingerboard from the 7069 PCB must plug into pin 1 of each female test connector on the 7018 PCB.

If a pin on the new tester cable breaks, the cable must be replaced. The cable and test points for the 6718 board can be ordered domestically and internationally through the Home Office.

2.4.3 *OPERATIONAL USE OF TEST UNITS*

Each set of light indicators (labeled accordingly) represent current outputs of the following:

1. Designated Registers
   A register (A_7 - A_0 indicators)
   K register (K_7 - K_0 indicators)
   ST_0, ST_1 registers (C_7 - C_0 indicators)

2. ALU Output (C_7 - C_0 indicators)

3. ROM Output (R_{15} - R_0)

4. ROM Address (IC_8 - IC_0)

5. RAM Output Register (M_7 - M_0)

6. RAM Address (AD_8 - AD_0); 6769
   (MA_7 - MA_0); 6452

7. CRB (CPU $\overline{\text{Ready}}$/Busy); 6452

Item 3 is actually dual purpose; indicators R_{15} - R_0 can also represent a manually set ROM instruction, to be used in lieu of (supercedes) 6718 ROM outputs. Such manually introduced commands to the microprocessor are set on ROM bit switches S_{15} - S_0 (See pictorials and schematics of 6769 and 7069). The ROM switch at schematic coordinates H, 14 (both 6769, 7069) must be in the UP position to allow indicators R_{15} - R_0 to display manual settings of ROM bit switches S_{15} - S_0. Use of this feature follows in proceeding text.

Item 4, ROM Address indicators IC_8 - IC_0 can be used in conjunction with the Compare Switch to halt the microprogram at any step manually preset on switches SI_9 - SI_0 (SI_9 should always be UP; AUTO/STEP in AUTO mode). Halt occurs when the indicators IC_{8-0} = switch settings. Two other switches control test unit operation: the AUTO/STEP toggle switch and the STEP pushbutton microswitch. With AUTO/STEP in the STEP mode, the microprocessor will complete one cycle each time the STEP pushbutton is depressed. When the AUTO/STEP switch is in the AUTO mode, and the STEP pushbutton is depressed once, the microprocessor begins to cycle continuously.

If a Halt was performed at a desired step by using the COMPARE switch (DOWN = ON), the microprogram will continue if the STEP pushbutton is depressed. To disable the COMPARE halt function, turn the COMPARE switch OFF (UP). The COMPARE feature is useful for stopping the microprocessor so that key points in the microprogram may be monitored. Monitoring key points in the program sometimes reveals exactly where the microprocessor is failing. Also, some failures occur only during full speed ("on the fly") operation and may not occur during manual stepping of given routine.

Again, note that when manually stepping through the microprogram, the IC may not continue past certain locations. This condition could be normal if the present command is a conditional branch command (e.g. a situation where the microprogram branches on itself until a condition is met).

It may be desirable to do a single command repeatedly, particularly if the command is suspected of intermittent failure. To accomplish this, place AUTO/STEP in the AUTO mode, ROM switch OFF (disable ROM output; enable $S_{15} - S_0$ manually simulated command), and depress the STEP pushbutton. The manually set ROM command will execute repetitively.

Generally speaking, a good procedure for manual checkout of the microprocessor would be to manipulate data from register to register, using Register commands and Immediate commands. Control Commands verify communication to CPU or Shugart disk drive. Load Auxiliary commands will verify contents and proper addressing of RAM.

Hands-on use is the most valuable tool for developing solid approaches to microprocessor troubleshooting with these test units.

2.4.4 *6718/7018 REPAIR*

The following items are required to aid in the repair of the 6718/ 7018 board:

1) The outline of the microcode steps involving a format, write and read (Section 2.2.4).
2) The flow charts and microprogram (Section 2.2.4).
3) The 2270 Test/Exercise program (at end of this section).

By using the outline of the microcode steps and the A=B comparator output test point on the 6769 light board, the subroutine in which a failure occurs can be located. The 2270 Test/Exercise program is a necessary aid in checking the manual operation of the microprocessor and the manipulation of data from register to register using register, immediate, control and load auxiliary commands.

TROUBLESHOOTING PROCEDURE

1. Check board visually for shipping or handling damage.
2. Load the board with tested PROMs (if applicable) and RAMs.
3. Check voltages with oscilloscope for noise and proper level.
4. Operate system (attempt a format, write and read) to check for failure.

a. Flex board lightly while operating system to check for possible opens or shorts.

b. Observe 2200 for any error codes.

5. Cut jumpers on board at L100-5 and L87-6 on the 6718 (Do not remove any jumpers on the 7018) and install light board.
6. Recheck voltages to insure against intermittent errors due to increased load.
7. Set the light board switches as follows:
   a) S/R switch must be down or in ROM position.
   b) AUTO/STEP switch to AUTO (up).
   c) ON/OFF switch to ON (Compare switch).
   d) SI9 switch must always be in the up position for testing 6718 and 7018 boards because the ROM only requires 512 addresses.
   e) SI8-0 switches should be set within the failing routine, as listed in the abbreviated microprogram in Section 2.2.4. Preferably the SI switches should be set between the starting or lowest step and the point of failure.

The board is now ready for troubleshooting. As an example, it will be assumed that a 6718 board is failing during a format command (for this example, the board fails at step 002F). The basic approach to locating the step that is failing is to use the abbreviated format routine listed in Section 2.2.4.

Set the IC switches at some address in the middle of the format routine, for instance, step 001F. Depress the format button on the disk. When the program reaches step 001F and stops (with the comparator switch on the light board in the ON position), this indicates that all steps up to but not including step 001F are good. Next, set the IC switches on the light board to 0031. Depressing the format switch again causes the disk to begin formatting, however, because step 002F is faulty (no exclusive OR command), the disk will hang-up and never reach step 0031.

As a result, the problem is known to be somewhere between steps 001F and 0031, and with the same logical approach as above, it will be found that step 002F is failing.

The Test/Exercise program can be used to check basic data manipulation from register to register and a majority of the instructions. As a general rule, if a disk does not complete a format routine, the problem can be found using this program. Under normal conditions, the exercise program should run completely to the end and unconditionally branch to step 0000 and finally prime out at step 00D4 waiting for a 2200 strobe.

To use the test/exercise program, an unconditional branch must be given via the light board to step 01D0. This is accomplished by setting the switches in the following manner:

a) Set the AUTO/STEP switch in the STEP position (down).
b) ON/OFF switch to OFF (UP) or non-compare position.
c) S/R switch to S (up) position.
d) S 15-0 switches to equal $89D0_{16}$.
e) Depress the STEP pushbutton.
f) Put the AUTO/STEP switch to AUTO (up).
g) Place the S/R switch to R (down) and insure that the RI indicators are decoding EC00 (this is the first step of the exercise program).
h) Depress the step pushbutton; this initiates the program.
i) If a failure occurs, use the same procedure as outlined in the above paragraphs.

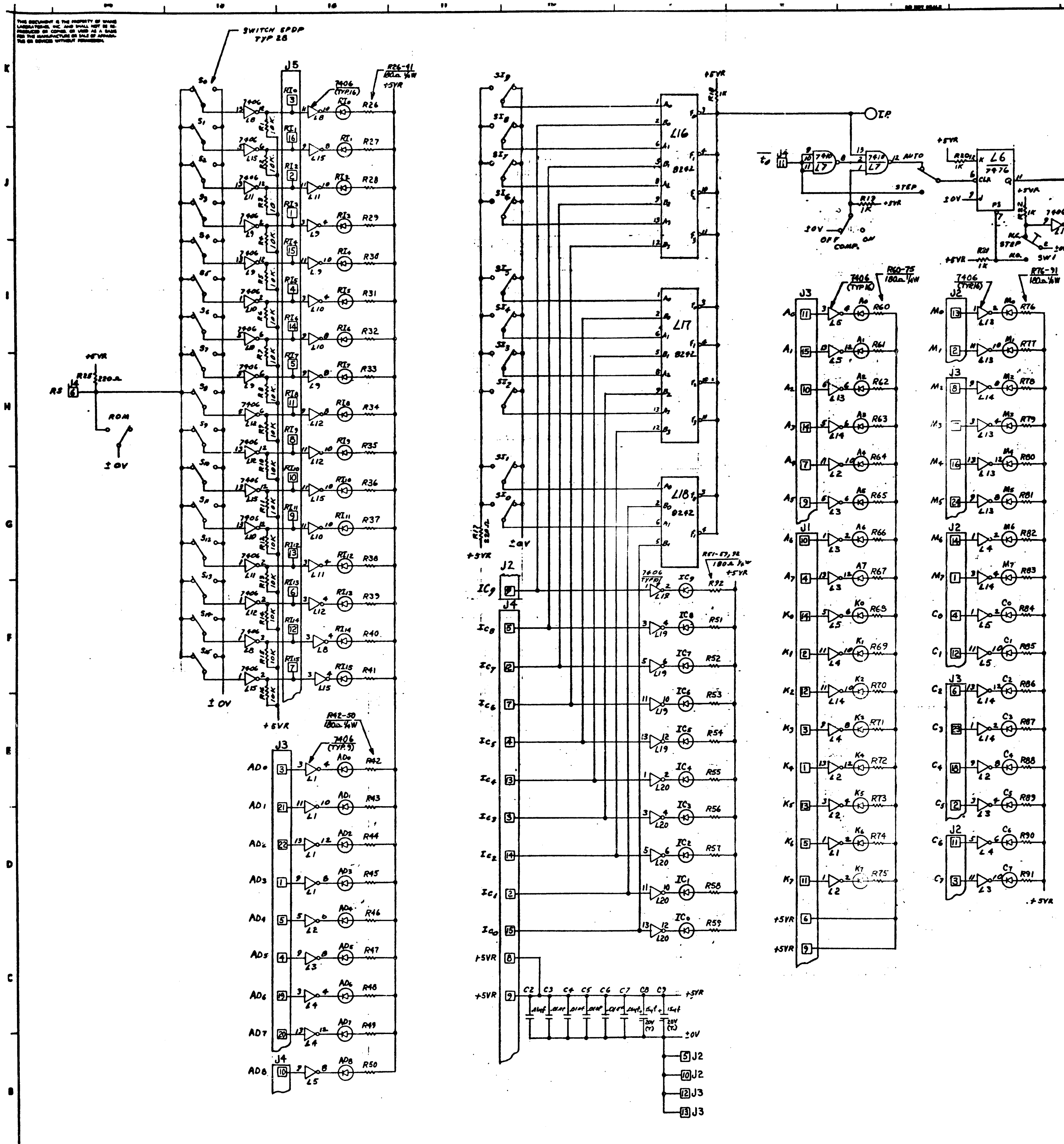
2270 TEST/EXERCISE PROGRAM

STEP	CODE	COMMENTS
01D0	EC00	Turn RDG off. Deselect the disk from A register.
01D1	8C00	Load memory address to 00.
01D2	F900	Clear K register.
01D3	F800	Clear A register.
01D4	C955	Put 55 in K register.
01D5	C8AA	Put AA in A register.
01D6	1000	Puts contents of A register (AA) in Loc. 00. NO PCH or -1.
01D7	5100	⊕ K register with Loc. 00 result should be FF in 00.
01D8	2000	Loc. 00 to A register.
01D9	E801	Add one to A register result 00.
01DA	DCD0	Branch to D0 if A ≠ to 0.
01DB	7D00	AND K register with Loc. 00 PC+1 Result 55 in K.
01DC	9150	Branch to D0 low 4 Bits in K ≠ 5.
01DD	9550	Branch to D0 High 4 bits in K ≠ 5.
01DE	7100	AND K register with Loc. 01.
01DF	4100	OR K register with Loc. 01 result 55 in 01.
01E0	2800	Loc. 01 to A register PC-1 result 55 in A.
01E1	5C00	⊕ A register with Loc. 00 result AA to A register PC+1.
01E2	7C00	AND A register with Loc. 01 result 00 to A register PC+1.
01E3	CCE5	Branch to E5 if A register = 0.
01E4	89D0	Branch to D0 because of ERROR A ≠ 0.
01E5	E801	ADD one to A register.
01E6	1400	A register to present memory address PC+1.
01E7	B2D5	Branch to E5 if AD8 not on.
01E8	1000	FE is contents of A register to Loc. 512.
01E9	2100	Loc. 512 to K register.
01EA	8C00	Set memory address to 00.
01EB	5D00	⊕ K register with Loc. 00 FF + FE result 01 in K PC+1.
01EC	911C	Branch to self if not 01 in K register.
01ED	8C02	Set memory address to 02.
01EE	5100	⊕ memory with K register result to memory.
01EF	2400	Memory to A register PC+1.
01F0	E901	Add one to K register.

01F1	A224	Branch to F4 if AD8 on.
01F2	CCEE	Branch to EE if A = 0.
01F3	89F3	Branch to self if ERROR A ≠ 0.
01F4	FC00	Deselect all disks.
01F5	FC01	Select Disk #3.
01F6	EC80	Load Head D #3.
01F7	FC02	Select disk #2 deselect all others.
01F8	EC80	Load Head D #2.
01F9	FC04	Select disk #1 deselect all others.
01FA	EC80	Load Head D #1.
01FB	B77B	Branch to self head unloaded.
01FC	A78C	Branch to self head loaded.
01FD	A71D	Branch sector mask low.
01FE	B7EE	Branch sector mask High.
01FF	8800	Branch to prime routine.

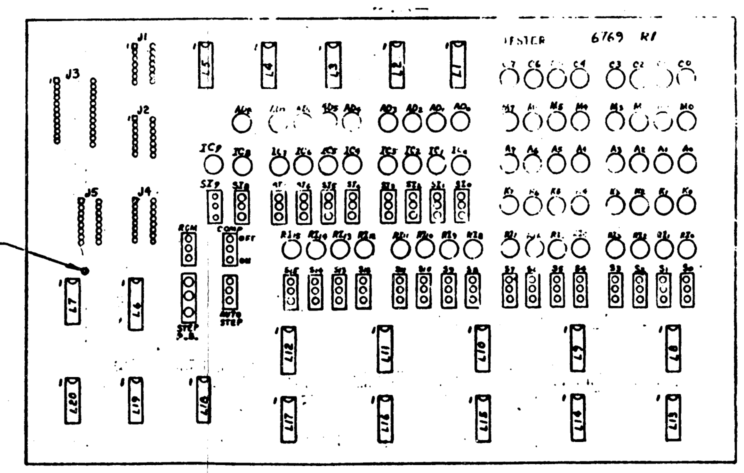
At this point go to Auto and hit the step pushbutton. The program should delay at 01FC for approximately 600 MS until the head unloads; if the sector counter is working the program will increment through 01FD & 01FE to the prime routine.

THIS PAGE INTENTIONALLY LEFT BLANK



LOCATION	W.L. PART No.	±0V	+5VR
L1-5, 8-15, 19, 20	376-0055	7	14
L6	376-0007	13	5
L7	376-0003	7	14
L16, 17, 18	376-0040	7	14

COMPONENT	W.L. PART No.
R1 THRU 16	330-4010
R17, 23, 25	330-2022
R18, 19, 20, 21, 22	330-3010
R24	330-3022
R26-92	330-2018
C1, 8, 9	300-4022
C2, 3, 4, 5, 6, 7	300-1903
SW1	279-0300
SWITCH 2-30	325-0006
LED	370-0026



TESTER

E-REV 1

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION

WANG LABORATORIES, INC. TEWKSBURY MASS. U.S.A.

	BY	DATE	APPROVED BY	DATE
DWN		6-11-75	E ENGR	
CHK		6-13-75	M ENGR	
E C CONTROL			MFG ENGR	

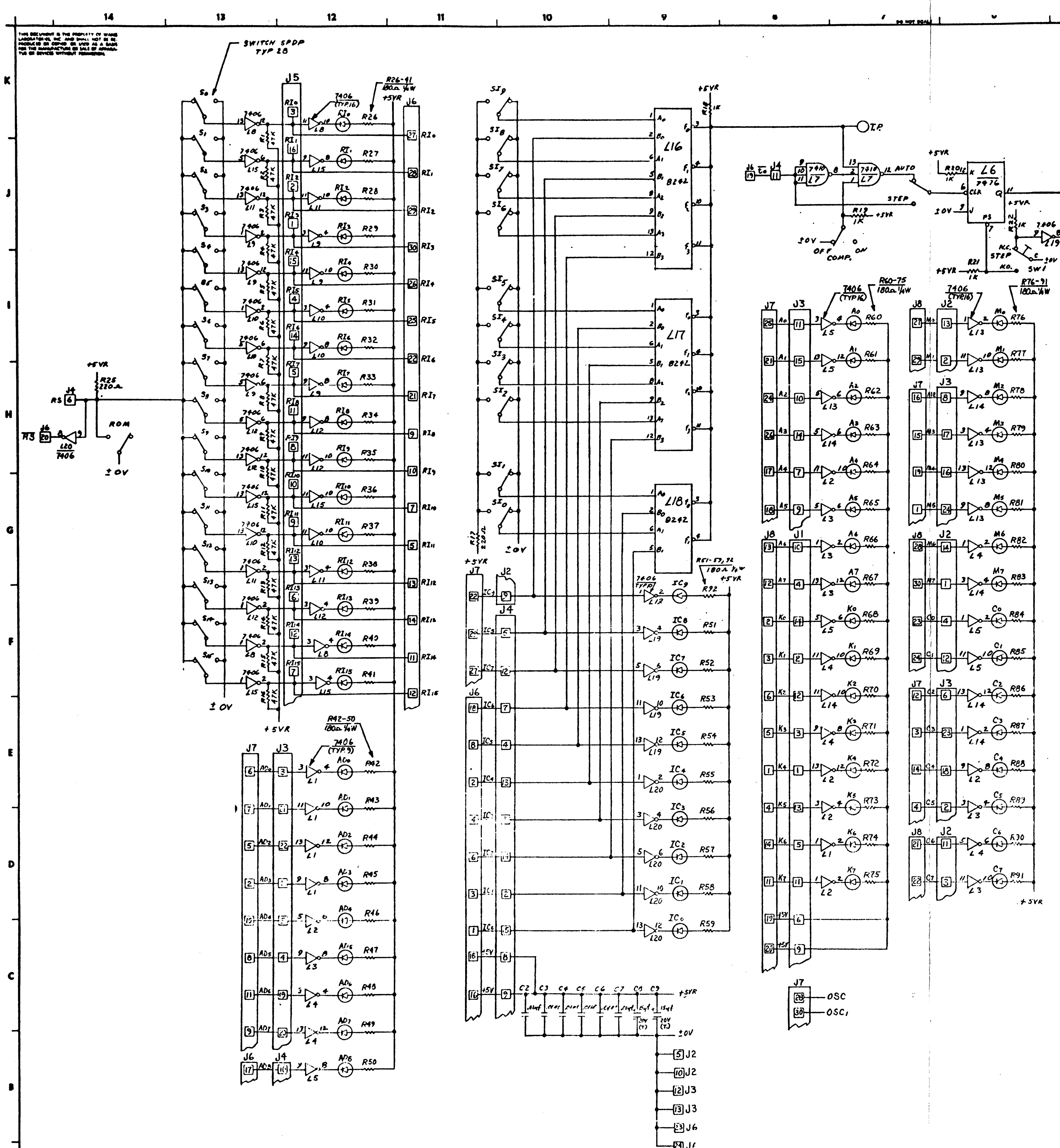
MATERIAL

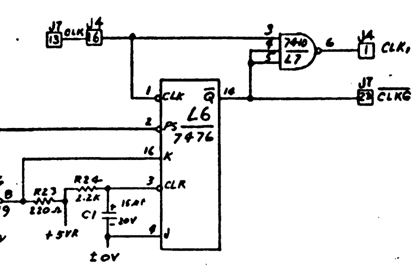
FINISH

MODEL NO WCS-FLOPPY

TITLE SCHEMATIC LOGIBLOC MICROPROCESSOR LIGHT TEST BOARD

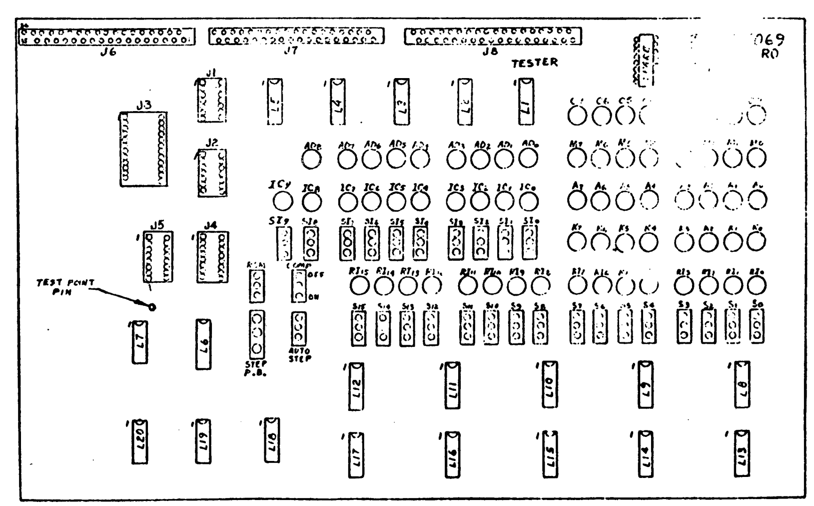
WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-6769	E	6769	1





LOCATION	W.L. PART No	±0V	+5VR
L1-5,8-15, 19, 20	376-0055	7	14
L6	376-0007	13	5
L7	376-0003	7	14
L16,17,18	376-0040	7	14

COMPONENT	W.L. PART No
R1 THRU 16	330-4047
R17, 23, 25	330-2022
R18, 19, 20, 21, 22	330-3010
R24	330-3022
R26-92	330-2018
C1, 8, 9	300-4022
C2, 3, 4, 5, 6, 7	300-1903
SW1	279-0300
SWITCH 2-30	325-0006
LED	370-0026
J1, 2	376-9001
J3	376-9003
J4, 5	376-9002



TESTER

E-REV 0

WANG LABORATORIES INC.

TITLE SCHEMATIC LOGIMEC UNIVERSAL SHUGART FLOPPY TESTER

210-7069 E 7069

THIS PAGE IS INTENTIONALLY LEFT BLANK

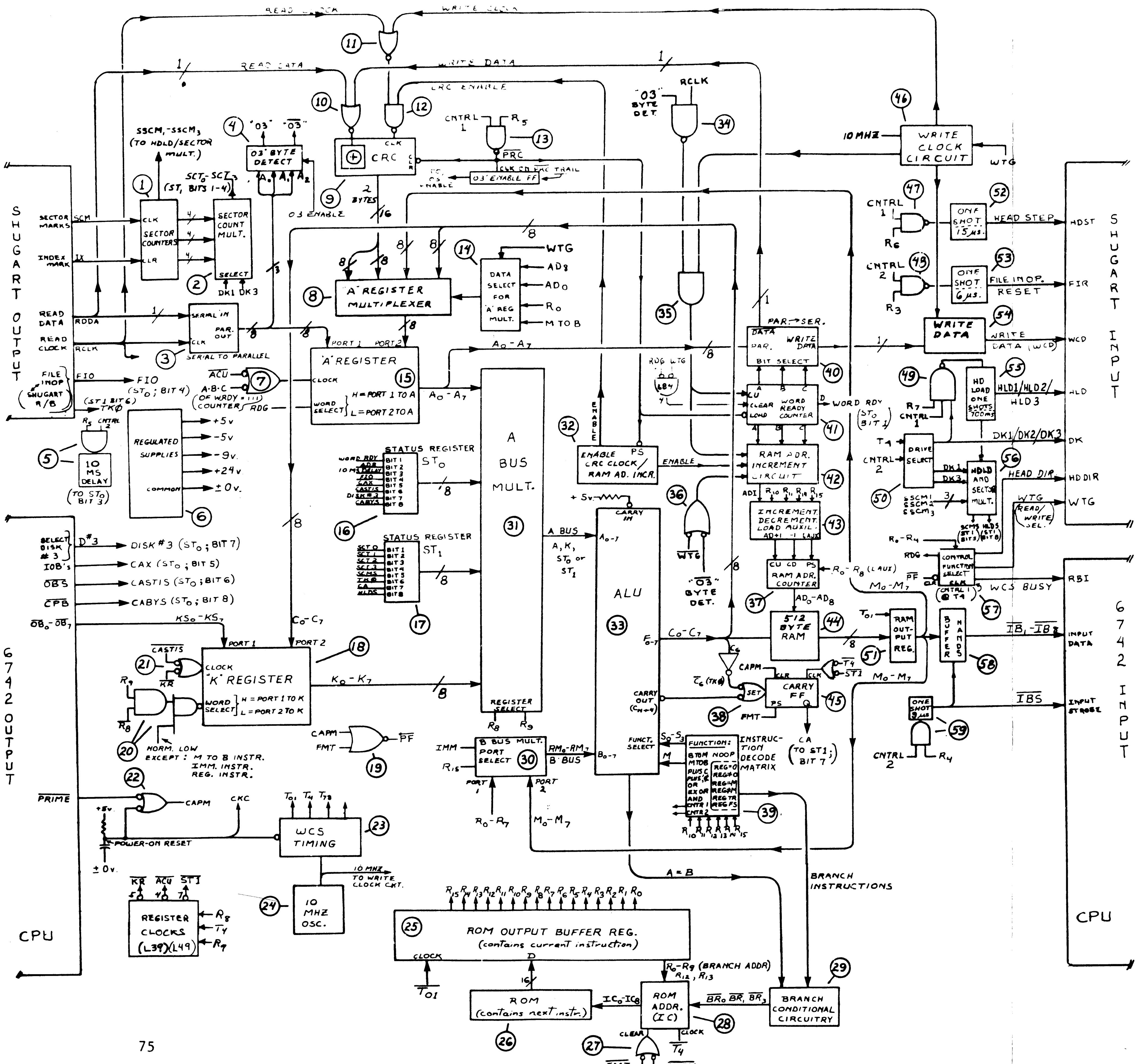
2.5 MODEL 2270 BLOCK DIAGRAM AND SCHEMATICS

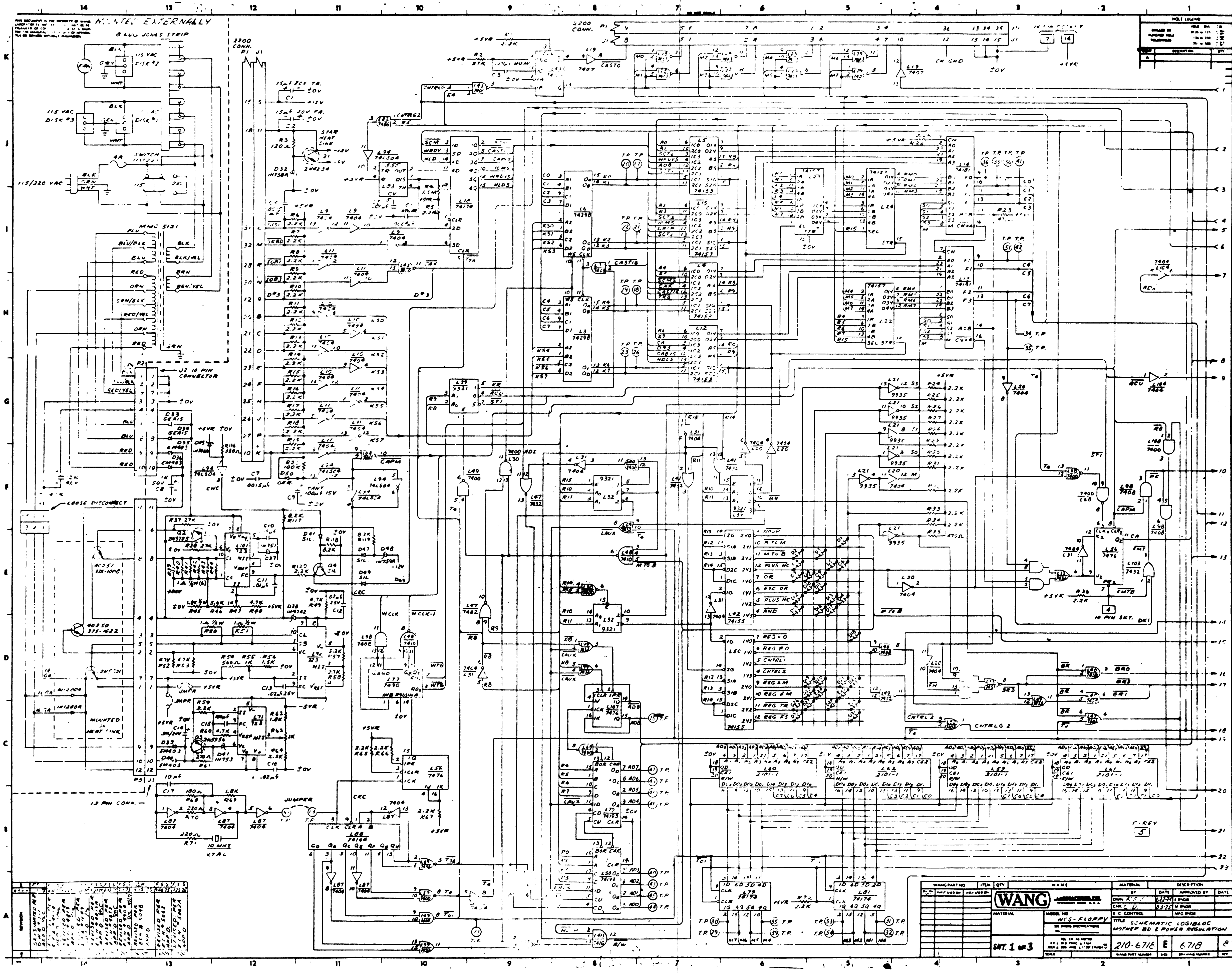
Each block of the diagram to follow is numbered; the integrated circuits which comprise each numbered block are listed below on three pages. The block diagram and the IC listing should be used to further comprehend the "HARDWARE OPERATIONAL THEORY" section of this publication.

BLOCK #	INTEGRATED CIRCUITS UTILIZED
1	L1-12/13, L9-8, L9-6, L8-12/13, L9-4, L8-9/8, L34-8/9/11/12, L17-8/9/11/12, L7-8/9/11/12
2	L16-4/7/9/12, L25-4/7/9/12
3	L2-4, L2-2, L2-12, L73-15, L76-3 thru 6 and 10 thru 13.
4	L95-11, L84-13, L73-10/11
5	L82-3, L94-10, L83-3
6	L71, L92, L108
7	L74-11, L104-2
8	L38, L55, L54, L37
9	L53, L36, L45, L46-6, L46-3, L46-11
10	L72-11
11	L74-8
12	L95-6
13	L51-6
14	L102-8, L102-6, L102-11, L102-3, L72-6, L72-8, L82-8, L46-8, L1-8/9
15	L67, L66
16	L18, L5, L15, L4, L12
17	L18, L5, L15, L4, L12
18	L11, L10, L6, L3
19	L98-3
20	L30-11, L47-10, L31-6, L48-6

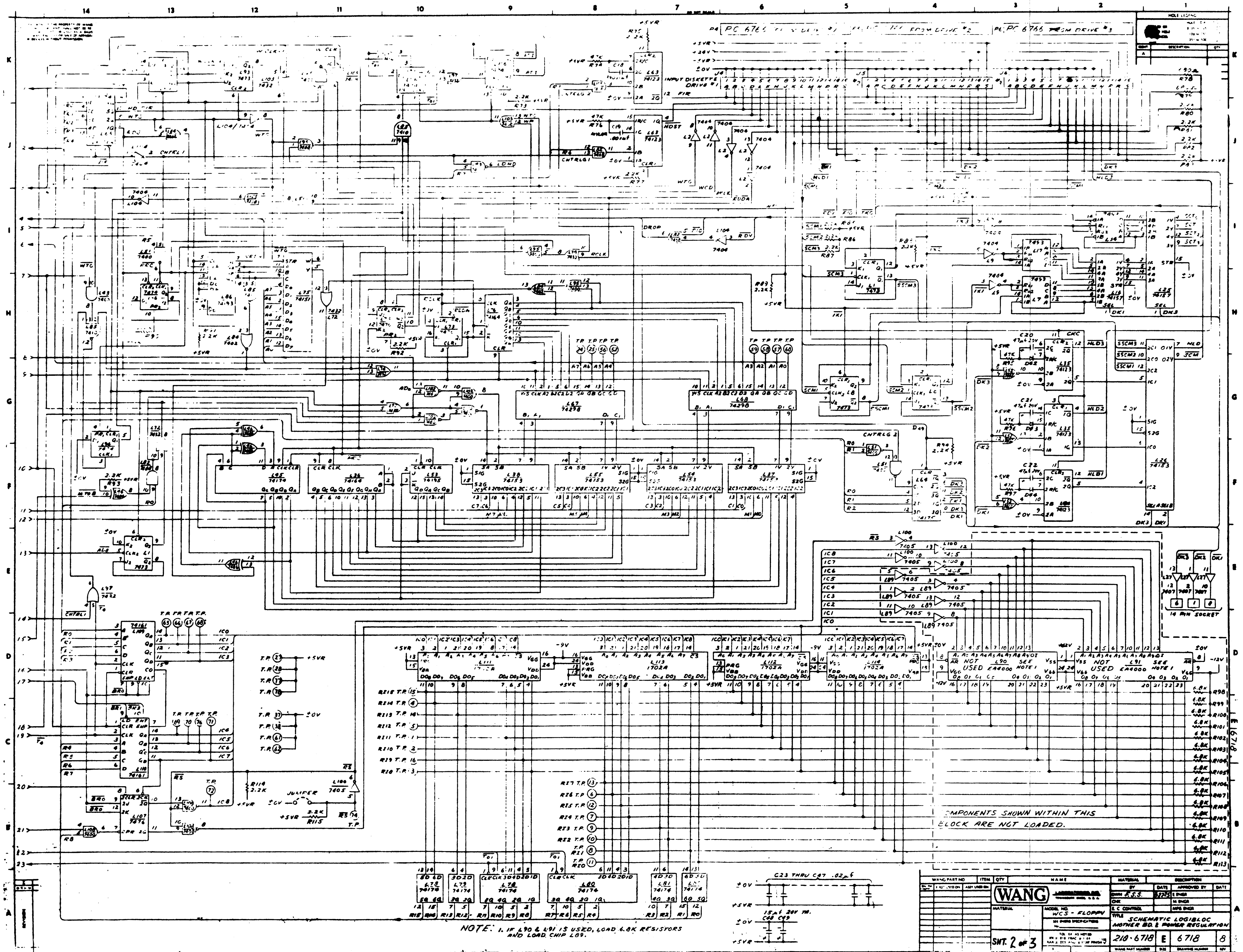
BLOCK #	INTEGRATED CIRCUITS UTILIZED
21	L30-3
22	L11-8, L94-12, L84-10, L94-4
23	L88, L87-10, L87-8, L69-3, L57-8, L49-8, L99-11
24	L87-2, L87-4, L87-6
25	L78-12/15/2/5/9/10, L80-12/15/2/5/7/10, L81-7/10
26	L111, L113, L112, L114-(Present) L90, L91-(Future)
27	Same as Block #19 (L98-3)
28	L109, L110 L107, L108-8, L108-11; For future: add L89-8, 10, 12, 2, 6, 4, also L100-2, 4, 6, 8, 10, 12
29	L40-8, L40-3, L40-6, L49-11, L20-10, L33-8, L69-11, L47-4, L108-3, L108-6, L21-6, L98-6
30	L22, L23, L24
31	L5, L15, L4, L12
32	L96-5 (Both Enables)
33	L13, L14
34	L51-8
35	L105-6
36	L95-3
37	L107, L70, L58, L99-6, L99-3, L68-3
38	L31-18, L33-6
39	L42, L50, L31-12, L21-12, L21-10, L21-8, L21-2, L20-12, L21-4
40	L75-6/5

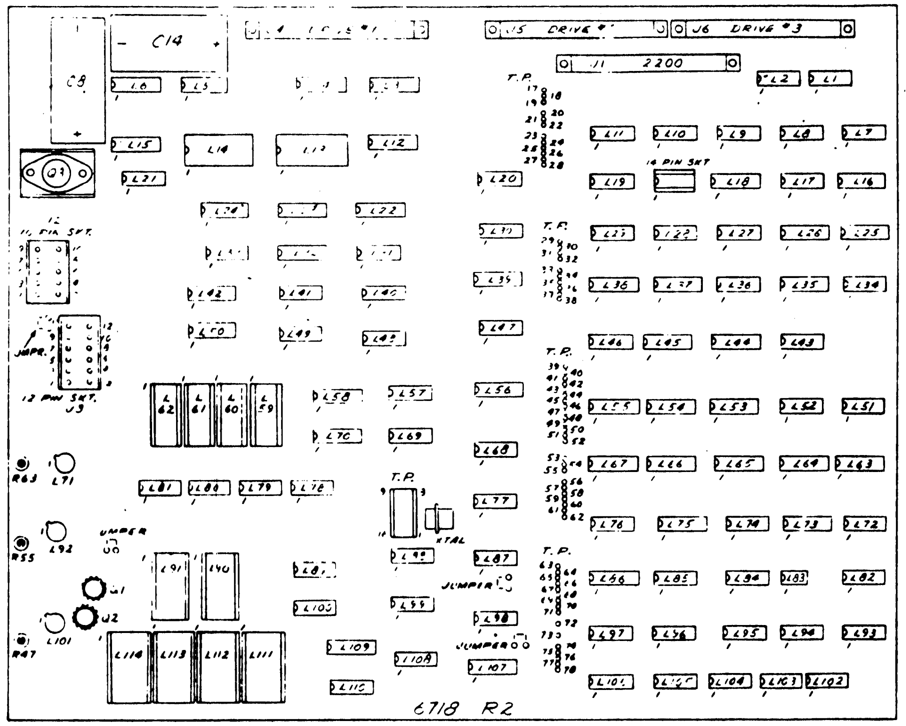
BLOCK #	INTEGRATED CIRCUITS UTILIZED
41	L86-2/3/6/7
42	L85-8, L85-6, L85-12, L106-6, L104-6, L97-3, L97-11, L106-8/9, L43-8, L84-1
43	L47-13, L69-8, L41-6, L41-8
44	L48-12, L47-1, L60, L62, L59, L41
45	L56-11, L68-8, L68-11, L20-2
46	L56-15, L77-8/9/11/12, L98-11, L48-8, L93-12/13, L93-8, L103-6
47	L82-11
48	L105-3
49	L43-6, L52-10, L52-13, L52-4
50	L52-1, L51-3, L51-11, L64-2/3/6/10/11
51	L79-2/10/12/15, L81-2, 5, 12, 15
52	L63-4
53	L63-12
54	L95-8, L105-8, L2-10
55	L35-5/12, L35-4/13, L44-5/12
56	L26
57	L97-6, L65-2/5/7/12, L19-12
58	L28-3, L28-6, L28-8, L28-11, L29-3, L29-6, L29-8, L29-11
59	L43-3, L44-4/13, L19-8


SHUGART OUTPUT
SHUGART INPUT
6742 OUTPUT
6742 INPUT
CPU
CPU
CRC
03 BYTE DETECT
SECTOR COUNTERS
SECTOR COUNT MULT.
'A' REGISTER MULTIPLEXER
DATA SELECT FOR 'A' REG MULT.
'A' REGISTER
A BUS MULT.
ALU
'K' REGISTER
STATUS REGISTER ST_0
STATUS REGISTER ST_1
REGULATED SUPPLIES
WRITE CLOCK CIRCUIT
WRITE DATA
WORD READY COUNTER
RAM ADR. INCREMENT CIRCUIT
INCREMENT DECREMENT LOAD AUXIL.
RAM ADR. COUNTER
512 BYTE RAM
RAM OUT-PUT REG.
CARRY FF
ENABLE CRC CLOCK/ RAM AD. INCR.
B BUS MULT. PORT SELECT
INSTRUCTION DECODE MATRIX
WCS TIMING
10 MHZ OSC.
REGISTER CLOCKS (L39)(L49)
ROM OUTPUT BUFFER REG. (contains current instruction)
ROM (contains next instr.)
ROM ADDR. (IC)
BRANCH CONDITIONAL CIRCUITRY
BRANCH INSTRUCTIONS
POWER-ON RESET
HEAD STEP
FILE INOP. RESET
WRITE DATA (WCD)
HEAD DIR
WCS BUSY



MOUNTED EXTERNALLY
WANG
WCS - FLOPPY
SCHEMATIC LOGIBLOC
MOTHER BD & POWER REGULATION
SHT. 1 OF 3
210-6716
E
6718


PC 6765 FROM DRIVE #3
INPUT DISKETTE DRIVE
COMPONENTS SHOWN WITHIN THIS
BLOCK ARE NOT LOADED.
C23 THRU C47 .02µf
15µf 20V TN.
C48 C49
14 PIN SOCKET
JUMPER
NOTE: 1. IF L90 & L91 IS USED, LOAD 6.8K RESISTORS AND LOAD CHIP L89.
WANG
MODEL NO. WCS - FLOPPY
TITLE SCHEMATIC LOGIBLOC MOTHER BD. & POWER REGULATION
SHT. 2 OF 3
210-6718
E
6718
8
DWN F.S.S.



IC	LOCATION SHEET 1	LOCATION SHEET 2	IC	LOCATION SHEET 1	LOCATION SHEET 2
L1		E13, H5	L58	B8	
L2		J7, J6	L59	C3	
L3	H8		L60	C6	
L4	I7		L61	C2	
L5	J7		L62	C5	
L6	I8		L63		K7, J7
L7		H3	L64		F4
L8		G5, G4	L65		J14
L9	I11, I10	I3	L66		G6
L10	H11		L67		G8
L11	I11, G11		L68	C8, F2	
L12	H7		L69	B10, F8, D3	
L13	I4		L70	B8	
L14	J4		L71	C12	
L15	I7		L72		H11, G13, G10
L16		H2	L73		H10
L17		I3	L74		I8, G11
L18	I10		L75		H11
L19	K8, K4		L76		H9
L20	F6, G5, G3, F5, D4		L77	D10	
L21	G5, F5		L78		A10, A9
L22	H5		L79	B6	A10
L23	J5		L80		A8, B7
L24	I5		L81	B5	B7
L25		H1	L82	J10	F13, J8, I7
L26		F2	L83	I10	
L27		E1	L84	F11	J13, H12, H9
L28	K7		L85		H14, H12, J10
L29	K6	H14	L86		H12
L30	I8, F9, E8, A9		L87	B12, B11, A11	
L31	G7, F8, D9, E7, E2		L88	B11	
L32	F8, D8		L89		E5
L33	D3, E2		L90		D3
L34		I2	L91		D2
L35		G3, F3	L92	D11	
L36		F11	L93		K13, K12
L37		F6	L94	J10, F13, F11	
L38		F9	L95		K11, J11, I9
L39	G10, F6		L96		H13, F14
L40	F8, D5, D2		L97		E14, K10
L41	F7, A9		L98	D11, F2	
L42	E6		L99	A10, D8	
L43	I10	J9	L100		E4, B11
L44	K8	F3	L101	E12	
L45		F12	L102		G10
L46		F14, F12, E12	L103	E2	K12
L47	F9, E9, A9, C2		L104	G1	J13, J12, I6
L48	D10, E8, A8		L105		I12, K11, J9, J8
L49	A10, F9, D5		L106		K10, K9
L50	D6		L107	D8	E14
L51		I11, I13, F5	L108	G1	E14, E13
L52	D4	G3, F3	L109		D13
L53		F10	L110		C13
L54		F7	L111		D9
L55		F8	L112		D6
L56	C10, E2		L113		D7
L57	A10		L114		D5

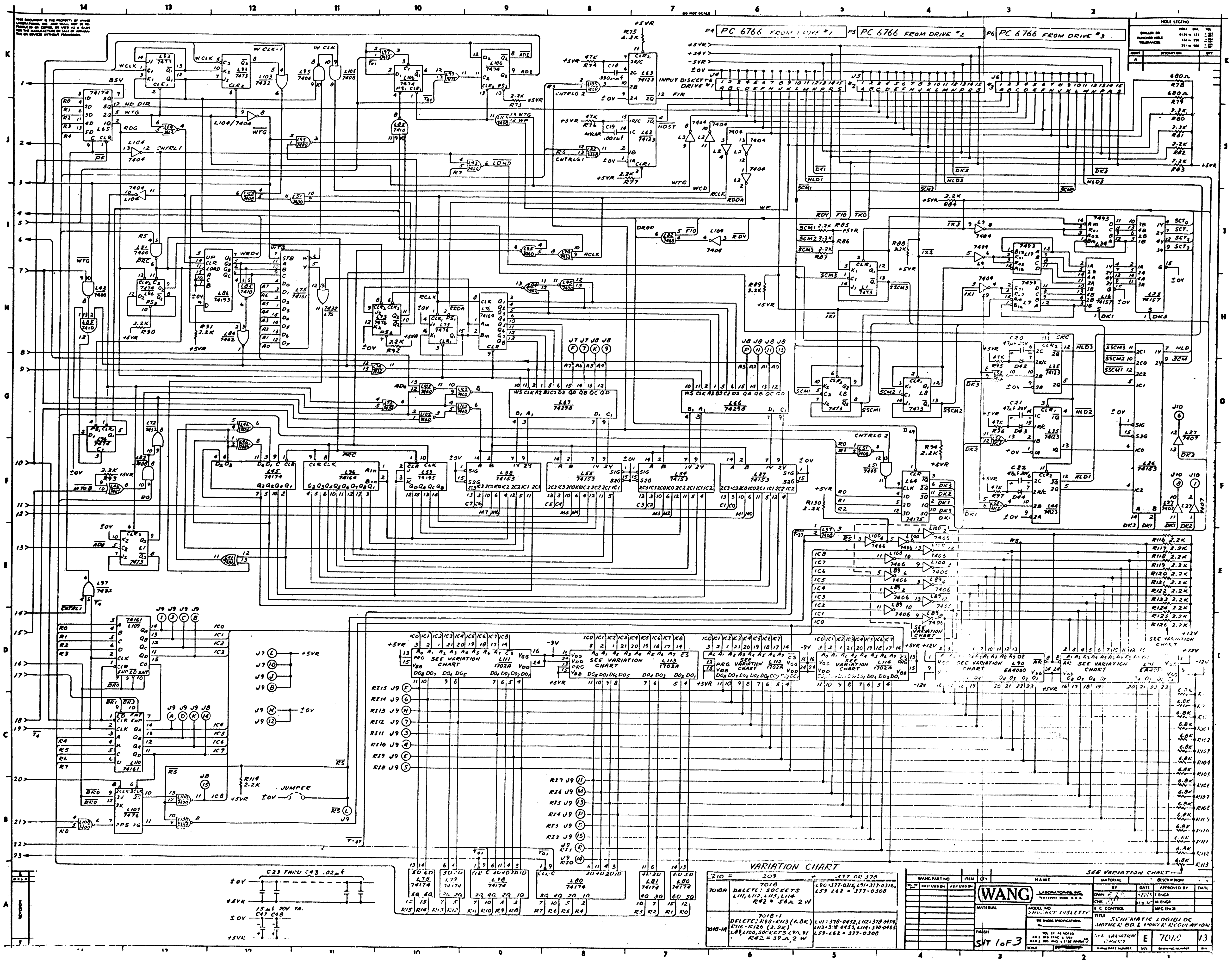
I.C. LOCATION	W.L. NO.	TERM ±0V	TERM +5VR
L1, 8, 93	376-0005	11	4
L2, 9, 10, 11, 20, 31, 87, 104	376-0010	7	14
L3, 6, 66, 67	376-0138	8	16
L4, 5, 12, 15, 26, 37, 38, 54, 55	376-0048	8	16
L7, 17, 34	376-0011	10	5
L13, 14	376-0099	12	24
L16, 22, 23, 24, 25	376-0082	8	16
L18, 45, 65, 78, 79, 80, 81	376-0098	8	16
L19, 27	376-0056	7	14
L21	376-0025	7	14
L28, 29	376-0028	7	14
L30, 43, 51, 69, 75, 102, 108	376-0002	7	14
L32, 39	376-0096	9	18
L33	376-0012	7	14
L35, 44, 63	[illegible]	5	11
L36, 76, 88	376-[illegible]	7	14
L40, 57, 82, 98, 105	376-[illegible]	7	14
L41, 68, 72, 74, 97, 99, 103	376-0003	7	14
L42, 50	376-0049	8	16
L46	376-0036	7	14
L47, 52, 84	376-0016	7	14
L48, 85	376-[illegible]	7	14
L53	376-0057	8	16
L56, 73, 107	376-0007	13	5
L58, 70, 86	376-0053	8	16
L59, 60, 61, 62	377-0308	8	[illegible]
L64	376-0119	8	16
L71, 92, 101	376-0066		
L75	376-0047	8	16
L77	376-0073	10	5
L83	376-0126	1	8
L89, 100	376-0029	7	14
L90, 91			24
L96, 106	376-0006	7	14
L109, 110	376-0094	8	16
L111	378-0452R1		12
L112	378-0454R1		12
L113	378-0453R1		12
L114	378-0455R1		12
L94	376-0180	7	14

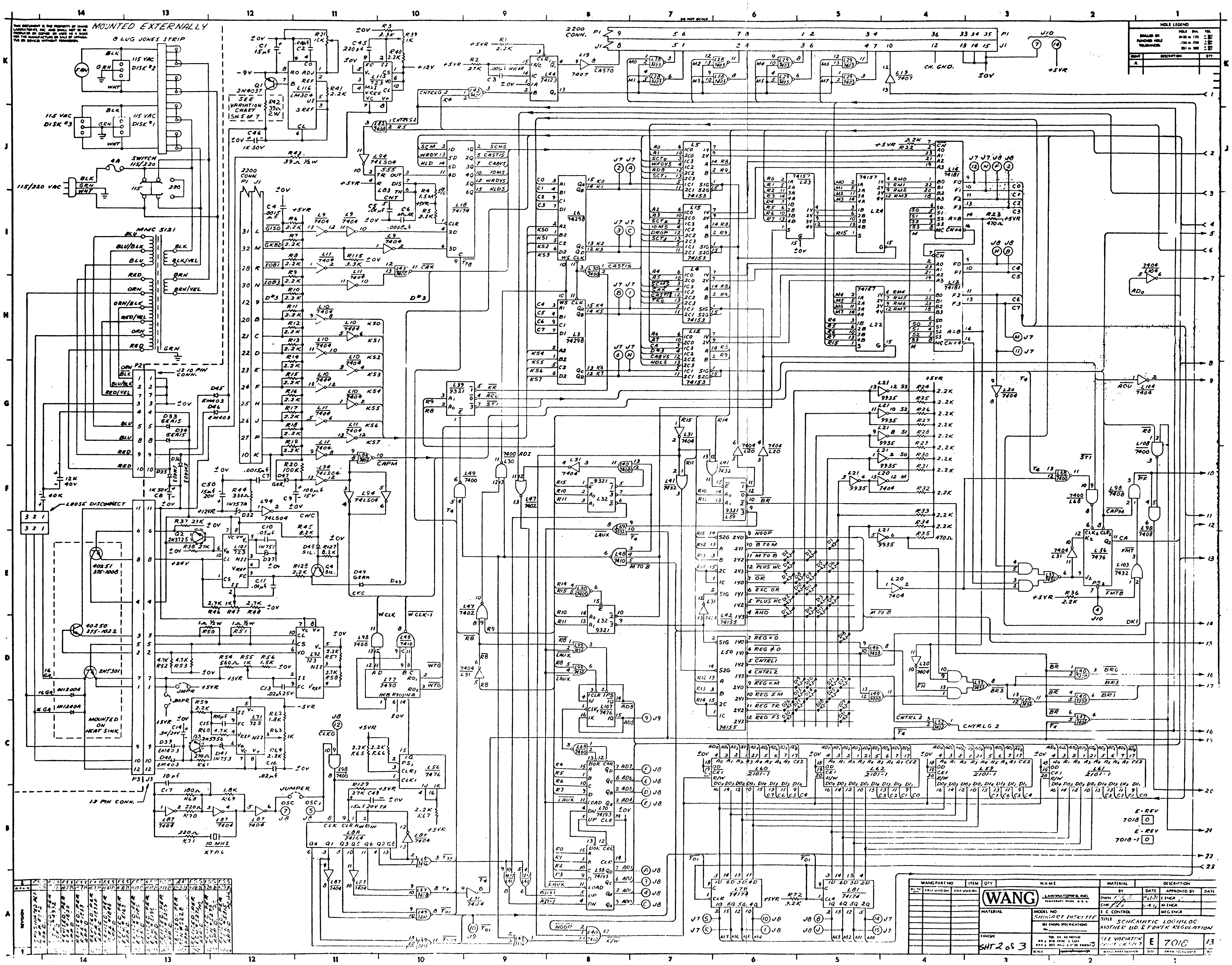
COMPONENT	W.L. NO.
R1, 5-19, 22, 24-34, [illegible], 57, 59, 64-67, 72, 73, 75, 77, [illegible] 93, 114, 115, 120	330-3022
R2, 37, 38	330-4027
R3	330-[illegible]
R4	330-6016
R20	330-5016
R23, 35	330-2047
R39-44, 50, 51	[illegible]
R45	[illegible]
R46	330 [illegible]
R47, 55, 63	[illegible]
R48, 49, 52, 53, 60	[illegible]
R54	[illegible]
R56	330-2015
R58	[illegible]
R61	330-[illegible]
R62, 69	[illegible]
R68	330-2018
R70, 71	330-2022
R74, 76, 95-97	330-4047
R78, 79	330-2068
R98-113	330-3068
R116	330-2033
R117-119	330-3082
C1, 2, 48, 49	300-4022
C3, 19	300-2010
C4, 7	300-1907
C5, 11	300-[illegible]
C6	300-[illegible]
C8	300-3055
C20-22	300-4034
C10	300-1900
C12, 13, 16, C23-47	300-1904
C14	300-3054
C15	300-1100
C17	300-10[illegible]0
C18	300-[illegible]
C9	300-4021
XTAL	321-3008
[illegible]1-31, 42-44, 46, 47	[illegible]90-1001
D32	380-2100
D33, 34	380-3004
D35, 36, 39, 40	380-4000
D37	380-2051
D38	[illegible]
D41	380-2062
D45	380-2013
Q1	375-1024
Q2	375-1027
Q3	375-1031
TRANSIPAD (LG)	375-9001
HEATSINK (BIRTCHTER)	375-9010
D48	350-2120
D49	369-1004
D50	380-0000
Q4	375-1006

COMPONENT	W.L. NO.
J1, 4-6	[illegible]
J2	654-1188
J3	654-11[illegible]
T.P. SKT LOW PROFILE	654-1157
16 PIN I.C. SOCKET	376-9002
24 PIN I.C. SOCKET	376-9003
I.C. PAD 16 PIN	376-9008
12 PIN I.C. SOCKET	376-9010
14 PIN I.C. SOCKET	376-[illegible]012

SHT. 3 OF 3

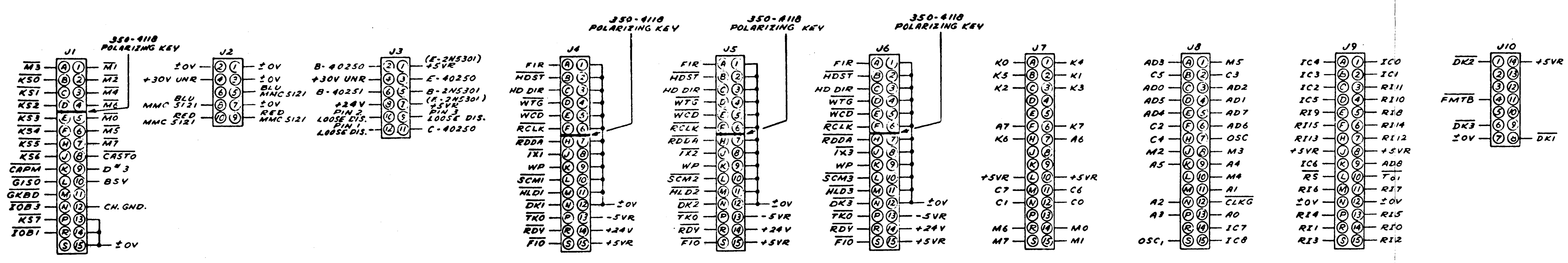
6718

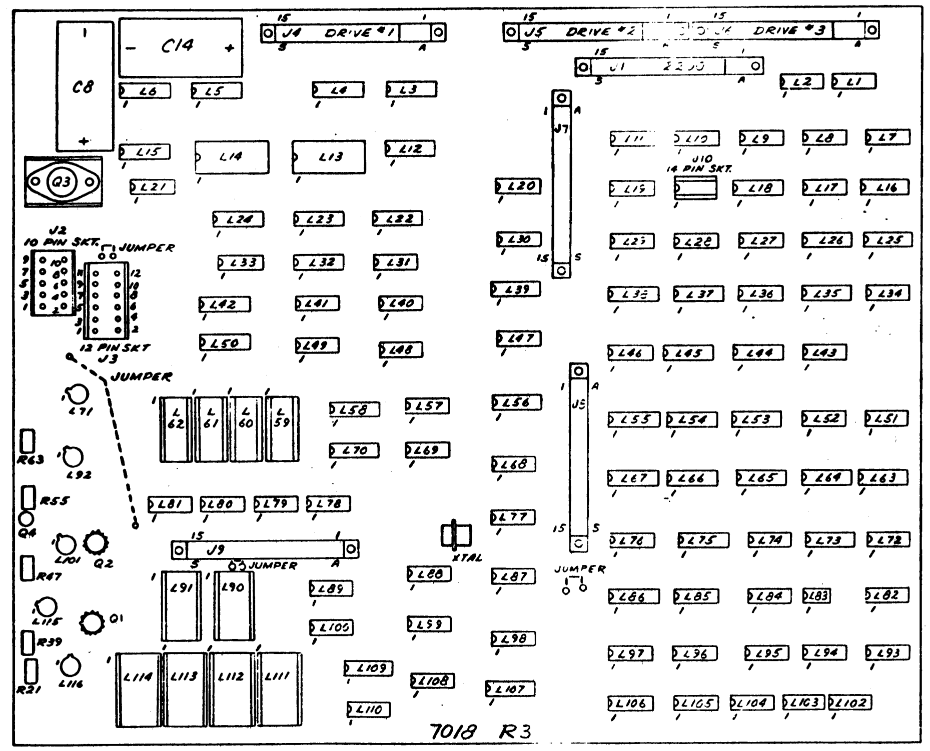

PC 6766 FROM DRIVE #1
PC 6766 FROM DRIVE #2
PC 6766 FROM DRIVE #3
VARIATION CHART
SEE VARIATION CHART
WANG LABORATORIES, INC.
MODEL NO SHUGART DISKETTE
TITLE SCHEMATIC LOGIBLOC MOTHER BD & POWER REGULATION
SHT 1 OF 3
E 7018 13



MOUNTED EXTERNALLY
8 LUG JONES STRIP
115/220 VAC
MMC 5121
LOOSE DISCONNECT
MOUNTED ON HEAT SINK
12 PIN CONN.
2200 CONN.
HOLE LEGEND
E-REV
7018
7018-1
WANG
LABORATORIES, INC.
MODEL NO SHUGART DISKETTE
TITLE SCHEMATIC LOGIBLOC MOTHER BD. & POWER REGULATION
SEE VARIATION CHART SHEET 7
E
7018
13
SHT 2 of 3

HOLE LEGEND





I.C. LOCATION	W.L. NO.	TERM ±OV	TERM +5VR
L1,8,93	376-0005	11	4
L2,9,10,11,20,31,87,104	376-0010	7	14
L3,6,66,67	376-0138	8	16
L4,5,12,15,26,37,38,54,55	376-0048	8	16
L7,17,34	376-0011	10	5
L13,14	376-0099	12	24
L16,22,23,24,25	376-0082	8	16
L18,45,65,78,79,80,81	376-0098	8	16
L19,27	376-0056	7	14
L21	376-0025	7	14
L28,29	376-0028	7	14
L30,43,49,51,68,95,102,108	376-0002	7	14
L32,39	376-0096	8	16
L33	376-0012	7	14
L35,44,63	376-0080	8	16
L36,76,88	376-0102	7	14
L40,57,82,98,105	376-0081	7	14
L41,69,72,74,97,99,103	376-0093	7	14
L42,50	376-0049	8	16
L46	376-0036	7	14
L47,52,84	376-0016	7	14
L48,85	376-0003	7	14
L53	376-0097	8	16
L56,73,107	376-0007	13	5
L58,70,86	376-0053	8	16
L59,60,61,62	377-0308	8	22
L64	376-C119	8	16
L71,92,101,115	376-0066		
L75	376-0047	8	16
L77	376-0073	10	5
L83	376-0126	1	8
L89,100	376-0055	7	14
L90,91			24
L96,106	376-0006	7	14
L109,110	376-0094	8	16
L111	378-0452R1		12
L112	378-0454R1		12
L113	378-0453R1		12
L114	378-0455R1		12
L94	376-0180	7	14
L116	376-0134	9	

COMPONENT	W.L. NO.
R40,41,128,130,116-126 R1,5-19,22,24-34,36,57,59 64-67,72,73,75,77,80-94,114	330-3022
R2,37,38,129	330-4027
R3,115	330-3073
R4	330-6016
R20	330-5010
R31	336-1015
R23,35	330-2047
R42	337-1039
R45,127	330-3082
R50,51	331-0010
R39,47,55,63	336-1014
R52,53,60	330-3047
R54	330-2056
R56	330-3015
R46,48,58	330-3027
R61	330-2027
R62,69	330-3018
R68	330-2018
R70,71	330-2022
R74,76,95-97	330-4047
R78,79	330-2068
R98-113	330-3068
R44	330-2033
C1,47,48,49,50	300-4022
C3,19	300-2010
C4,7	300-1907
C5,11	300-1903
C6	300-2068
C8,46	300-3055
C2	300-1906
C10	300-1900
C13,16,C23-43	300-1904
C14	300-3054
C15	300-1100
C17	300-1010
C18	300-1390
C9	300-3011
C45	300-1220
XTAL	321-0006
D1-31,42-44,48	380-1001
D32	380-2031
D33,34	380-3004
D35,36,39,40,45,46	380-4000
D37	380-2051
D41	380-2062
D47,49	380-0000
C20-22	300-4034
Q1	375-0016
Q2	375-1027
Q3	375-1031
Q4	375-1006
TRANSIPAD (LG)	375-9001
HEATSINK (BIRTCHER)	375-9010
R42 SEE VARIATION CHART SH.5 OF 7	331-1056 (7018) 337-1039 (70..)

COMPONENT	W.L. NO.
J1,4-9	350-0011
J2	654-1188
J3	654-1172
T.P. SKT. LOW PROFILE	654-1157
16 PIN I.C. SOCKET	376-9002
24 PIN I.C. SOCKET	376-9003
I.C. PAD 16 PIN	376-9008
22 PIN I.C. SOCKET	376-9010
14 PIN I.C. SOCKET	376-9012
POLARIZING KEY	350-4118

I.C. TYPE	LOCATION	SPARES
7400	L30	1
7400	L49	1
7400	L68	1
7404	L2	1
7404	L11	1
7407	L19	4
7407	L27	3
7408	L57	2
7432	L63	1
7432	L72	1
7432	L74	2
7432	L97	1
7432	L99	1
7432	L103	2
74LS04	L94	1

ECN NO. PENDING

ECN NO. 3604 Pa.a PENDING 7018

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

BY	DATE	APPROVED BY	DATE
DWN F.S.S.		E ENGR	
CHK		M ENGR	
E C CONTROL		MFG ENGR	

MATERIAL

MODEL NO ... FLOPPY

SEE ENGRG SPECIFICATIONS No.

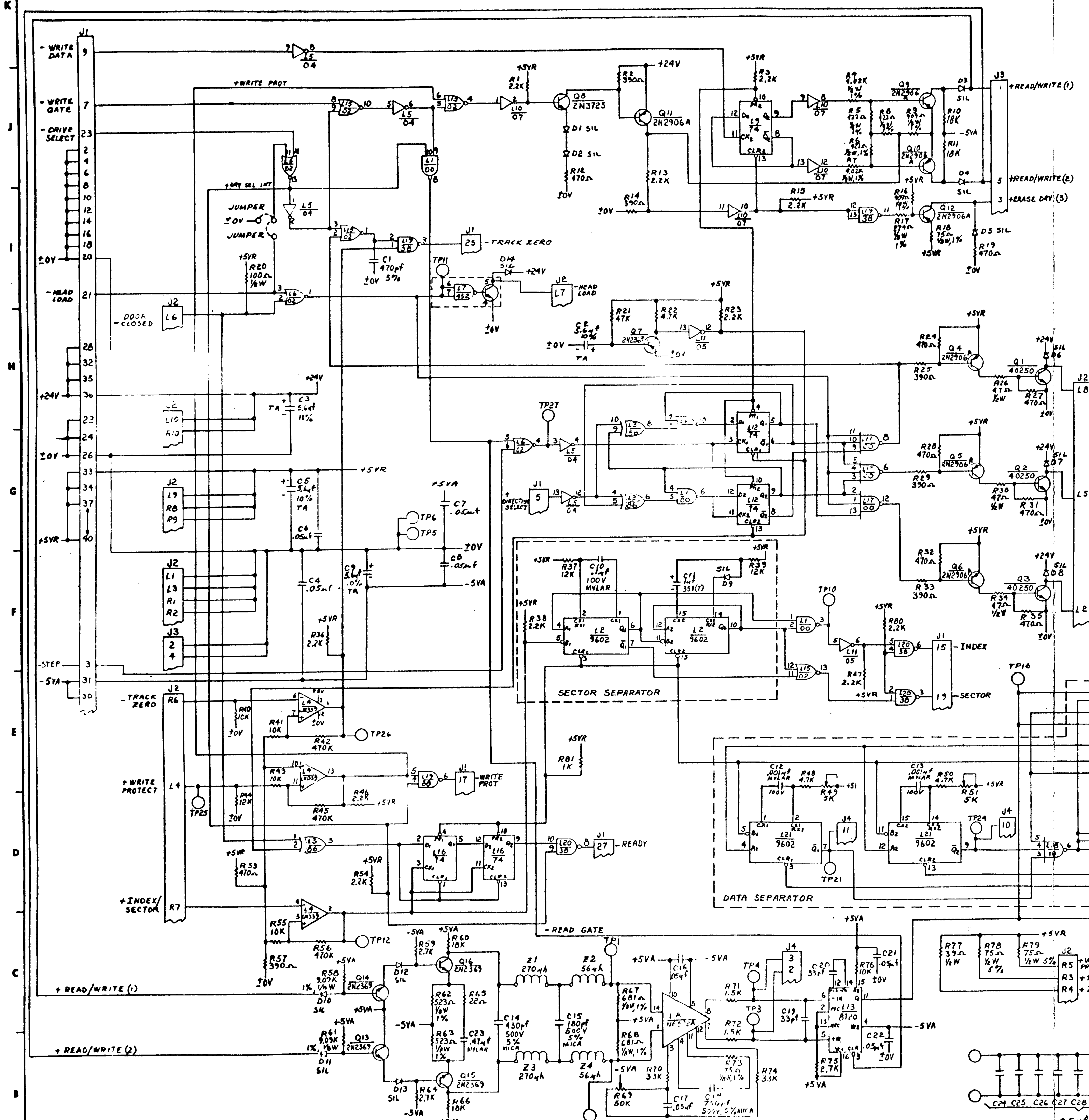
FINISH SHT 3 of 3

TOL EX. AS NOTED

SCALE

TITLE MOTHER BOARD & PARTS LIST

210-7018 | E | 7018



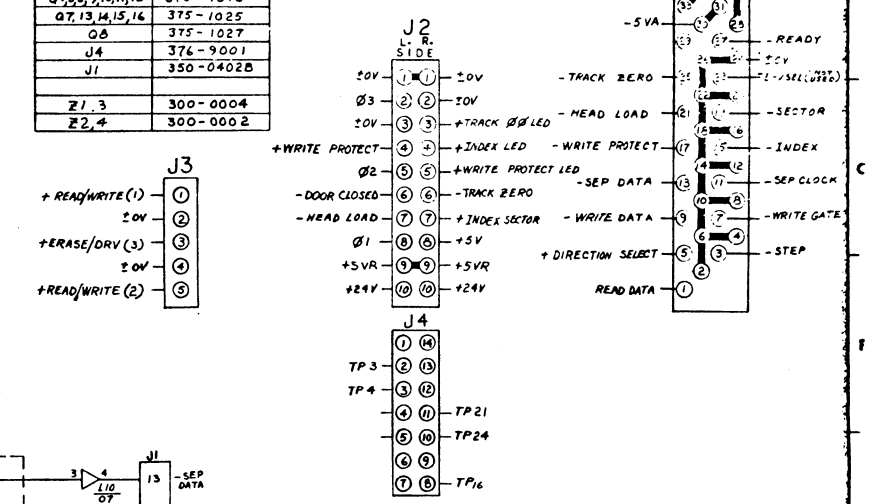
LOCATION	W.L. PART NO.	TERM. NO. ±0V	TERM. NO. Vcc+5VR
L1,14	376-0002	7	14
L2,21	376-0104	8	16
L3	376-0036	7	14
L4	376-0240	12	3
L6,15,	376-0016	7	14
L7	376-0145	4	8
L8	376-0239		10
L9,12,16	376-0006	7	14
L10	376-0056	7	14
L11	376-0029	7	14
L13	376-0241	8	
L17,18	376-0003	7	14
L19,20	376-0128	7	14
L5	376-0010	7	14

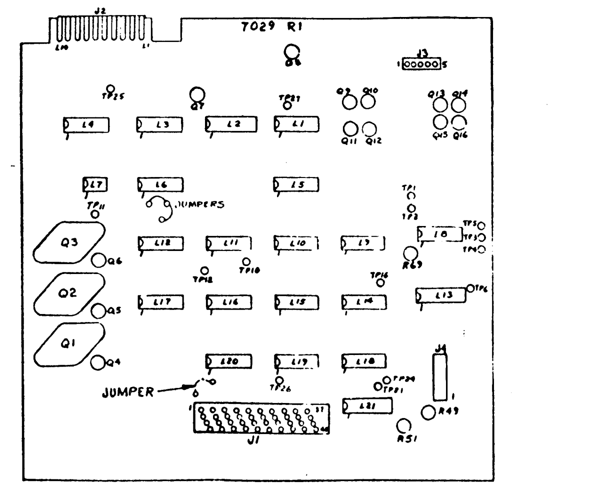
COMPONENT	W.L. PART NO.
C1	300-1471
C2,3,5,9	300-4017
C4,17,6-8,16,21,22,24-35	300-1900
C10	300-2210
C11	300-4000
C12,13	300-2010
C14	300-5015
C15	300-5001
C18	300-5014
C19,20	300-1033
C23	300-2247
D1-14	380-1001
Q1,2,3	375-1022
Q4,5,6,9,10,11,12	375-1016
Q7,13,14,15,16	375-1025
Q8	375-1027
J4	376-9001
J1	350-04028
Z1,3	300-0004
Z2,4	300-0002

COMPONENT	W.L. PART NO.
R1,3,15,23,36,38,46,47,54,13,80	330-3022
R2,14,25,29,33,57	330-2039
R4,7	333-0060
R5,6,8	333-0056
R9,16	333-0059
R10,11,60,66	330-4018
R12,19,24,27,28,31,32,35,53	330-2047
R17	333-0055
R78,79	331-1076
R20	331-2010
R21	330-4047
R22,48,50	330-3047
R26,30,34	331-1047
R37,39,44	330-4012
R40,41,43,55,76	330-4010
R42,45,56	330-5047
R49,51	336-1020
R52,81	330-3010
R58,61	333-0061
R59,64,75	330-3027
R62,63	333-0057
R65	330-1022
R67,68	333-0058
R69	336-0017
R70,74	330-4033
R71,72	330-3015
R18,73	333-0054
R77	331-1039

SPARES

I.C. CHIPS	LOCATION	NO. OF SPARES
7400	L1	1
7486	L3	1
7404	L5	1
75452	L7	1
7405	L11	4
7410	L18	1
7438	L20	1
LM339	L4	1





COMPONENT LAYOUT

1. ALL IC CHIPS ARE 7400 SERIES UNLESS OTHERWISE SPECIFIED.

NOTES

E-REV 0

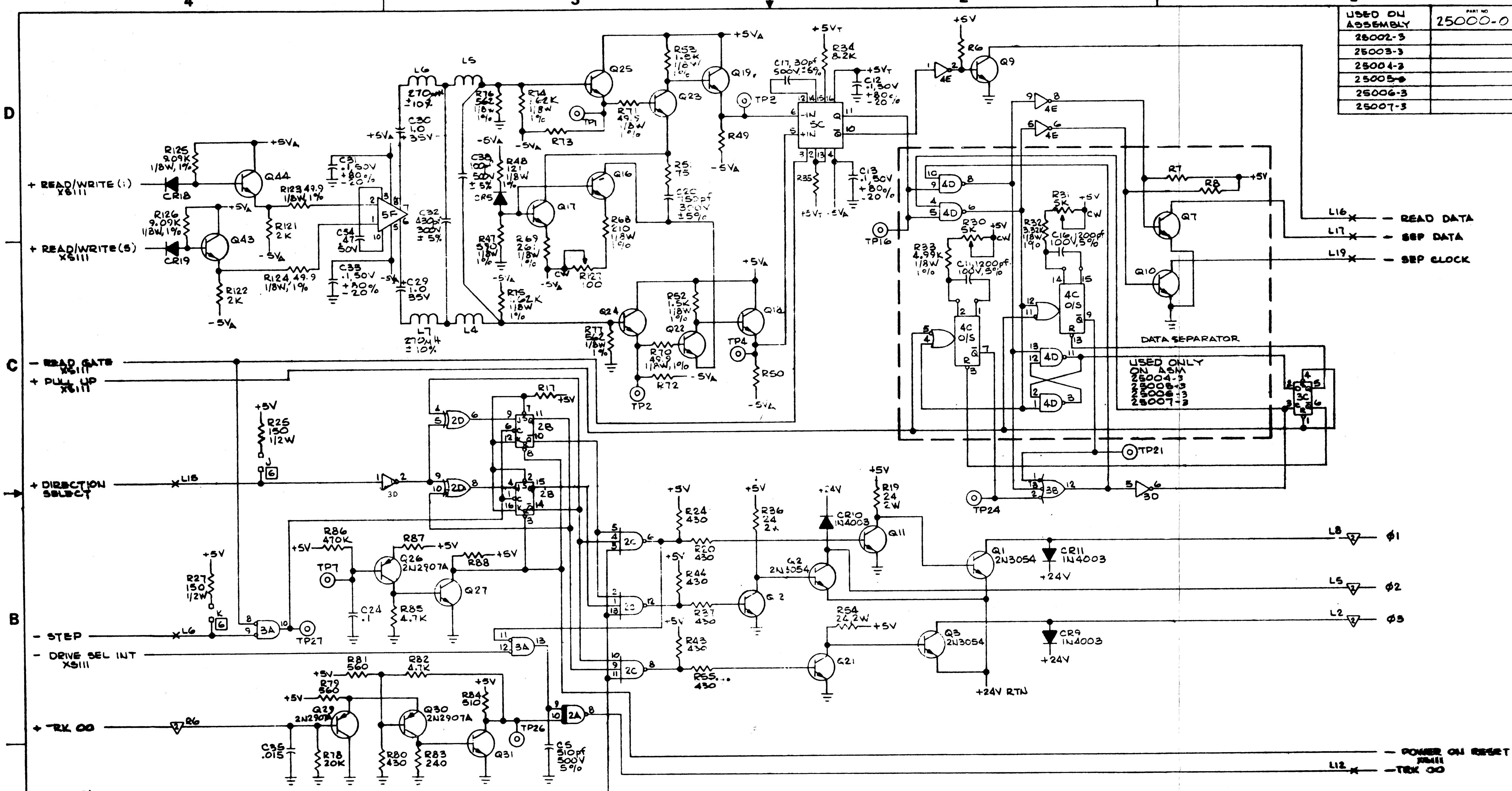
WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION

WANG LABORATORIES, INC.

TITLE SCHEMATIC LOGIBLOC SHUGART ELECTRONICS

210-7029 E 7029 3

USED ON ASSEMBLY	25000-0
25002-3	
25003-3	
25004-3	
25005-3	
25006-3	
25007-3	



NOTES: UNLESS OTHERWISE SPECIFIED;

1. ALL RESISTORS ARE 1K, 1/4W, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS, 100V, 10%.
3. ALL CHOKES ARE 100UH, 10%.
4. ALL DIODES ARE IN4148.
5. ALL TRANSISTORS ARE 2N2222A.
6. SYMBOL: O-O = TRACE CUT CAPABILITY.
7. SYMBOL: O O = JUMPER CAPABILITY.
8. CONNECTOR SYMBOL REFERENCES; (X)=J1 (▽)=J2 (▽)=J3 (▽)=J5

TYPE	POSITION	UNUSED ELEMENTS	+5V (PIN)	GND (P.N.)
7400	1D, 4D, 2E	1D1	14	7
7402	1A, 3A	1A		
7404	3D, 3E			
7406	4E			
74 0	3B, 2C			
7438	2A, 1B	B...		
7474	1E, 3C		4	1
7476	2B		5	13
7486	2D		14	7
UA733	5F		–	–
8T20	5C		–	8
9602	1C, 4C		16	5

REF DESIGNATION LAST USED	REF DESIGNATION NOT USED
C38	
CR19	
L9	
Q44	
R128	R9, 10, 11, 39, 13
TP35	TP10, 17, 18, 19, 22, 23, 25, 28, 29, 30, 31, 32, 33, 34

FOR WANG LABS' USE:

1. CUT JUMPERS C, F, G, H, J, K, R, S.
2. INSTALL JUMPERS B, E, AND FROM E TO R.
3. REMOVE R13 150 Ω.

MUST CONFORM TO ENGINEERING SPEC. ES 30000-0		EC HISTORY	
MATERIAL	TOLERANCE UNLESS OTHERWISE NOTED	DATE	NO.
		3-16-4	0114
	LINEAR ±.XX ±.XXX	4-11-4	0150
CASE DEPTH		7-30-4	0191
HARDNESS	ANGULAR±	9-74	0257
SURFACE TREATMENT ES	CORNERS EDGES BROKEN OUTSIDE MAX INSIDE MAX	12-74	
		3-75	

TITLE: SCHEMATIC DIAG, DISKET

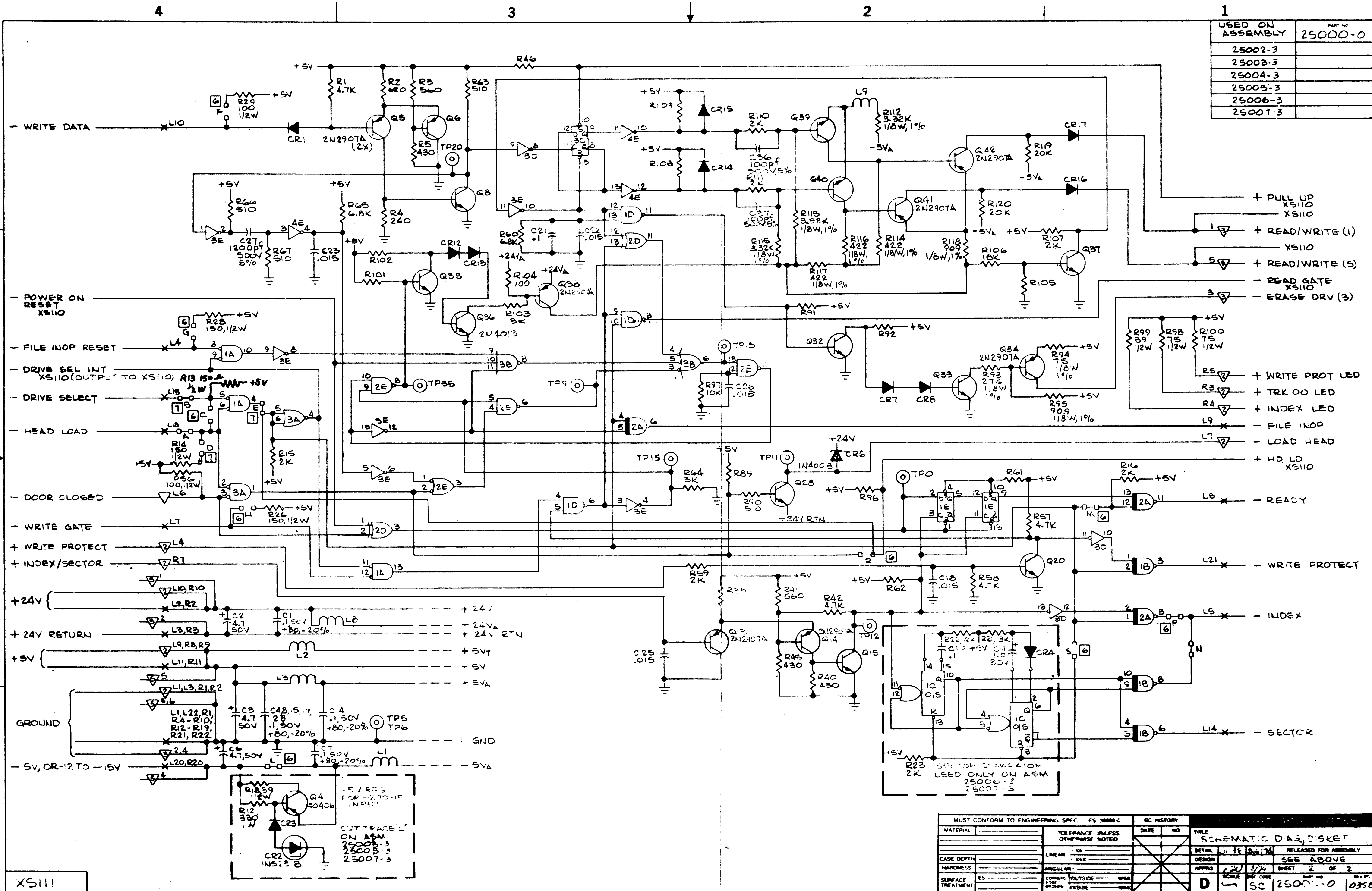
USED FOR ASSEMBLY: SEE ABOVE

SHEET 1 OF 2

D — SC 25000-0 0358

XS110

2



USED ON ASSEMBLY
25000-0
25002-3
25003-3
25004-3
25005-3
25006-3
25007-3
- WRITE DATA
- POWER ON RESET XS110
- FILE INOP RESET
- DRIVE SEL INT XS110 (OUTPUT TO XS110)
- DRIVE SELECT
- HEAD LOAD
- DOOR CLOSED
- WRITE GATE
+ WRITE PROTECT
+ INDEX/SECTOR
+24V
+ 24V RETURN
+5V
GROUND
- 5V, OR -12 TO -15V
+ PULL UP XS110
XS110
+ READ/WRITE (1)
XS110
+ READ/WRITE (5)
- READ GATE XS110
- ERASE DRV (3)
+ WRITE PROT LED
+ TRK 00 LED
+ INDEX LED
- FILE INOP
- LOAD HEAD
+ HD LD XS110
- READY
- WRITE PROTECT
- INDEX
- SECTOR
+5V/R23 FOR -12 TO -15 INPUT
CUT TRACE "L" ON ASM 25005-3 25006-3 25007-3
SECTOR SEPARATOR USED ONLY ON ASM 25006-3 25007-3
XS111
MUST CONFORM TO ENGINEERING SPEC FS 30000-C
TOLERANCE UNLESS OTHERWISE NOTED
SCHEMATIC DIAG, DISKET
RELEASED FOR ASSEMBLY
SEE ABOVE
SHEET 2 OF 2
D
SC
2500_-0
0358

2.6 MODEL 2270 SIGNAL MNEMONICS

$A_0 - A_7$:	Output of the A Register 8-bit data path for R/W data.
A = B	An output from the ALU; when active, $A_{0-7}=B_{0-7}$.
$\overline{\text{ACU}}$:	A register clock.
$AD_0 - AD_8$:	Output of RAM address counter.
$\overline{\text{AD+1}}$:	RAM address increment at T78 time.
$\overline{\text{AD-1}}$:	RAM address decrement at T78 time.
$\overline{\text{ADI}}$:	RAM address increment.
$\overline{\text{AND}}$:	Logical AND instruction decoded.
$\overline{\text{BR}}$:	Unconditional Branch.
$\overline{\text{BRO}}$, $\overline{\text{BR1}}$, $\overline{\text{BR3}}$:	Directly control the ROM address for sequential addressing as well as addressing for Branch command.
$\overline{\text{BRH}}$, $\overline{\text{BRL}}$:	Branch Low and Branch High originated on the 6297 board controlled by ROM bit 10.
$\overline{\text{BSY}}$:	Microprocessor ready/busy.
$\overline{\text{B TO M}}$:	Selected register to memory instruction decoded.
$C_0 - C_7$:	Output from ALU 8 bit data path known as C Bus. Carries data to selected registers as indicated by micro-instruction.

CA:	Carry FF output (used as status bit).
$\overline{\mathrm{CABYS}}$:	Calculator reads/busy.
$\overline{\mathrm{CAX}}$:	Made up from the IOB terms IOB_1, and IOB_3. They distinguish the select address from a data transfer operation.
$\overline{\mathrm{CAPM}}$:	Calculator prime.
$\overline{\mathrm{CASTIS}}$:	Calculator strobe to disk microprocessor.
$\overline{\mathrm{CASTO}}$:	Strobe from microprocessor to CPU (Calculator Strobe Out).
$\overline{\mathrm{CCMD}}$:	Control Command decoded.
CKC:	Clear 6718 clock.
$\overline{C_{N+4}}$:	ALU carry-out bit.
$\overline{\mathrm{CNTRL}}$: (1 or 2)	Control command generated by microprogram to access peripheral functions.
CNTRLG: (1 or 2)	Control gate used to enable various disk mechanical operations, such as R/W head stepping.
D#3:	Select Disk Drive #3.
DK_1 - DK_3:	Disk select lines from microprocessor.
DROP:	Reinitialize microprocessor.

$\overline{\text{EXOR}}$: Logical Exclusive OR instruction decoded.

$\overline{\text{FH}}$: Indicates adder output is NOT EQUAL.

FHG: Controls the MODE CONTROL INPUT on the ALU for determining if the ALU will perform a logic function or an arithmetic function.

FIR: File Inoperable Reset.

FMT: Format pushbutton.

$\overline{\text{FMTB}}$: Format pushbutton.

$\overline{\text{G1SO}}$: Calculator strobe to disk microprocessor; same as $\overline{\text{OBS}}$.

$\overline{\text{GKBD}}$: Calculator ready/busy to microprocessor: same as $\overline{\text{CPB}}$.

HD DIR: Selects R/W head direction; in or out.

HD ST: Head Stop.

HLD_1 - HLD_3: Head Load One-Shots.

HLDS: Status bit indicating a R/W head load operation has taken place.

IC_0 - IC_8: ROM address bits.

$\overline{\text{IMM}}$: Immediate instruction decoded.

$\overline{\text{IOB}_1}$: AD6 from CPU,

$\overline{IOB_3}$:	AD8 from CPU,
$K_0 - K_7$:	The K Register output. High order and low order bits from CPU_1 or ALU microprocessor.
$KS_0 - KS_7$:	The K Register inputs. High order and low order bits of an 8-bit word received from the CPU.
$\overline{KR}$:	K register clock.
$\overline{LAUX}$:	Load Auxilliary instruction decoded.
$\overline{LD\ HD}$:	Load head.
M:	See FHG.
$M_0 - M_7$:	MEMORY output.
$\overline{M\ TO\ B}$:	Memory to selected register instruction decoded.
10 MHZ:	10 mega hertz oscillator output.
10 MS:	10 millisecond delay for disk access.
$\overline{NOOP}$:	No operation. 1.6 microsecond delay.
$\overline{OR}$:	Logical OR instruction decoded.
$\overline{PLUS\ WC}$:	Add with carry instruction decoded.
$\overline{PLUS\ NC}$:	Add without carry instruction decoded.

$\overline{\text{PM}}$: Prime.

$\overline{\text{PRC}}$: Clears CRC, also enables CRC and RAM address increment via FF L96-5.

$R_0 - R_{15}$: 16 Bit ROM output. Makes up micro-instruction for WCS microprocessor.

$\overline{\text{RDDA}}$: Read data. Serial data from disk.

RDG: Read gate. Selects either C Bus or A register data as input to memory.

REG = 0: Branch if selected register = 0.

REG ≠ 0: Branch if selected register ≠ 0.

REG = M Branch if selected register = ROM Mask.

REG ≠ M: Branch if selected register ≠ ROM Mask.

REG TR: Branch if True bits in selected register match True bits in mask.

REG FS: Same (False instead of True).

$RM_0 - RM_7$: Originates from a multiplexed selection of ROM bits or RAM bits, the B Bus to the ALU.

$\overline{\text{R/W}}$: Input to RAM, low for Write mode and high for Read mode.

$\overline{\text{SCM}}$: Sector mark pulse from disk unit.

$\overline{SCMS}$: Status bit indicating that a sector mark pulse has occurred.

SCT_0 - SCT_3: Sector address count from disk.

$\overline{SSCM_1}$ - $\overline{SSCM_3}$: Sector mark status input from disk drives 1, 2, and 3.

$\overline{ST1}$: Clock for Carry FF; results in setting of Carry FF if TKØ (Bit 6, C_6) is active.

$\overline{T_{01}}$: RAM/ROM buffer registers clock time.

$\overline{T_{37}}$: RAM R/W Time.

$\overline{T_4}$: ROM address increment/branch Time.

$\overline{T_{78}}$: RAM Address increment/decrement time; also clocks certain status bits.

$\overline{TKØ}$: Track zero sensing indicator for selected disk drive.

WCD: Write clock data.

WCLK: Clock 1 for write data.

$\overline{WCLK\ 1}$: Write clock 1 (for parallel to serial conversion during a write).

WORD RDY: Indicates 8 bits are ready for a R/W.

WP: Write protect.

WRDYS:	**Word ready status bit.**
WTG:	**Write gate.**

THIS PAGE IS INTENTIONALLY LEFT BLANK.

3. MODEL -30, -40 AND -60 MICROPROCESSORS

This section is written with the assumption that Section 2 has been read. Since the -30, -40 and -60 microprocessors are very similar to the -70 microprocessor, only the block diagram and circuit board descriptions are included in this section. Refer to the *Schematic Manual* for board descriptions.

3.1 6295 I/O TERMINATOR

This board contains inputs from and outputs to both the CPU and the disk. Its function in the microprocessor is providing proper terminations for all incoming and outgoing signals.

3.2 6395/6537 I/O TERMINATOR

These two boards perform similar functions for their individual disks. The main difference is that one board controls 2 floppy disk units (6395) and the other controls 3 floppy disk units (6537).

There are several functions which they perform:

1. Provide a sector count from the selected disk.
2. Provide step in and step out pulses for the selected disk as well as head load circuits for each.
3. Write clock circuit.
4. The remaining circuitry is concerned with gating read data, write data, or status conditions from the disk, or to the disk to their proper place.

On the 6395 there are two identical sector counter circuits, one for each disk and function is as follows: the sector pulses are divided by two, that is, every other pulse is counted. The reason for this is that in a single sector there is only room for 128 bytes of data, and we need a 256 byte data field. Thus the sector counter cycles from 0 to 15 rather than 0-31. During each revolution, the count is reset to 0 by index mark. These inputs are synchronized with the machine cycle by T4. The outputs of the two sector counters are input to a multiplexer whose input select line is controlled by the disk select line. The 6537 has 3 sector counters operating the same as the one just described. The major difference is in the data multiplexers; there are two, one to select between disks 0 and 1 and a second to select between the output of the first MUX and disk 2.

Head movement is controlled by R_6 and CNTRLG to step the head in and R_4 with CNTRLG to step it out. Head loading is controlled by R_2 and CNTRLG through signal ESG which is the result of these two being on. If any head is loaded, a status bit indicates this in the 2240 and 2243. However, this status bit is already used in the 640 and 740, therefore to insure that the head is loaded on a 640 and 740 it must be reloaded before each operation.

The write clock circuit is the same for both boards; 10 MHZ is divided by two then presented to a 7490 wired to allow BCD count. The outputs of this counter are gated to develop CLK and CLK1 which are connected to the 6399 board where the dual frequency format is developed. The reason for the additional circuitry in this area is that the bit cell is much longer on a floppy that on a Diablo. The 6395 has an additional difference in that it has place for a jumper in this circuit. The jumper in one position allows 10 MHZ to be used as the controller time base (2240), and in the other position 5 MHZ is used as the time base (640, 740).

The remaining circuitry is concerned with selecting the proper data or status information (Read data $_{0,1,2}$; Track Ø $_{0,1,2}$; File Ready $_{0,1,2}$; Read Clock $_{0,1,2}$) from the selected disk. Included also are circuits to distribute data and initialize the disk (File Unsafe reset 0,1,2; Write Enable 0,1,2; Write Data 0,1,2). Inputs from the CPU with terminations and outputs to the CPU and terminations are on this board also.

3.3 6296 DISK CONTROLLER

The 6296 board makes up one part of the microprocessor disk controller. Contained on this board is:

1. The K register (L16, L18).
2. The ALU function decoding circuitry (L14-11, L23-8, L5-3, L2, L3, L4).
3. The ALU and carry circuitry (L11, L20, L12-2-6-12, L13, L21, L22).
4. The A bus data selection multiplexers (L7, 8, 9, 10).
5. The calculator/disk status circuits (L1, 1A, 1B, 1C, L6, L23-6).

The K register receives inputs from either the calculator (K_{S0} - K_{S7}) or the C bus (C_0 - C_7). Its inputs are selected by the state of signal KX which is derived from $\overline{R}_8$ or R_9 and $\overline{WRI}$. KX is normally high selecting the K inputs; it goes low for register instructions using the K register, thus selecting the C bus inputs. K register outputs are made available to the ALU through the A bus Multiplexer, or to the disk drive as track address bits via the 6295 board. The A bus multiplexer selects data from one of four sources: St_0, St_1, A register, or K register, and makes this data available to the ALU. The register is selected by the configuration of ROM bits R_8 and R_9 (Refer to Tables 1, 2 and 3 of Section 2.2.3).

The ALU function decoding circuits determine the type of instruction being performed by decoding ROM bits R_{11} thru R_{15}. When the instruction is decoded the appropriate output of L3 or L4 will go low and the diode matrix will determine the mode of operation of the ALU. The ALU has two modes of operation: arithmetic and logic. These are selected by the state of pin 8 on L11 and L20.

Logic high = logic functions
Logic Low = arithmetic functions

Once the mode is determined, the specific function must be selected; this is accomplished by S_0 thru S_3 inputs to L11 and L20. Below is a listing of configurations and there functions.

S_3	S_2	S_1	S_0	Pin 8 = H LOGIC	Pin 8 = L ARITHMETIC
L	L	L	L	$F = \overline{A}$	$F = A$
L	L	L	H	$F = \overline{A + B}$	$F = A + B$
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$
L	L	H	H	F = LOGIC 0	F = Minus 1 (2's comp.)
L	H	L	L	$F = \overline{AB}$	$F = A$ Plus $A\overline{B}$
L	H	L	H	$F = \overline{B}$	$F = (A + B)$ Plus $A\overline{B}$
L	H	H	L	$F = A \oplus B$	$F = A$ Minus B Minus 1
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ Minus 1
H	L	L	L	$F = \overline{A} + B$	$F = A$ Plus AB
H	L	L	H	$F = \overline{A \oplus B}$	$F = A$ Plus B
H	L	H	L	$F = B$	$F = (A + B)$ Plus AB
H	L	H	H	$F = AB$	$F = AB$ Minus 1
H	H	L	L	F = LOGIC 1	$F = A$ Plus A
H	H	L	H	$F = A + \overline{B}$	$F = (A + B)$ Plus A
H	H	H	L	$F = A + B$	$F = (A + \overline{B})$ Plus A
H	H	H	H	$F = A$	$F = A$ Minus 1

The carry circuit is used for arithmetic functions in conjunction with the ALU. It is also used as a status bit to indicate which disk is selected in a format operation. The carry flip-flop L22 is preset if the removable disk is selected and cleared if the fixed disk is selected.

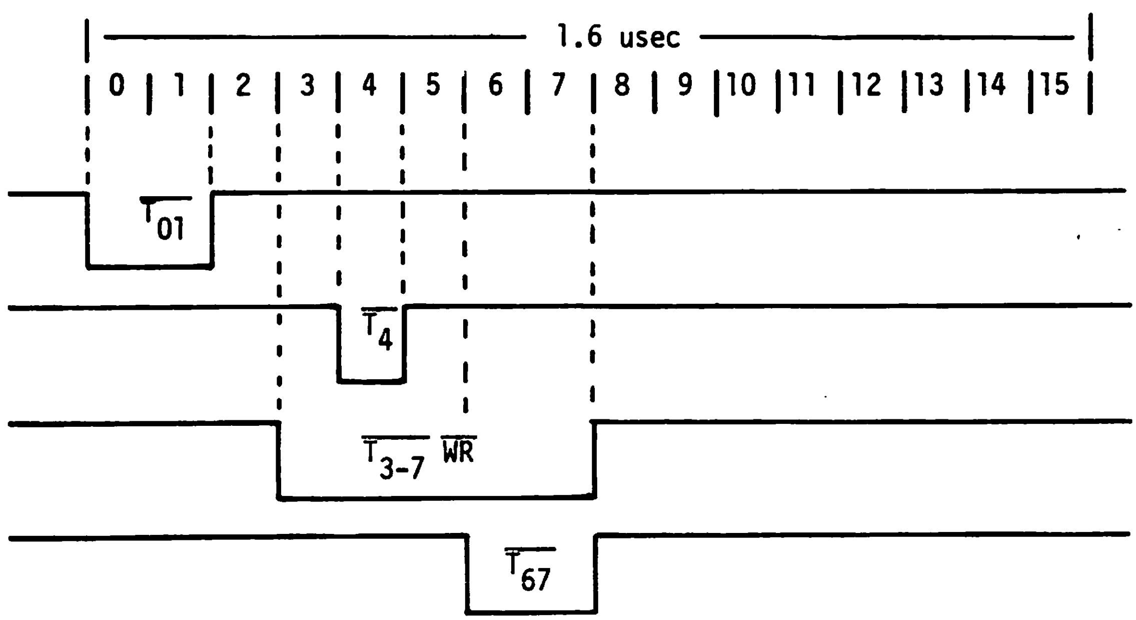
The calculator/disk status circuits simply synchronize status conditions with the microprocessor timing cycle. L1C and L1B-11,3 gate calculator strobe and busy according to the type of information being transferred (address information or data). The only circuit remaining is found at zones A2 and A3 of the schematic. This logic configuration decodes branch instructions. The signal $\overline{BLC}$ is active for the four bit branches and the eight bit branches. Signal $\overline{BC}$ is active only for eight bit branches. So if only $\overline{BLC}$ is on, the processor is doing a four bit branch, if both are on ($\overline{BLC}$ and $\overline{BC}$), an eight bit branch is being performed.

3.4 6297 DISK CONTROLLER

The 6297 board is divided into the following sections:

1. Timing (Zones F, G, 6-11 on the 6297 schematic).
2. ROM instruction decoding (Zones C, D, E, 7-11).
3. B bus multiplexer (Zones D, E, 5 & 6).
4. RAM address registers (Zones D-G, 1-4).
5. IOB decoder (Zones C 2, 3).

Timing for the microprocessor is derived from a 10 MHZ crystal, the output of which is divided into the following timing sequence.



The processor cycle begins with T01 which loads data at the current RAM address into the RAM output register. T01 also loads the new ROM instruction into the ROM output register. $\overline{T4}$ is the microprocessor execution time, that is, the ROM instruction present on the ROM output register outputs is performed at T4 time.

At T3, a signal designated $\overline{WR}$ is generated; this begins the RAM write cycle which lasts 500 ns through T7. If data is going to be written in RAM, it can be done during this time. The last clock time is T6, 7 which loads a new RAM address either by incrementing, decrementing the present address or by loading a completely new address through a load auxiliary instruction. The machine cycle time for a 2260 is decreased from 1.6 usec to 1.4 usec.

The various ROM instructions are decoded on this board. The logic decodes the ROM bit configurations to determine:

1. Type of instruction.
2. Data used in branch commands.
3. Increment, decrement or load new memory address.
4. Whether to strobe selected register.
5. Whether RAM should be written in or not.
6. Whether a 4 bit or an 8 bit branch is being performed.

Each of the outputs of this decoding circuitry will change state if a particular ROM bit configuration is present. This happens at T01 time and remains until a new ROM instruction is loaded.

The logic used to determine the type of instruction varies with the instruction. There are 5 different types of instructions which are decoded in the following manner:

1. Register Instructions

These instructions do not have any decoded outputs on this board unless the result of the instruction is to be stored in the selected register rather than RAM. This is indicated by L8 pin 7. This output goes low if the above condition is present. This line being low causes two things to happen; first it will cause memory address to be incremented by gating a count up pulse to L29 pin 5 at T4 time through L21 pin 6. Secondly, it will inhibit anything from being written in RAM for that entire machine cycle. This is accomplished through L4 pin 13 being low, forcing its output pin 12 high which results in signal $\overline{WRI}$ going low. This inhibits $\overline{R/W}$ from going low and writing in RAM. R_8 & R_9 indicate the selected register by their binary configuration. With L4 pin 12 high L7 pin 6 allows the selected register to be clocked at T4 time, through L10 pins 4, 5, 6, or 7 depending on R_8 & R_9.

2. Immediate Instructions

Immediate instructions are identified by R_{15}, R_{14} and R_{11} being on. This configuration will inhibit memory address from changing by disabling 1/2 of L8 at pin 1. Immediate instructions use the ROM bits R_0 - R_7 as an operand. These bits have to be gated onto the B bus to be made available to the ALU. L8 pin 2 is low because of ROM bits R_{15}, R_{14} and R_{11}; this selects the A inputs to multiplexer L19, L8 pin 2 also forces L4 pin 8 high selecting the B inputs to L32 and L33. This allows R_0 - R_7 to pass onto the B bus (RM_0 - RM_7). These instructions also inhibit writing in RAM through the same gating as mentioned in the previous instruction, and they strobe the selected register through L10 pins 4, 5, 6, or 7.

3. Branch Instructions

There are 2 major types of branch instructions; one type designated branch instructions which includes unconditional and 8 bit branches, and a second type designated MASK branch instructions. A branch instruction is decoded to determine first; the number of bits to be loaded as the new ROM address and secondly, to indicate which register bits are to be compared to MASK (high or low order). The first part of the decoding is done partly on the 6296 board which generates signals $\overline{BC}$ (active only for 8 bit branches) and $\overline{BLC}$ (active for both 4 and 8 bit branches). These signals are gated through L25 pin 6 and L15 pins 8 and 11 to generate $\overline{BRI}$ and $\overline{BRO}$, which directly control the loading of the ROM address counter. If a 4 bit branch is decoded, only $\overline{BRO}$ will be active, and if an 8 bit branch is decoded both will be active. The second part of this decoding is done by 1/2 of L10. ROM bits R_{15}, R_{14}, R_{11} and R_{10} are decoded to determine if an unconditional branch is being performed L10 pin 10, if a branch high is in process L10 pin 11, or a branch low is being executed L10 pin 12. The outputs of this chip go on to set up the necessary conditions to execute the instruction. If an unconditional branch is decoded $\overline{BR}$, which is the signal name for L10 pin 10, it turns on $\overline{BRI}$ and $\overline{BRO}$. These two signals along with $\overline{BR}$ go to the ROM instruction counter and enable it to load a completely new ROM address. Therefore, a branch to any step in the microprogram can be performed.

If a branch high, or branch low is decoded, BRH or BRL will be generated. These signals go on to select the high or low order register bits on the 6296, and gate the MASK bits to the high or low order B bus lines.

EXAMPLE 1. BRANCH HIGH

If a branch high is being executed. L10 pin 11 will be low. This is inverted and applied to L32 pin 15 which disables the chip causing its outputs to remain low. It also goes to the 6296 board to select the high order register bits. The signal from L10 pin 11 is also applied to L4 pin 10 which forces its output pin 8 high. This high is applied to L32 and L33 pin 1 selecting the B inputs to the multiplexer allowing the MASK bits to be put on to the high order lines of the B bus because BRL is low enabling L33.

EXAMPLE 2. BRANCH LOW

For a branch low instruction L10 pin 12 is low, inverted, and applied to L33 pin 15, disabling that chip thus keeping its outputs low. It also goes to the 6296 board and selects the low order register bits. That line (L10 pin 12) is also tied to L4 pin 11 forcing L4 pin 8 high, again, selecting the B inputs to L32 and L33. Since L19 pin 1 goes low only for immediate instructions, L19 allows the B inputs to appear on its outputs. With BRH low L32 is enabled allowing the MASK ROM bits to be on the low order lines of the B bus.

There are two instructions which remain to be decoded, one is the control command which is a controller function generating all commands to the disk or CPU e.g. turn on RDG or strobe 2200. This instruction's ROM bit configuration is much the same as an immediate instruction, thus it is decoded in the same way with one exception. Both R_{10} and R_{11} are on, causing L8 pin 9 to go low resulting in a signal labeled CC which is tied to the 6296 ALU function decoding circuit.

4. Load Auxiliary Instruction

The last instruction is a load auxiliary; this is a means of setting the memory address to any location. This is accomplished by loading ROM bits R_0 - R_9, R_{12} and R_{13}, in the hex configuration of the address desired, into the RAM address register. This is accomplished with the following logic. Initially L10 pin 3 is high; this line goes to the select input of the RAM address multiplexer (L26, L30, L31). In this state the B inputs are selected and normal operating sequence is incremented at T4, then loaded into L27, L28, and L29 on the leading edge of T6, 7. When a load auxiliary instruction is decoded, the select line of the RAM address multiplexer goes low selecting the A inputs; this allows the ROM bits (R_0 - R_9, R_{12}, R_{13}) to be loaded as RAM address at T6, 7.

This circuit is used to determine whether disk address information or data is going to be sent from the 2200. If AB_6 - AB_8 equal 101, $\overline{CAX}$ is active indicating that address information is being sent. If AB_6 - AB_8 equal 010 $\overline{CAN}$ is active indicating data is being sent. These signals ($\overline{CAX}$ and $\overline{CAN}$) go to the 6296 board where they are used as enabling signals for calculator strobe and $\overline{CAX}$ is a status bit in ST_0.

3.5 6298 ROM/RAM

The 6298 board is made up of the RAM with associated circuitry and the ROM with its circuits.

The ROM is the heart of the microprocessor and contains the instruction sequences that tailor it to the disk it is interfacing. The circuits associated with the ROM are:

1. ROM address counter.
2. ROM output register.
3. Hardware trap for format.
4. Hardware trap for prime.

The ROM address counter is made up of three 74161 ICs. These are controlled by a number of different means:

1. These counters can be incremented by the trailing edge of T4; this is the normal mode of operaion.
2. They can be set to an address by loading $R_0 - R_9$, R_{12} and R_{13} as that address. This is controlled by the various branch indicators ($\overline{BR_0}$, $\overline{BR_1}$, $\overline{BLC}$, or $\overline{BR}$).
3. Prime from the calculator resets the ROM address to 0000 thru L35 pin 12 which is gated with format at L16 pins 9 and 10.
4. Format is a hardware trap generated by L35 pins 8 and 9; this forces the ROM address to 0100 which begins the format routine.

The PROMs are accessed two at a time thus making available 256 x 16 bit words. PROM chip select is controlled by IC8 and IC9. The hardware traps must therefore, function by controlling $\overline{IC8}$ and $\overline{IC9}$. Prime does a reset to the IC register thus forcing $\overline{IC8}$ and $\overline{IC9}$ to 00. Format also does this however, one side of the format flip-flop (L35 pins 8 & 9) is gated with $\overline{IC8}$ and $\overline{IC9}$ so that if $\overline{IC8}$ and $\overline{IC9}$ = 00, and the flip-flop is set, PROMs L4 and L8 are selected thus initiating the format routine. The 16 bit output of the PROMs is stored in an output register (L12, L13, L14, L15) at T01.

The RAM and its associated circuitry contain the following: RAM address (L28, 29, 30), input data select (L33, 34), RAM (L18-L25), and the RAM output register (L31, 32). At the beginning of the machine cycle at T01, data at the present RAM address is loaded into the RAM output register and made available for processing. The next clock time begins the RAM write cycle which lasts 500 ms therefore, at instruction execution time T4, if anything is to be written in RAM, it is done at that time. Once all RAM operations have been concluded, the RAM address is changed; this is done on the trailing edge of T6, 7. The address loaded is that which was developed on the 6297 board.

The only remaining circuitry is L36 which is a one shot used to generate four strobes:

1. MCC - data output enable.
2. $\overline{\text{CASTO}}$ - calculator strobe.
3. $\overline{\text{DKST}}$ - disk strobe line.
4. $\overline{\text{RSTR}}$ - restore pulse to the disk.

These are all initiated by control instructions in the microprogram.

3.6 6299 DISK CONTROLLER

The 6299 contains the following circuitry:

1. Write clock and Write circuitry.
2. Read circuitry.
3. CRC circuits.
4. Memory Increment circuits (while reading or writing only).
5. Disk control circuits.

The write circuits operate in the following sequence. Data from memory is loaded one byte per machine cycle into the A register. From here it is serialized then combined with write clock to develop the dual frequency recording format used on the disk. This sequence continues until the 256 data bytes are written, then the two bytes of CRC are written and the write operation is terminated. The easiest way to explain the logic is to perform the above sequence. Once the decision has been made to write in the present sector, a control command is issued which turns on write gate and erase gate. ROM bits R_0 - R_3 are decoded by L39 to turn these on. One machine cycle later the actual writing of data begins when a control command turns on start write (STW) and PRC. PRC loads the word ready flip-flop (L35) with 1000 and clears the CRC register (L9, L10). When STW goes on, it starts write clock by removing a clear from L29 and L40. STW also enables the parallel to serial converter L34 to begin operating. To allow time for data separation circuits to synchronize when reading, the first few bytes written are zeroes.

When the word ready counter reaches a count of seven, L26 pin 6 will go low; this sets L15 pin 1 high. On the next write clock pulse, L15 pin 1 goes low again loading the next byte to be written on the disk into the A register. Since everything that is written on the disk is stored in RAM, RAM address has to be incremented for each byte written. When L15 pin 1 goes low it causes the first stage of the memory address flip-flop to be preset, then at T01 time the second stage is set. This goes on to increment RAM address later in the machine cycle. This cycle continues until 256 bytes have been written on the disk. During the time the data is being written on the disk a cyclic redundancy code (CRC) is developed by the circuit consisting of L1, L2, L3 and L4. This CRC is shifted into a 16 bit shift register L9, L10, then written on the disk following data. This is done by monitoring the 512 RAM address bit; when it comes on the A register data select changes the data input from RAM to CRC register, byte #1. This is accomplished through L6 pins 3 and 6. After this byte is written on the disk, memory address is incremented again (address 513) causing two events to occur: first through L26 pin 12 and L7 pin 6, flip-flop L25 pin 15 is reset thus inhibiting memory address from incrementing and inhibiting anything else from going through the CRC circuit. Secondly, the A register input is again changed to allow the second byte of CRC to be written on the disk. At this point the write is complete and the microprogram waits to see sector pulse before terminating the operation. This consists of checking for errors and branching back to its ready routine.

When a read is requested, the procedure must be reversed thus, the circuitry is different however, some of the same circuitry is used but in a different manner. The read sequence is as follows: the separated clock and data are input to a serial to parallel converter, then loaded into the A register. As each byte is assembled then loaded into the A register, it is immediately made available to the RAM data inputs for storage. This sequence continues for the 256 bytes, then RAM is inhibited and the CRC is checked against the one that was developed when data was read. After this the operation is terminated if no errors were detected, or an error is flagged if any were detected. After the processor determines that it is in the proper sector and a read was requested, the read begins. ROM bits $R_0 - R_3$ are decoded by L39 to turn on read gate and $\overline{PRC}$. This conditions the 03 flip-flop to monitor incoming data and flag the 03 byte, indicating that the next bit is data. Read gate also causes the A_2, B_2, C_2 and D_2 inputs to the A register to be selected and enables the serial to parallel conversion circuitry (L11, L12, and L23). When the 03 byte is detected the word ready counter (L35) is enabled allowing read clock to increment it. As each byte is assembled it is stored in the A register; when the RAM write cycle occurs the byte is written into memory, then the RAM address is changed by ADI as it was for a write. This cycle continues until all bytes in the data field have been read at which time the 512 address bit (ED9) will come on. When this bit is on the first byte of CRC is being read and the microprogram begins monitoring the 513 bit (ED0); this flags the 2nd byte of CRC. When the ED0 comes on again, L25 is set (when WORD RDY comes on), as it was for a write, thus inhibiting memory from being incremented and keeps any more data from being shifted thru the CRC circuits. The termination routine includes checking of data integrity by checking the CRC. During the read operation all the data read has been shifted thru the CRC circuit thus, what is contained in the CRC register (L9 and L10) should be the same as that written on the disk if no errors occurred during the read. If the CRC written on the disk is allowed to shift through the CRC circuit the result should be zero. Therefore, to check the CRC this is done; then the microprogram does an M to A with the 512 address bit on which selects the CRC inputs to the A register loading the result into A. The A register is then checked for a zero value; if A equals zero no errors were found and the controller increments RAM to address 513 and checks the second CRC byte. If no errors are found, the controller returns to its ready routine monitoring OBS. If any errors were found in either CRC byte, the microprogram branches to an error routine flagging a data error.

In explaining the logic operations involved in a read and a write most of the 6299 circuitry is used. There are however, a few loose ends. The error flip-flop (L25 pin 11) checks four conditions from the disk.

1. Write Check (WTCK).
2. File Ready (FR).
3. Seek Incomplete (SI).
4. Logical Address Interlock (LAI).

If any one of these are active the flip-flop will be set. It can also be set internally by C_5 and $\overline{ST1}$ to indicate a controller error. Part of ST_0 is contained in L5, L13, and L23; these chips control:

1. Head selection (L5 pin 12).
2. Disk selection (L23 pin 11).
3. Controller ready/busy (L5 pin 9).
4. 5 or 10 meg operation (L13 pin 12).
5. Format (L13 pin 9).

3.7 6399 DISK CONTROLLER

The 6399 board is operationally the same as the 6299. The differences are in the timing of the Write Clock. Since the floppy disk is much slower than the Diablo, the bit cell is much longer (4 usec as opposed to 640 ns) therefore, a change was necessary in the write clock to accomplish this. The error indication from the disk is reduced to one line indicating whether or not the file is ready. The only other differences are that one of the control and status bits are used differently. The erase gate output is not used to turn on erase gate but rather to turn on head load. The 1/2 TA status bit is used to generate the file unsafe reset signal.

3.8 MODEL 2230, 2240 AND 2260 MNEMONICS

$A_0 - A_7$	Output of the 'A' Register (6399 origin) 8 bit data path for data being read from disk to RAM.
$\overline{ACU}$	A Register count up.
$\overline{ADI}$	Address increment.

$\overline{\text{ADSS}}$	Status indicator for Group II address.
$\overline{\text{BC}}$	Goes low on execution of either Branch if Register = or ≠ to 0. It, along with $\overline{\text{BLC}}$ enables for a 256 instruction branch.
$\overline{\text{BLC}}$	Active during any of the branch instructions, (= or ≠ 0, = or ≠ MASK, and branch on True or False).
$\overline{\text{BR}}$	Unconditional Branch.
$\overline{\text{BRL}}$	Branch low.
$\overline{\text{BRH}}$	Branch high.
BR0	When on indicates max. jump of 16 steps.
BR1	When on indicates max. jump of 256 steps.
$C_0 - C_7$	Output from ALU (6296 origin) 8 bit data path known as C-Bus. Carries data to selected registers as indicated by micro-instruction.
$\overline{\text{CAAD 1-3}}$	Calculator addressing derived from IOB_1, IOB_2, and IOB_3; they determine device selection, addressing, or data functions; also derived from $AD_6 - A_8$ in a 2200 perform the same job.
CABY	Calculator busy.
$\overline{\text{CAN}}$ $\overline{\text{CAX}}$	Made up from the IOB_1, IOB_2 and IOB_3. They distinguish the select address (group II) or a data transfer operation.

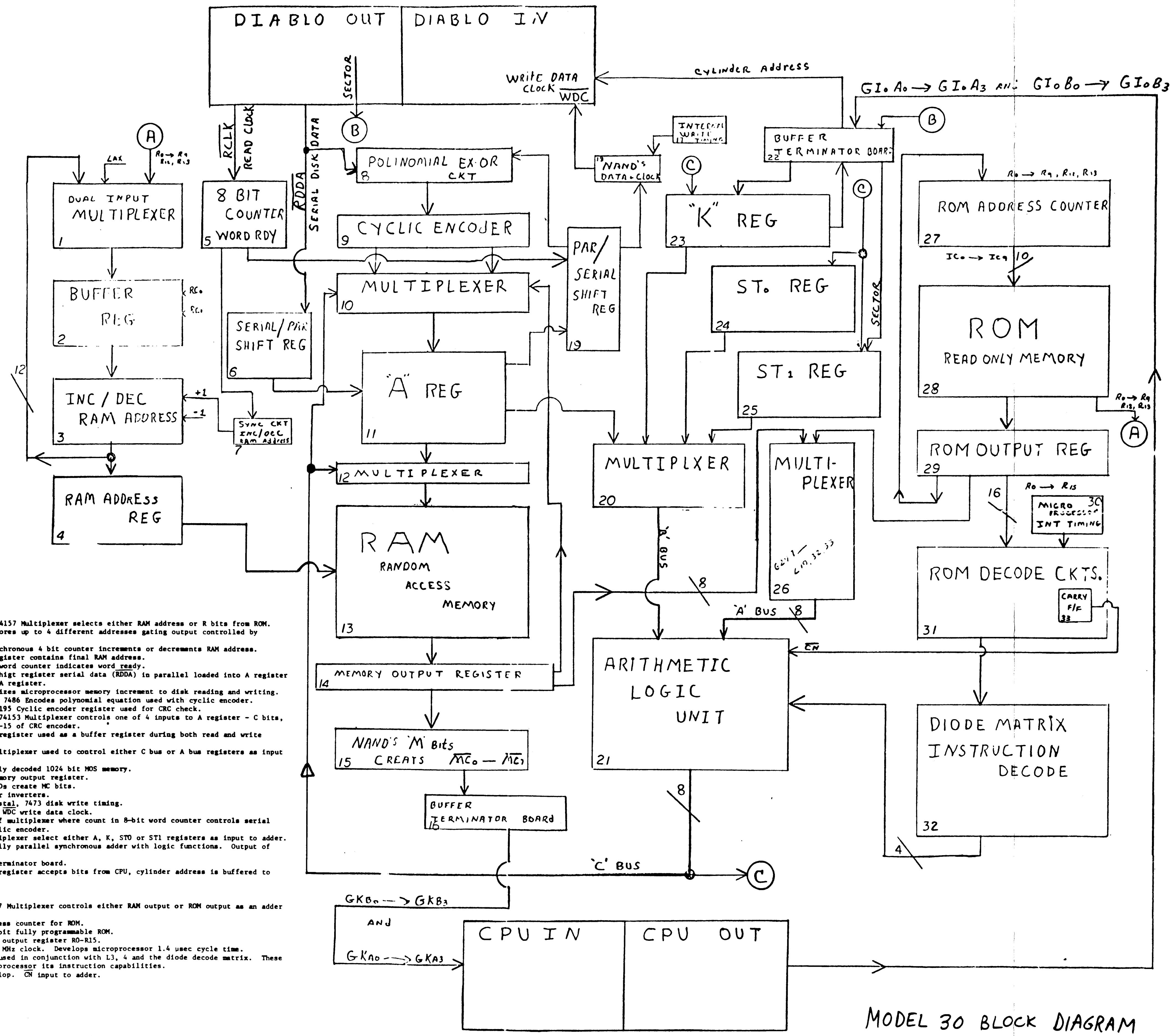
$\overline{\text{CAPM}}$	Calculator prime.
CAST 1	Calculator strobe.
CC	Instruction set word used to decode $\overline{\text{CNTRL}}$ Control Command.
$\overline{\text{CLK}}$	Clock for Write clock data.
$\overline{\text{CLK-1}}$	Clock for parallel to serial conversions.
$\overline{\text{CNTRL}}$	Control command generated by microprogram to access peripheral functions.
CNTRLG	Control gate used to enable STEP IN STEP OUT signals to stepping motors.
CWC	Prevents head loading on power up of disk controller.
D SEL	Disk select.
DISL	Disk select.
ED_{0-11}	Outputs of the subroutine stack registers, also make up the AD bits for memory addressing.
EJ2	Clock jumper point.
ERROR	File not ready indicator or may be set by C5 at $\overline{\text{STI}}$ time.
ESG	Erase gate.
$\overline{\text{FD}}$	Fixed disk.

$\overline{\text{FH}}$	Indicates adder output is not equal.
FHG	Controls the MODE CONTROL INPUT on the ALU for determining if the ALU will perform a logic function or an arithmetic function.
$\overline{\text{FILE UNSF RES L}}$	Left file unprotected reset.
$\overline{\text{FILE UNSF RES R}}$	Right file unprotected reset.
$\overline{\text{FMT}}$	Format push-button.
$\overline{\text{FOMT}}$	Format.
$\overline{\text{FR}}$	File ready.
$\overline{\text{FRL}}$	File ready left.
$\overline{\text{FRR}}$	File ready right.
HESL	Head select.
$\overline{\text{INDEX L}}$	Index mark input for left file.
$\overline{\text{INDEX R}}$	Index mark input for right file.
$KC_{0-3}S$	Group address bits on front panel.
KC_{0-7}	The "K" Register output High Order and Low Order bits from the controller to the CPU.
KS_{0-7}	The "K" Register INPUTS (input to 6396) High Order, and Low Order bits of an 8 bit word received from the CPU.

$\overline{KR}$	K register strobe.
$\overline{KSW}$	Key switch.
LD HD L	Load head left file.
LD HD R	Load head right file.
$\overline{LIND}$	Left file indicator.
MCC	Strobe for Memory of controller to calculator.
MC_{0-7}	Buffered output from Controller memory (6399, 6299 origin).
M_{0-7}	MEMORY output (6298 origin).
10 MHZ	10 MHZ clock.
NOOP	No I/O operation.
$\overline{PM}$	Prime.
$\overline{PRC1}$	Preset redundancy check.
$R_0 - R_{15}$	16 BIT ROM output (6298 origin) make up the Microinstruction set.
RM_{1-7}	Originates on the 6297/6597 from a multiplexed selection of ROM bits or RAM bits.
$\overline{RCLK}$ LEFT	Read clock for left file.
$\overline{RCLK}$ RIGHT	Read clock for right file.

$\overline{\text{RCLK}}$	Read clock.
$\overline{\text{RD}}$	Removable disk.
$\overline{\text{RDDA}}$	Read data. Serial data from disk.
$\overline{\text{RDDL}}$	Read data from left file.
$\overline{\text{RDDR}}$	Read data from right file.
RDG	Read gate. Selects A register inputs.
RDG	Read gate. Selects either C-Bus or A register data as input to memory.
$\overline{\text{RIND}}$	Right file indicator.
$\overline{\text{R/W}}$	Input to Memory, low for Write and high for Read. Memory is normally enabled to read.
SCT_{0-4}	Sector Mark from disk (6395 origin) Sector Count.
$\overline{\text{SCM}}$	Sector mark pulse.
$\overline{\text{SECTOR LEFT}}$	Sector mark input for left file.
$\overline{\text{SECTOR RIGHT}}$	Sector mark inputs if on right file.
$\overline{\text{STEP IN L}}$	Left Stepping motor increment (IN) towards track 0.
$\overline{\text{STEP IN R}}$	Right Stepping motor increment (IN) towards track 0.

$\overline{\text{STEP OUT L}}$	Left Stepping motor decrement (out) towards hub center.
$\overline{\text{STEP OUT R}}$	Right Stepping motor decrement (out) towards hub center.
$\overline{\text{ST}}_0$	Clock for status register 0.
$\overline{\text{STI}}$	Clock for status register 1.
$\overline{\text{STW}}$	Start write.
1/2 TA	Half track address.
$\overline{\text{TRK 0 L}}$	Track zero sensing indicator for left file.
$\overline{\text{TRK 0 R}}$	Track zero sensing indicator for right file.
T (X)	Timing which controls logic sequence in controller.
WCD	Write clock data.
Word RDY	Indicates 8 bits are ready for a R/W.
$\overline{\text{WR}}$	Clock for format.
$\overline{\text{WRI}}$	Inhibits data from calculator when high, enables when low.
$\overline{\text{WRITE ENBL R}}$	Right file write enables.
$\overline{\text{WRITE ENBL L}}$	Left file write enable.
$\overline{\text{WRITE DATA L}}$	Write data left file.
$\overline{\text{WRITE DATA R}}$	Write data right file.
WTG	Write gate.



MODEL 30 BLOCK DIAGRAM

1. 6297-L26, 30 and 31. 74157 Multiplexer selects either RAM address or R bits from ROM.
2. 6297-L16-L18. 71470 Stores up to 4 different addresses gating output controlled by RCO and RC1.
3. 6297-L27-29. 74193 Synchronous 4 bit counter increments or decrements RAM address.
4. 6298-L28-L30. 74195 Register contains final RAM address.
5. 6299-L35. 74193 8-bit word counter indicates word ready.
6. 6299-L11, L12. 74195 Shigt register serial data ($\overline{\text{RDDA}}$) in parallel loaded into A register then to memory through A register.
7. 6299-L8. 7476 Synchronizes microprocessor memory increment to disk reading and writing.
8. 6299-L1, L2, L4. 7473, 7486 Encodes polynomial equation used with cyclic encoder.
9. 6299-L9, L10. 7464, 74195 Cyclic encoder register used for CRC check.
10. 6299-L20, 21, 31, 32. 74153 Multiplexer controls one of 4 inputs to A register - C bits, M bits, 0-7 of CRC or 7-15 of CRC encoder.
11. 6299-L22, 37. 74298 A register used as a buffer register during both read and write operations to the disk.
12. 6298-L34, 33. 74157 Multiplexer used to control either C bus or A bus registers as input to RAM.
13. 6298-L18-L25. 2102 Fully decoded 1024 bit MOS memory.
14. 6298-L31, 32. 74195 Memory output register.
15. 6299-L19, 30. 7400 NANDs create MC bits.
16. 6295-L8, 4. 7407 Buffer inverters.
17. 6299-L40. 6.25 MHz crystal, 7473 disk write timing.
18. 6299-L28. 7400 Creates $\overline{\text{WDC}}$ write data clock.
19. 6299-L34. 74151 Type of multiplexer where count in 8-bit word counter controls serial data out to $\overline{\text{WDC}}$ and cyclic encoder.
20. 6296-L7-10. 74158 Multiplexer select either A, K, STO or ST1 registers as input to adder.
21. 6296-L11, 20. 74181 Fully parallel synchronous adder with logic functions. Output of adder is C bus.
22. 6295-L13, 14. Buffer terminator board.
23. 6296-L16, [illegible]. 74298 K register accepts bits from CPU, cylinder address is buffered to disk from K register.
24. 6296-STO.
25. 6296-ST1.
26. 6297-L19, 32, 33. 74157 Multiplexer controls either RAM output or ROM output as an adder input.
27. 6298-L9-11. 74161 Address counter for ROM.
28. 6298-L1-8. 1702, 2048 bit fully programmable ROM.
29. 6298-L13-15. 74195 ROM output register R0-R15.
30. 6297-L1, 2, 12, 14. 10 MHz clock. Develops microprocessor 1.4 usec cycle time.
31. 6297-Several chips are used in conjunction with L3, 4 and the diode decode matrix. These
32. circuits give the microprocessor its instruction capabilities.
33. 6297-L22. Carry flip-flop. $\overline{\text{CN}}$ input to adder.

WANG LABORATORIES (CANADA) LTD.
49 Valleybrook Drive
Don Mills, Ontario M3B 2S6
TELEPHONE (416) 449-2175
Telex: 069-66546

WANG EUROPE, S.A.
Buurtweg 13
9412 Ottergem, Belgium
TELEPHONE 053/704514
Telex: 26077

WANG DO BRASIL COMPUTADORES LTDA.
Rua Barao de Lucena No. 32
Botafogo ZC-01 20,000
Rio de Janeiro RJ, Brasil
TELEPHONE 226-4326, 266-5364
Telex: 2123296 WANG BR

WANG COMPUTERS (SO. AFRICA) PTY. LTD.
Corner of Allen Rd. & Garden St.
Bordeaux, Transvaal
Republic of South Africa
TELEPHONE (011) 48-6123
Telex: 960-86297

WANG INTERNATIONAL TRADE, INC.
836 North Street
Tewksbury, Massachusetts 01876
TELEPHONE (617) 851-4111
TWX 710-343-6769
Telex: 94-7421

WANG SKANDINAVISKA AB
Pyramidvaegen 9A
S-171 36 Solna, Sweden
TELEPHONE 08/27 27 95
Telex: 11498

WANG NEDERALND B.V.
Damstraat 2
Utrecht, Netherlands
(030) 93-09-47
Telex: 47579

WANG PACIFIC LTD.
902-3 Wong House
26-30, Des Voeux Road, West
Hong Kong
TELEPHONE 5-435229
Telex: 74879 WANG HX

WANG INDUSTRIAL CO., LTD.
110-118 Kuang-Fu N. Road
Taipei, China
TELEPHONE 784181-3
Telex: 21713

WANG GESELLSCHAFT M.B.H.
Murlingasse 7
A-1120 Vienna, Austria
TELEPHONE 85.13.54, 85.13.55
Telex: 74640 Wang a

WANG S.A./A.G.
Markusstrasse 20
CH-8042 Zurich 6, Switzerland
TELEPHONE 41-1-60 50 20
Telex: 59151

WANG COMPUTER PTY. LTD.
55 Herbert Street
St. Leonards, 2065 , Australia
TELEPHONE 439-3511
Telex: 25469

WANG ELECTRONICS LTD.
Argyle House
Joel Street
Northwood Hills
Middlesex, HAG ILN
TELEPHONE Northwood 28211
Telex: 923498

WANG FRANCE S.A.R.L.
Tour Gallieni, 1
78/80 Ave. Gallieni
93170 Bagnolet, France
TELEPHONE 33.1.3602211
Telex: 680958F

WANG LABORATORIES GmbH
Moselstrasse 4
6000 Frankfurt AM Main
West Germany
TELEPHONE (0611) 252061
Telex: 04-16246

WANG DE PANAMA (CPEC) S.A.
Apartado 6425
Calle 45E, No. 9N. Bella Vista
Panama 5, Panama
TELEPHONE 69-0855, 69-0857
Telex: 3282243

WANG COMPUTER LTD.
302 Great North Road
Grey Lynn, Auckland
New Zealand
TELEPHONE Auckland 762-219
Telex: CAPENG 2826

WANG COMPUTER PTE., LTD.
37, Hill Street
Singapore 6, Republic of Singapore
TELEPHONE 333641, 321791
Telex: RS 23987 GENERCO

WANG COMPUTER SERVICES
836 North Street
Tewksbury, Massachusetts 01876
TELEPHONE (617) 851-4111
TWX 710-343-6769
Telex: 94-7421

DATA CENTER DIVISION
20 South Avenue
Burlington, Massachusetts 01803
TELEPHONE (617) 272-8550

WANG LABORATORIES, INC.
836 NORTH STREET, TEWKSBURY, MASSACHUSETTS 01876, TEL. (617) 851-4111, TWX 710 343-6769, TELEX 94-7421

Printed in U.S.A.
13-684
6-76-3.5C

MICROPROCESSOR MANUAL OF MASS STORAGE DEVICES

ADDENDUM #1 APRIL, 1976

This addendum contains several corrections and updates. The microcode has been updated to include PROM changes in the program. The 6452 test board, with miniature lamp indicators and chassis mounted power supply, has been superceded by the 7069 test board capable of testing 6718 and 7018 boards. Schematics for 6718 and 7018 Printed Circuit Boards have also been updated.

Follow these instructions for incorporating the addendum into the Microprocessor Manual of Mass Storage Devices:

REMOVE PAGES	INSERT PAGES
1. Table of Contents iii/iv.	1. Table of Contents iii/iv Rev. 1.
2. Pages 41 thru 48, 59 thru 72.	2. Pages 41 thru 48, 59 thru 72 Rev. 1.
3. Page 75/76 (E6718 Rev 8).	3. Page 75/76 (E6718 Rev 9).
4. Page 77/78.	4. Page 77/78 (E6718 Rev 9).
5. Page 79/80.	5. Page 79/80 (E7018 Rev 13).
6. Page 81.	6. Page 81/82 (E7018 Rev 13/ E7029 Rev 1).

PRINTED IN U.S.A.

TABLE OF CONTENTS

READ HEADER BYTES AND STORE IN RAM	0058	8D20	LA	Cyl. Byte Loc.
	0059	F900	K and IM	Clr K Reg.
	005A	E901	K add IM	Add 1 to K
	005B	956A	Br K ≠ MH	Br ≠ 307.2us
	005C	EC95	CNTRL-1	RDG On
	005D	ECB5	CNTRL-1	PRC On
	005E	A21E	BOTL	BR WR = 1
	005F	1400	A to M(+1)	Cyl. Byte to M
	0060	B2E0	BOFL	BR WR = 0
	0061	1400	A to M(+1)	Sec. Byte to M
	0062	ECB5	CNTRL-1	PRC
	0063	8D20	LA	Cyl. Byte
COMPARE HEADER BYTES WITH REQUESTED ADDRESS	0064	2100	M to K(N)	Cyl. Loc. to K
	0065	8DE9	LA	Track Address
	0066	5D00	K $\oplus$ M(+1)	1 See footnote
	0067	DDA3	BR K ≠ 0	Track Error
	0068	2100	M to K(N)	Sec. to K Reg.
	0069	8D21	LA	Sector Byte
	006A	5D00	K $\oplus$ M(+1)	2 See footnote
	006B	DDA8	BR K ≠ 0	Sector Error
	006C	8D31	LA	Status Loc.
	006D	C980	K or IM	CRC Error
	006E	4900	K or M(-1)	CRC ER to M
	006F	F900	K and IM	Clr K
	0070	A745	BITH	Br Carry On
	0071	8D10	LA	1st Add Byte
	0072	2100	M to K(N)	1st byte to K
	0073	B5B5	BKFH	BR If Read
	0074	897B	UB	Br to Write
READ ROUTINE - INCLUDES FORMAT (READ HIGH ORDER 1ST)	0075	F900	K and IM	Clr K Reg.
	0076	8C00	LA	Data Buffer
	0077	E901	K add IM	Add 1 to K Reg
	0078	95B7	K ≠ MH	Br ≠ 563.2us
	0079	F900	K and IM	Clr K Reg
	007A	ECA5	CNTRL-1	PRC
	007B	A21B	BOTL	BR WR = 1
	007C	1400	A to M(+1)	Data to Mem
	007D	8880	UB	Br Check AD8
	007E	C904	K or IM	
	007F	88C4	UB	Br Send CRC Err
	0080	A225	BOTL	Br AD8 On
	0081	B2E1	BOFL	BR WR = 0
	0082	1400	A to M(+1)	Data to Mem.
	0083	A225	BOTL	Br AD8 On
	0084	887B	UB	Br Wait for WR
	0085	A215	BOTL	B WR = 1 (1st CRC)
	0086	1400	A to M(+1)	
	0087	B2E7	BOFL	B WR = 0 (2nd CRC)
	0088	EC90	CNTRL-1	Stop Read
CHECK CRC	0089	2401	CRC to A(+1)	1st CRC to A
	008A	DCA3	BR A ≠ 0	BR If CRC Err
	008B	2001	CRC to A	2nd CRC to A
	008C	DCA3	BR A ≠ 0	BR If CRC Err
	008D	A74F	BITH	BR Carry On
	008E	8959	UB	B Send Data 2200

1. $\oplus$ Requested track with track read
2. $\oplus$ Requested sector with sector read

CHECKS SECTOR COUNT FMT READ	008F	8DEA	LA	Sector Loc.
	0090	2000	M to A(N)	Sector to A
	0091	D80F	A ⊕ IM	
	0092	8007	BR A = ML	BR = Sector 15
	0093	2000	M to A(N)	Sector to A
	0094	E801	A add IM	Add 1 to Sect
	0095	1000	A to M(N)	Next Sctr to M
	0096	8828	UB	Look Next Sctr
KEEPS CHECKING CYLINDERS AND STEPS HEAD DURING FORMAT READ	0097	1800	A to M(-1)	
	0098	2000	M to A(N)	Cyl to A Reg.
	0099	E8FF	A add IM	A Reg - 1
	009A	1000	A to M(N)	Next Cyl to M
	009B	D8FF	A ⊕ IM	
	009C	DC9F	BR A ≠ 0	Br to Step HD
	009D	FB00	STI and IM	Clr Carry
	009E	8800	UB	Br to Stop Fmt
	009F	ECD4	CNTRL-1	Step Head
	00A0	FC23	CNTRL-2	ST 10 ms
	00A1	A241	BOTL	Br 10 ms On
	00A2	8828	UB	Look Next Sctr
ERROR ROUTINE	00A3	EC84	CNTRL-1	Stop Read
	00A4	8D31	LA	Status Loc.
	00A5	2000	M to A(N)	Status Loc. To A
	00A6	C808	A or IM	Trk Error Bit
	00A7	1000	A to M(N)	Trk Error To M
	00A8	EC84	CNTRL-1	Stop Read
	00A9	F900	K and IM	Clr K Reg
	00AA	8D30	LA	Err Count
	00AB	2000	M to A(N)	Err Count To A
	00AC	E801	A add IM	Add 1 to Count
	00AD	1400	A to M(+1)	Err Count To M
	00AE	0000	NOOP	Not Used
	00AF	0000	NOOP	Not Used
	00B0	A082	BATL	Br 8 Errors
	00B1	8828	UB	Br Reread Sctr
	00B2	B7B4	BIFH	Br Carry Off
	00B3	899D	UB	BR FMT Retry
	00B4	2000	M to A(N)	Status to A
	00B5	F900	K and IM	Clr K Reg.
	00B6	B478	BAFH	Br Fmt Byte Err
	00B7	887E	UB	CRC Er to 2200
	00B8	A08B	BATL	Br Trk Err
	00B9	C902	K or IM	02 to K
	00BA	88C4	UB	Sect. Err to 2200
	00BB	A419	BATH	Br if HD Moved
	00BC	C810	A or IM	
	00BD	1000	A to M(N)	HD Moved Stat→M
	00BE	8D10	LA	1st Addr. Byte
	00BF	2000	M to A(N)	1st Byte to A
	00C0	C820	A or IM	
	00C1	8911	UB	Br to Zero HD
FIRST AND LAST STROBE TO CPU	00C2	F900	K and IM	Clr K Reg.
	00C3	C9C0	K or IM	Rein Reply
	00C4	8D32	LA	*
	00C5	1100	K to M(N)	
	00C6	B676	BOFH	Wait KBD
	00C7	FC13	CNTRL-2	Strobe to 2200

* Address, error or reinitialize to 2200.

PRIME (CONTINUED) PREPARING FOR FIRST STROBE OF ANY OPERATION	00C8	FB00	STI and IM	Clr Carry
	00C9	EC00	CNTRL-1	Clr Busy
	00CA	FC00	CNTRL-2	Clr Select
	00CB	8C00	LA	Data Buffer
	00CC	F800	A and IM	Clr A Reg.
	00CD	8D30	LA	Error Count
	00CE	1400	A to M(+1)	Clr Err Count
	00CF	1400	A to M(+1)	Clr Status Loc.
	00D0	1400	A to M(+1)	Fmt Retries
	00D1	1400	A to M(+1)	Clr Loc. 33
	00D2	1400	A to M(+1)	Clr Loc. 34
	00D3	8D0F	LA	
3 INITIAL ADDRESS BYTES FROM CPU	00D4	A624	BOTH	Look 2200 Str.
	00D5	B6D5	BOFH	Look End Str.
	00D6	A618	BOTH	Br Not Reint
	00D7	88C2	UB	Br to Reint
	00D8	0400	NOOP (+1)	Mem (+1)
	00D9	1100	K to M(N)	Addr Byte to M
	00DA	E801	A add IM	Add 1 to A
	00DB	B67B	BOFH	Wait KBD
	00DC	FC13	CNTRL-2	Str to 2200
	00DD	A03F	BATL	BR = 3rd Byte
	00DE	88D4	UB	Look Next Byte
CHECK FOR ILLEGAL ADDRESS	00DF	0000	NOOP	Delay
	00E0	0000	NOOP	Delay
	00E1	8D10	LA	1st Addr Byte
	00E2	2400	M to A(+1)	1st Addr Byte→A
	00E3	9007	BR A ≠ ML	Br Ill Addr
	00E4	2400	M to A(+1)	2nd Addr Byte→A
	00E5	9407	BR A ≠ MH	Br Ill Addr
	00E6	B03A	BAFL	BR ≠ Ill Addr
	00E7	F900	K and IM	Clr K Reg
	00E8	C901	K or IM	Hex 01 to K Reg
	00E9	88C4	UB	Ill Addr→2200
TRACK & SECTOR CONVERSION	00EA	F900	K and IM	Clr K Reg
	00EB	B0ED	BAFL	Br 256 Bit Off
	00EC	C910	K or IM	Hex 10 to K Reg
	00ED	B0DF	BAFL	BR 512 Bit Off
	00EE	C920	K or IM	Hex 20 to K Reg
	00EF	2800	M to A(-1)	3rd Addr Byte→A
	00F0	B472	BAFH	Br 128 Bit Off
	00F1	C908	K or IM	Hex 08 to K Reg
	00F2	B4B4	BAFH	Br 64 Bit Off
	00F3	C904	K or IM	Hex 04 to K Reg
	00F4	B4D6	BAFH	Br 32 Bit Off
	00F5	C902	K or IM	Hex 02 to K Reg
	00F6	B4E8	BAFH	Br 16 Bit Off
	00F7	C901	K or IM	Hex 01 to K Reg
	00F8	8DE9	LA	Trk Loc.
	00F9	1500	K to M(+1)	Trk Loc. to M
	00FA	F80F	A and IM	Mask Hi Bits
	00FB	1000	A to M(N)	Sctr Loc→M
	00FC	2100	M to K(N)	Sctr to K
	00FD	F803	A and IM	
	00FE	1000	A to M(N)	
	00FF	6000	A add M(N)	

TRACK & SECTOR CONVERSION (CONT'D)	0100	2000	M to A(N)	
	0101	6000	A add M(N)	
	0102	F800	A and IM	Clr A Reg.
	0103	B1B5	BKFL	
	0104	C801	A or IM	
	0105	B177	BKFL	
	0106	C802	A or IM	
	0107	6000	A add M(N)	Sctr Conv to M
SELECT DESIRED DISK FROM CONVERSION	0108	8D10	LA	1st Add Byte
	0109	2000	M to A(N)	1st Byte to A
	010A	B6BF	BOFH	Br Disk #3
	010B	A41D	BATH	BR Disk #2
	010C	880F	UB	BR Sel Disk #1
	010D	FC02	CNTRL-2	Sel Disk #2
	010E	8810	UB	Br Ck Hdld Fi
	010F	FC01	CNTRL-2	Sel Disk #3
	0110	8810	UB	Br Ck Hdld Fi
LOAD HEAD & SELECT APPROPRIATE TRACK ADDRESS	0111	EC80	CNTRL-1	Load Head
	0112	8DE9	LA	Trk Addr
	0113	2100	M to K(N)	Trk Addr to K
	0114	B6BB	BOFH	Br Disk #3
	0115	A41C	BATH	Br Disk #2
	0116	8D25	LA	D #1 Trk Loc.
	0117	A42E	BATH	Trk Err, Zero HD
	0118	2000	M to A(N)	Trk Loc. to A
	0119	A48D	BATH	Al Rdy Zero HD
	011A	8821	UB	Br to Zero HD
	011B	8921	UB	Br Trk 3 Loc.
	011C	8923	UB	Br Trk 2 Loc.
	011D	8925	UB	
	011E	F800	A and IM	Clr A Reg
	011F	1000	A to M(N)	Set Trk Loc. to 0
	0120	8821	UB	Br to Zero HD
	0121	8D27	LA	Disk #3 Trk Loc.
	0122	8917	UB	
	0123	8D26	LA	Disk #2 Trk Loc.
	0124	8917	UB	
STEP HEAD TO DESIRED TRACK	0125	F87F	A and IM	
	0126	C980	K or IM	
	0127	1100	K to M(N)	
	0128	D87F	A $\oplus$ IM	
	0129	3C00	A ADD M(+1)	
	012A	A74D	BITH	Br Carry On
	012B	D8FF	A $\oplus$ IM	
	012C	8933	UB	
	012D	E801	A ADD IM	Add 1 to A
	012E	EC80	CNTRL-1	Set Dir 77
	012F	ECC0	CNTRL-1	Step Head

STEP HEAD TO DESIRED TRACK (CONTINUED)	0130	FC23	CNTRL-2	Start 10 ms
	0131	A241	BOTL	Br 10 ms
	0132	E8FF	A add I	Subt. 1 From A
	0133	CC39	BR A = 0	
	0134	B7B6	BIFH	Br Carry Off
	0135	892E	UB	
	0136	EC90	CNTRL-1	Set Dir→0
	0137	ECD0	CNTRL-1	Step Head
	0138	8930	UB	
	0139	FB00	STO and IM	C/R Carry
	013A	FC23	CNTRL-2	Start 10 ms
	013B	A24B	BOTL	Br 10 ms On
HEAD MOVED PREVIOUSLY? POSSIBLE RETRY	013C	8D31	LA	Status Loc.
	013D	2000	M to A(N)	Status to A
	013E	0000	NOOP	
	013F	0000	NOOP	
	0140	B4E3	BAFH	Br HD not moved
	0141	8828	UB	Br to R/W
	0142	88C2	UB	BR to Reint
ANSWER LAST ADDRESS BYTE	0143	8D10	LA	1st Add Byte
	0144	2800	M to A(-1)	
	0145	B675	BOFH	Wait KBD
	0146	FC13	CNTRL-2	Str To 2200
	0147	A44C	BATH	Br If Write
	0148	A628	BOTH	Wait 2200 Str
	0149	B6D9	BOFH	Wait End Str
	014A	B6E2	BOFH	Wait KBD
	014B	8957	UB	
	014C	F800	A AND IM	CLR A Reg
DATA FROM CPU (WRITE)	014D	8C00	LA	Data Buffer
	014E	A62E	BOTH	Wait Str
	014F	B6DF	BOFH	Wait End Str
	0150	A612	BOTH	Br Not Reint
	0151	88C2	UB	Br to Reint
	0152	1100	K to M(N)	Data Byte to M
	0153	89C0	UB	Br to Gen LRC
	0154	0000	NOOP	Not Used
ACCEPT LRC BYTE FROM CPU	0155	0000	NOOP	Not Used
	0156	0000	NOOP	Not Used
	0157	EC84	CNTRL-1	Bsy On
	0158	8828	UB	Br to Write
RAM LOCATION OF CONTAINS A 00 BYTE	0159	F900	K and IM	Clr K Reg
	015A	8D10	LA	1st Add Byte
	015B	2800	M to A(-1)	
	015C	B67C	BOFH	Wait KBD
	015D	FC13	CNTRL-2	Str to 2200
	015E	0000	NOOP	Delay
	015F	0000	NOOP	Delay
	0160	0000	NOOP	Delay
	0161	8C00	LA	Data Buffer
	0162	A48E	BATH	Br If compare
	0163	F800	A and IM	Clr A Reg

SEND DATA & CRC ON READ	0164	B674	BOFH	Wait KBD
	0165	FC13	CNTRL-2	Str to 2200
	0166	0000	NOOP	Delay
	0167	0000	NOOP	Delay
	0168	6C00	A ADD M(+1)	Generate LRC
	0169	B2D4	BOFL	Br AD8 Off
	016A	1000	A to M(-1)	LRC to Mem
	016B	B67B	BOFH	Wait KBD
	016C	FC13	CNTRL-2	LRC to 2
DATA FROM CPU FOR WRITE COMPARE	016D	88C8	UB	Br to Beg
	016E	A62E	BOTH	Wait 2200 Str
	016F	B6DF	BOFH	Wait End Str
	0170	5D00	K $\oplus$ M(+1)	*
	0171	CD73	BR K = 0	Br Data Compare
	0172	C8FF	A or Im	
	0173	A225	BOTL	Br AD8 On
	0174	896E	UB	Br to Compare
	0175	A625	BOTH	Wait 2200 Str
	0176	B6D6	BOFH	Wait End Str
	0177	8009	BR A = ML	B No Err On Comp
	0178	88E7	UB	Br Send Err
	0179	F900	K and IM	Clr K Reg
	017A	898A	UB	
WRITE ROUTINE (WRITE HIGH ORDER 1ST)	017B	EC84	CNTRL-1	Stop Read
	017C	F800	A and IM	Clr A Reg
	017D	F900	K and IM	Clr K Reg
	017E	E901	K ADD IM	Add 1 to K
	017F	959E	BR K $\neq$ MH	Br $\neq$ 460.8us
	0180	8DF9	LA	
	0181	ECA6	CNTRL-1	WTG
	0182	ECA6	CNTRL-1	PRC
	0183	A716	BITH	Br Sm On
	0184	EC80	CNTRL-1	Stop Write
	0185	88E7	UB	Br Send Err
	0186	A223	BOTL	Br AD8 On
	0187	A717	BITH	BR SM ON
	0188	B7E8	BIFH	BR SM OFF
	0189	EC80	CNTRL-1	Stop Write
	018A	B2D5	BOFL	Br AD8 Off
	018B	B275	BOFL	Br Rdy Err
	018C	F900	K and IM	Clr K Reg
	018D	88C4	UB	Last Byte$\rightarrow$2200
	018E	0000	NOOP	Not Used
	018F	0000	NOOP	Not Used
100 MS DELAY TO CHECK FORMAT INSTRUCTION LEGITMATE	0190	F800	A and IM	Clr A Reg
	0191	FB00	STI AND IM	Clr Carry
	0192	FC23	CNTRL-2	Start 10 ms
	0193	A243	BOTL	Br 10 ms
	0194	E801	A ADD IM	Add 1 to A
	0195	90A1	BR a $\neq$ ML	BR $\neq$ 10 (100 ms)
	0196	A748	BITH	Br Carry On
	0197	8800	UB	Br to Prime
	0198	880F	UB	Br to Fmt

*Data read with data from 2200

COUNT FORMAT RETRIES	0199	0000	NOOP	Not Used
	019A	0000	NOOP	Not Used
	019B	A74D	BITH	Br Carry On
	019C	88E7	UB	Err to 2200
	019D	8D33	LA	Format Retries
	019E	2000	M to A(N)	
	019F	E801	A ADD IM	
	01A0	1000	A to M(N)	Add 1 to A Reg.
	01A1	A043	BATL	Br = 4 Retries
	01A2	89B0	UB	
FLASH FORMAT LIGHT	01A3	F800	A AND IM	Clr A Reg
	01A4	E801	A ADD IM	Add 1 to A
	01A5	FC23	CNTRL-2	START 10 ms
	01A6	A246	BOTL	Br 10 ms On
	01A7	90F4	BR A $\neq$ ML	Br A $\neq$ 15 (150 ms)
	01A8	F800	A and IM	Clr A Reg
	01A9	FC00	CNTRL-2	Turn Off D1
	01AA	E801	A ADD IM	Add 1 to A
	01AB	FC23	CNTRL-2	Start 10 ms
	01AC	A24C	BOTL	BR 10 ms On
	01AD	90FA	BR A $\neq$ ML	Br A $\neq$ 15 (150 ms)
	01AE	FC04	CNTRL-2	Turn on DK1
	01AF	89A3	UB	
BRANCH TO RETRY FORMAT	01B0	F800	A and IM	Clr A Reg
	01B1	8DE9	LA	Trk Loc.
	01B2	1400	A to M(+1)	Clr Trk
	01B3	1400	A to M(+1)	Clr Sector
	01B4	880F	UB	Br to Retry
	01B5	0000	NOOP	
	01B6	0000	NOOP	
	01B7	0000	NOOP	
	01B8	0000	NOOP	
	01B9	0000	NOOP	
	01BA	0000	NOOP	
	01BB	0000	NOOP	
	01BC	0000	NOOP	
	01BD	0000	NOOP	
	01BE	0000	NOOP	
	01BF	0000	NOOP	
	01C0	6C00	A add M(+1)	Generate LRC
	01C1	A223	BOTL	Br AD8 On
	01C2	894E	UB	Br to Next Byte
	01C3	A623	BOTL	Wait 2200 Str
	01C4	B6D4	BOFH	Wait End of Str
	01C5	8D34	LA	LRC Loc
	01C6	1100	K to M(N)	LRC to M
	01C7	5C00	A $\oplus$ M(+1)	*
	01C8	DCCA	BA $\neq$ 0	Br LRC Bad
	01C9	8957	UB	Br to Write
	01CA	88E7	UB	Br to Send Error
	01CB	0000	NOOP	
	01CC	0000	NOOP	
	01CD	0000	NOOP	
	01CE	0000	NOOP	
	01CF	0000	NOOP	

* $\oplus$ LRC byte from 2200 with LRC byte generated.

01D0	EC00	CNTRL-1	Turn Off RDG
01D1	8C00	LA	Mem to 00
01D2	F900	K and IM	Clr K Reg
01D3	F800	A and IM	Clr A Reg
01D4	C955	K or IM	55 to K
01D5	C8AA	A or IM	AA to A
01D6	1000	A to M(N)	AA to M
01D7	5100	K ⊕ M(N)	FF in Mem
01D8	2000	M to A(N)	FF to A
01D9	E801	A ADD IM	Add 1 (result 0)
01DA	DCD0	BR A ≠ 0	
01DB	7D00	K and M(+1)	Result to K
01DC	9150	BR K ≠ ML	BR 1 4-bit ≠ 1
01DD	9550	BR K ≠ MH	Br 10 40-bit ≠ 1
01DE	7100	K and M	A
01DF	4100	K or M	
01E0	2800	M to A(-1)	
01E1	5C00	A ⊕ M(+1)	Result to A
01E2	7C00	A and M(+1)	Result to A
01E3	CCE5	BR A = 0	
01E4	89D0	UB	
01E5	E801	A ADD IM	Add 1 to A
01E6	1400	A to M(+1)	
01E7	B2D5	BOFL	Br AD8 Off
01E8	1000	A to M(N)	
01E9	2100	M to K(N)	
01EA	8C00	LA	Mem→0
01EB	5D00	K ⊕ M(+1)	Result to K
01EC	911C	BR K ≠ ML	B ≠ 01
01ED	8C02	LA	
01EE	5100	K ⊕ M	Result to M
01EF	2400	M to A(+1)	
01F0	E901	K ADD IM	Add 1 to K
01F1	A224	BOTL	Br AD8 On
01F2	CCEE	BR A = 0	
01F3	89F3	UB	
01F4	FC00	CNTRL-2	Deselect Drives
01F5	FC01	CNTRL-2	Sel Disk 3
01F6	EC80	CNTRL-1	Load HD 3
01F7	FC02	CNTRL-2	Sel Disk 2
01F8	EC80	CNTRL-1	Load HD 2
01F9	FC04	CNTRL-2	Sel Disk 1
01FA	EC80	CNTRL-1	Load HD 1
01FB	B77B	BIFH	Br Sm Off
01FC	A78C	BITH	Br Sm On
01FD	A71D	BITH	Br HD Loaded
01FE	B7EE	BIFH	Br HD Unloaded
01FF	8800	UB	

2.4 TROUBLESHOOTING PROCEDURES

2.4.1 *INTRODUCTION*

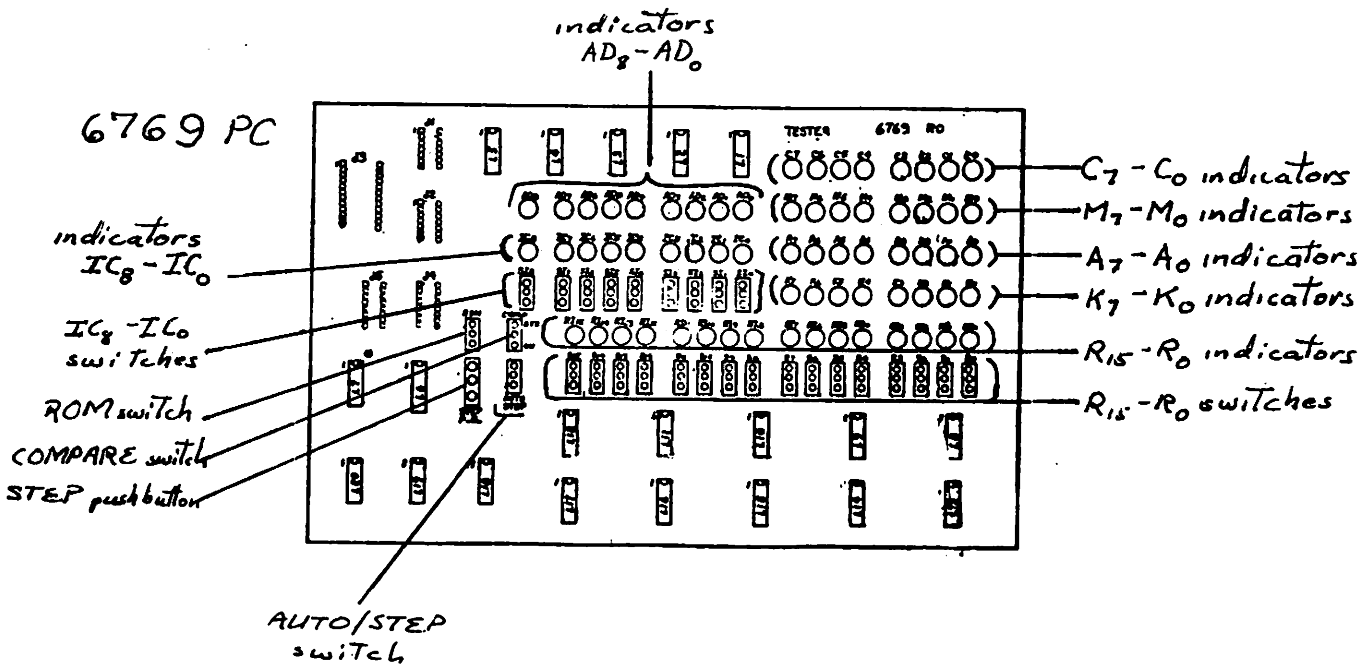
The purpose of these test units is to observe internal microprocessor conditions and to exercise, via manual control, all microprocessor functions.

Two versions of 2270 test units exist: one board for use with the 6718 only (a 6769 tester) and another capable of testing both the 6718 and 7018 (a 7069 tester). The 6769 test board has the test cables for testing the 6718 hard-wired to the 6769. The 7069 has three 36 lead ribbon test cables for testing the 7018 hard-wired to the 7069 and, five IC sockets to connect the test cables to the 6718 board.

Schematic diagrams for the 6769 and 7069 testers are included at the end of this section.

2.4.2 *FAMILIARIZATION WITH PHYSICAL LAYOUT OF TEST UNITS*

Version 1 - 6769 Tester



Version 2 - 7069 tester

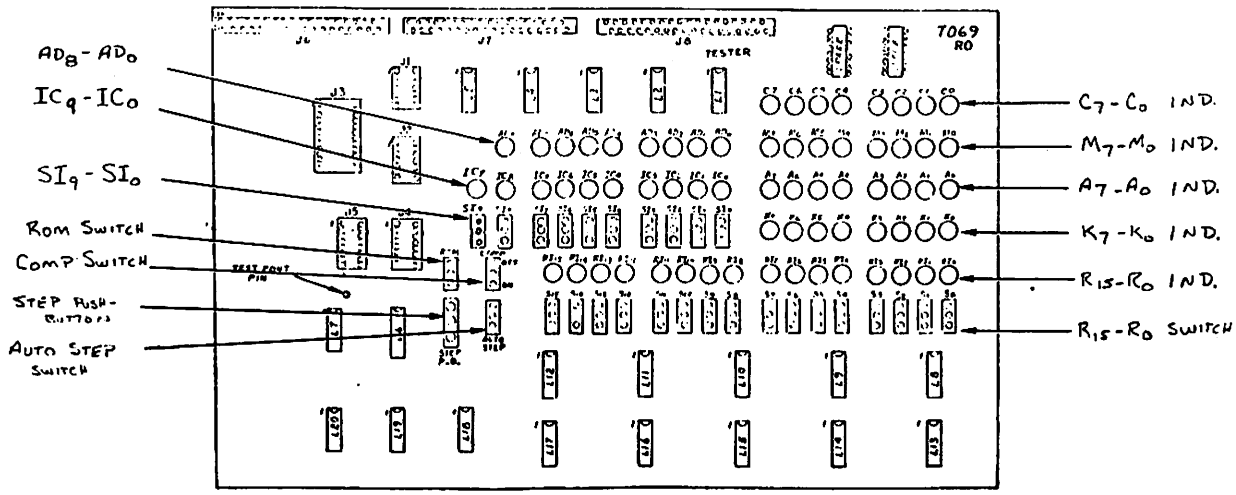


CHART 2.4.1

	ON 6718 PCB	PART #	7069 PCB CONN
CABLE# 1	T.P.s	(None) 16 Lead Ribbon	J5
CABLE# 2	T.P.s	881000	J1
CABLE# 3	T.P.s	860000	J2
CABLE# 4	T.P.s	883000	J3
CABLE# 5	T.P.s	882000	J4
6718 PCB T.P.s		654-1157R	

CHART 2.4.2

7069 PCB	PART #	7018 PCB
J6	220-3013	P9
J7	220-3013	P7
J8	220-3013	P8

NOTE:

Pin 1 of each test cable fingerboard from the 7069 PCB must plug into pin 1 of each female test connector on the 7018 PCB.

If a pin on the new tester cable breaks, the cable must be replaced. The cable and test points for the 6718 board can be ordered domestically and internationally through the Home Office.

2.4.3 *OPERATIONAL USE OF TEST UNITS*

Each set of light indicators (labeled accordingly) represent current outputs of the following:

1. Designated Registers
   A register (A_7 - A_0 indicators)
   K register (K_7 - K_0 indicators)
   ST_0, ST_1 registers (C_7 - C_0 indicators)

2. ALU Output (C_7 - C_0 indicators)

3. ROM Output (R_{15} - R_0)

4. ROM Address (IC_8 - IC_0)

5. RAM Output Register (M_7 - M_0)

6. RAM Address (AD_8 - AD_0); 6769
   (MA_7 - MA_0); 6452

7. CRB (CPU $\overline{\text{Ready}}$/Busy); 6452

Item 3 is actually dual purpose; indicators R_{15} - R_0 can also represent a manually set ROM instruction, to be used in lieu of (supercedes) 6718 ROM outputs. Such manually introduced commands to the microprocessor are set on ROM bit switches S_{15} - S_0 (See pictorials and schematics of 6769 and 7069). The ROM switch at schematic coordinates H, 14 (both 6769, 7069) must be in the UP position to allow indicators R_{15} - R_0 to display manual settings of ROM bit switches S_{15} - S_0. Use of this feature follows in proceeding text.

Item 4, ROM Address indicators IC_8 - IC_0 can be used in conjunction with the Compare Switch to halt the microprogram at any step manually preset on switches SI_9 - SI_0 (SI_9 should always be UP; AUTO/STEP in AUTO mode). Halt occurs when the indicators IC_{8-0} = switch settings. Two other switches control test unit operation: the AUTO/STEP toggle switch and the STEP pushbutton microswitch. With AUTO/STEP in the STEP mode, the microprocessor will complete one cycle each time the STEP pushbutton is depressed. When the AUTO/STEP switch is in the AUTO mode, and the STEP pushbutton is depressed once, the microprocessor begins to cycle continuously.

If a Halt was performed at a desired step by using the COMPARE switch (DOWN = ON), the microprogram will continue if the STEP pushbutton is depressed. To disable the COMPARE halt function, turn the COMPARE switch OFF (UP). The COMPARE feature is useful for stopping the microprocessor so that key points in the microprogram may be monitored. Monitoring key points in the program sometimes reveals exactly where the microprocessor is failing. Also, some failures occur only during full speed ("on the fly") operation and may not occur during manual stepping of given routine.

Again, note that when manually stepping through the microprogram, the IC may not continue past certain locations. This condition could be normal if the present command is a conditional branch command (e.g. a situation where the microprogram branches on itself until a condition is met).

It may be desirable to do a single command repeatedly, particularly if the command is suspected of intermittent failure. To accomplish this, place AUTO/STEP in the AUTO mode, ROM switch OFF (disable ROM output; enable S_{15} - S_0 manually simulated command), and depress the STEP pushbutton. The manually set ROM command will execute repetitively.

Generally speaking, a good procedure for manual checkout of the microprocessor would be to manipulate data from register to register, using Register commands and Immediate commands. Control Commands verify communication to CPU or Shugart disk drive. Load Auxiliary commands will verify contents and proper addressing of RAM.

Hands-on use is the most valuable tool for developing solid approaches to microprocessor troubleshooting with these test units.

2.4.4 *6718/7018 REPAIR*

The following items are required to aid in the repair of the 6718/7018 board:

1) The outline of the microcode steps involving a format, write and read (Section 2.2.4).
2) The flow charts and microprogram (Section 2.2.4).
3) The 2270 Test/Exercise program (at end of this section).

By using the outline of the microcode steps and the A=B comparator output test point on the 6769 light board, the subroutine in which a failure occurs can be located. The 2270 Test/Exercise program is a necessary aid in checking the manual operation of the microprocessor and the manipulation of data from register to register using register, immediate, control and load auxiliary commands.

TROUBLESHOOTING PROCEDURE

1. Check board visually for shipping or handling damage.
2. Load the board with tested PROMs (if applicable) and RAMs.
3. Check voltages with oscilloscope for noise and proper level.
4. Operate system (attempt a format, write and read) to check for failure.

a. Flex board lightly while operating system to check for possible opens or shorts.

b. Observe 2200 for any error codes.

5. Cut jumpers on board at L100-5 and L87-6 on the 6718 (Do not remove any jumpers on the 7018) and install light board.
6. Recheck voltages to insure against intermittent errors due to increased load.
7. Set the light board switches as follows:

a) S/R switch must be down or in ROM position.

b) AUTO/STEP switch to AUTO (up).

c) ON/OFF switch to ON (Compare switch).

d) SI9 switch must always be in the up position for testing 6718 and 7018 boards because the ROM only requires 512 addresses.

e) SI8-0 switches should be set within the failing routine, as listed in the abbreviated microprogram in Section 2.2.4. Preferably the SI switches should be set between the starting or lowest step and the point of failure.

The board is now ready for troubleshooting. As an example, it will be assumed that a 6718 board is failing during a format command (for this example, the board fails at step 002F). The basic approach to locating the step that is failing is to use the abbreviated format routine listed in Section 2.2.4.

Set the IC switches at some address in the middle of the format routine, for instance, step 001F. Depress the format button on the disk. When the program reaches step 001F and stops (with the comparator switch on the light board in the ON position), this indicates that all steps up to but not including step 001F are good. Next, set the IC switches on the light board to 0031. Depressing the format switch again causes the disk to begin formatting, however, because step 002F is faulty (no exclusive OR command), the disk will hang-up and never reach step 0031.

As a result, the problem is known to be somewhere between steps 001F and 0031, and with the same logical approach as above, it will be found that step 002F is failing.

The Test/Exercise program can be used to check basic data manipulation from register to register and a majority of the instructions. As a general rule, if a disk does not complete a format routine, the problem can be found using this program. Under normal conditions, the exercise program should run completely to the end and unconditionally branch to step 0000 and finally prime out at step 00D4 waiting for a 2200 strobe.

To use the test/exercise program, an unconditional branch must be given via the light board to step 01D0. This is accomplished by setting the switches in the following manner:

a) Set the AUTO/STEP switch in the STEP position (down).
b) ON/OFF switch to OFF (UP) or non-compare position.
c) S/R switch to S (up) position.
d) S 15-0 switches to equal $89D0_{16}$.
e) Depress the STEP pushbutton.
f) Put the AUTO/STEP switch to AUTO (up).
g) Place the S/R switch to R (down) and insure that the RI indicators are decoding EC00 (this is the first step of the exercise program).
h) Depress the step pushbutton; this initiates the program.
i) If a failure occurs, use the same procedure as outlined in the above paragraphs.

2270 TEST/EXERCISE PROGRAM

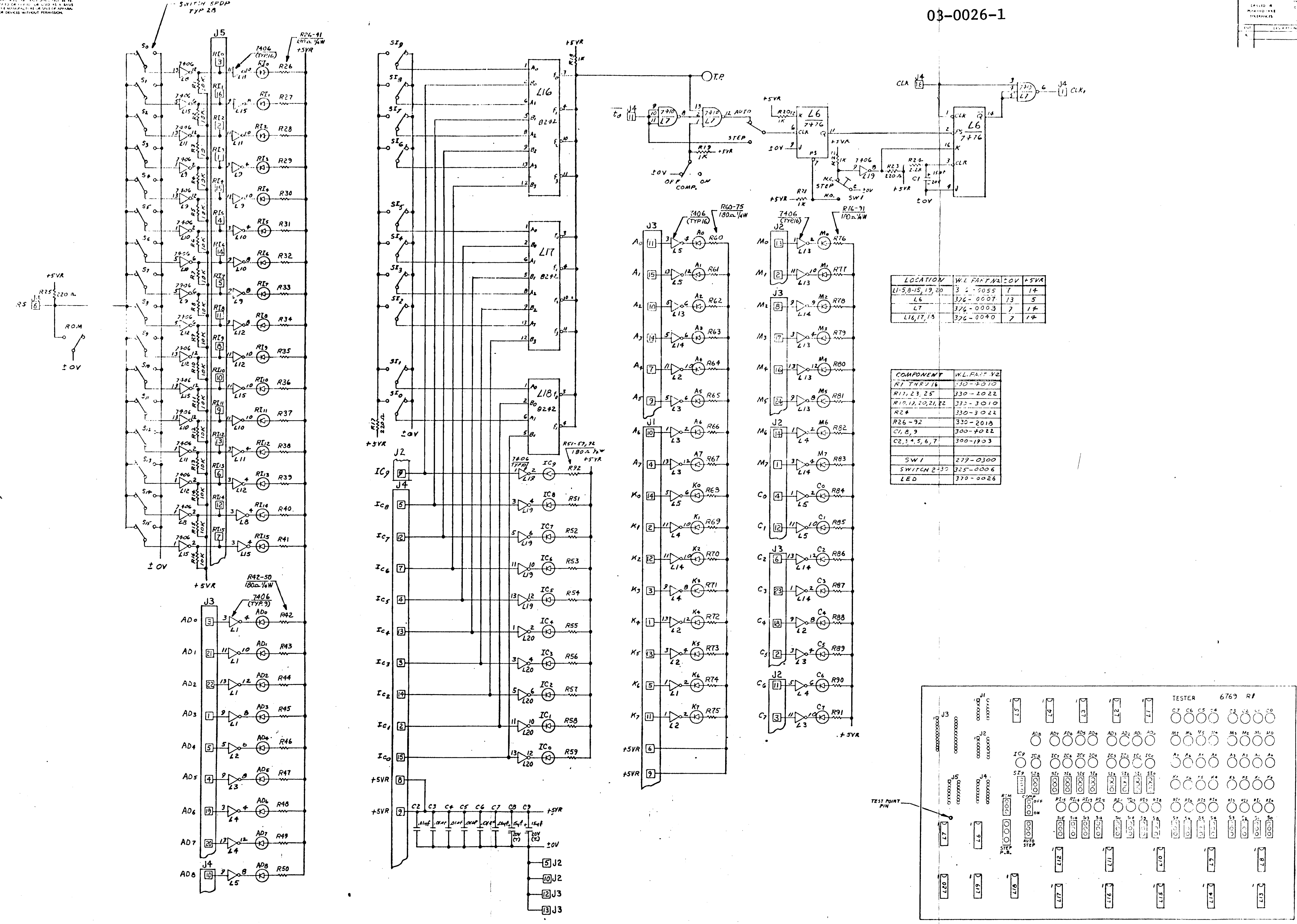
STEP	CODE	COMMENTS
01D0	EC00	Turn RDG off. Deselect the disk from A register.
01D1	8C00	Load memory address to 00.
01D2	F900	Clear K register.
01D3	F800	Clear A register.
01D4	C955	Put 55 in K register.
01D5	C8AA	Put AA in A register.
01D6	1000	Puts contents of A register (AA) in Loc. 00. NO PCH or -1.
01D7	5100	⊕ K register with Loc. 00 result should be FF in 00.
01D8	2000	Loc. 00 to A register.
01D9	E801	Add one to A register result 00.
01DA	DCD0	Branch to D0 if A ≠ to 0.
01DB	7D00	AND K register with Loc. 00 PC+1 Result 55 in K.
01DC	9150	Branch to D0 low 4 Bits in K ≠ 5.
01DD	9550	Branch to D0 High 4 bits in K ≠ 5.
01DE	7100	AND K register with Loc. 01.
01DF	4100	OR K register with Loc. 01 result 55 in 01.
01E0	2800	Loc. 01 to A register PC-1 result 55 in A.
01E1	5C00	⊕ A register with Loc. 00 result AA to A register PC+1.
01E2	7C00	AND A register with Loc. 01 result 00 to A register PC+1.
01E3	CCE5	Branch to E5 if A register = 0.
01E4	89D0	Branch to D0 because of ERROR A ≠ 0.
01E5	E801	ADD one to A register.
01E6	1400	A register to present memory address PC+1.
01E7	B2D5	Branch to E5 if AD8 not on.
01E8	1000	FE is contents of A register to Loc. 512.
01E9	2100	Loc. 512 to K register.
01EA	8C00	Set memory address to 00.
01EB	5D00	⊕ K register with Loc. 00 FF + FE result 01 in K PC+1.
01EC	911C	Branch to self if not 01 in K register.
01ED	8C02	Set memory address to 02.
01EE	5100	⊕ memory with K register result to memory.
01EF	2400	Memory to A register PC+1.
01F0	E901	Add one to K register.

01F1	A224	Branch to F4 if AD8 on.
01F2	CCEE	Branch to EE if A = 0.
01F3	89F3	Branch to self if ERROR A $\neq$ 0.
01F4	FC00	Deselect all disks.
01F5	FC01	Select Disk #3.
01F6	EC80	Load Head D #3.
01F7	FC02	Select disk #2 deselect all others.
01F8	EC80	Load Head D #2.
01F9	FC04	Select disk #1 deselect all others.
01FA	EC80	Load Head D #1.
01FB	B77B	Branch to self head unloaded.
01FC	A78C	Branch to self head loaded.
01FD	A71D	Branch sector mask low.
01FE	B7EE	Branch sector mask High.
01FF	8800	Branch to prime routine.

At this point go to Auto and hit the step pushbutton. The program should delay at 01FC for approximately 600 MS until the head unloads; if the sector counter is working the program will increment through 01FD & 01FE to the prime routine.

THIS PAGE IS INTENTIONALLY LEFT BLANK

03-0026-1



LOCATION	W.L PART No	±OV	+5VR
L1-5,8-15,19,20	3[illegible]-0055	7	14
L6	376-0007	13	5
L7	376-0003	7	14
L16,17,18	376-0040	7	14

COMPONENT	W.L. PART No
R1 THRU 16	330-4010
R17, 23, 25	330-2022
R18,19,20,21,22	330-3010
R24	330-3022
R26-92	330-2018
C1, 8, 9	300-4022
C2,3,4,5,6,7	300-1903
SW1	279-0300
SWITCH 2-30	325-0006
LED	370-0026

TESTER

WANG LABORATORIES INC. TEWKSBURY MASS. U.S.A.

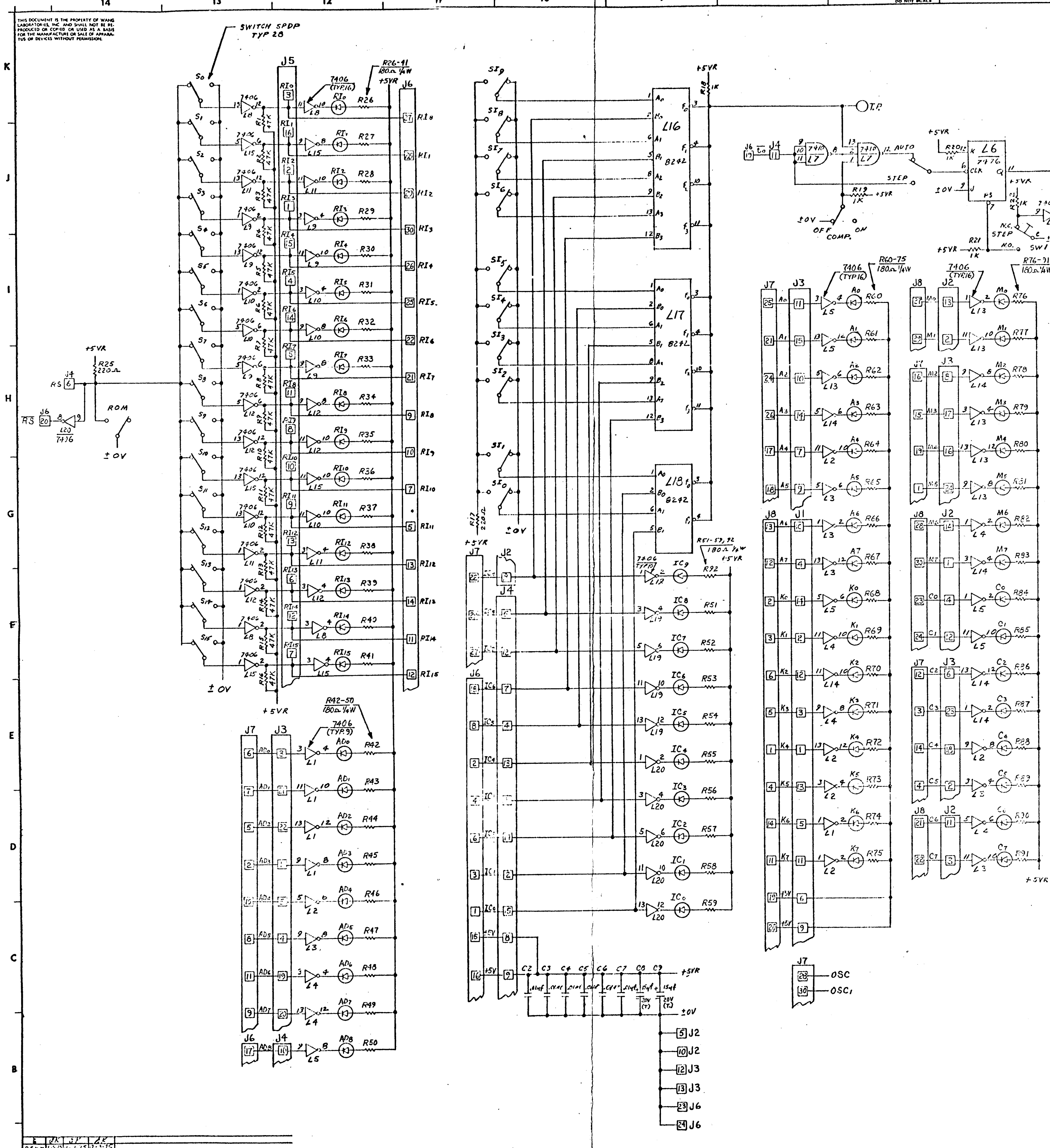
MODEL NO WCS-FLOPPY

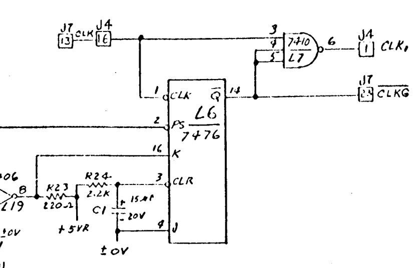
TITLE SCHEMATIC [illegible] STRAPPABLE [illegible] TEST BOARD

E 6769

69

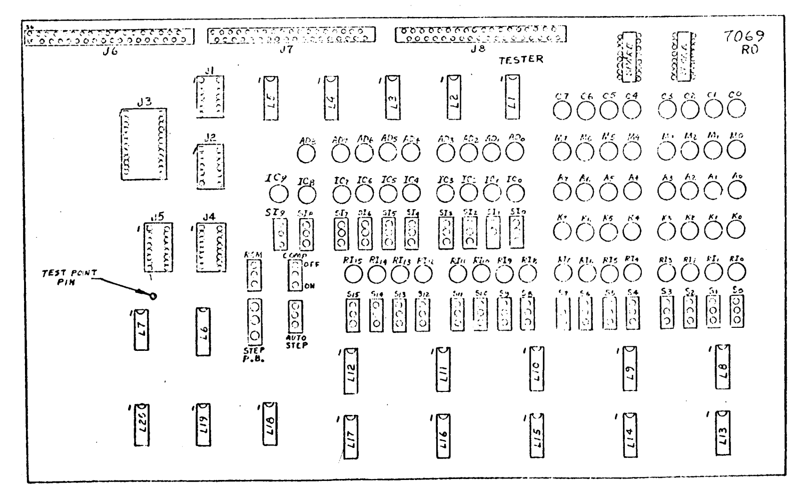
03-0026-1





LOCATION	W.L. PART NO.	±OV	+5VR
L1-5, 8-15, 19, 20	376-0055	7	14
L6	376-0007	13	5
L7	376-0003	7	14
L16, 17, 18	376-0040	7	14

COMPONENT	W.L. PART NO.
R1 THRU 16	330-4047
R17, 23, 25	330-2022
R18, 19, 20, 21, 22	330-3010
R24	330-3022
R26-92	330-2018
C1, 8, 9	300-4022
C2, 3, 4, 5, 6, 7	300-1903
SW1	279-0300
SWITCH 2-30	325-0006
LED	379-0026
J1, 2	376-9001
J3	376-9003
J4, 5	376-9002



70

TESTER

WANG LABORATORIES, INC. TEWKSBURY MASS. U.S.A.

TITLE: SCHEMATIC LOGIBLOC UNIVERSAL SHUGART FLOPPY TESTER

210-7069 | E | 7069 | 2

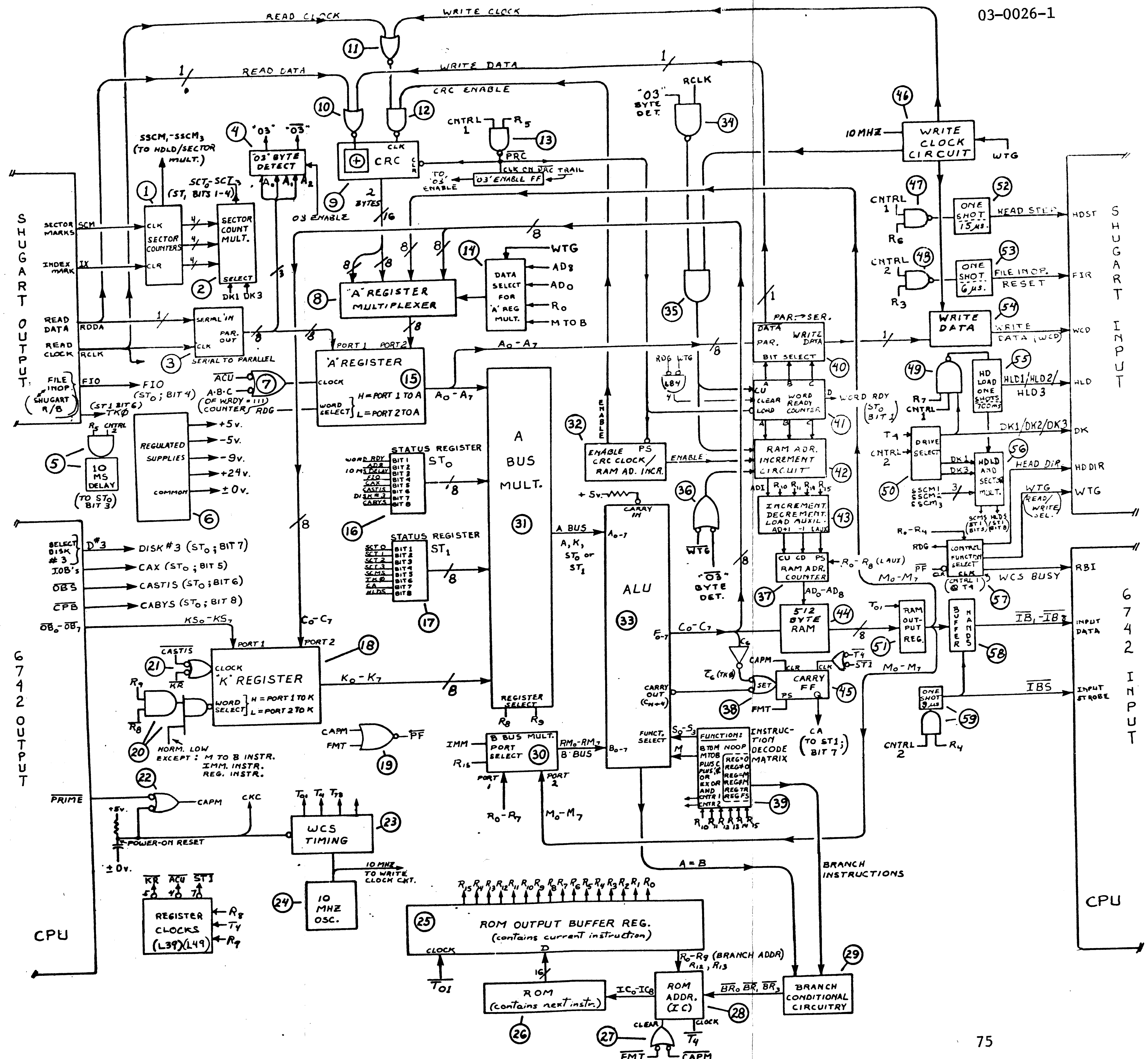
THIS PAGE IS INTENTIONALLY LEFT BLANK

2.5 MODEL 2270 BLOCK DIAGRAM AND SCHEMATICS

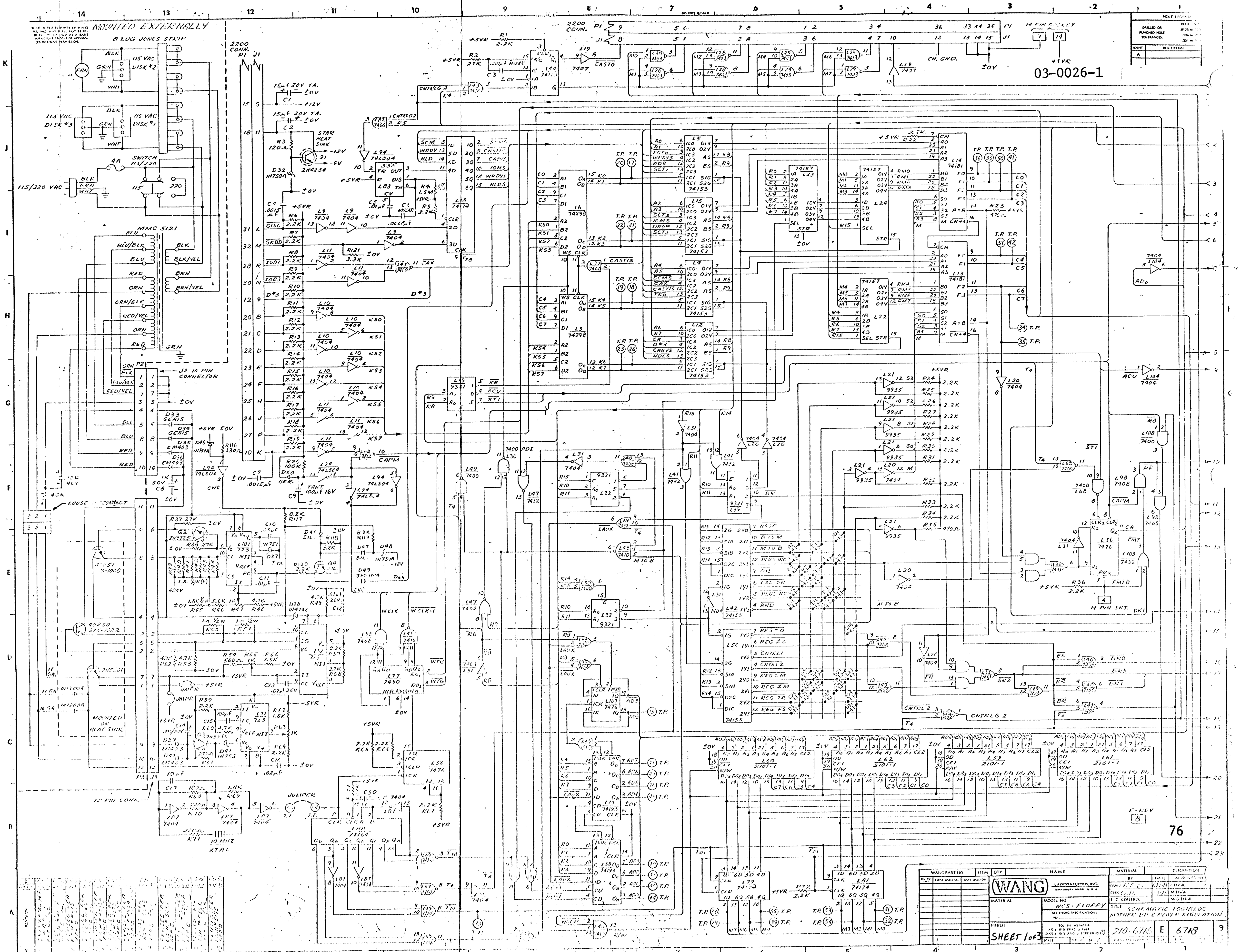
Each block of the diagram to follow is numbered; the integrated circuits which comprise each numbered block are listed below on three pages. The block diagram and the IC listing should be used to further comprehend the "HARDWARE OPERATIONAL THEORY" section of this publication.

BLOCK #	INTEGRATED CIRCUITS UTILIZED
1	L1-12/13, L9-8, L9-6, L8-12/13, L9-4, L8-9/8, L34-8/9/11/12, L17-8/9/11/12, L7-8/9/11/12
2	L16-4/7/9/12, L25-4/7/9/12
3	L2-4, L2-2, L2-12, L73-15, L76-3 thru 6 and 10 thru 13.
4	L95-11, L84-13, L73-10/11
5	L82-3, L94-10, L83-3
6	L71, L92, L108
7	L74-11, L104-2
8	L38, L55, L54, L37
9	L53, L36, L45, L46-6, L46-3, L46-11
10	L72-11
11	L74-8
12	L95-6
13	L51-6
14	L102-8, L102-6, L102-11, L102-3, L72-6, L72-8, L82-8, L46-8, L1-8/9
15	L67, L66
16	L18, L5, L15, L4, L12
17	L18, L5, L15, L4, L12
18	L11, L10, L6, L3
19	L98-3
20	L30-11, L47-10, L31-6, L48-6

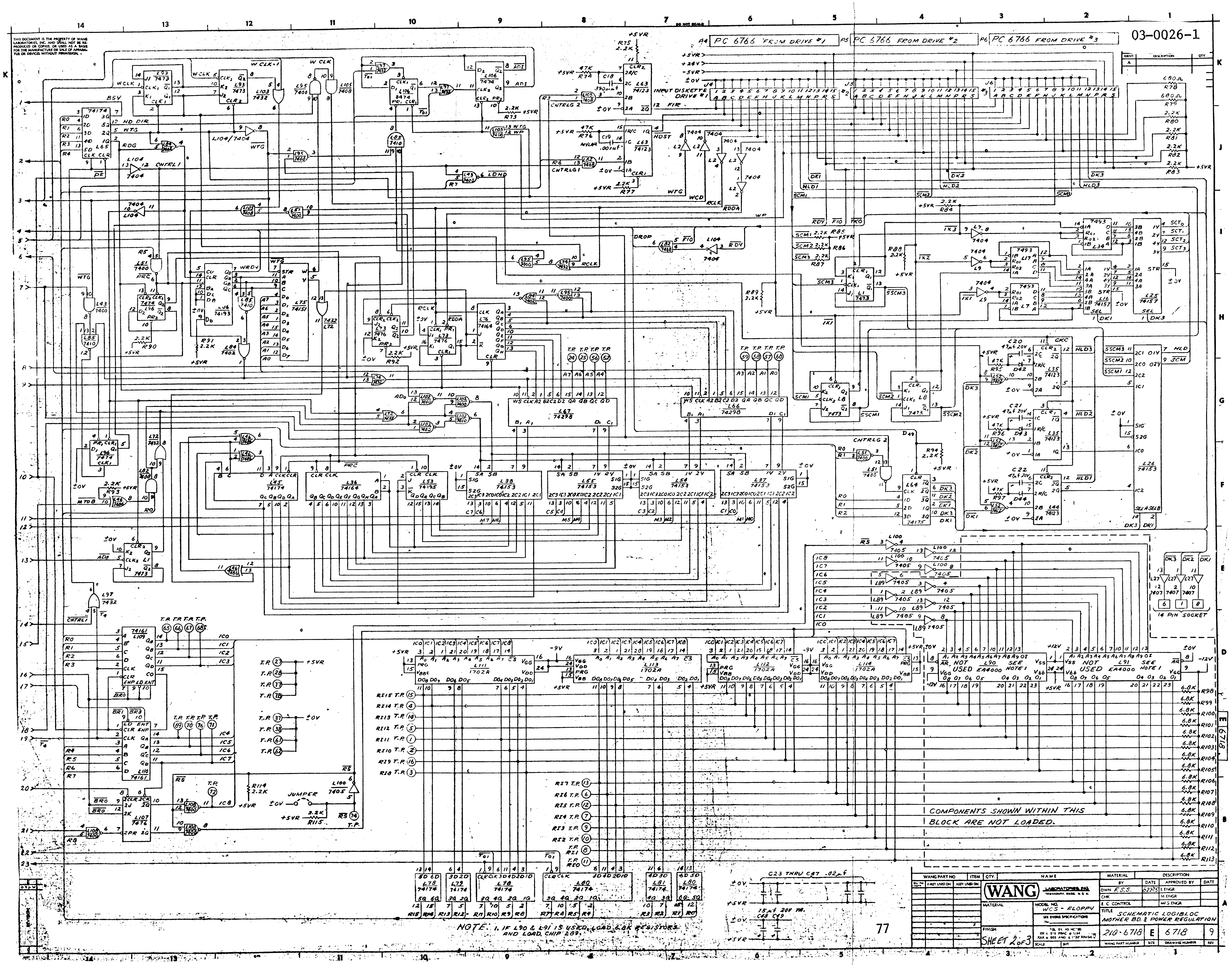
03-0026-1



SHUGART OUTPUT
SHUGART INPUT
6742 OUTPUT
6742 INPUT
CPU
CPU
READ CLOCK
WRITE CLOCK
READ DATA
WRITE DATA
CRC ENABLE
SECTOR MARKS
INDEX MARK
READ DATA
READ CLOCK
FILE INOP.
SHUGART R/B
SSCM₁-SSCM₃ (TO HDLD/SECTOR MULT.)
SECTOR COUNTERS
SECTOR COUNT MULT.
'03' BYTE DETECT
CRC
'03' ENABLE FF
SERIAL TO PARALLEL
'A' REGISTER MULTIPLEXER
DATA SELECT FOR 'A' REG MULT.
'A' REGISTER
REGULATED SUPPLIES
+5v.
-5v.
-9v.
+24v.
±0v.
10 MS DELAY
STATUS REGISTER
A BUS MULT.
ALU
'K' REGISTER
ENABLE CRC CLOCK/ RAM AD. INCR.
WORD READY COUNTER
RAM ADR. INCREMENT CIRCUIT
INCREMENT DECREMENT LOAD AUXIL.
RAM ADR. COUNTER
512 BYTE RAM
RAM OUT-PUT REG.
CARRY FF
WRITE CLOCK CIRCUIT
WRITE DATA
ONE SHOT 15μs.
ONE SHOT 6μs.
HEAD STEP
FILE INOP. RESET
HD LOAD ONE SHOTS 700ms
DRIVE SELECT
HDLD AND SECT. MULT.
CONTROL FUNCTION SELECT
WCS BUSY
BUFFER NANDS
INPUT DATA
INPUT STROBE
B BUS MULT. PORT SELECT
INSTRUCTION DECODE MATRIX
WCS TIMING
10 MHZ OSC.
REGISTER CLOCKS (L39)(L49)
ROM OUTPUT BUFFER REG. (contains current instruction)
ROM (contains next instr.)
ROM ADDR. (IC)
BRANCH CONDITIONAL CIRCUITRY
BRANCH INSTRUCTIONS
POWER-ON RESET

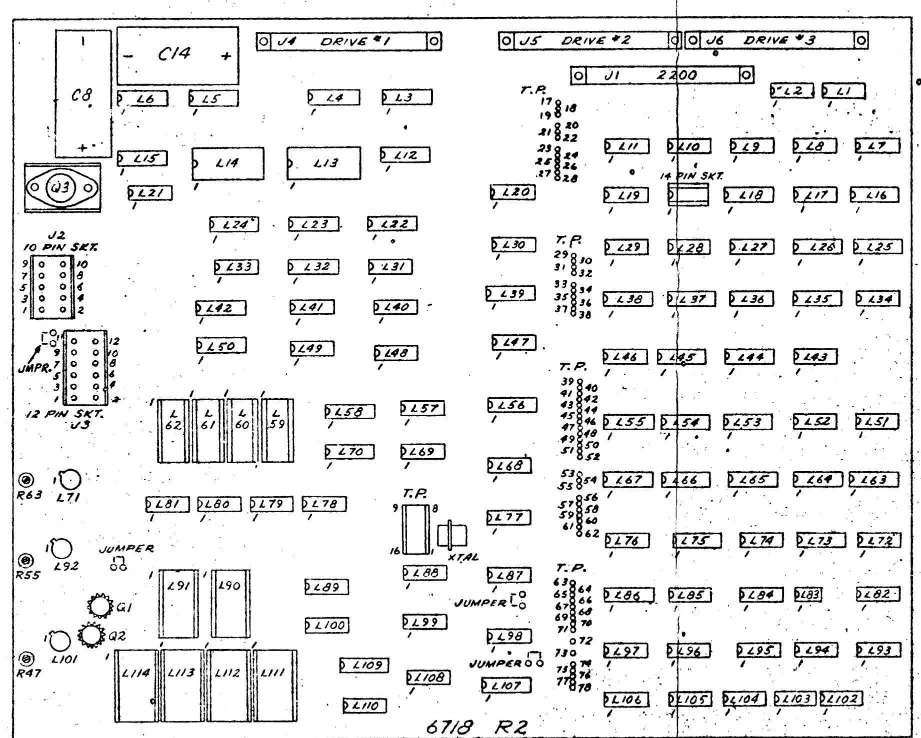


MOUNTED EXTERNALLY
8 LUG JONES STRIP
115 VAC DISK #2
115 VAC DISK #3
115 VAC DISK #1
SWITCH 115/220
115/220 VAC
MMC 5121
J2 10 PIN CONNECTOR
2200 CONN.
STAR HEAT SINK
12 PIN CONN.
JUMPER
10 MHZ XTAL
MOUNTED ON HEAT SINK
LOOSE CONNECT
14 PIN SOCKET
14 PIN SKT.
03-0026-1
76
E-REV 8
WANG LABORATORIES, INC. TEWKSBURY MASS. U.S.A.
MODEL NO WCS-FLOPPY
TITLE SCHEMATIC LOGIBLOC MOTHER BD & POWER REGULATION
SHEET 1 of 3
210-6718
E
6718
9



03-0026-1
THIS DOCUMENT IS THE PROPERTY OF WANG LABORATORIES, INC. AND SHALL NOT BE REPRODUCED OR COPIED, OR USED AS A BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS OR DEVICES WITHOUT PERMISSION.
P4 PC 6766 FROM DRIVE #1
P5 PC 6766 FROM DRIVE #2
P6 PC 6766 FROM DRIVE #3
INPUT DISKETTE DRIVE #1
14 PIN SOCKET
COMPONENTS SHOWN WITHIN THIS BLOCK ARE NOT LOADED.
C23 THRU C47 .02μF
NOTE: 1. IF L90 & L91 IS USED, LOAD 6.8K RESISTORS AND LOAD CHIP 209.
WANG LABORATORIES, INC.
WCS - FLOPPY
SCHEMATIC LOGIBLOC MOTHER BD. & POWER REGULATION
SHEET 2 OF 3
210-6718
E
6718
9

77



I.C. LOCATION	W.L. NO.	TERM ±OV	TERM +5VR
L1,8,93	376-0005	11	4
L2,9,10,11,20,31,87, 104	376-0010	7	14
L3,6,66,67	376-0138	8	16
L4,5,12,15,26,37,38,54,55	376-0048	8	16
L7,17,34	376-0011	10	5
L13,14	376-0099	12	24
L16,22,23,24,25	376-0082	8	16
L18,45,65,78,79,80,81	376-0098	8	16
L19,27	376-0056	7	14
L21	376-0025	7	14
L28,29	376-0028	7	14
L30,43,49,51,68,95,102,108	376-0002	7	14
L32,39	376-0096	8	16
L33	376-0012	7	14
L35,44,63	376-0080	8	16
L36,76,88	376-0102	7	14
L40,57,82,98,105	376-0081	7	14
L41,69,72,74,97,99,103	376-0093	7	14
L42,50	376-0049	8	16
L46	376-0036	7	14
L47,52,84	376-0016	7	14
L48,85	376-0003	7	14
L53	376-0097	8	16
L56,73,107	376-0007	13	5
L58,70,86	376-0053	8	16
L59,60,61,62	377-0308	8	22
L64	376-0119	8	16
L71,92,101	376-0066		
L75	376-0047	8	16
L77	376-0073	10	5
L83	376-0126	1	8
L89,100	376-0029	7	14
L90,91			24
L96,106	376-0006	7	14
L109,110	376-0094	8	16
L111	378-0452R1		12
L112	378-0454R1		12
L113	378-0453R1		12
L114	378-0455R1		12
L94	376-0180	7	14

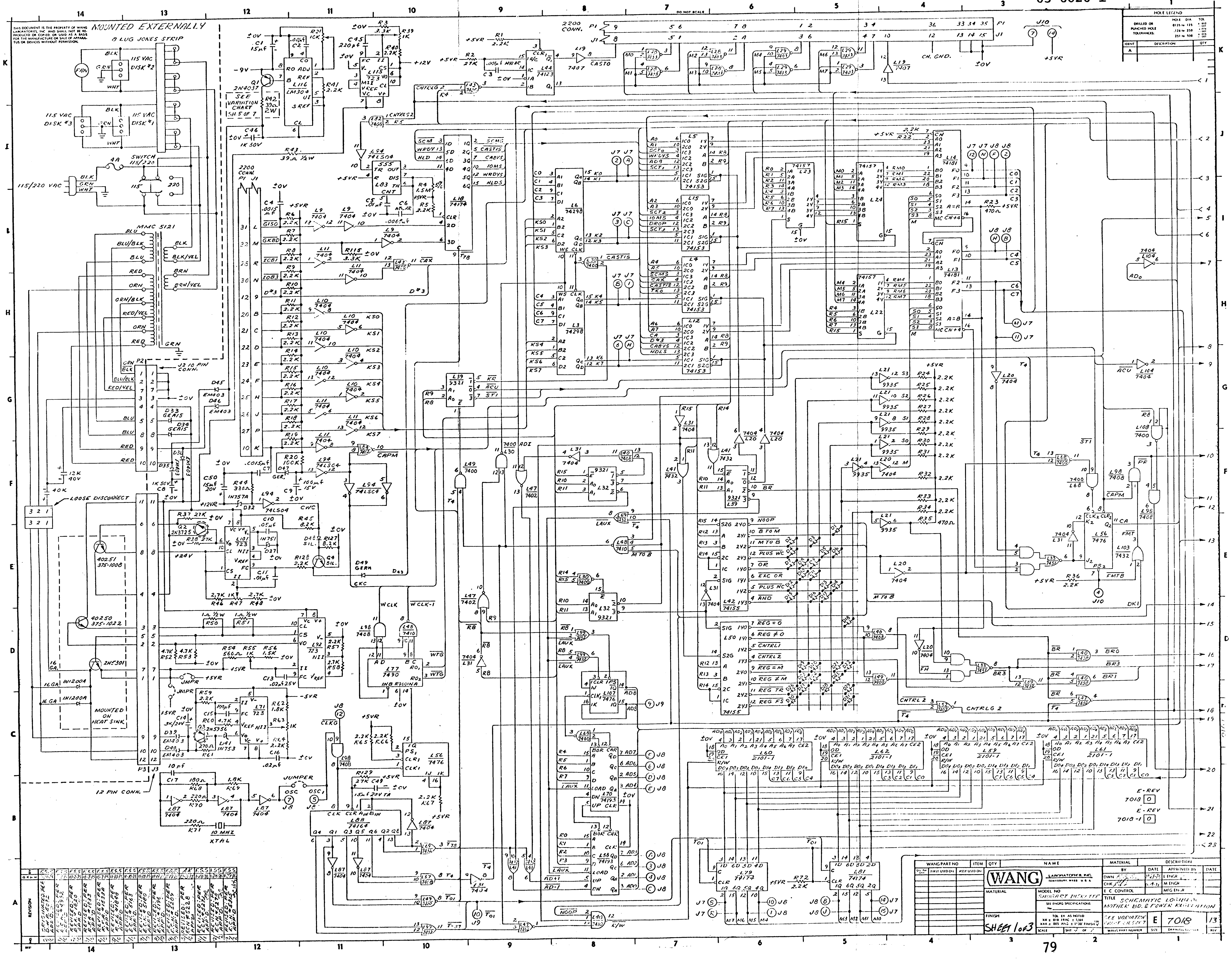
COMPONENT	W.L. NO.
R1, 5-19, 22, 24-34, 36, 57, 59, 64-67, 72, 73, 75, 77, 80-94, 114, 115, 120	330-3022
R2, 37, 38, 21	330-4027
R3	330-2012
R4	330-6016
R20	330-5010
R23, 35	330-2047
R39-44, 50, 51	331-0010
R45	331-3018
R46	330-3056
R47, 55, 63	336-1001
R48, ,52, 53, 60	330-3047
R54	330-2056
R56	330-3015
R58	330-3027
R61	330-2027
R62, 69	330-3018
R68	330-2018
R70, 71	330-2022
R74, 76, 95-97	330-4047
R78, 79	330-2068
R98-113	330-3068
R116	330-2033
R117-119	330-3082
C1, 2, 48, 49, 50	300-4022
C3, 19	300-2010
C4, 7	300-1907
C5, 11	300-1903
C6	300-2068
C8	300-3055
C20-22	300-4034
C10	300-1900
C13, 16, C23-47	300-1904
C14	300-3054
C15	300-1100
C17	300-1010
C18	300-1390
C9	300-4021
XTAL	321-0008
D1-31, 42-44, 46, 47	380-1001
D32	380-2100
D33, 34	380-3004
D35, 36, 39, 40	380-4000
D37	380-2051
D41	380-2062
D45	380-2033
Q1	375-1024
Q2	375-1027
Q3	375-1031
TRANSIPAD (LG)	375-9001
HEATSINK (BIRTCHTER)	375-9010
D48	380-2120
D49, 50	380-0000
R121	330-3033
Q4	375-1006

COMPONENT	W.L. NO.
J1, 4-6	3[illegible]0-0011
J2	654-1188
J3	654-1172
T.P. SKT. LOW PROFILE	654-1157
16 PIN I.C. SOCKET	376-9002
24 PIN I.C. SOCKET	376-9003
I.C. PAD 16 PIN	376-9008
22 PIN I.C. SOCKET	376-9010
14 PIN I.C. SOCKET	376-9012

SHEET 3 OF 3

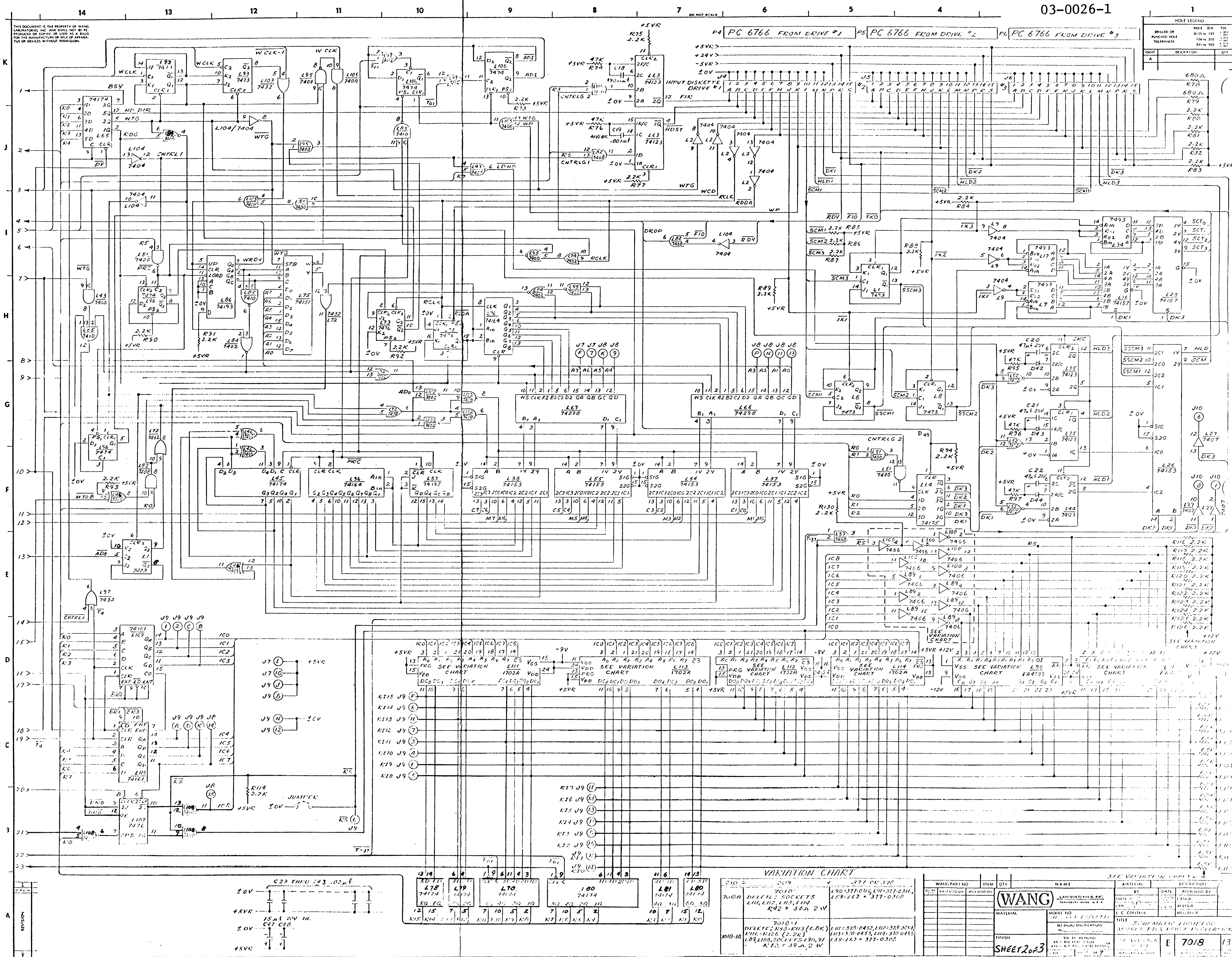
6718 9

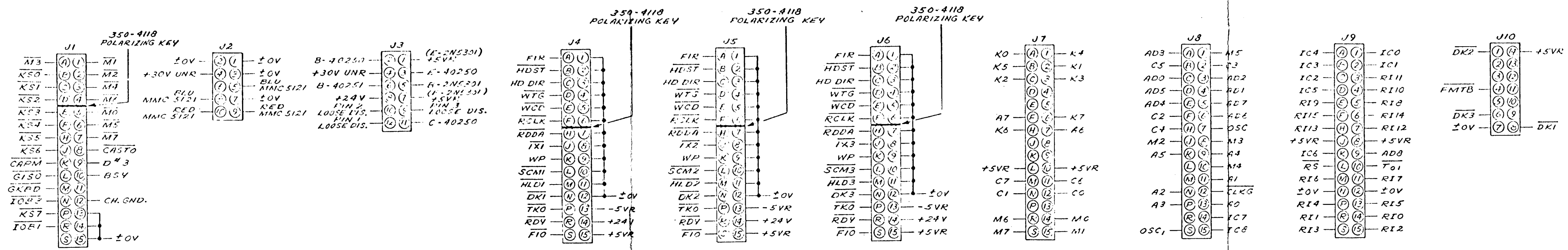
03-0026-1

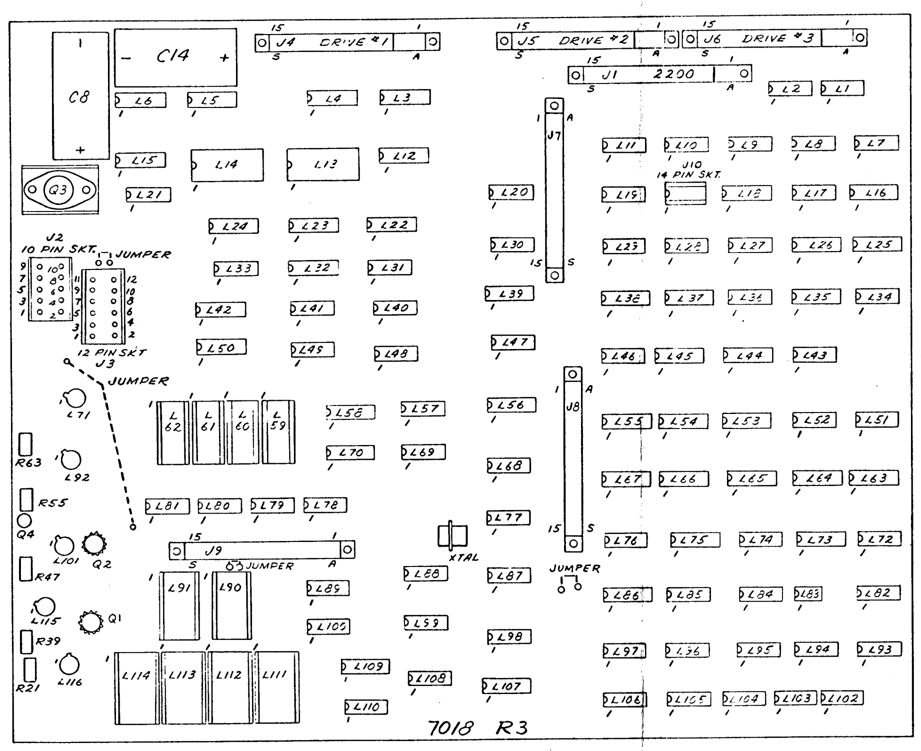


MOUNTED EXTERNALLY
8 LUG JONES STRIP
115 VAC DISK #2
115 VAC DISK #3
115 VAC DISK #1
115/220 VAC
SWITCH 115/220
MMC 5121
LOOSE DISCONNECT
MOUNTED ON HEAT SINK
12 PIN CONN.
J2 10 PIN CONN.
2200 CONN.
SEE VARIATION CHART SH 5 OF 7
10 MHZ XTAL
JUMPER
CH. GND.
E-REV 7018
E-REV 7018-1
WANG
SCHEMATIC LOGIC MOTHER BD. & POWER REGULATION
SHEET 1 of 3
E 7018

03-0026-1


THIS DOCUMENT IS THE PROPERTY OF WANG LABORATORIES, INC. AND SHALL NOT BE REPRODUCED OR COPIED, OR USED AS A BASIS FOR THE MANUFACTURE OR SALE OF APPARATUS OR DEVICES WITHOUT PERMISSION.
DO NOT SCALE
HOLE LEGEND
P4 PC 6766 FROM DRIVE #1
P5 PC 6766 FROM DRIVE #2
P6 PC 6766 FROM DRIVE #3
INPUT DISKETTE DRIVE #1
VARIATION CHART
SEE VARIATION CHART
JUMPER
C23 THRU C43 .02µf
WANG
SCHEMATIC LOGIC DIAGRAM
SHEET 2 OF 3
E 7018 13





I.C. LOCATION	W.L. NO.	TERM ±OV	TERM +5VR
L1, 8, 93	376-0005	11	4
L2, 9, 10, 11, 20, 31, 87, 104	376-0010	7	14
L3, 6, 66, 67	376-0138	8	16
L4, 5, 12, 15, 26, 37, 38, 54, 55	376-0048	8	16
L7, 17, 34	376-0011	10	5
L13, 14	376-0099	12	24
L16, 22, 23, 24, 25	376-0082	8	16
L18, 45, 65, 78, 79, 80, 81	376-0098	8	16
L19, 27	376-0056	7	14
L21	376-0025	7	14
L28, 29	376-0028	7	14
L30, 43, 49, 51, 68, 95, 102, 108	376-0002	7	14
L32, 39	376-0096	8	16
L33	376-0012	7	14
L35, 44, 63	376-0080	8	16
L36, 76, 88	376-0102	7	14
L40, 57, 82, 98, 105	376-0081	7	14
L41, 69, 72, 74, 97, 99, 103	376-0093	7	14
L42, 50	376-0049	8	16
L46	376-0036	7	14
L47, 52, 84	376-0016	7	14
L48, 85	376-0003	7	14
L53	376-0097	8	16
L56, 73, 107	376-0007	13	5
L58, 70, 86	376-0053	8	16
L59, 60, 61, 62	377-0308	8	22
L64	376-C119	8	16
L71, 92, 101, 115	376-0066		
L75	376-0047	8	16
L77	376-0073	10	5
L83	376-0126	1	8
L89, 100	376-0055	7	14
L90, 91			24
L96, 106	376-0006	7	14
L109, 110	376-0094	8	16
L111	376-0452R1		12
L112	376-0454R1		12
L113	378-0453R1		12
L114	378-0455R1		12
L94	376-0180	7	14
L116	376-0134	9	

COMPONENT	W.L. NO.
R40, 41, 128, 130, 116-126 R1, 5-19, 22, 24-34, 36, 57, 59 64-67, 72, 73, 75, 77, 80-94, 114,	330-3022
R2, 37, 38, 129	330-4027
R3, 115	330-3033
R4	330-6016
R20	330-5010
R21	336-1015
R23, 35	330-2047
R42	337-1039
R45, 127	330-3082
R50, 51	331-0010
R39, 47, 55, 63	336-1014
R52, 53, 60	330-3047
R54	330-2056
R56	330-3015
R46, 48, 58	330-3027
R61	330-2027
R62, 69	330-3018
R68	330-2018
R70, 71	330-2022
R74, 76, 95-97	330-4047
R78, 79	330-2068
R98-113	330-3068
R44	330-2033
C1, 47, 48, 49, 50	300-4022
C3, 19	300-2010
C4, 7	300-1907
C5, 11	300-1903
C6	300-2068
C8, 46	300-3055
C2	300-1906
C10	300-1900
C13, 16, C23-43	300-1904
C14	300-3054
C15	300-1100
C17	300-1010
C18	300-1390
C9	300-3011
C45	300-1220
XTAL	321-0006
D1-31, 42-44, 48	380-1001
D32	380-2091
D33, 34	380-3004
D35, 36, 39, 40, 45, 46	380-4000
D37	380-2051
D41	380-2062
D47, 49	380-0000
C20-22	300-4034
Q1	375-0018
Q2	375-1027
Q3	375-1031
Q4	375-1006
TRANSIPAD (LG)	375-9001
HEATSINK (BIRTCHER)	375-9010
R42 SEE VARIATION CHART SH. 5 OF 7	331-1056 (7018) 337-1039 (7018-1)

COMPONENT	W.L. NO.
J1, 4-9	350-0011
J2	654-1188
J3	654-1172
T.P. SKT. LOW PROFILE	654-1157
16 PIN I.C. SOCKET	376-9002
24 PIN I.C. SOCKET	376-9003
I.C. PAD 16 PIN	376-9008
22 PIN I.C. SOCKET	376-[illegible]
14 PIN I.C. SOCKET	376-9012
POLARIZING KEY	350-4118

I.C. TYPE	LOCATION	SPARES
7400	L30	1
7400	L49	1
7400	L68	1
7404	L2	1
7404	L11	1
7407	L19	4
7407	L27	3
7408	L57	2
7432	L69	1
7432	L72	1
7432	L74	2
7432	L97	1
7432	L99	1
7432	L103	2
74LS04	L94	1

WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.

WANG PART NO	ITEM	QTY	NAME	MATERIAL	DESCRIPTION

BY	DATE	APPROVED BY	DATE
DWN F.S.S.		E ENGR	
CHK	11/9/75	M ENGR	
E C CONTROL		MFG ENGR	

MATERIAL

MODEL NO. SHUGART FLOPPY

SEE ENGRG SPECIFICATIONS No

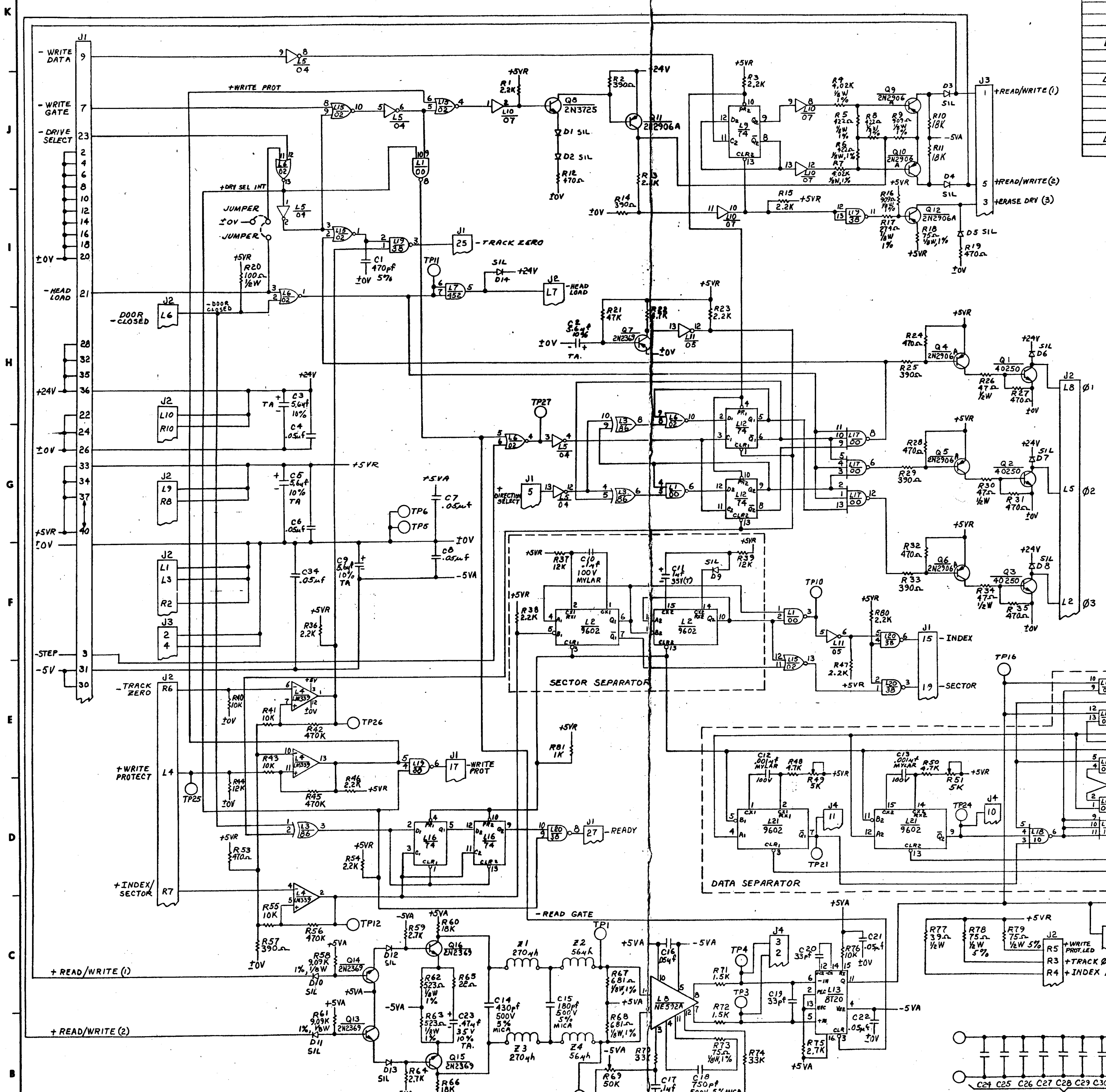
FINISH SHEET 3 OF 3

TOL EX AS NOTED XX ± .010 FRAC ± 1/64 XXX ± .005 ANG ± 1°30' FINISH

SCALE SHT 6 OF 7

TITLE MOTHER BOARD & PARTS LIST

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV
210-7018	E	7018	13



LOCATION	W.L. PART NO.	TERM. NO. ±0V	TERM. NO. Vcc+5VR
L1,14	376-0002	7	14
L2,21	376-0104	8	16
L3	376-0036	7	14
L4	376-0240	12	3
L6,15,	376-0016	7	14
L7	376-0145	4	8
L8	376-0239		
L9,12,16	376-0006	7	14
L10	376-0056	7	14
L11	376-0029	7	14
L13	376-0241	8	
L17,18	376-0003	7	14
L19,20	376-0128	7	14
L5	376-0010	7	14

COMPONENT	W.L. PART NO.
C1	300-1471
C2,3,5,9	300-4017
C4,6-8,16, 21,22,24-34	300-1900
C10	300-2210
C11	300-4000
C12,13	300-2010
C14	300-5015
C15	300-5001
C18	300-5014
C19,20	300-1033
C23	300-2247
D1-14	380-1001
Q1,2,3	375-1022
Q4,5,6,9,10,11,12	375-1016
Q7,13,14,15,16	375-1025
Q8	375-1027
J4	376-9001
J1	350-0402B
C17	300-1918
Z1.3	300-0004
Z2,4	300-0002

COMPONENT	W.L. PART NO.
R1,3,15,23,36,38, 46,47,54,13,80	330-3022
R2,14,25,29,33,57	330-2039
R4,7	333-0060
R5,6,8	333-0056
R9,16	333-0059
R10,11,60,66	330-4018
R12,19,24,27,28, 31,32,35,53	330-2047
R17.	333-0055
R78,79	331-1076
R20	331-2010
R21	330-4047
R22,48,50	330-3047
R26,30,34	331-1047
R37,39,44	330-4012
R40,41,43,55,76	330-4010
R42,45,56	330-5047
R49,51	336-1020
R52,81	330-3010
R58,61	333-0061
R59,64,75	330-3027
R62,63	333-0057
R65	330-1022
R67,68	333-0058
R69	336-0017
R70,74	330-4033
R71,72	330-3015
R18,73	333-0054
R77	331-1039

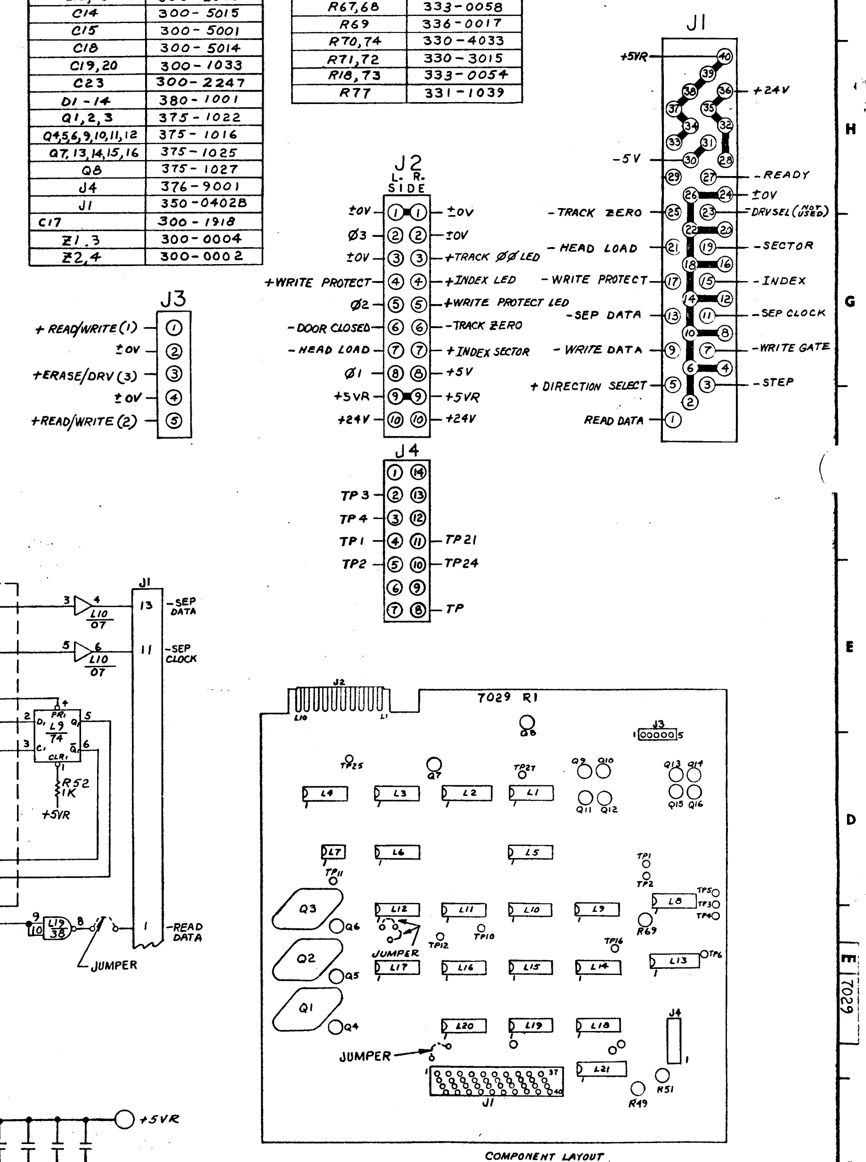
HOLE LEGEND

DRILLED OR PUNCHED HOLE TOLERANCES:	HOLE DIA.	TOL.
	.0135 to .125	+.003 −.001
	.126 to .250	+.004 −.001
	.251 to .500	+.005 −.001

IDENT.	DESCRIPTION	QTY.
A		

SPARES

I.C. CHIPS	LOCATION	NO. OF SPARES
7400	L1	1
7486	L3	1
7404	L5	1
75452	L7	1
7405	L11	4
7410	L18	1
7432	L20	1



1. ALL I.C. CHIPS ARE 7400 SERIES UNLESS OTHERWISE SPECIFIED.

NOTES

E-REV 0

WANG PART NO.	ITEM	QTY.	NAME	MATERIAL	DESCRIPTION
WANG LABORATORIES, INC. TEWKSBURY, MASS. U.S.A.					

	BY	DATE	APPROVED BY
DWN	GK	1-14-76	E ENGR
CHK			M ENGR
E. C. CONTROL			MFG ENGR

TITLE SCHEMATIC LOGIBLOC SHUGART ELECTRONICS

TOL. EX. AS NOTED XX ± .010 FRAC ± 1/64 .XXX ± .005 ANG. ± 1°30' FINISH

SCALE — SHT 4 OF 5

WANG PART NUMBER	SIZE	DRAWING NUMBER	REV.
210-7029	E	7029	1