WANG LABORATORIES, INC.
ONE INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851, TEL. (617) 459-5000, TWX 710 343-6769, TELEX 94-7421

DATA SHEET

MODEL 2250 or OPTION 67 8-BIT-PARALLEL I/O INTERFACE CONTROLLER

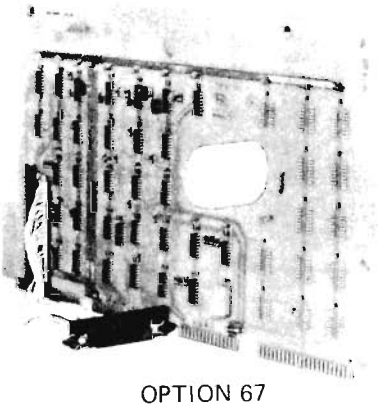
For an on-line instrumentation application where data transfer is to be serial-by-character and parallel-by-bit, the 8-bit-parallel I/O Interface Controller facilitates direct connection of a non-Wang device to a Wang System 2200 central processor (except the 2200VS). The non-Wang device may be one of the following types: (1) input only, (2) output only, or (3) input and output.

Although Wang systems use an 8-bit character set with 7-bit ASCII codes and the high-order bit set to zero, individual characters in any single or packed 8-bit codes (e.g., EIA, two 4-bit BCD digits, etc.) can be transmitted between a non-Wang device and a Wang central processor via the 8-Bit-Parallel I/O Interface Controller. Furthermore, discrete binary information in an 8-bit format can be transmitted via the controller.

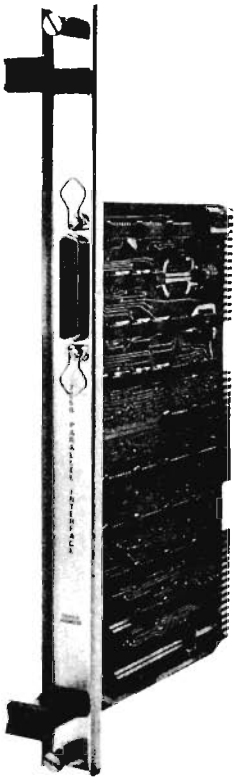
The interface controller implements the sequential transfer of information one-byte-at-a-time under program control from a user-written BASIC language application program operating in the central processor. If the interfaced device has characteristics suited to the *built-in* signal sequences of an input operation such as INPUT, KEYIN, or DATALOAD BT, or an output operation such as PRINT, PRINTUSING, HEXPRINT, or DATASAVE BT, any of these BASIC statements may be included in an application program. However, the $GIO statement is recommended for control of most non-Wang devices. By a technique similar to machine language programming, a $GIO statement can be *custom-tailored* using a sequence of microcommand codes to specify a desired signal sequence for special input or output operations suited to the interfaced device.

Data transfer rates depend upon the particular BASIC language statement being executed and the central processor model. Rates up to 10,000 characters per second are possible with a 2200T central processor, or up to 80,000 characters per second with a 2000VP.

The 8-Bit-Parallel I/O Interface Controller is available in two physically different but functionally equivalent versions, called the Model 2250 and Option 67. If a Wang system is equipped with a *separately housed* central processor, such as a 2200T or 2200VP, the Model 2250 controller is the proper choice. If a Wang system is equipped with a *console-housed* central processor (i.e., the keyboard, CRT display screen, and central processor are combined in one unit), the Option 67 controller is the proper choice.



OPTION 67



MODEL 2250

DATA SHEET

I/O CONNECTOR PIN ASSIGNMENTS

PIN NO.	SIGNAL MNEMONIC	I/O*	REMARKS
			8-Bit-Parallel, Buffered Input Data from External Device
1	$\overline{IB5_I}$	I	10 High-order
2	$\overline{IB6_I}$	I	20 hex-digit
3	$\overline{IB7_I}$	I	40 8-4-2-1
4	$\overline{IB8_I}$	I	80 bit positions. One byte
5	$\overline{IB1_I}$	I	1 Low-order
6	$\overline{IB2_I}$	I	2 hex-digit
7	$\overline{IB3_I}$	I	4 8-4-2-1
8	$\overline{IB4_I}$	I	8 bit positions.
9	$\overline{IBS_I}$	I	Input Strobe from External Device
10	$\overline{PRMS_O}$	O	Prime Output Strobe
11	$\overline{ENDI}$	I	End-of-Input Control Level, Buffered
12	$\overline{COB1_O}$	O	1 4-Bit Buffered
13	$\overline{COB2_O}$	O	2 Control Information
14	$\overline{COB4_O}$	O	4 Output by $\overline{CBS_O}$
15	$\overline{COB8_O}$	O	8
16	$\overline{CBS_O}$	O	Control Output Strobe
17	$\overline{IRB}$	O	Input-Buffer Empty/Full Level
18	$\overline{ACK}$	I	External Device Acknowledge Strobe
19	$\overline{RBI}$	I	External Device Ready/Busy Level
			8-Bit-Parallel, Buffered Output Data from System 2200/2250
20	$\overline{OB1_O}$	O	1 Low-order
21	$\overline{OB2_O}$	O	2 hex-digit
22	$\overline{OB3_O}$	O	4 8-4-2-1
23	$\overline{OB4_O}$	O	8 bit positions. One byte
24	$\overline{OB5_O}$	O	10 High-order
25	$\overline{OB6_O}$	O	20 hex-digit
26	$\overline{OB7_O}$	O	40 8-4-2-1
27	$\overline{OB8_O}$	O	80 bit positions.
28	$\overline{DORB}$	O	Data-Output-Buffer Ready/Busy Level
28, 30			Spare
31	$\overline{OBS_O}$	O	Data Output Strobe
32	$\overline{CPB_O}$	O	CPU/2250 Ready/Busy Level
33, 34, 35			±o v common
36			Chassis Ground

*As seen by the CPU/controller.

SPECIFICATIONS

Signal Levels

Input/Output circuitry is TTL/DTL compatible.

Voltage levels:

Logic "0" (False) is between +2.4 and 3.6 volts.

Logic "1" (True) is between 0 and +0.4 volts.

Strobes

Input strobe pulse width is 5 to 20 microseconds.

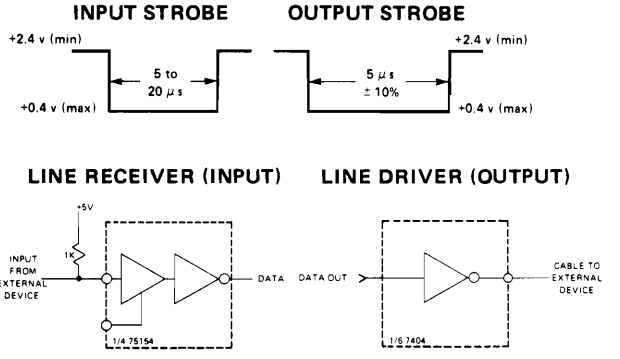
Output strobe pulse width is 5 microseconds ±10%.

Power Requirements

Supplied by the central processor.

Standard Warranty Applies.

I/O SIGNAL LEVELS AND TYPICAL CIRCUITS



Note:

1. The system is adequate for short lines up to 100 feet in length, where environmental noise is not severe.
2. For minimum transmission error, Wang Laboratories recommends that the input/output circuitry of interfaced devices include the same (or equivalent) line driver/receiver circuits.

ORDERING SPECIFICATIONS

An input/output interface controller providing direct transfer of 8-bit-parallel data between a non-Wang digital device and a Wang central processor, using TTL/DTL compatible logic. The controller must be available in a version suitable for installation in the central processor which is to be used for an on-line application.

Wang Laboratories reserves the right to change specifications without prior notice.

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