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DATA SHEET

The Model 9027 Scanning Input Interface Controller (BCD* 1-to-10-Digit-Parallel) is an input-only interface directly compatible with many digital instruments for on-line applications using a Wang 2200 WS, PCS, or PCS-II Series configuration.

The interface controller board fits inside the housing of the Central Processing Unit (CPU). A 50-pin female Amphenol connector is mounted to the rear of the WS, PCS or PCS-II chassis and serves as an input plug. A matching 50-pin male Amphenol connector is supplied with the Model 9027 for witing to a cable from a digital device.

The logic levels used for Data and Control Signals are defined by a $GIO statement prior to operation of the Model 9027. Once set, the logic levels remain defined until reset by another $GIO sequence or until power is turned OFF.

INPUT DATA SIGNALS

The Model 9027 interface can accept, in parallel, a readout consisting of a one-bit algebraic sign (plus or minus) and up to ten decimal digits (0 through 9) in BCD 8-4-2-1 notation, i.e. four bits per decimal digit. Alternately, the interface can accept up to forty data bits and one sign bit in parallel. Numeric readouts can be fixed or floating point formats.

The "number of digits" must be set by a $GIO statement to indicate the exact number of BCD digits (or the number of 4-bit groups of discrete binary data) to be processed per readout. Any value from one through ten BCD digits per readout is valid. The sign-bit for each readout is processed automatically. The number-of-digits selectivity feature offers two advantages for applications involving readouts consisting of fewer than 10 BCD digits. Less time is required to transfer each readout to the CPU, and less memory is required when storing multireadouts in alphanumeric arrays.

Input circuits for the Model 9027 interface are TTL/DTL** comible. Acceptable voltage levels for low-level signals from an interfaced device are 0 to +0.4 volts DC; acceptable levels for high-level signals are +2.5 to 5.0 volts DC. Since designers do not use standard conventions when letting low and high voltage levels represent two-state conditions such as logic "0" and "1" or "on" and "off", six logic-level-selection parameters, set by a $GIO statement assure compatibility with a wide range of digital instruments. For example, if the DATA parameter is set high, low level signals represent logic "0" and high level signals represent logic "1" on the forty input data circuits; on the other hand, if the DATA parameter is set low, the logic level definition is reversed (i.e. low = "1" and high = "0"). Similarly, the SIGN parameter independently determines the logic level definition for the one-bit sign input circuit.

*BCD = binary coded decimals.

**TTL = transistor-transistor-logic; DTL = diode-transistor-logic

MODEL 9027 SCANNING INPUT INTERFACE CONTROLLER

INPUT CONTROL SIGNALS

The IS (Input Strobe), EXEC (Execute), TRANS (Transfer-in-progress), and EOT (End of Transfer) parameters independently determine the logic level definitions for the four control signal circuits on the Model 9027 interface. Three of the four control circuits provide outgoing signals which can be utilized or ignored by a particular interfaced device, as required.

The outgoing Execute signal is set when the interface is ready to receive an input strobe (or level transition) from the interfaced device. Then a two microsecond minimum-pulse-width Input Strobe (or level transition) must be received from the interfaced device to initiate data transfer to the CPU. (If a device cannot provide input strobes or does not have settling requirements, the Execute circuit can be tied to the Input Strobe circuit when the Model 9027 connector is wired to a device.) The Execute signal level is reset five microseconds after the leading edge of an input strobe is received. Upon request, a Wang Service Representative can modify the Execute circuit if an application requires the Execute signal to be an extended duration signal not reset until data transfer is completed. Such a modification is useful for an instrument which requires a single signal level to initiate a settling condition and also to indicate a data holding condition.

The outgoing Transfer-in-progress signal level is set after an input strobe is received and is reset when data transfer is complete. The data output from a device should remain stable (unchanged) for the duration of a Transfer-in-progress signal, if utilized. The End of Transfer output strobe is provided for instruments requiring a strobe to initiate a readout change or a settling condition. A Prime output strobe is generated when the RESET button on a Wang keyboard is depressed to interrupt processing and return system control to the operator; generally, the signal is utilized by a device as a reset/initialization signal.

SCANNING INPUT MODE

The scanning mode capability is useful when instruments or devices with relatively slow settling times (sampling rates in excess of 50 milliseconds) are interfaced to a Wang system with a Model 9027 interface controller. Two BASIC language statements can be used to initiate a scanning mode of operation, the KEYIN statement and the $IF ON statement.

Upon execution, a KEYIN or a $IF ON statement sets the Execute signal and then tests the input Ready/not-ready condition of the interface. If a not-ready condition is sensed, the interface is disabled, and program execution continues with subsequent statements. Meanwhile, the Execute signal remains set, and the interface can receive one input strobe while other CPU processing is in progress. Whenever a ready condition is sensed during later execution of either statement, program execution branches to a specified line number, where an INPUT statement can be used to received the data.

SPECIFICATIONS

Power Requirements

Supplied by the CPU

Connector

A 50-pin female Amphenol connector is mounted on the unit.

A 50-pin male Amphenol connector, to be wired to the cable from a device, is supplied with the unit.

Operating Environment

50° F to 90° F (10° C to 32° C)

20% to 80% relative humidity

Programmable Parameters

Six logic-level-program selectable parameters reverse signal level definitions, as required, for the following signals: (1) the input strobe, (2) the sign bit, (3) all BCD or discrete input data, (4) the execute signal, (5) the transfer-in-progress signal and (6) the end-of-transfer output strobe.

A number-of-digits program selectable parameter defines the exact number of BCD digits (or 4-bit groups of discrete data) to be processed per readout.

Program Reversible Logic Levels

High-level signals: +2.5 to 5 vdc.

Low-level signals: 0 to +0.4 vdc.

If a parameter is set ON, high = "1" and low = "0"; if a parameter is OFF, high = "0" and low = "1"

Typical Impedance

Input: 4K ohms

Output: 1K ohms

Control Signals

1) Execute Signal –

An output level from the Model 9027 indicating the interface is ready to receive a readout.

SPECIFICATIONS (CONT.)

2) Input Strobe –
   A two microsecond minimum-pulse-width strobe or level transition from an interfaced device to indicate a readout is available.
3) Transfer-in-progress Signal –
   An output level indicating a readout is being transferred to the CPU.
4) End of Transfer Strobe –
   A five microsecond output strobe indicating transfer of the current readout is completed.
5) Prime Strobe –
   A five microsecond ouptut strobe generated when the RESET button on a Wang keyboard is depressed to interrupt an operation and return system control to the operator.

Number Code

BCD (8-4-2-1) Code

Number Size

1-to-10 BCD digits and a sign bit (or up to 41 discrete bits for non-numeric applications). The number of BCD digits to be processed is program selectable.

Transfer Format

Parallel

Transfer Rate

Up to 100 readings per second using INPUT or MAT INPUT statements.

Up to 800 readings per second using DATALOAD BT statements.

Up to 1000 readings per second using $GIO statements.

Model 9027 Connector Pin Assignments*

Pin Number	Function	8-4-2-1 Position	Pin Number	Function	8-4-2-1 Position
01	D_0 (most	1	37	D_7 (eighth	1
02	significant	2	38	significant	2
03	digit)	4	39	digit)	4
04		8	40		8
19	D_1 (second	1	41	D_8 (ninth	1
20	significant	2	42	significant	2
21	digit)	4	43	digit)	4
22		8	44		8
05	D_2 (third	1	45	D_9 (tenth	1
06	significant	2	46	significant	2
07	digit)	4	47	digit)	4
08		8	48		8
23	D_3 (fourth	1	17	Sign bit	
24	significant	2			
25	digit)	4	18	Input strobe	
26		8	31	Execuit signal	
09	D_4 (fifth	1	49	Transfer-in-progress	
10	significant	2			
11	digit)	4	50	EOT output strobe	
12		8			
27	D_5 (sixth	1	32	Prime strobe	
28	significant	2			
29	digit)	4	33	±0 volts	
30		8	34		
13	D_6 (seventh	1	35	+5 volts	
14	significant	2			
15	digit)	4	36	Chassis ground	
16		8			

*All logic is BCD 8-4-2-1 TTL compatible, positive true. Open input circuit pins are at high level. Pins 01 through 16, Pin 17, Pins 19 through 30, and Pins 37 through 48 can be used for input of up to 41 bits of discrete binary data rather than BCD data.

ORDERING SPECIFICATIONS

An interface directly compatible with many digital instruments for on-line data input to a Wang 2200 WS, PCS and PCS-II. The interface must accept, in parallel, a readout consisting of a sign-bit and up to ten BCD digits in 8-4-2-1 notation, or up to 41 bits of discrete binary data. The exact number of BCD digits to be processed per readout must be program-selectable. Four control signal circuits must be provided. Logic-level-definitions must be program-selectable for all input data circuits and all control signal circuits.

Standard Warranty Applies

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700-4288
8-77-5M