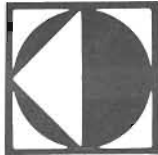


PRELIMINARY



Diablo Systems Incorporated

**Model 44B Disk Drive
Maintenance Manual**

WARRANTY

The Diablo Model 44B Disk Drive is warranted against defects in materials and workmanship for 1 year from the date of shipment. Any questions with respect to the warranty should be taken up with your Diablo Sales Representative.

All requests for repairs should be directed to the Diablo Repair Depot in your area. This will assure you the fastest possible service.

PREFACE

This preliminary maintenance manual for the Model 44B Disk Drive contains the latest information available at the time of writing. Subsequent engineering design changes will be accounted for in later editions of the manual.

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SECTION 1

GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 OPERATIONAL CHARACTERISTICS

The Diablo Model 44B Disk Drive, shown in Figure 1-1, provides up to 100 megabits of on-line random access storage, and unlimited off-line storage for small, general purpose digital computers. Its design incorporates features which ensure a high degree of flexibility, reliability, speed of access, and data integrity. It uses both a fixed disk and a removable Type 5440 top loading disk cartridge. A capacity of up to 100 megabits is provided at a data transfer rate of 2.5 Mbits/second, a recording density of 2200 bits-per-inch (bpi), and a lateral track density of 200 tracks-per-inch (tpi).

Options and accessories which are available for the Model 44B are described in Section 6.

The Model 44B consists of six functional groups:

- The Spindle Assembly rotates the recording disks, and provides ventilation for the drive.
- Four Read/Write Head Assemblies "write" data onto, or "read" data from, the two disks.
- The Head Positioner Assembly moves the read/write heads to the disk track locations commanded by the using system.
- Controls, Indicators, and Interlocks provide the means for front panel operation of the drive, and prevent improper operating sequences.
- The Electronics group accepts, processes, generates, and/or supplies the electrical signals necessary for the disk drive to perform its intended function.
- An Internal Power Supply converts AC line power to the several DC operating voltages required by the drive.

The spindle drive motor is mounted directly on the spindle shaft. Spindle speed is controlled electronically, and is independent of normal fluctuations in line voltage or frequency. An air blower for the ventilation system is also mounted on the spindle shaft. Disk contamination from outside sources is virtually eliminated by passing all air drawn into the unit through an absolute no-bypass air filter. This filter retains 99.97% of all particles 0.3 microns or larger. Filtered air is then directed into both disk areas and through them to cool the electronics areas before exhausting at the rear of the machine. In addition, each disk surface is swept with a cleaning brush each time the drive is switched from the Load mode to the Run mode.

The head positioning system's case is designed to contain the strong magnetic field of its ceramic magnets and drive coil. This reduces stray magnetic flux at the read/write heads to a negligible level, eliminating a common cause of disk

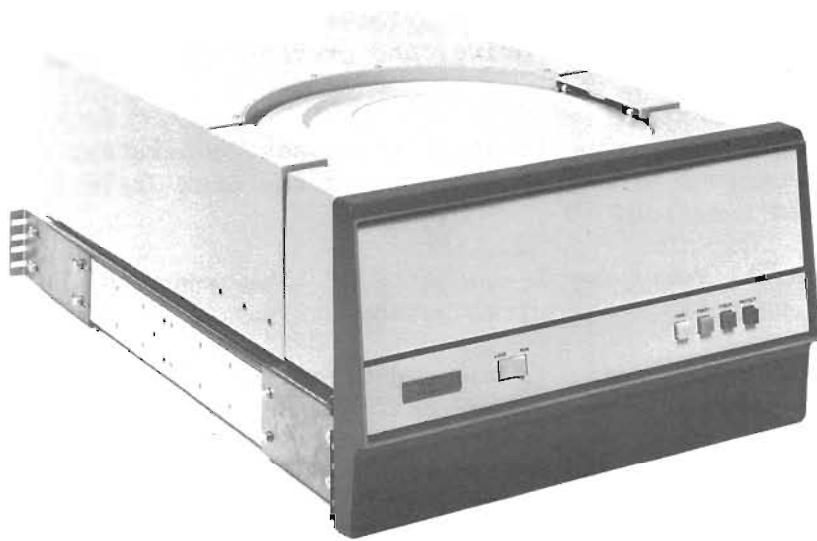


Figure 1-1. DIABLO SYSTEMS, INC.
MODEL 44B DISK DRIVE

system data error. The thermal characteristics of the drive are designed to minimize head-to-track error due to ambient temperature, rate of change of ambient temperature, start-up transients, cold packs placed on warm drives, etc. By minimizing head-to-track alignment error, highly reliable data transfer is achieved.

Head loading is accomplished gently, with no head-to-disk contact, by a ramp load mechanism. The heads load automatically as they arrive over the disk from the retract position. In the event of power failure, the heads immediately retract and unload, providing protection for heads, disks, and data. A system of interlocks guards against operator error which could otherwise damage the heads and disk surfaces.

1.2 GENERAL SPECIFICATIONS

General specifications for the Model 44B Disk Drive are listed in Table 1-1.

1.3 RELATED DOCUMENTS

Several documents which pertain to maintenance of the Model 44B Disk Drive are listed below. Those marked with an asterisk (*) are not available at the time of this writing but will be released in the near future. In addition to these publications, Field Service Aid bulletins are published as necessary to inform the user of design changes, new service procedures, etc.

Model 44B Disk Drive Maintenance Manual
Publication No. 81903

* Model 44B Disk Drive Parts Catalog
Publication No. 81904

Model 44B Disk Drive Parts Price List
Publication No. CS503-08

Maintenance and Special Items Pricing
Publication No. CS500-04

Alignment Cartridges User's Manual
Publications No. 81619

TABLE 1-1
SPECIFICATIONS

Specifications for 100 TPI are the same as for 200 TPI except where noted.

PARAMETER	200 TPI	100 TPI (Optional)
Storage Medium:		
Type	Type 5440 cartridge and a fixed disk.	-----
Diameter	14 inches (35.56 cm)	-----
Lateral Track Density	200 tracks per inch (25.4 mm)	100 tracks per inch (25.4 mm)
Recording Technique Double frequency		
Tracks	1632 (400 plus 8 spares on each surface on each disk.)	816 (200 plus 4 spares on each surface on each disk.)
Cylinders	408 (4 tracks per cylinder, 2 per disk)	204 (4 tracks per cylinder, 2 per disk)
Capacity, Bits: *		
Per Drive	100,000,000	50,000,000
Per Disk	50,000,000	25,000,000
Per Inch (innermost track)	2200	-----
Per Cylinder	250,000	-----
Per Track	62,500	-----
Access Time:		
Track-to-Track	8 ms	10 ms
Average	38 ms	-----
Full Stroke	70 ms	-----
Disk Rotation:	2400 rpm $\pm 0.2\%$	**
Average Latency	12.5 ms	**
Bit Transfer Rate	2500 kHz	**
Power Requirement	100, 120, 220 or 240 VAC, 50 or 60 Hz	-----
Environment (operating):		
Temperature	50°F (10°C) to 104°F (40°C)	-----
Temp Change Rate	18°F (10°C) per hour	-----
Relative Humidity	20% to 80% (non-condensing)	-----
Maximum Altitude	10,000 ft (3048 m)	-----
Environment (shipping):		
Temperature	-40°F (C) to 140°F (60°C)	-----
Relative Humidity	5% to 90% (non-condensing)	-----
Physical:		
Width	17-1/4 inches (43.815 cm)	-----
Height	10-5/16 inches (26.19 cm)	-----
Depth	(See Figure 2-1)	-----
Weight:		
Disk Drive	113 lbs (51.36 kg)	-----
Rack Mounting Hardware	12 lbs (5.45 kg)	-----

* The capacity figures shown are nominal. Actual capacity will depend on formatting and data check methods used.

** See 1500 RPM option in Section 6 for variations.

SECTION 2

INSTALLATION AND OPERATION

2.1 INSTALLATION

2.1.1 Dimensions

Figure 2-1 shows the basic dimensions of the Model 44B Disk Drive, including its rack slides for mounting in a standard 19-inch (48.26 cm) rack. The standard Model 44B Disk Drive is furnished with rack slides and a cable carrier kit to properly position the I/O cable. Dimensions pertinent to rack mounting the drive are shown in Figure 2-4 and Figure 2-5.

A desk top version of the Model 44B is available also.

2.1.2 Unpacking/Packing

2.1.2.1 Unpacking Procedure

The unpacking procedure for the disk drive is readily apparent by referring to the shipping container assembly drawing shown in Figure 2-3. When unpacking the disk drive, the packing materials should be retained for possible later use. Before initial operation of the disk drive, the head positioner shipping clamp, shown in Figure 2-2, must be removed.

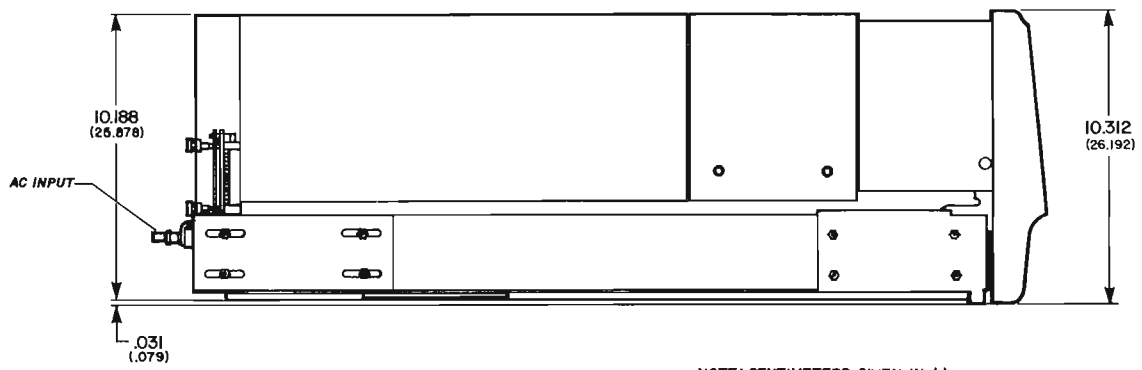
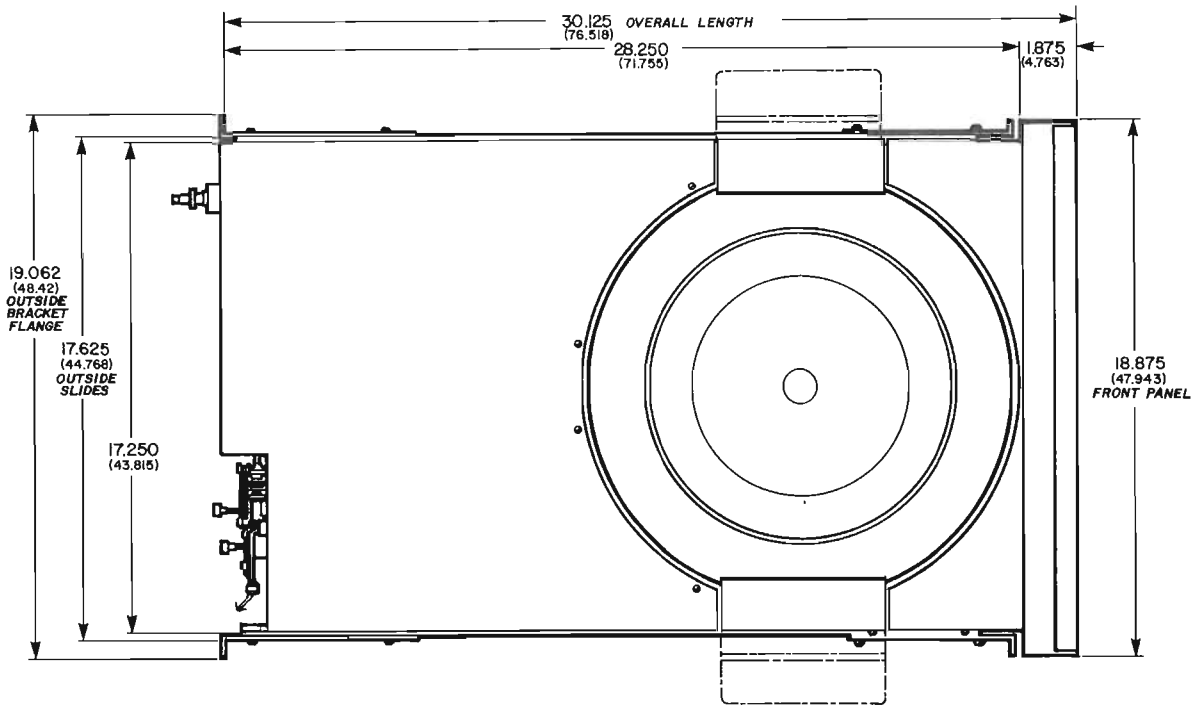
2.1.2.2 Packing Procedure

1. Install head positioner shipping clamp inside disk drive, as shown in Figure 2-2.

Refer to Figure 2-3, in the following sequence:

2. Cover disk drive with plastic bag (Item 1).
3. Set disk drive in opened inner container (Item 2).
4. Fold inner container around disk drive, place rack slides* (Item 3) on top of inner container, and secure with banding straps (Item 4).
5. Place end pads (Item 5) in outer container (Item 6) and fold top flaps outward.
6. Slide inner container with disk drive down into end caps..
7. Place cable carrier assembly* (Item 7) in open space between inner and outer containers.
8. Fold end cap flaps and outer container flaps inward, and seal outer container securely with tape.

* When disk drive is being shipped for repair, do not include rack slides or cable carrier.



NOTE: CENTIMETERS GIVEN IN ().

Figure 2-1. MODEL 44B BASIC DIMENSIONS

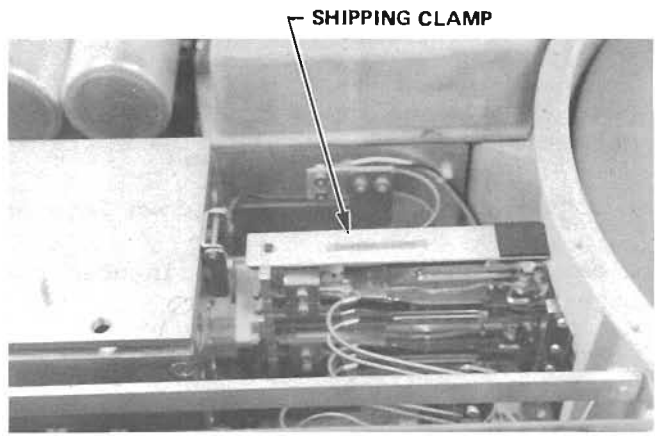


Figure 2-2. HEAD POSITIONER SHIPPING CLAMP

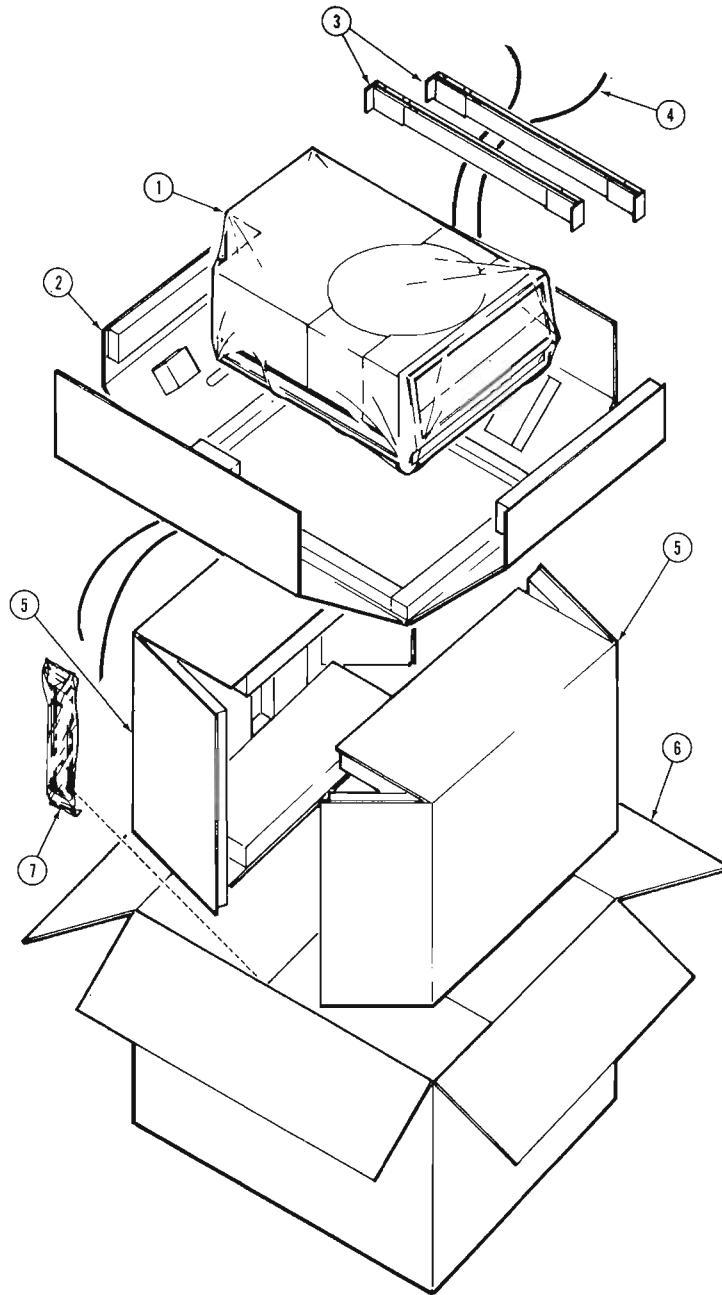


Figure 2-3. SHIPPING CONTAINER ASSEMBLY

2.1.3 Rack Mount Installation

The Model 44B may be installed in a standard 19-inch (48.26 cm) rack with 27-1/2 to 28-5/8 inch (69.85 to 72.71 cm) rail spacing as follows:

1. Install the two slides in the rack, with hole alignment as shown in Figure 2-4. Adjust the rear mounting bracket on each slide as necessary to fit the rack rails. Secure each mounting bracket to the rail with four(4) screws.
2. Install the I/O Cable Carrier Kit on the left rear rail as described in Section 2.1.4.
3. Extend each slide out until it stops. Locate the intermediate stop under the slide center, press it in and continue to extend the slide to its maximum extension.
4. Position the unit on the fully extended slides.

CAUTION

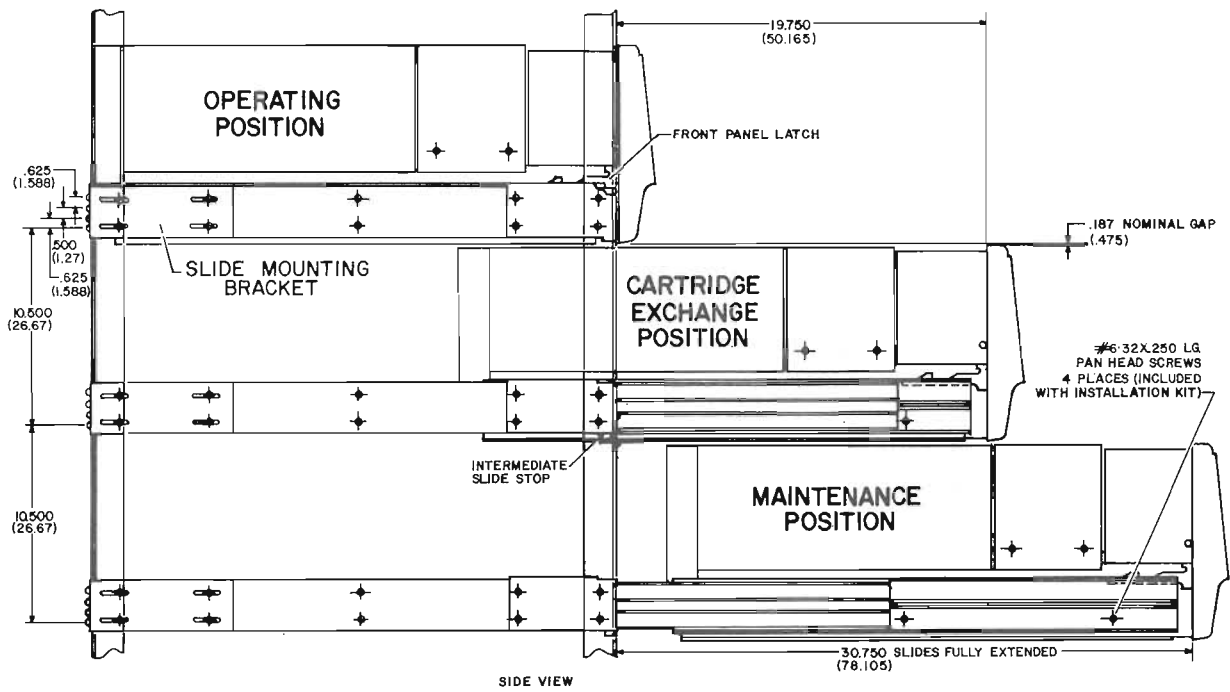
The Model 44B weighs approximately 113 pounds (51.36 kg). Make sure the rack, if free standing, has enough counterweight to prevent it from tipping forward when the unit is placed on the slides.

5. Secure the unit to the slides with two screws on each side, as shown on the bottom unit in Figure 2-4.
6. Adjust the I/O cable in the cable carrier to provide the necessary length of cable from the end of the carrier to the I/O connector on the drive. Connect the I/O cable to the drive.
7. Slide the unit fully into the rack, while checking for proper operation of the I/O cable carrier. Adjust the latch plate on each slide as necessary for proper operation of the drawer latches.

2.1.4 Cable Carrier Installation

Refer to Figure 2-5.

1. Beginning at the disk drive end of the I/O cable, fold the cable as shown in Figure 2-5(1), using one section of the cable carrier as a guide for the distance between folds. Mark a line on the cable at each fold, for later reference.
2. Install the Cable Carrier Mounting Bracket on the left rear rail of the rack, as shown in Figure 2-5(2).
3. Install section A of the cable carrier on the mounting bracket, as shown in Figure 2-5(3). Use two #10 flat washers and one #6-32 screw on each pivot stud, as shown.



NOTE: CENTIMETERS GIVEN IN ().

Figure 2-4. MODEL 44B RACK MOUNT POSITIONS

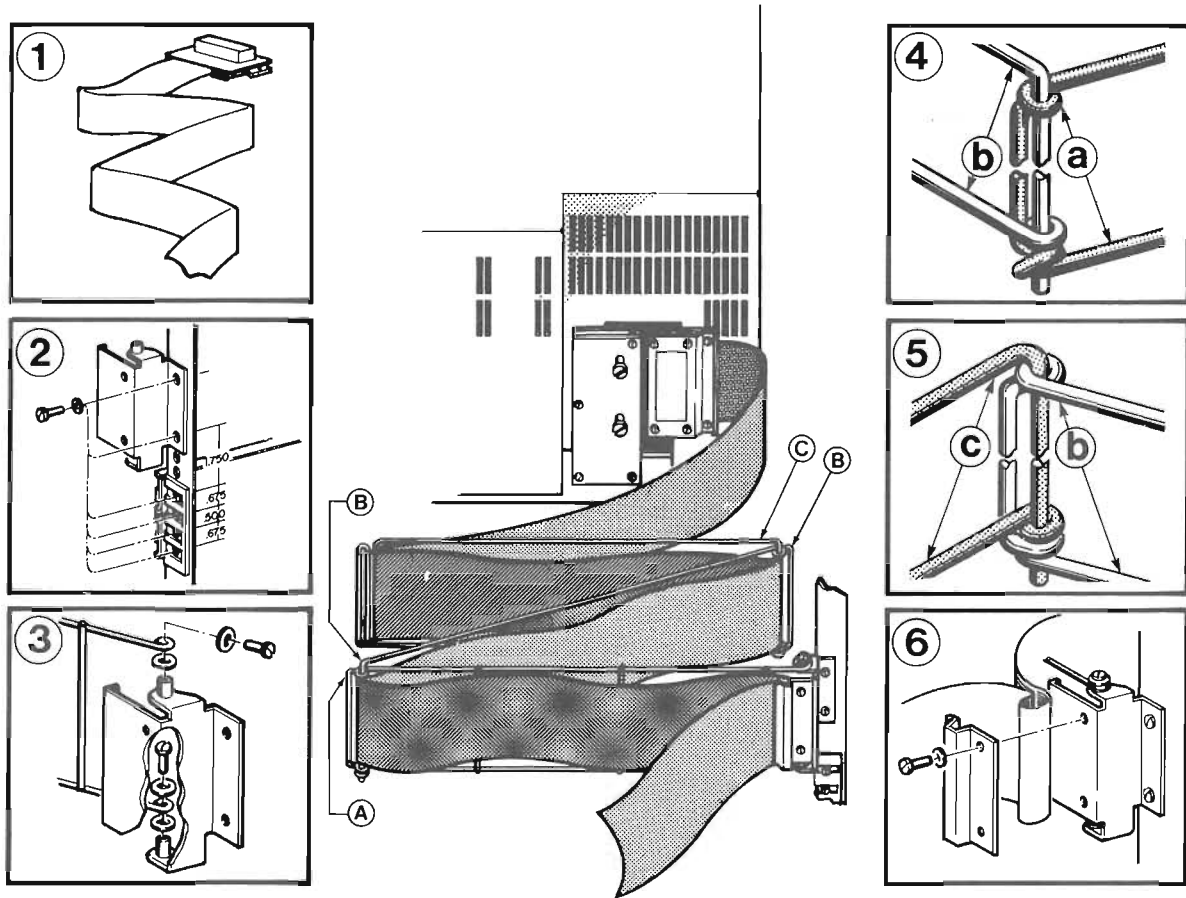


Figure 2-5. I/O CABLE CARRIER ASSEMBLY

4. Using the fold marks for reference, position the I/O cable on Section A of the carrier while installing Section B as shown in Figure 2-5(4).
5. Position the cable on section B and install Section C as shown in Figure 2-5(5).
6. Slide the cable down into the slot at the end of Section C as shown in the complete view of the carrier assembly.
7. Adjust the position of the cable in the carrier to ensure that an adequate length of cable will be available to reach from the end of Section C to the I/O connector on the drive.
8. Clamp the I/O cable to the carrier mounting bracket, using the metal cable clamp, as shown in Figure 2-5(6).
9. Fold and extend the cable carrier assembly several times to verify proper operation.

2.2 OPERATING INSTRUCTIONS

2.2.1 Operating Precautions

2.2.1.1 Disk Drive Operation

To obtain the best performance and reliability from the Model 44B, and to prevent equipment damage, the following precautions should be observed:

1. Do not connect or disconnect the I/O cables while power is turned on.
2. Keep the equipment drawer closed to prevent airborne contamination. Either a disk cartridge or the dust cover should be in place in the bowl at all times.
3. The drive should be left in the RUN mode whenever possible so that clean filtered air will be supplied to the interior of the machine.
4. A sustained audible tinging or scratching sound may be caused by head-to-disk contact. If it persists, discontinue machine operation and investigate the cause.
5. Do not force or attempt to override any interlock. Interlocks are safety devices, included to prevent injury, equipment damage, and loss of data.

2.2.1.2 Cartridge Handling and Storage

The following precautions should be observed when handling or storing disk cartridges:

1. Cartridges are magnetically recorded records. They MUST be kept away from strong magnetic fields, such as large rotating electrical machines, high-current bus bars or cables, welding equipment, etc.

2. The cartridge dust cover should be in good condition and kept on the cartridge while it is out of the disk drive. This ensures a positive dust seal and immobilizes the disk inside.
3. Cartridges may be stored on edge or flat. When stored flat, avoid stacking more than five(5) high. Cartridges should never be stored in direct sunlight, or in very dusty or dirty areas.
4. Any Disk Cartridge that has been dropped should be inspected by the disk cartridge manufacturer before attempting to use it.
5. Refer to cartridge manufacturer's instructions for maintenance and cleaning procedures.

2.2.1.3 Head Crash

Head Crash, in most cases, is easily preventable by observing the foregoing precautions. A head crash occurs when a R/W head contacts the disk. This is usually audible. The vast majority of head crashes are due to contamination caused by careless handling and careless operation of the disk drive and disk cartridges, and failure to change the air filter at the recommended intervals. If a head crash occurs, the crashed head and the disk must both be replaced, and the cause of the head crash must be eliminated.

2.2.2 Controls and Indicators

The Model 44B Disk Drive has two front panel controls and four front panel indicators. These are shown in Figure 2-6 and described in the paragraphs which follow. For service convenience, an AC Power ON-OFF switch is located at the rear of the disk drive.

2.2.2.1 LOAD/RUN Switch

The LOAD/RUN Switch is a two-position rocker switch that provides a means for starting and stopping the spindle. Cartridges may be removed and inserted when the switch is in the LOAD position and the LOAD light is on. With a cartridge inserted, and the cartridge clamps closed, switching to the RUN position starts the disk drive and brings the disk up to its normal operating speed in about 60 seconds. When the switch is moved to the LOAD position, the disk decelerates to a stop in about 15 seconds, after which the LOAD light turns on.

NOTE: This switch does not control power to the drive.

2.2.2.2 LOAD Indicator

The LOAD Indicator is a white indicator light which shows that cartridges can be loaded or unloaded. The light is on only when the LOAD/RUN switch is in the LOAD position, the disk is not rotating, the brushes are retracted, and power is on.

2.2.2.3 READY Indicator

The READY Indicator is a yellow indicator light which shows that the drive has completed its start-up sequence. The light comes on when the disk is rotating at its correct speed, heads are in position and no other conditions are present which would prevent a Seek, Read, or Write command from being executed.

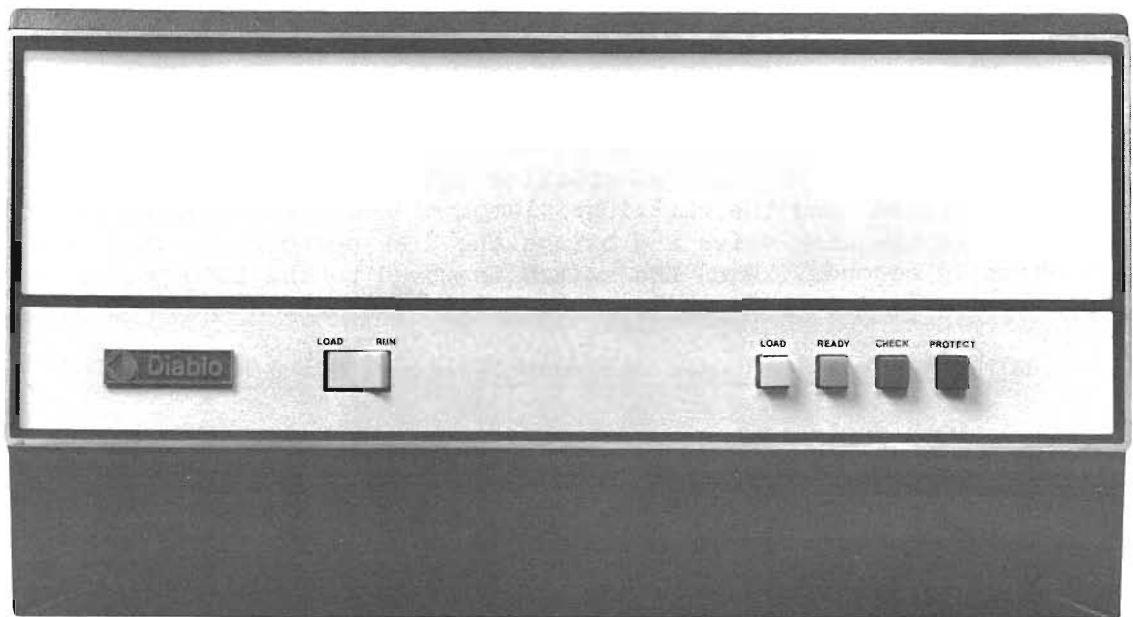


Figure 2-6. FRONT PANEL, MODEL 44B DISK DRIVE

The light remains on through a Seek, Read, or Write operation. The light extinguishes when the LOAD/RUN switch is set in the LOAD position.

2.2.2.4 CHECK Indicator

The CHECK Indicator is an orange indicator light which shows that due to some abnormal condition the disk drive may be incapable of writing. When the abnormal condition no longer exists, the disk drive is reset by moving the LOAD/RUN switch to LOAD position and then back to RUN.

2.2.2.5 PROTECT Switch/Indicator

The PROTECT Switch/Indicator is a red back-lighted momentary-contact push-button switch. In units with the internal Write Protect option switches set to activate the Write Protect feature, the PROTECT switch glows and writing is inhibited whenever one of the following steps is performed.

1. Initial turn-on of drive.
2. LOAD/RUN switch changed from RUN to LOAD. (Condition remains when switch is returned from LOAD to RUN.)
3. Using system sends Write Protect command to drive.

To allow writing, Write Protect is turned off by the operator depressing the PROTECT switch.

In units where the Write Protect feature has been deactivated for one or both disks by the internal Write Protect option switches, the PROTECT indicator continues to function as described above; however, disks with Write Protect so deactivated are NOT write protected.

2.2.3 Interlocks

The cartridge clamps cannot be operated while the disks are rotating, the heads or brushes are over the disk surface, or equipment power is off. When all of these conditions are satisfied, the LOAD indicator is illuminated to indicate that the cartridge clamps can be opened.

The spindle motor will not rotate if the cartridge dust cover is not installed, or if the cartridge clamps are open. Although the drive will operate with the equipment drawer open, for safety and other reasons it is recommended that the drawer be kept closed whenever practical to do so.

2.2.4 Typical Operating Procedures

Initial Checkout

NOTE: Prior to initial checkout, and alignment if needed, completely unpack the Model 44B, and remove the shipping clamp shown in Figure 2-2. If not installed in a rack or cabinet, place the unit on a stable flat surface.

Connect the power cord and I/O cables. Set the drive's front panel LOAD/RUN switch to the LOAD position. Apply AC power. Verify that the PROTECT indicator is on. Verify that the LOAD indicator comes on within 60 seconds after applying power.

1. If rack mounted, open the equipment drawer by pulling out on the door handle as shown in Figure 2-7.
2. Open the two cartridge clamps located on each side of the spindle bowl.
3. Refer to Figure 2-8. Slide the tab on the cartridge handle to the left, raise the handle, and lift the cartridge clear of its dust cover lower half.
4. Place the opened cartridge over the spindle hub oriented so that its handle will fold toward the rear. Lower the cartridge into place with a gentle back and forth rotary motion to ensure that its lower notches engage the alignment tabs inside the bowl. Lower the cartridge as far as it will go, then lower its handle to lock it in place.
5. Place the cartridge dust cover upside down inside the drive's cartridge bowl on top of the cartridge just installed, and close the two cartridge clamps.
6. Slide the drive back into its compartment until the latches engage the slides.
7. Set the LOAD/RUN switch to RUN. Verify that the front panel LOAD light goes out.
8. Allow the equipment about 60 seconds to complete its start-up cycle. Verify that the READY light comes on at the completion of this cycle.

NOTE: With the Write Protect feature active for one or both disks, the PROTECT light must be depressed to extinguish the light and allow 'writing' on the protected disk or disks.

Further checkout or operation as appropriate to the using system may now be performed.

NOTE: After installation of the disk drive, verify alignment of the R/W heads as described in Section 5 of the Maintenance Manual.

When disk operation is complete, or when it is desired to exchange cartridges, the following steps are to be followed:

1. Set the LOAD/RUN switch to LOAD. Wait for the LOAD light to come on (about 15 seconds).
2. For rack mounted drives, open the equipment drawer (Figure 2-7), and slide the drive out to its first stop.

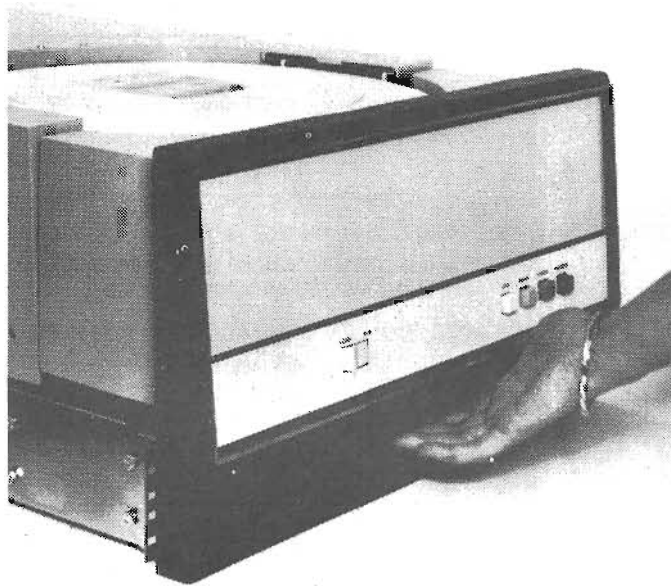


Figure 2-7. OPENING THE EQUIPMENT DRAWER

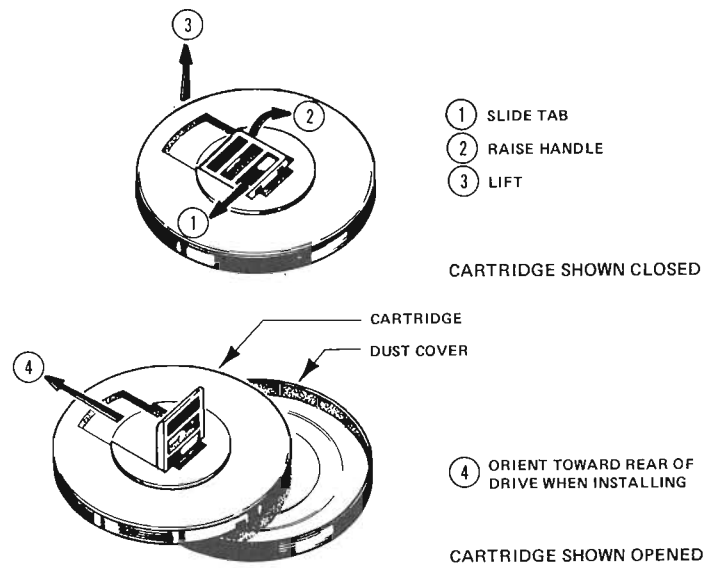


Figure 2-8. OPENING THE TYPE 5440 DISK CARTRIDGE

3. Open the cartridge clamps and lift off the cartridge dust cover.
4. Slide the tab on the cartridge handle to the left, raise the handle to disengage the cartridge from the spindle, and lift the cartridge clear of the drive.
5. Invert the dust cover, lower the cartridge into it, and fold the handle down all the way to engage the cover magnets and release the tab. The cartridge is now ready for storage.
6. Install another cartridge and dust cover, close the equipment drawer, and place the drive in the RUN mode or completely deenergize the system.

NOTE: If no cartridge is to be installed at this time, cover the spindle bowl area with a plastic sheet or other lint-free cover.

SECTION 3

INTERFACE INFORMATION

3.1 AC POWER REQUIREMENTS

The Model 44B Disk Drive is designed to operate over an AC frequency range of 49 to 61 Hertz, single phase.

A tap changing PCB, located in the AC power socket assembly can be positioned for nominal line voltages of 100, 120, 220 or 240 VAC. Line voltage should remain within +10% of the nominal value selected.

The AC power socket is a recessed three-pin socket with power, return and ground pins.

3.2 SIGNAL INTERFACE

3.2.1 Interface Connector

The Model 44B Disk Drive has two interface connectors. Viewed from the rear of the drive, the right-most connector is considered to be the input connector, receiving input information from a controller or from another disk drive preceding it in a daisy chain system. The left-most connector is considered to be the output connector, providing circuit connection facilities for a succeeding disk drive in a daisy chain system. If this is the last drive in a daisy chain system, or the only drive in the system, the left-most connector receives the required terminator. Table 3-1 shows the part numbers for the I/O connectors and mating cable connectors.

3.2.2 Interface Pin Assignment Summary

Interface connector pin assignments are summarized in Table 3-2, and are defined in the following paragraphs.

3.2.2.1 Input Lines

The following input lines are found on the standard Model 44B Disk Drive. Unless otherwise stated, the signals on control input lines must be held for the duration of the function controlled. Signal Levels are 0 volts for low (LO), and +3.5 volts for high (HI). As shown in Table 3-2, a signal title prefixed with a negative (-) symbol represents a signal that is active when in its LO state. A signal title prefixed with a positive (+) symbol represents a signal that is active when in its HI state.

Select Lines

The interface has four lines assigned to unit-select function, in order for the using system to select one particular drive in a system where more than one drive is used. Two switches on the Address Logic PCB are used to identify the drive as unit 1,2,3, or 4. The drive will then respond only to a unit select signal that appears on the corresponding unit select line. For example, if the switch settings identify a drive as unit #2, it will respond only to a select signal on the SELECT UNIT 2 input line. A LO signal selects the drive. All interface lines, except the Attention line, are inactive until a SELECT signal is applied to the proper select line. When LO, this line qualifies all of the drive's other interface lines.

Table 3-1.
I/O Connector Part Numbers

	Supplier	Shell	Pins
Right I/O Box Connector -	Diablo Winchester	10667-01 MRAC50PJ6	10583-01 1024P
Right I/O Cable Connector -	Diablo Winchester	10670-02 MRAC50SJTDH	10525-13 100-0927S
Left I/O Box Connector -	Diablo Winchester	10667-02 MRAC50SJ6	10583-02 1024S
Left I/O Cable Connector -	Diablo Winchester	10670-01 MRAC50PJTDH	10525-12 100-0917P

Table 3-2

Interface Pin Assignments

<u>Input Signal</u>	<u>Pin</u>	<u>Output Signal</u>	<u>Pin</u>
-Select Unit 1	L	-File Ready	U
Unit 2	R	-Ready to S/R/W	F
Unit 3	V	-Address Acknowledge	p
Unit 4	Z	-Logical Address Interlock	y
Disk Select	AA	-Seek Incomplete	u
Head Select	a	-Index Mark	Y
-Cylinder Address Bit 1	N	-Write Check	h
Bit 2	s	-Read Clock	A
Bit 4	J	-Read Data	C
Bit 8	X	+Attention 1 **	CC
Bit 16	f	+Attention 2 **	DD
Bit 32	T	+Attention 3 **	EE
Bit 64	b	+Attention 4 **	FF
Bit 128	BB	-200 TPI Line	z
Bit 256*	m	Write Protect Status	P
-Strobe	t	-Sector Mark	W
-Restore	w	-Sector Bit 1	c
-Write Gate	e	-Sector Bit 2	j
-Erase Gate	K	-Sector Bit 4	k
-Write Data & Clock	B	-Sector Bit 8	n
-Read Gate	E	-Sector Bit 16	v
-Write Protect Input	H	+Not Run	D
		<u>Other Lines</u>	
		+5V for terminator	r
		Ground	S
		Ground	x
		Ground	HH
		Unused	M
		Unused	d

* Hold Cylinder Address Bit 256 at 0 volts on 100 tpi units.

** -Attention option available (Option No. 490)

Disk Select

This line selects the disk to be used in a forthcoming operation. LO selects the removable cartridge disk; HI selects the fixed disk.

Head Select

This line selects the upper or lower head for use with the selected disk. LO selects the upper surface head; HI selects the lower surface head.

Cylinder Address

These lines accept a 9-bit (8-bit for 100 tpi) binary absolute cylinder address. When strobed, their content is supplied to an internal address register to control head movement. These lines must be settled prior to application of the strobe signal, and should be held until the trailing edge of the strobe signal.

Strobe

This line is used to enable the track address and restore lines. Strobe should be applied only after the appropriate signal lines have settled, and must be held until at least the leading edge of the -ADDRESS ACKNOWLEDGE signal. Rise and fall times are to be compatible with commercially available DTL and TTL integrated circuits. The strobe pulse is LO.

Restore

This line carries the "head positioner restore to 0" command. When this command has been completed, the heads are located over cylinder 0, the address registers have been set to address 0, and the Seek Incomplete condition is reset. The RESTORE line must have settled to $\pm 10\%$ of its steady value prior to the application of the strobe signal. The restore pulse is LO.

Write Gate

This line turns on write current in the selected head. The signal must be applied not more than 2 microseconds prior to writing the first flux transition, and held for the duration of the write operation. The write gate is LO for current on.

Erase Gate

This line, when LO, turns on erase current to the selected head. There is no built-in delay of erase current.

Write Data & Clock

This line accepts multiplexed data and clock pulses for double frequency or phase encoding type recording; one complete pulse for each recorded flux reversal. Pulses must have a minimum width of 100 nanoseconds. Leading edge must have a transition time of not more than 50 nanoseconds. This line is held at +3.5 volts when not writing. Write pulses swing from +3.5 volts to 0 volts.

Read Gate

When LO, this line enables the READ CLOCK and READ DATA output lines.

Write Protect Input

A LO signal on this line restores the write protect condition for either or both disks, depending on the settings of the write protect option switches. If both of the write protect option switches are set to ON, both disks will be restored to write protect simultaneously by a single pulse from the controller. The pulse to restore write protect must be at least 1 microsecond in duration.

3.2.2.2 Output Lines

File Ready

This line supplies a maintained LO level when all the following conditions are met:

- Power on
- Cartridge loaded
- LOAD/RUN switch in RUN position
- Start-up cycle complete
- WRITE CHECK line HI
- FILE SELECT line LO

Ready to Seek, Read or Write (Ready to S/R/W)

A LO level on this line indicates that the disk drive is in the File Ready condition and is not in the process of executing a seek operation. Following a seek command to a valid address (other than the present address), or a restore command, the READY TO S/R/W line goes HI within 1 microsecond after detecting the leading edge of the -STROBE signal. The return of the READY TO S/R/W line to the LO state indicates that seek (or restore) operation has been completed, the heads are fully settled and the machine is ready to Seek, Read or Write to another address. This line does not change when the present cylinder is readdressed.

Address Acknowledge

A LO level on this line indicates that a valid command to move the heads (seek command) has been accepted, and the heads have begun to move. An -ADDRESS ACKNOWLEDGE signal (1.2 microsecond LO) is issued 500 nanoseconds after the leading edge of the Strobe, even if there is no change from the previous address. This signal will not be issued if a command to move to a track position greater than 407 (203 for 100 tpi drives) is received. In this case, execution of the command is suppressed, and a -LOGICAL ADDRESS INTERLOCK signal is issued on another line.

Logical Address Interlock

A LO level on this line indicates that a track address greater than 407 (203 for 100 tpi drives) has been received, and that the command cannot be

executed. The seek command is suppressed. This signal, from a latch circuit in the output, resets with the next -ADDRESS ACKNOWLEDGE signal or RESTORE command.

Seek Incomplete

A LO level on this line indicates that a malfunction has caused an incomplete seek operation. This signal level will be maintained until a RESTORE command is received and executed by the disk drive or until the Load/Run Switch is switched to LOAD and then back to RUN.

Index Mark

This line supplies one LO, 40 microsecond pulse per disk revolution, as a mechanical index mark on the hub of the selected disk passes its transducer.

Write Check

When the drive is selected, a LO level on this line indicates that one or more of the following conditions exist:

1. Write current without LO WRITE GATE.
2. WRITE GATE LO without write current.
3. Write and select of multiple heads, or an open R/W coil.
4. Erase current without LO ERASE GATE.
5. ERASE GATE LO without erase current.

When WRITE CHECK is LO, execution of all external commands is suppressed. The operator may reset Write Check by moving the LOAD/RUN switch to LOAD and then back to RUN.

Read Clock

This line supplies clock pulses which have been separated from the data signals during reading. Pulse width is nominally 100 nanoseconds, +50 nanoseconds. The leading negative-going edge must be used for reference.

Read Data

This is the output line for data signals which have been separated from clock signals during reading. Pulse width is nominally 100 nanoseconds, +50 nanoseconds. The leading negative-going edge must be used for reference.

Attention Lines

A logical combination of output lines that informs the using system, by means of a LO signal, when the disk drive is ready, completes seek, fails to complete seek, accepts a seek command to the present address, or receives an invalid address. The ATTENTION line number and the SELECT line number correspond.

200 tpi Line

This line notifies the controller that the drive is a 200 tpi machine. The output is HI until the drive is selected and the heads are loaded, at which time it goes LO.

Write Protect Status

The signal level on this line provides an indication of the Write Protect Status. A LO level indicates that the disk drive's write capability is inhibited. The operator can change the status manually by depressing the momentary action PROTECT switch on the front panel, thereby enabling the disk drive's write capability.

Sector Mark

This line supplies one LO 40 microsecond pulse for each sector slot on the disk hub as it passes its transducer. The leading edge of the pulse must be used as reference.

Sector Address

These five lines continuously define, in binary form, the sector address under the heads. This address is derived from one of two counters, determined by the DISK SELECT input line. Each counter is reset to zero by the leading edge of the SECTOR MARK following the index mark, and is advanced by the leading edge of subsequent SECTOR MARKS. The status of the sector address counter is valid if the read-out occurs at the trailing edge of the SECTOR MARK signal, or 3 to 5 microseconds after the leading edge of SECTOR MARK.

Not Run

This line informs the controller whether the drive is in the Run mode or the Load mode. NOT RUN is HI when the drive is in the Load mode, and LO when it is in the Run mode.

+5V for Terminator

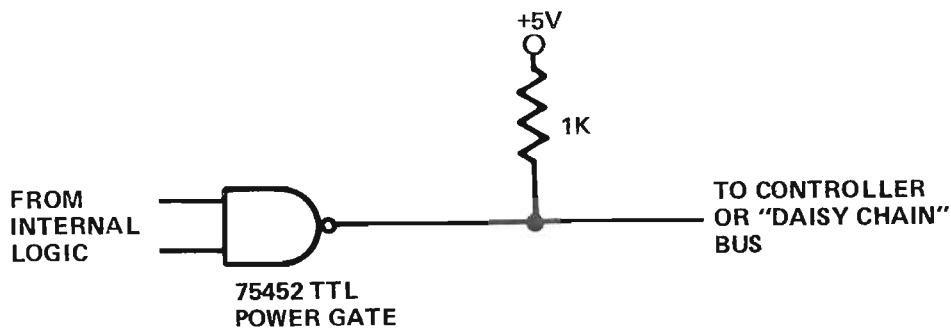
This line supplies +5 volts to the terminator circuits. A terminator must be connected to the I/O output connector of a single drive or the last drive in a daisy chain configuration.

3.2.2.3 Output Line Drive Capability

An output driver circuit for the READ CLOCK and READ DATA lines is shown in Figure 3-1, for the standard configuration. All other lines are driven as shown in Figure 3-2.

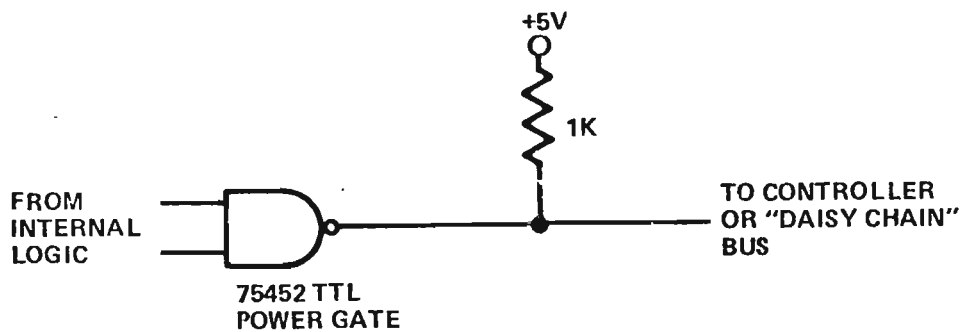
3.2.2.4 Input Gates

The Model 44B Disk Drives use an 8836 type NOR gate as the input circuit. This device has a higher input threshold in the low logic state than most commercially available DTL or TTL circuits, assuring a higher noise margin on all input lines. Input hysteresis of the 8836 gates further increases noise immunity. Low input current, even with no Vcc, prevents a Model 44B with power down from affecting other drives in a daisy chain system. In addition, the 8836 input circuit loads the signal transmission lines with



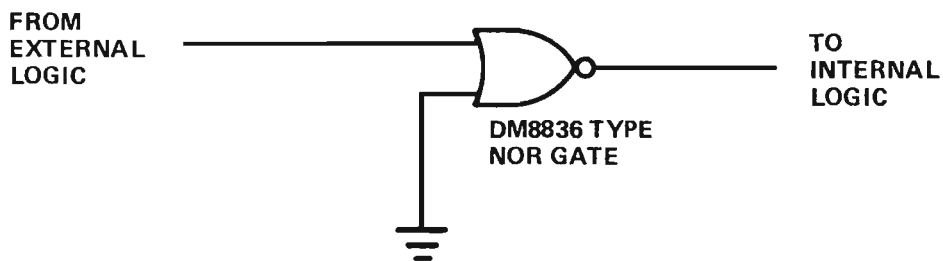
Logic "Low" Output Level = Max +0.4V at 100 milliamp sink current
 Logic "High" Output Level = Min +3.5V with external pull-up resistor

Figure 3-1. OUTPUT DRIVER - READ CLOCK AND READ DATA



Logic "Low" Output Level = Max +0.4V at 100 milliamp sink current
 Logic "High" Output Level = Min +3.5V with external pull-up resistor

Figure 3-2. OUTPUT DRIVER CIRCUIT



Logic "Low" Input Threshold = Min +1.05V; no current load.
 Logic "High" Input Threshold = Max +2.5V; 180 microamp max current load (pull up).

Figure 3-3. STANDARD INPUT CIRCUIT

significantly less input current under operating conditions, causing less local reflections on the line.

The input of the 8836 circuit has to be pulled up in the high logic state. For this reason, it cannot be driven by an open collector driver stage without collector resistance. This collector resistance is in the terminator which must be installed on the last disk drive in a daisy chain, or on any drive used alone. Figure 3-3 shows the input circuit used in the Model 44B.

3.3 INPUT/OUTPUT CABLES

Two types of cable may be considered for use with the Model 44B. One type is the conventional round cable consisting of twisted pairs for each signal, with a PVC jacket. The other type is a PVC flat cable with a flexible ground plane.

3.3.1 Flat Cable

Because of the uniform transfer characteristics and production efficiency, a flat cable type is recommended. The flat cable, ordered by option number from Diablo, has the following physical characteristics:

Number of conductors	50
Wire size	30 AWG solid
Shield	Flexible ground plane
Insulation	PVC

The characteristic wave impedance is 80 ohms, with the shield plane grounded on both ends.

3.3.2 Round Cable Twisted Pair

For those applications where, in spite of the drawbacks, a round cable is preferred, the type recommended is made of twisted pairs insulated with heat sealed overlapping MILENE tapes. Physical characteristics of round cables are:

Number of twisted pairs	50
Wire size	28 (7/36) AWG (4.94mm)
Nominal OD of insulated wire	.023" (.584mm)
Nominal OD of PVC jacket	.370" (9.398mm)
UL rating	Style No. 2384

The characteristic wave impedance of one single twisted pair is approximately 85 Ohms. If all ground leads of the twisted pairs are grounded on both ends, the wave impedance drops to approximately 45 Ohms, which results in excessive current from the drive circuits. Individually shielded twisted pairs cable is not recommended.

Figure 3-4 shows one practical method of dressing the twisted pair wires at the cable end.

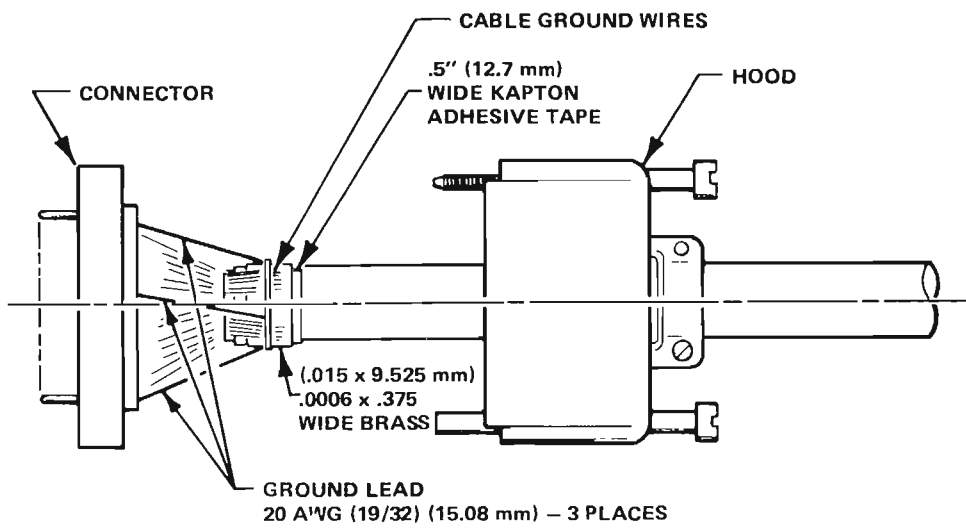


Figure 3-4. INTERFACE CONNECTOR ASSEMBLY

3.3.3 Cable Lengths

Maximum recommended cable length between the controller and the first disk drive is 15 feet (4.57m). Cables between disk drives in a daisy chain configuration should not normally exceed 12 feet (3.65m) in length, although one 15-foot (4.57m) cable between the second and third drive would be permitted if necessary to use more than one cabinet. The total cable run in a daisy chain configuration should not exceed 50 feet (15.24m).

3.4 TERMINATING RESISTORS

The signal lines carrying pulses transmitted by any disk drive will cause reflection on both ends of the cable if the cable is not properly terminated. Figure 3-5 shows two waveshapes taken on the terminated end of a cable when the other end was left unterminated. The negative-going leading edge is not affected significantly, and can be used as an input to logic circuits if properly handled. The trailing edge, however, is determined by the time duration of the pulse, and the length of the cable. Those lines carrying signals of short duration should always be terminated on both ends. Satisfactory system performance cannot be achieved, even with relatively short cable lengths, if the signal lines are not properly terminated on both ends.

A typical circuit for termination of the cables is shown in Figure 3-6. Cable terminators matched to Diablo-supplied flat cable are available.

3.5 DOUBLE FREQUENCY RECORDING

In double frequency recording, a clock bit is recorded at the beginning of each bit cell time. Recording a clock bit in each bit cell time results in the read-back data being self-clocking.

To write a series of logical zeros, only the clock bit is recorded at the beginning of each bit cell time. To record a one bit, a flux reversal, or bit, is inserted in the center of a bit cell time. To write a series of ones, a clock bit and a data bit will be recorded in each bit cell time. It then can be seen that the frequency of bits for a series of ones is twice the frequency for a series of zeros. Hence the method is called Double Frequency Recording.

Figure 3-7 shows the bit and time relationship for recording and reading back a data bit series of 0-0-0-1-0-1-1-1. Nominal pulse width for the system is 100 nanoseconds.

Multiplexed data and clock pulses are sent to the drive on one line; each pulse received on the line results in one current and flux reversal. The data and clock pulses read from the disk are sent to the controller on separate interface lines.

3.6 DISK FORMAT

Prior to consideration of the disk format information in this paragraph, the reader should become familiar with the basic functioning of the disk drive, as described in Section 4.

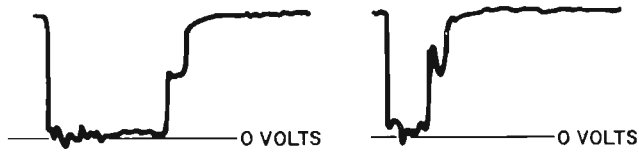


Figure 3-5. WAVESHAPES

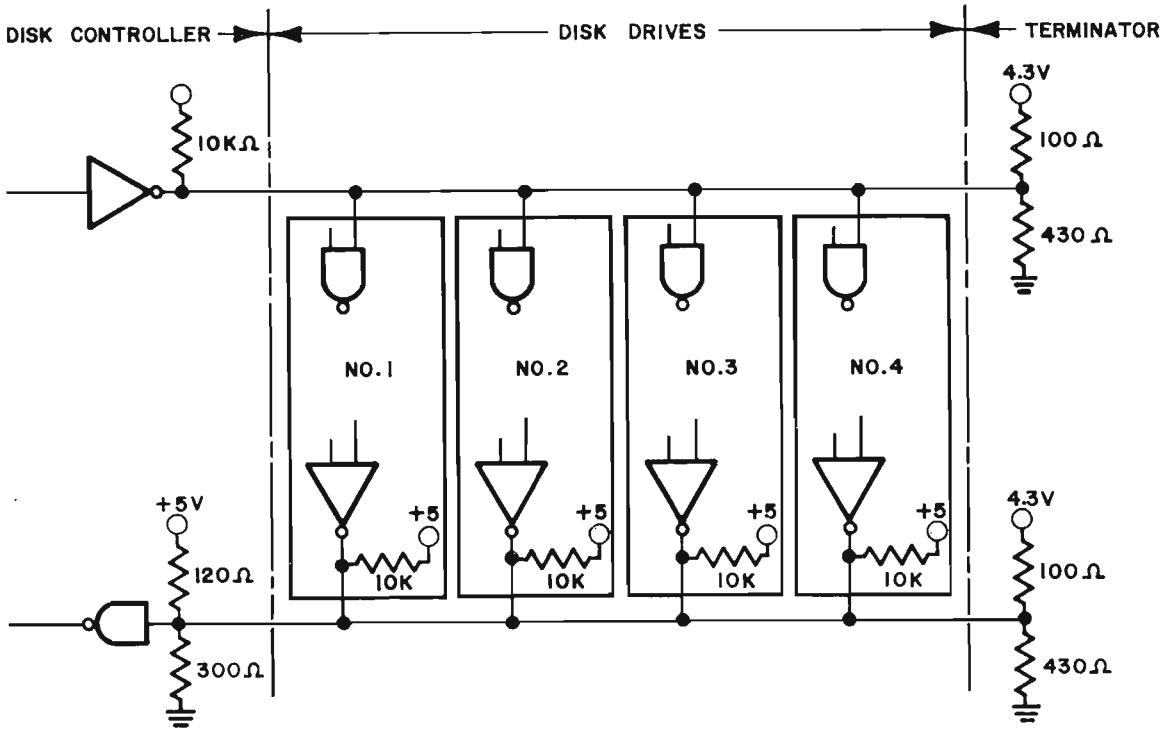


Figure 3-6. DAISY CHAIN AND TERMINATOR

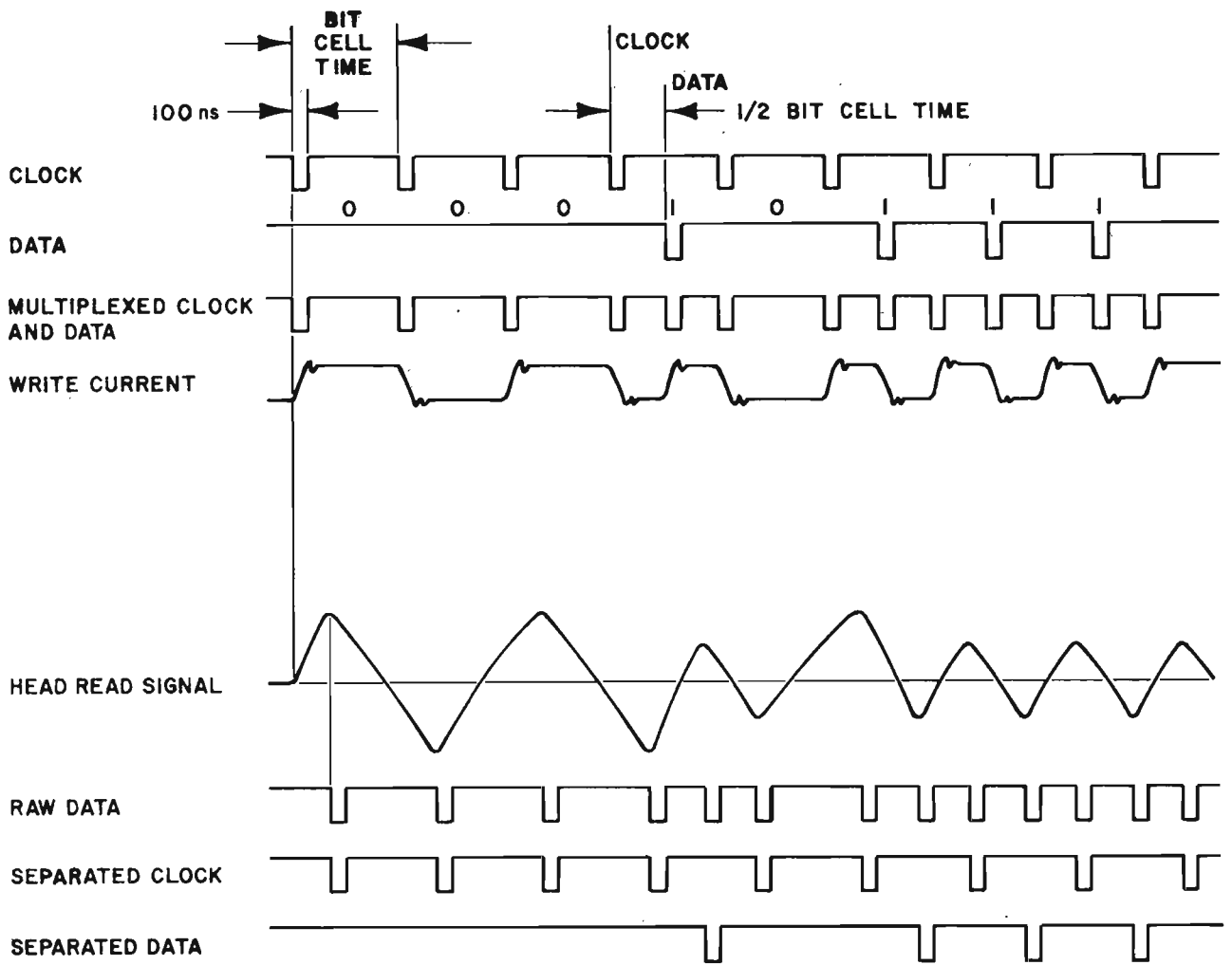


Figure 3-7. DOUBLE FREQUENCY RECORDING

Each track on the disk is divided into a number of sectors of equal length, as shown in Figure 3-8. This is accomplished by means of slots on the disk hub, or electronically in the using system. The time between index marks is equal to the time of one disk revolution. This is nominally 25ms (40ms for 1500 rpm units). The time duration of each sector is the time between index marks divided by the number of sectors. If the disk rotation speed varies, the sector time varies by the same percentage. The spindle motor speed tolerance is $\pm 2\%$; consequently, it can cause the sector time to vary by this amount. Other tolerance factors for which allowances must be made in disk formatting include physical separation of the erase and write coils, variation in the spacing of sector slots, alignment of the index transducers, sector jitter, alignment cartridge variation, write clock frequency, read amplifier recovery time, and variations in the transducers and their associated circuitry.

Formatting of the disk is the organized placement of data zones and guard zones in each sector, and the placement of clock pulses and/or data pulses within these zones. The data zones are those areas within each sector where data is to be recorded or read. To provide disk interchangeability and reliable read recovery of data, these data zones must contain a constant number of data cells, even in the presence of disk speed variation and other tolerances described above. The guard zones are variable in length, and ensure a constant number of data cells in each data zone by absorbing variations in sector time.

Each guard zone is a series of recorded clock pulses. The guard zone is recorded at the beginning and ending of each data zone, and is normally defined as a preamble (when located at the beginning of the data zone) and as a postamble (when located at the end of the data zone). The length of each guard zone must be adequate to allow for a reliable reading of each data zone even under worst case conditions of tolerances. Each data zone typically contains synchronizing, header, data, and check information. A guard zone and a data zone are defined as a sector, and typically are recorded by a combination of hardware and software control. When sector slots on the disk hub are used, a sector mark format method is commonly employed. Sector mark formatting is explained in paragraph 3.6.1. When only the index slot is on the disk hub, it is common to use address mark format. The address mark is a unique recorded pattern on the disk which is detected by the R/W heads. It serves the same function as the sector slots. Address mark format is explained in paragraph 3.6.2.

3.6.1 Sector Mark Format

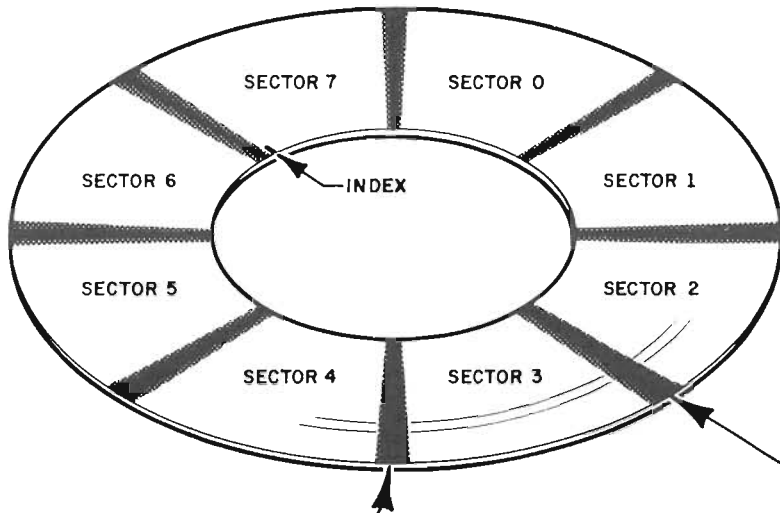
A typical sector format is shown in Figure 3-8 for an eight-sector disk. For any number of sectors, the amount of available data field in each sector can be determined by reference to Table 3-3.

Table 3-4 shows nominal values of typical system tolerances. The format shown in Figure 3-8, using the time per field shown in Table 3-3, provides a reasonable margin of allowance for these variations.

The fields shown in Figure 3-8 are described as follows:

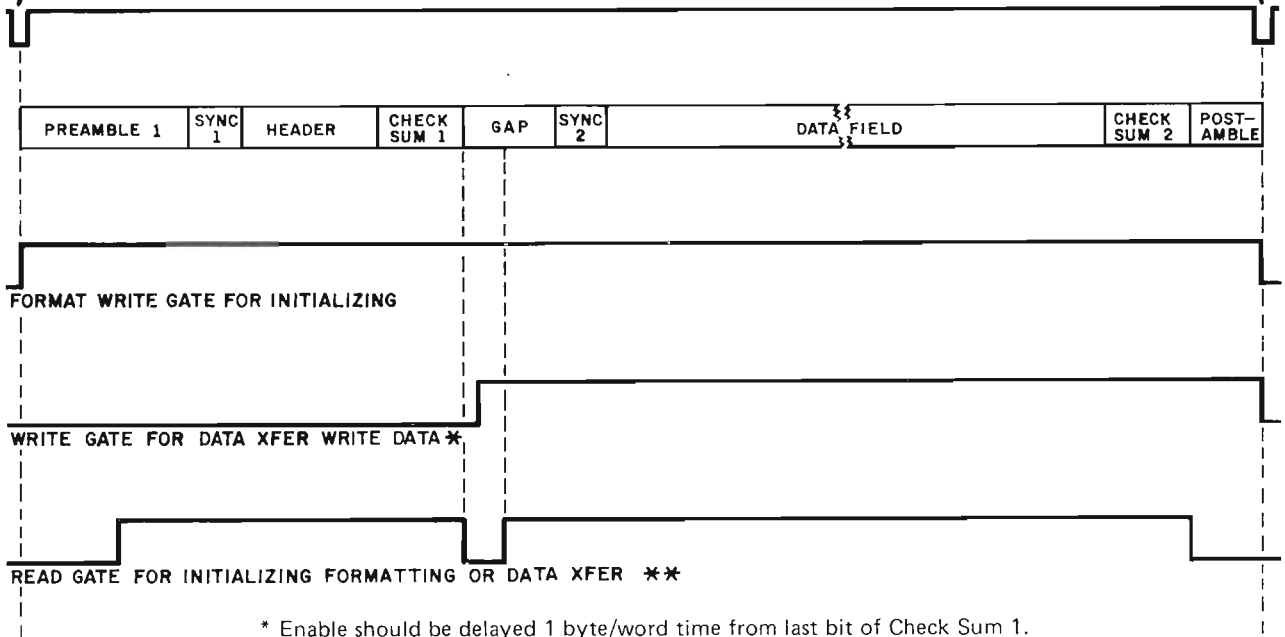
PREAMBLE - allows for differences in index transducers, alignment cartridge differences, and read amplifier recovery time. There is an overlap of these tolerances within system considerations. The Preamble is generally filled with hexadecimal 00 characters.

TOP VIEW OF DISK



- 1) SHADED AREAS INDICATE GUARD ZONES.
- 2) SOLID LINE IN GUARD ZONE INDICATES SECTOR MARK.

DETAIL OF ONE TRACK ON TYPICAL SECTOR



* Enable should be delayed 1 byte/word time from last bit of Check Sum 1.

** Read gate should be enabled 1/2 way through the Preamble area. This insures reading a zero field for data separator synchronization.

Figure 3-8. TYPICAL SECTOR FORMAT

TABLE 3-3.

FORMAT REQUIREMENTS FOR MODEL 44B

	2400 RPM		1500 RPM	
	usec	Bytes	usec	Bytes
Preamble (Note 1 & 4)	19.2	6	30.72	6
-(Note 2 & 4)	51.2	16	81.92	16
Sync	6.4	2	10.24	2
Header	6.4	2	10.24	2
Header Check Sum	6.4	2	10.24	2
Gap (Note 3)	3.2	1	5.12	1
Sync	6.4	2	10.24	2
Data Field (Note 4)	T_{DF}	$T_{DF}/3.2$	T_{DF}	$T_{DF}/5.12$
Data Check Sum	6.4	2	10.24	2
Postamble (Note 4)	6.4	2	10.24	2
Sector Time	T_{sector}	---	T_{sector}	---

$$T_{sector} = \left[\frac{.998 * (6) (10^7)}{R \cdot N} - S \right] \text{ usec}$$

S = Sector slot placement error from Table 3-4

R = RPM option

N = Number of sectors per revolution

* See Note 1, Table 3-4

Maximum time available for the Data Field is:

$$T_{DF} = \left[T_{sector} - \sum \text{Time For Tolerances} \right] \text{ usec}$$

NOTES:

- (1) Assuming that read channel is settled before sector mark
- (2) Assuming that read channel is turned on at sector mark
- (3) This is the time required by the Model 44B Disk Drive. The controller turnaround time must be added to this Gap for proper system operation.
- (4) Time not used by the Data Field should be divided between the Preamble and Postamble.

TABLE 3-4.

MAXIMUM SYSTEM TOLERANCES

	2400 RPM	1500 RPM
Sector Slot Placement	14 usec/sector	22.4 usec/sector
Transducer Alignment	7 usec/sector	11.2 usec/sector
Alignment Cartridge Differences	3 usec/sector	4.8 usec/sector
Write Gap Placement	3.6 usec/sector	5.76 usec/sector
Disk Rotation Speed (Note 1)	100 usec/rev	160 usec/rev
Read Channel Recovery	30 usec	30 usec

NOTES: (1) This number represents a $\pm 0.2\%$ disk speed tolerance. If the total system contains drives other than the Diablo Model 44B, and the data on the removable disk is expected to be stored/retrieved from any disk, interchangeably, in the system, it is suggested that the system designer consult the specifications of the other drives used in the system. The system format must allow for the maximum time variation of any drive used in the complete system.

SYNC 1 - a known bit pattern, commonly two characters of hexadecimal 03, detected within the controller and used to gate subsequent pulses into the using system. The amount of Preamble read is variable, because of tolerance; consequently, detection of the Sync 1 field is necessary to signal the end of the Preamble and the beginning of the Header.

HEADER - this field is typically recorded with the cylinder, head, and sector address located beneath the R/W heads. This field is generally compared with the address to which the heads were addressed by the controller, to ensure the seek operation was successfully completed. This field also typically contains masking bits to indicate track surface condition.

HEADER CHECK SUM (Check Sum 1) - a check character developed within the controller during the write cycle and recorded on the disk. This check character is compared with the character developed within the controller during the read cycle to ensure that the preceding field was read accurately.

GAP - all clock bits. This is an optional field that is used as a Preamble to the Data Field. It is used in system applications where the Header Field is not rewritten during data write operations. It is written when the disk surface is initialized. When this Gap is not used, the Header and Data Fields are both written during each Data Write Operation.

SYNC 2 - a known bit pattern, detected within the controller and used to gate subsequent pulses into the using system. Sync 2 is required to signal the end of the Gap and the beginning of data.

DATA FIELD - the data to be recorded or retrieved.

DATA CHECK SUM (Check Sum 2) - a check character developed within the controller during the write cycle and recorded on the disk. This check character is compared with the character developed within the controller during the read cycle to insure that the preceding field was read accurately.

POSTAMBLE - all clock bits recorded until the following sector is detected. The Postamble allows for Write/Erase Gap placement, disk rotation speed, and write clock frequency variations. Also shown in Figure 3-8 is typical turn-on and turn-off time of the WRITE GATE/ERASE GATE (assuming that they are turned on at the same time) in relation to the SECTOR MARK and data record. Typical READ GATE timing is also shown. Note that the leading edge of each SECTOR MARK is used as reference, and that the READ GATE is turned on at the midpoint of the Preamble. The leading edge of the SECTOR MARK is more predictable than the trailing edge. READ GATE is turned on at the midpoint of the Preamble to allow for the tolerances that add to or subtract from the nominal sector start time.

3.6.2 Typical Write Format, Write Data and Read Operations

Table 3-3 and Figure 3-8 should be used as references with the following explanations.

3.6.2.1 Typical Write Format Operation

1. Detect leading edge of Sector Mark 0.
2. Enable Write/Erase Gate.
3. Write Preamble (zeros pattern).
4. Write Sync 1, typically 03_{16} or 03_8 .
5. Write Header and Check Sum 1.
6. Write Gap (zeros pattern).
7. Write Sync 2, Data Field and Check Sum 2. Typically a zeros pattern, or Header/Check Sum 1 information will be written in the Data Field during format operations. Sync 2 is typically 03_{16} or 03_8 .
8. Write Postamble (zeros pattern) until the leading edge of the next Sector Mark is detected.
9. During format operations Write/Erase Gate would not be disabled until the last sector of that particular track is formatted. Each sector would follow the same format, with only Header and Check Sum 1 information changing. This same track should be read on the next revolution to verify a proper formatting operation. Timing considerations would be identical to a Read Data operation.

3.6.2.2 Typical Write Data Operation

1. Detect the leading edge of the desired Sector Mark.
2. Wait for one-half of the Preamble and enable Read Gate.
3. Read zeros Preamble to Sync Data Separator circuit.
4. Read Sync 1 and Header/Check Sum 1 to verify that the correct sector has been found.
5. Disable Read Gate after last bit of Check Sum 1.
6. Wait one byte/word time, then enable Write/Erase Gate.
7. Write Gap (zeros pattern).
8. Write Sync 2.
9. Write Data Field/Check Sum 2.
10. Disable Write/Erase Gate at the leading edge of the next Sector Mark.

3.6.2.3 Typical Read Operation

1. Detect the leading edge of the desired Sector Mark.
2. Wait for one-half of Preamble and enable Read Gate.
3. Read zeros Preamble to Sync Data Separator circuit.
4. Read Sync 1 and Header/Check Sum 1 to verify that the correct sector has been found.
5. Disable Read Gate after last bit of Check Sum 1.
6. Wait for one-half of Gap, and enable Read Gate.
7. Read zeros Preamble to Sync Data Separator circuit.
8. Read Sync 2, Data Field/Check Sum 2.
9. Disable Read Gate.

3.6.3 Address Mark Format

When the Address Mark Format is used, sector slots on the disk hub are not used. Instead, an Address Mark is recorded in each sector. The Address Mark serves the same purpose as the Sector Marks described in 3.6.1. This format is characterized by missing clock pulses in the Address Mark word, and is used with a Model 44B having the VFO Option. System tolerances affecting disk interchangeability are accounted for in the Gaps. Figure 3-9 shows a typical Address Mark Format.

The format is written while preparing or testing a new disk. Data recorded during subsequent Write Data Operations is written only between Gaps 3 and 4.

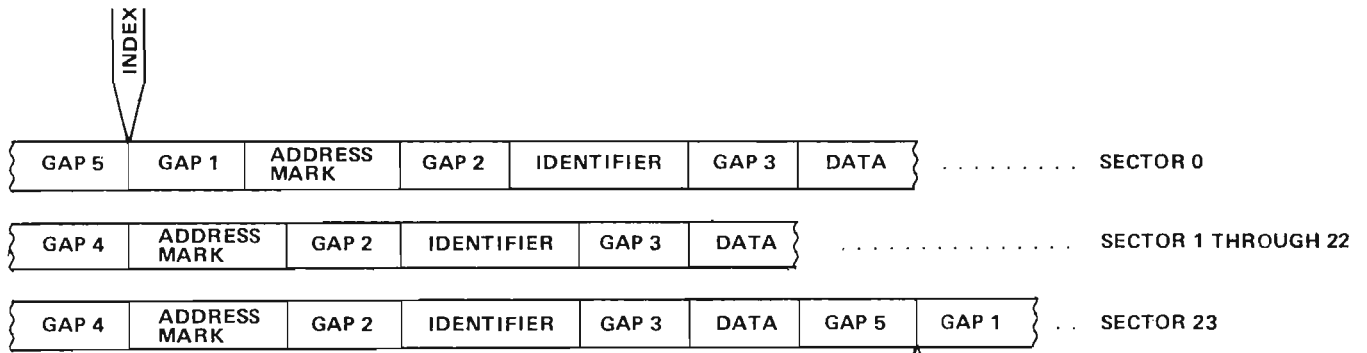
Typically, a Write Format command writes the entire track, starting at the index. Two bytes of F2 with 2 clock bits missing are recorded for Address Marks. Refer to Figure 3-10.

Cyclic code and bit count appendage characters are written at the end of an I.D. and Data Field. A read-verify command, which checks the cyclic code and bit count appendage characters, is used to check for write errors after the Write Format command.

3.6.3.1 Write Data

A typical Write Data Operation on a formatted disk would proceed as follows:

1. Seek to desired track.
2. Read for Address Mark.
3. Detect Address Mark and Sync Character.
4. Compare Identifier Field with desired address.



INDEX — Starting point for every track. Derived from physical slot on disk hub.
 Gap 1 — (nominal 260 us) 40 bytes of "1's" followed by 7 bytes of "0's". Only after INDEX.
 Address Mark — Two bytes of hex F2 with missing clock pulses. Refer to Figure 3-10.
 Gap 2 — Sync character — Hex OE. Nominal 5.12 us.
 I.D. — Six bytes total. 1 flag byte, 2 address bytes, and 3 bytes of check characters.
 Gap 3 — 10 bytes of all "1's", 4 bytes of "0's" and 1 byte Sync character Hex OE.
 Data — 256 bytes of data and 3 bytes of check characters.
 Gap 4 — 28 bytes of "1's" and 7 bytes of "0's".
 Gap 5 — all "1's" until INDEX detected. Only recorded after Sector 23.

Identifier Field explanation.

Flag Byte — Bits 0 - 5 not used

Track condition is indicated in bits 6 and 7.

- 0 0 = Good track
- 1 0 = Defective track
- 0 1 = Alternate track
- 1 1 = Defective alternate track

Address Bytes — Byte 1, Bits 0-7 contain the binary number of the cylinder (0 to 407)

Byte 2, Sector Address

Bit 0 is head number 0 = upper surface
 1 = lower surface

Bits 1-5 are sector address
 0 to 23 = upper surface
 32 to 55 = lower surface

Bits 6-7 are not used should be "0's"

Check characters — Bytes 1 and 2 are Cyclic Check Character.

Byte 3 is Bit Count Appendage.

Figure 3-9. ADDRESS MARK FORMAT

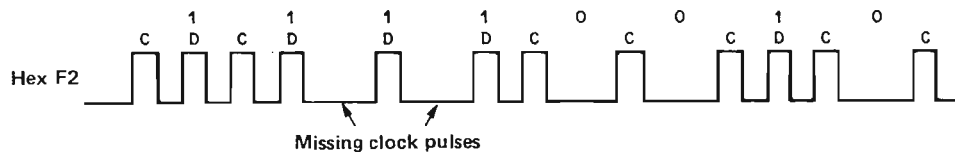


Figure 3-10. ADDRESS MARKS

5. Six byte times after desired address has been located, write four bytes of F.F., four bytes of 00 and Sync key character O.E.
6. Write Data field of 256 data bytes with cyclic check and bit count appendage.
7. Terminate Write Operation at end of bit count appendage.

3.6.3.2 Data Read

A typical Data Read Operation on a formatted disk would proceed as follows:

1. Seek to desired track.
2. Read for Address Mark.
3. Detect Address Mark and Sync Character.
4. Compare Identifier Field with desired address.
5. Detect Sync Character after desired Identifier, at end of Gap 3.
6. Read Data Field of 256 data bytes with cyclic check and bit count appendage.
7. Terminate Read Operation at end of bit count appendage.

3.7 TYPICAL SIGNAL TIMING AT THE INTERFACE

Figure 3-11 shows the timing relationship at the interface for one possible example of a typical write and read sequence using the single sector format described in paragraph 3.6.2. In the following description the terms input and output mean input to and output from, the disk drive.

Assuming that a cartridge is loaded, that the disk drive is in the Run mode, and that the start-up cycle is complete, a FILE SELECT LO input at time t_0 establishes a file ready condition. The FILE READY output goes LO when the disk drive is selected.

At this time, the controller selects the upper head of the lower disk by making the HEAD SELECT and DISK SELECT input lines LO and HI respectively. These lines could have been set up prior to time t_0 , but have no internal effect until the FILE SELECT line goes LO.

Since the disk drive is now ready and no seek is taking place, the READY to S/R/W output goes LO. The disk drive can now accept any valid command to Seek, Read, or Write. At time t_1 the appropriate Cylinder Address lines corresponding to the desired cylinder go LO. These are shown collectively in the figure rather than showing all nine cylinder address inputs separately. When the Cylinder Address lines have settled, at time t_2 , the STROBE input goes LO. The appropriate Cylinder Address lines must remain LO during the STROBE pulse. About 500 nanoseconds after the leading edge of the STROBE pulse, the ADDRESS ACKNOWLEDGE output goes LO, indicating that the command to move the heads to a specific Cylinder Address has been accepted, and that

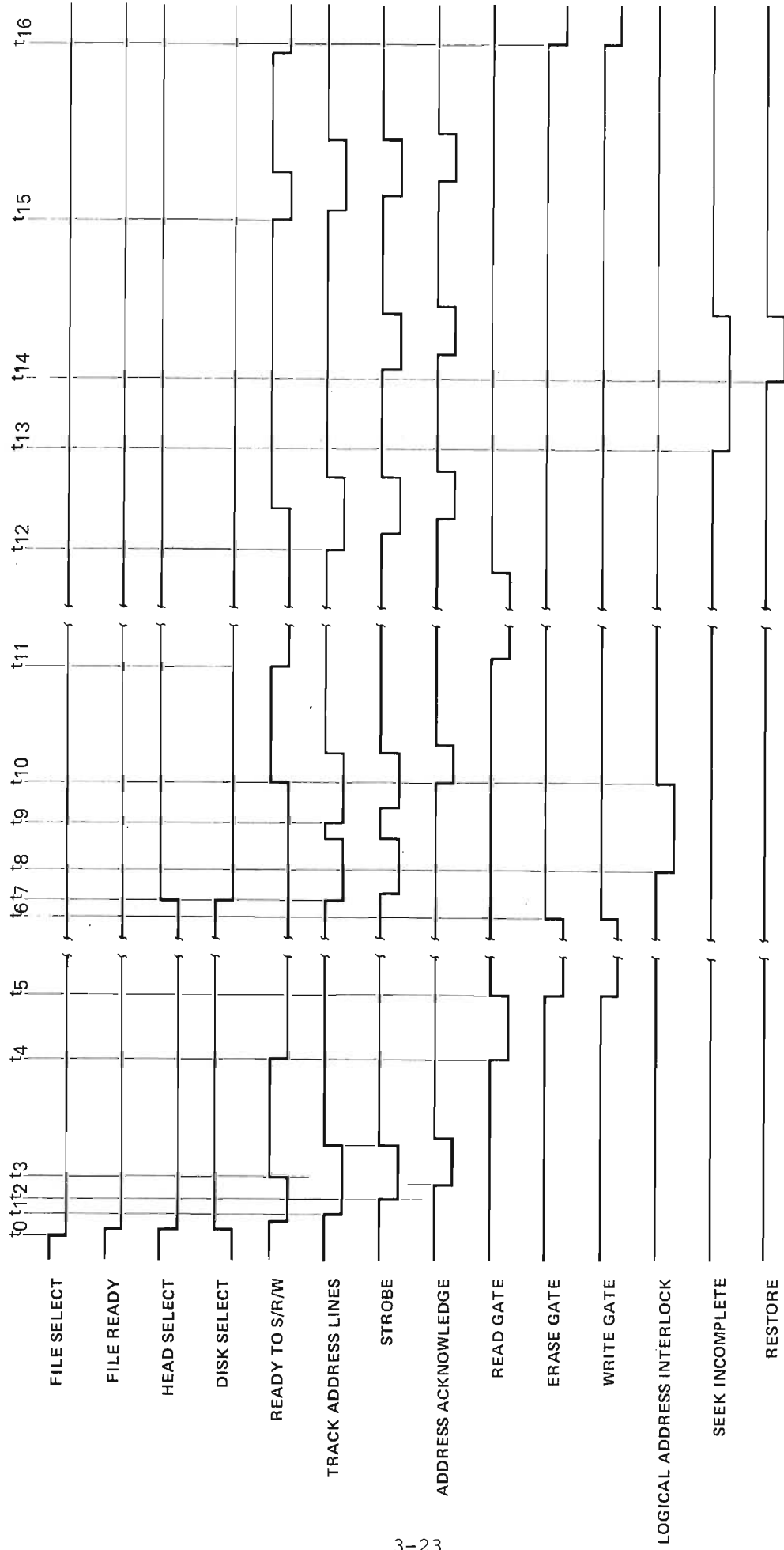


Figure 3-11. TYPICAL SYSTEM TIMING

Seek has commenced. Since a Seek is in process, the READY TO S/R/W output goes HI. This occurs at time t_3 , which is within 1 microsecond after the leading edge of the STROBE pulse. At time t_4 , the heads have settled at the desired Cylinder Address, and the disk drive is now ready to Seek, Read, or Write to another address. This is indicated by the READY TO S/R/W output going LO. In our example, the controller now makes the READ GATE input line LO so that the Address Mark can be read prior to writing. The Read Gate could have been made LO prior to time t_4 , but the internal read circuitry of the disk drive will not accept a read command unless READY TO S/R/W is LO.

When the desired address is reached, at time t_5 , the controller sets READ GATE HI, and WRITE GATE and ERASE GATE LO. Multiplexed data and clock pulses are now furnished by the controller to the WRITE DATA AND CLOCK input. Write Data, Read Data, and Clock pulses are not shown in Figure 3-11. Writing continues until time t_6 . Since the intervals between time t_5 and t_6 , and between time t_{11} and t_{12} are several hundred times longer than other intervals shown, they are not drawn to scale.

At time t_7 , the controller selects a different disk and head, and codes a new address on the CYLINDER ADDRESS lines. In our example, the controller has commanded an invalid address (greater than 407 for 200 tpi drives, or greater than 203 for 100 tpi drives), and the LOGICAL ADDRESS INTERLOCK output informs the controller of this fact by going LO at time t_8 . The ADDRESS ACKNOWLEDGE output remains HI. READY TO S/R/W remains LO, indicating that the drive is ready to accept a valid address.

At time t_9 , the controller codes a valid address into the disk drive's CYLINDER ADDRESS lines. Application of the STROBE starts a seek operation and, at time t_{10} , READY TO S/R/W goes HI, ADDRESS ACKNOWLEDGE goes LO, and the LOGICAL ADDRESS INTERLOCK is reset. When the heads have settled at time t_{11} , READY TO S/R/W goes LO and a Read Operation is started.

After the Read Operation is completed, a new seek is started at time t_{12} . In our example, a malfunction causes an incomplete seek, and the SEEK INCOMPLETE output goes LO. The controller then places a LO on the RESTORE input at time t_{14} . The subsequent STROBE input causes the heads to drive to track zero, where they are ready for another Seek command at time t_{15} . Figure 3-11 shows another Write Operation at time t_{16} .

SECTION 4

PRINCIPLES OF OPERATION

4.1 GENERAL

Subsection 4.2 presents a general description of the various functional subsystems of the Model 44B. Subsection 4.3 presents detailed descriptions of the circuitry contained on each printed circuit board.

Information concerning the disk drive/controller interface, which is presented in Section 3, is not repeated in this Section.

4.2 FUNCTIONAL DESCRIPTION

The major functional subsystems of the Model 44B Disk Drive are listed below and described in the subsections which follow. A Functional Block Diagram is shown in Figure 4-1.

1. Start-up and Interlock Control
2. Spindle Drive and Speed Control
3. Head Loading/Unloading
4. Head Positioning
5. Servo System
6. Index/Sector Information Control
7. Data Transfer Functions

4.2.1 Start-up and Interlock Control

4.2.1.1 Power-Off Condition

With no power applied to the Model 44B, normal status is that the R/W heads and disk cleaning brushes are in their home (retracted) positions, and the cartridge retaining clamps are locked closed by the deenergized cartridge interlock solenoid.

If power is turned off in the middle of a start-up cycle while the brushes are out over the disk, they will remain in that position until power is reapplied.

4.2.1.2 Initial Power-On

When power is first applied to the Model 44B, the following functions occur:

- 1) Voltage monitoring
- 2) Initial reset
- 3) Heads and brushes retract (if extended)
- 4) Cartridge unlock

Voltage Monitoring

The internal power supply of the Model 44B produces +24 VDC, -24 VDC, -24VDC UNFUSED, +15 VDC, -15 VDC and +5 VDC. The +15 VDC, -15 VDC and +5 VDC are monitored for failure or an out-of-tolerance condition. If either condition occurs, the monitor circuit initiates an immediate retract and unloading of the

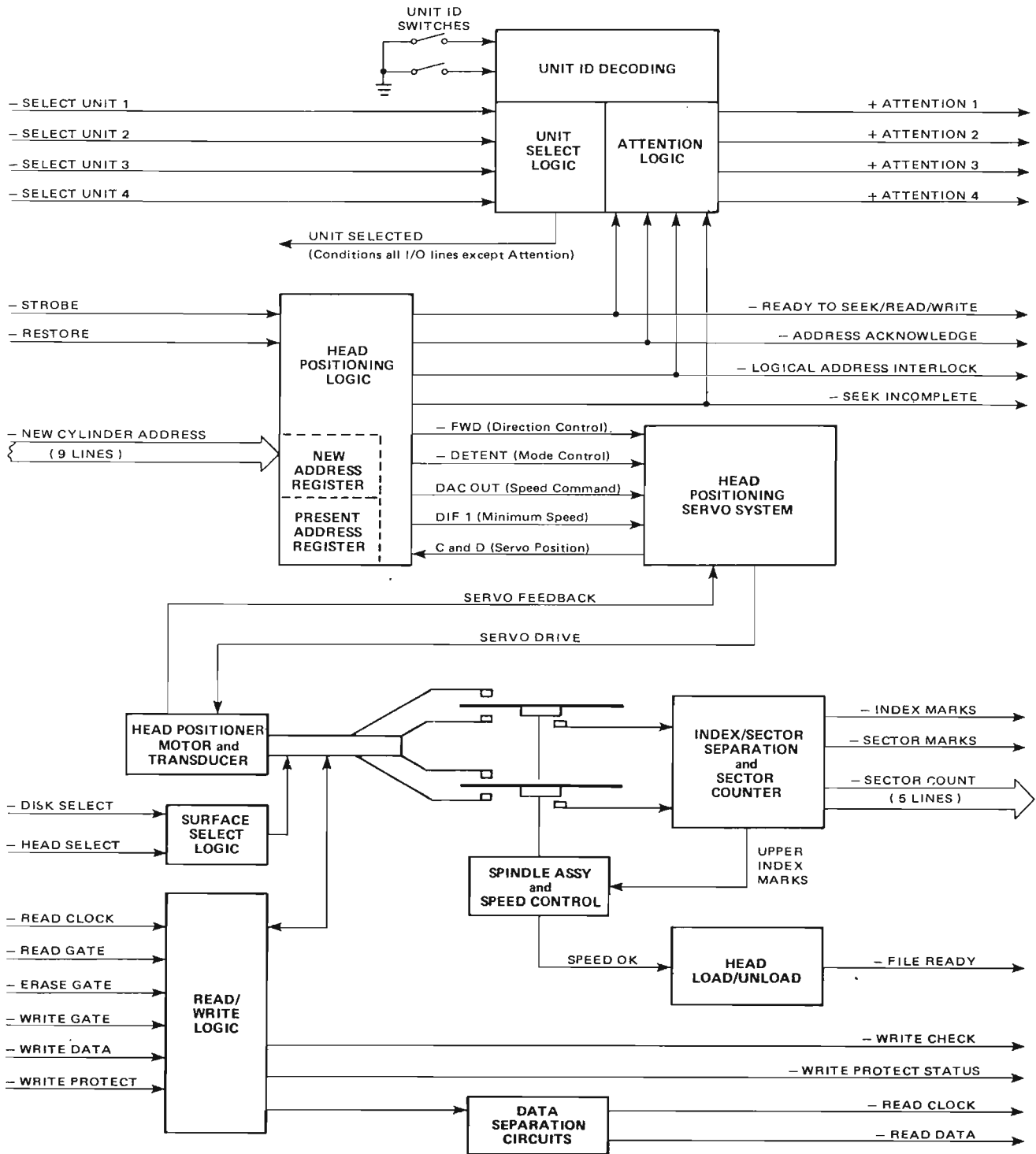


Figure 4-1. MODEL 44B FUNCTIONAL BLOCK DIAGRAM

R/W heads. This is done to prevent data errors resulting from erroneous voltage levels or head crash resulting from spindle speed reduction.

Initial Reset

Initial Reset is accomplished at power turn-on by a momentary Power On Reset pulse. The resultant actions are listed below.

1. The Write Check circuits are reset.
2. The Write Protect circuits are set if the internal Write Protect switches are ON.
3. The Head Retract circuits are conditioned to retract the heads if they were left out over the disk.
4. The New Address Register and Present Address Register are cleared. Since the Present Address Register actually holds the ones complement of the present address, it is cleared to Address 0 by loading it with ones.

Heads and Brushes Retract

If the R/W heads are not in their fully retracted position, they are immediately retracted at turn-on. Circuit control to accomplish this is performed by power-on reset.

Normally, at turn-on, the disk cleaning brushes are in their home position and the Brush Switch is in its Brush Home position. If, however, the last power turn-off occurred in the middle of a brush cycle, the brushes will be left out over the disk. In this case, the Brush Switch would be in its Brush Out position. At turn-on, the remainder of the brush cycle will immediately resume until the brushes reach their home position.

Cartridge Unlock

Four conditions must be met to energize the Cartridge Interlock Solenoid to unlock the cartridge clamps:

- 1) AC power must be ON.
- 2) The spindle must be stopped. Dynamic braking of the spindle occurs for approximately 20 seconds each time AC power is turned on or the Load/Run Switch is switched to the LOAD position. During this 20-second period, the cartridge clamps remain locked regardless of whether the spindle is actually rotating.
- 3) The R/W heads must be home.
- 4) The disk cleaning brushes must be home.

Conditions (3) and (4) ensure that the heads and brushes are not out over the disk where they could damage the disk and heads while the cartridge is being removed.

4.2.1.3 Start-up Sequence

With power on and a cartridge in position on the drive, the start-up sequence begins when the Load/Run switch is set to RUN. The spindle begins rotating and accelerating toward operating speed, the brush cycle begins, and the disk cartridge clamps are locked closed. When the spindle

has reached normal operating speed and the brush cycle has been completed, the head positioner carriage is released from its home (retracted) position. The heads advance and are loaded as they descend the load/unload ramp. The +READY signal goes HI as soon as the heads have left the home position.

The head positioning logic advances the heads out to approximately cylinder 8 and then immediately returns them to cylinder 0. With the heads at cylinder 0, the drive awaits the first instruction from the controller.

4.2.2 Spindle Drive and Speed Control

The spindle assembly, with integral two-phase induction motor, rotates the disk at 2400 rpm (or optional 1500 rpm). The lower disk is permanently fixed to the spindle shaft, while the upper disk is contained in a type 5440 removable cartridge. The removable disk is held to the spindle assembly during operation by a magnetic ring.

The spindle assembly is driven by two square-wave signals of slightly over 80 Hz (50 Hz for 1500 rpm), generated by a variable-frequency oscillator (VFO). The drive signals are phase separated by 90 degrees. The time between index pulses is referenced to a 6.6 MHz crystal oscillator, and any timing error is used to adjust the VFO frequency.

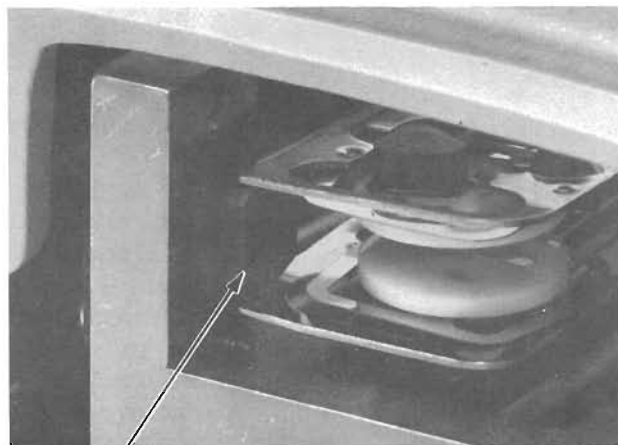
The hub of each disk has an index slot which is sensed by a stationary transducer as the slot passes the transducer. The repetition rate of the index mark signal for the lower disk is monitored by the speed control circuitry as a basis for spindle speed control. Spindle speed is maintained within $\pm 0.2\%$ of nominal by controlled variation of the drive signal frequency.

4.2.3 Head Loading/Unloading

Head Loading refers to positioning the R/W heads at the proper distance from the recording surface for data recording and retrieval.

Head Loading/Unloading is accomplished by means of a mechanical ramp (see Figure 4-2.) Loading occurs as part of the start-up sequence when the heads advance out from the home (retracted) position and descend the ramp. This is permitted only after the disk has accelerated up to approximately 98% of its normal operating speed. At this spindle speed, the loaded heads will "fly" on a cushion of air approximately 2 microns (80 microinches) above the recording surfaces. This flying condition can be achieved only when the spindle blower is forcing a relatively high volume of filtered air across the rapidly rotating disks. If head loading were to occur with the spindle stopped or at speeds below the loading threshold, a head crash (head contacts disk) would result, with consequent damage to the disks and heads.

Unloading of the heads occurs when the heads ascend the ramp while being retracted to the home position. This forces the heads away from the surfaces of the disks. Normally, head unloading is performed only when the disk drive is switched from Run mode to Load mode. In this case, the drop in spindle speed is sensed and the heads are immediately retracted and unloaded. Head unloading is also provided for in case of a power failure or malfunction in any of the internal power supplies of the disk drive. In this case, the voltage failure is sensed and an emergency retract is immediately performed. This protects the disks and heads from head crash, and also prevents data errors resulting from erroneous logic functions.



RAMP

Figure 4-2. HEAD LOAD/UNLOAD RAMP

The emergency retract driver circuit on the Power Driver PCB is supplied by the -24 VDC unfused supply. The storage capacity of this supply is sufficient to perform the emergency retract even in the event of a sudden complete power failure.

The backslope of the load/unload ramp mechanically detents the head positioner carriage in the home position.

4.2.4 Head Positioning

Head Positioning refers to relocating the R/W heads to a new cylinder location by a seek operation, or to cylinder 0 by a restore operation.

The head positioning control logic furnishes head positioning speed and direction instructions to the Servo System.

The heads are mounted on arms which are transported by a head carriage. The carriage moves the heads radially over the disk in either a forward (toward the spindle) or reverse direction. With the disk rotating and the head stationary, the position of the head describes a circular track over the surface of the disk, as shown in Figure 4-3. During a write operation, this track is magnetically recorded on the disk surface. The track consists of data signals and other signals which allow the accurate recording, retrieval and identification of data, as explained in Section 3 of this manual.

Similarly, the head can be positioned over a recorded track during a read operation. The representation in Figure 4-1 shows that there are four tracks aligned vertically. Together, these four tracks describe a cylinder. If the head carriage moves toward the center of the disks, a small cylinder is described by the four tracks.

The position of the carriage is referred to as the cylinder address. The combination of cylinder address, disk select signal, and head select signal constitutes the track address. Since the address logic in the Model 44B is used to position the head carriage, the term "address" is used in this manual to mean cylinder address.

4.2.4.1 Normal Seek

Refer to the block diagram in Figure 4-4, and the normal seek routine flowchart in Figure 4-5.

To accept a seek command from the controller, the disk drive must be in Ready to Seek/Read/Write status. To initiate a normal seek operation, the controller transmits a new cylinder address and a strobe pulse to the disk drive. The drive checks the new address for validity (<408 for 200 tpi and <204 for 100 tpi). An invalid address is not accepted by the drive, and a -LOGICAL ADDRESS INTERLOCK level is transmitted back to the controller. A valid address is accepted and stored in the New Address Register (NAR) of the drive. The drive also transmits an -ADDRESS ACKNOWLEDGE pulse back to the controller to confirm acceptance of the new address.

The address of the cylinder at which the heads are presently located is stored in the Present Address Register (PAR). The present address and the new address are sent to the Adder, where the difference is computed. The

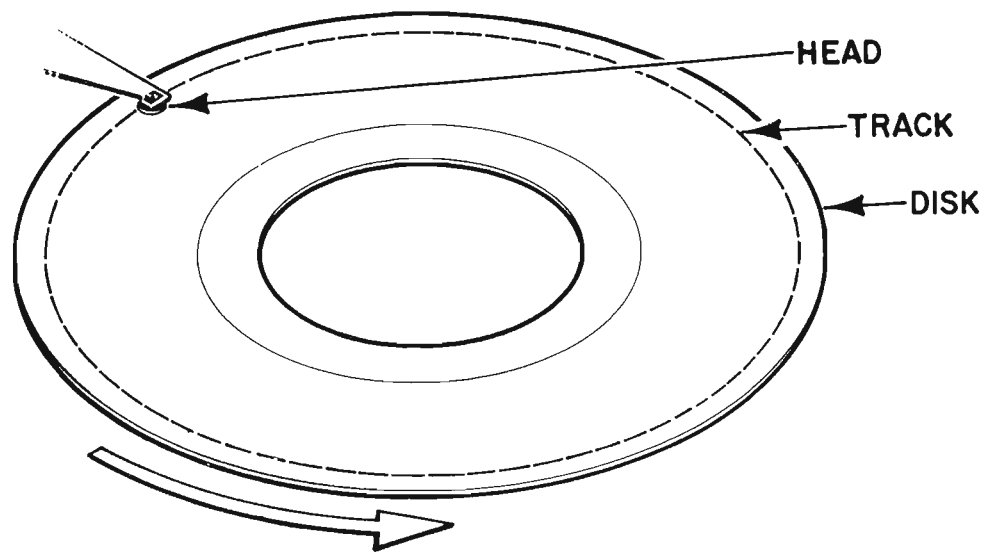


Figure 4-3. TRACK LAYOUT

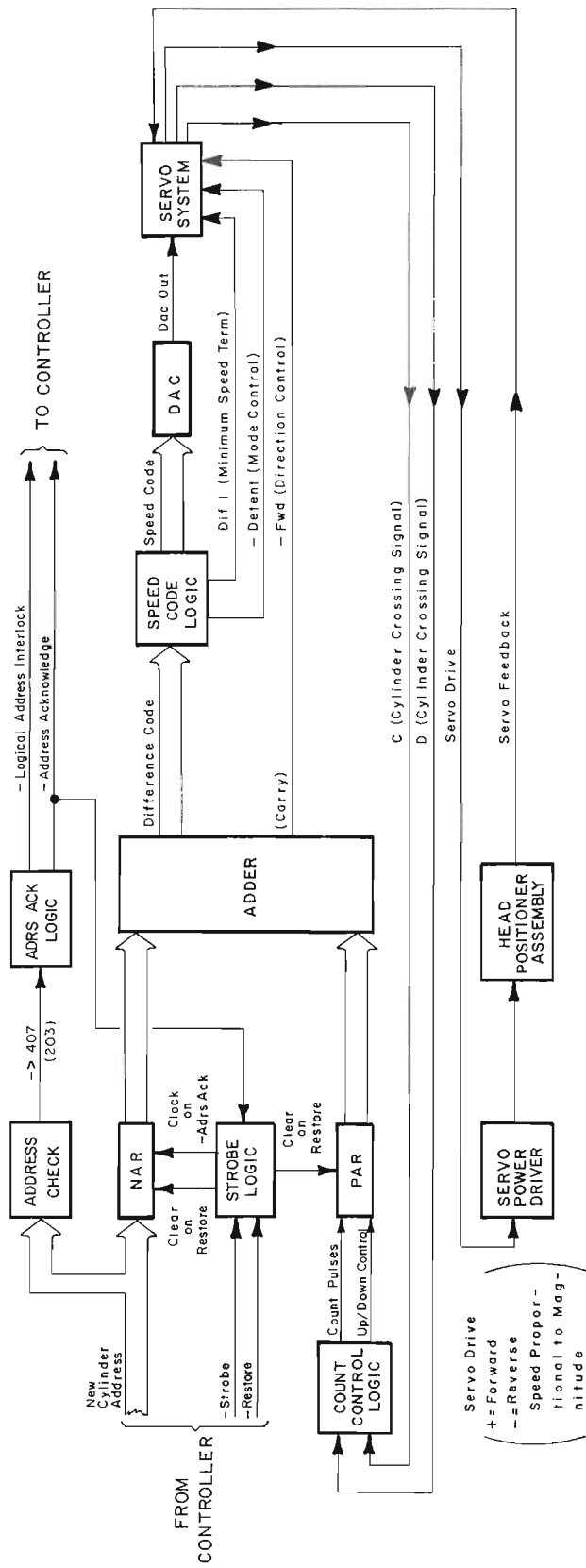


Figure 4-4. HEAD POSITIONING BLOCK DIAGRAM

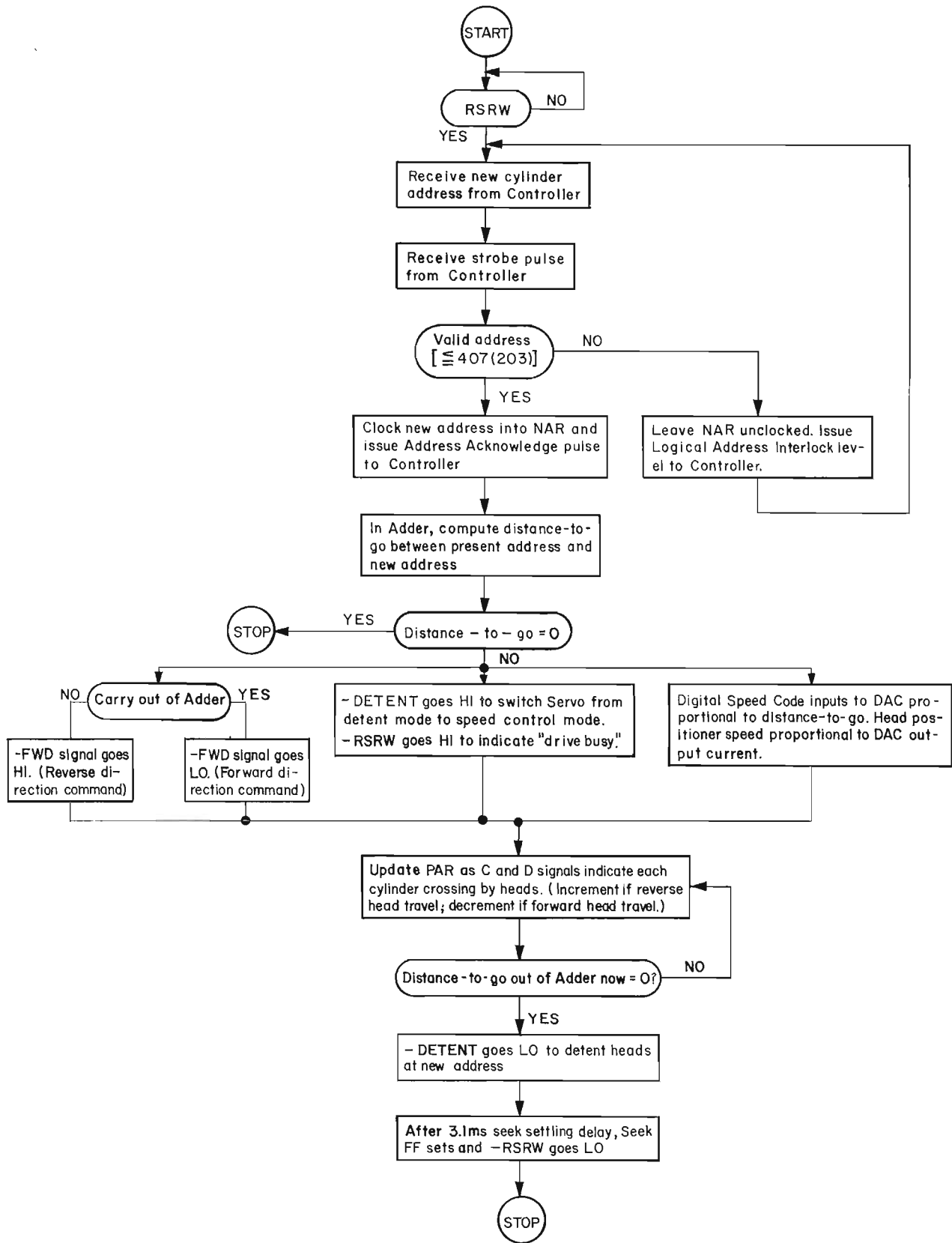


Figure 4-5. NORMAL SEEK FLOW CHART

carry output of the Adder serves as a direction term which indicates the direction of the head motion required; forward (toward the spindle) when a carry exists, or reverse when there is no carry. From the difference code out of the Adder a speed code is developed. Any non-zero speed code produced by the Speed Code Logic switches the Servo System from detent mode to speed control mode. This digital speed code is applied to the inputs of a Digital-to-Analog Converter (DAC). The analog current output of the DAC is directly proportional to the value of the digital speed code input. The least significant bit (entitled +DIF 1) of the speed code bypasses the DAC and is routed to the servo circuit separately.

The DAC output signal is sent to the Servo System, where it joins the +DIF 1 signal to become the Servo Drive signal for the Head Positioner motor. The magnitude of the Servo Drive signal determines Head Positioner motor speed, and its polarity determines direction of Head Positioner travel.

At each cylinder crossing during head travel, an incrementation or decrementation of one count updates the address in the Present Address Register.

During the early part of a long seek (>255 cylinders for 200 tpi or >127 cylinders for 100 tpi), the maximum speed code exists. This results in maximum DAC output and, consequently, maximum head positioner speed. When the speed code drops below the threshold for maximum, each cylinder crossing reduces the speed code by one count. This provides smooth deceleration of the head positioner as the heads approach the destination cylinder.

The DAC output reaches 0 when the heads are one cylinder away from their destination. Then, when the difference code out of the Adder goes to 0, +DIF 1 goes LO and the Servo System switches to detent mode to hold the heads at the new location.

An incomplete-seek condition is detected by monitoring the time/current product of head positioner motor current. If positioner motor drive current continues beyond a certain point exceeding the maximum time required to complete a normal seek, the disk drive transmits a -SEEK INCOMPLETE level back to the controller. Typical controller response is to restore the heads to track 0 and renew the original seek instruction.

4.2.4.2 Restore

A Restore operation is initiated by a Restore command and Strobe pulse from the controller.

The Restore operation repositions the heads at cylinder 0, and clears the New Address Register and Present Address Register to zero. The Present Address Register actually holds the ones complement of the present address; consequently, it is set to zero by loading it with ones. The heads are moved to cylinder 0 by switching the Servo System from detent to speed control; forcing a minimum speed code; and forcing a reverse direction signal.

4.2.5 Servo System

The servo system has two modes of operation; speed control mode and detent mode. It operates in the speed control mode during head positioning, and in the detent mode when the heads are held stationary. When the servo is in the speed control mode, it provides controlled drive current to the head positioning motor. The amount of drive current supplied determines head velocity. The polarity of the drive current determines direction of head motion.

When operating in the detent mode, the servo system provides current to the motor, as required, to counter any drift or forced movement of the heads away from the detented position.

The simplified block diagram in Figure 4-6 shows the principle elements in the servo system. There are basically three inputs to the summing junction: 1) the Speed Command input, 2) the Velocity Feedback input, and 3) the Position (detent) input.

When the servo is in the detent mode, the -DETENT signal disables the Speed Command input and couples the Position input to the summing junction. If the head positioner begins to drift away from its detented position, the Position signal shifts proportionally from zero potential to a polarity which opposes the drift. This forces the head positioner back to its detented position. The servo system switches to the speed control mode when the -DETENT signal goes HI. Head positioning is initiated by a Speed Command from the Address Logic.

Figure 4-7 shows, in simplified form, the relationship between Servo Drive, Speed Command and Velocity Feedback during a long seek operation. The Speed Command accelerates the head positioner toward the new address location. As the velocity increases, the Velocity Feedback signal increases with polarity opposite to that of the Speed Command. Due to the high amplifier gain, the Servo Amp saturates during acceleration and Servo Drive remains at its maximum level until Velocity Feedback has increased sufficiently to bring the amplifier out of saturation (waveform point b). Thereafter, increased Velocity Feedback decreases Servo Drive.

When the remaining distance to go drops below 256 cylinders (waveform point c), the Speed Command begins to diminish. As a result, the Velocity Feedback inputs exceeds the Speed Command input and Servo Drive polarity reverses. This produces a braking effect which smoothly decelerates the heads.

When the heads arrive at their destination, the Speed Command and Velocity Feedback have decreased to near zero and the servo system switches back to detent mode (point d on waveform). The velocity and position information is also used to develop cylinder crossing information in the form of signals C and D. These two signals are used by the Address Logic to update the Present Address Register at each cylinder crossing.

4.2.5.1 Expanded Servo Diagram

An expanded block diagram of the servo system is shown in Figure 4-8.

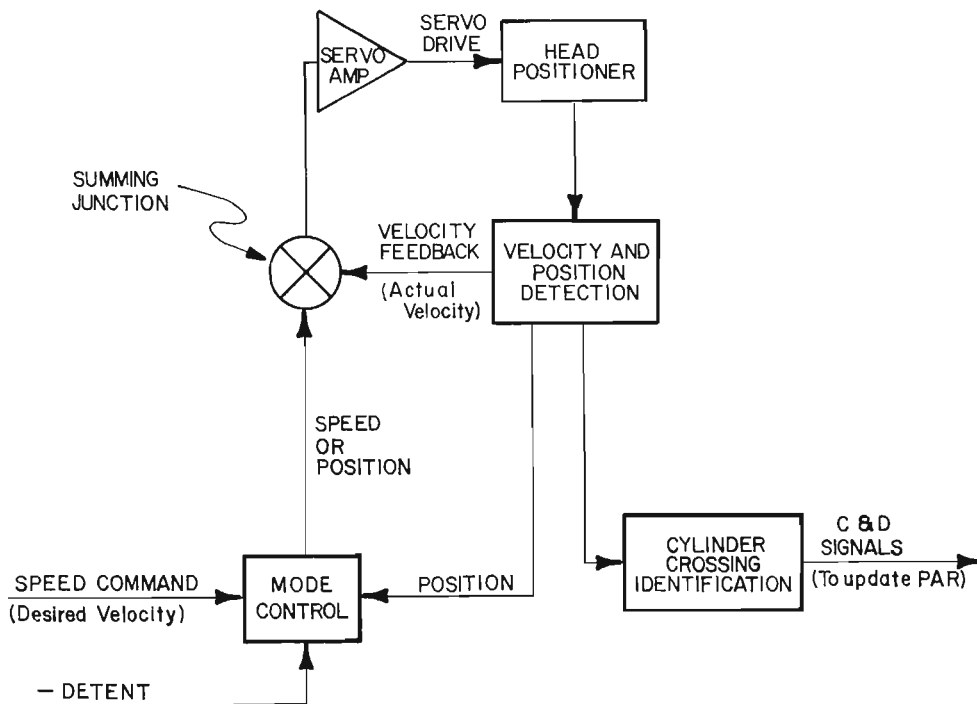


Figure 4-6. SERVO SYSTEM SIMPLIFIED BLOCK DIAGRAM

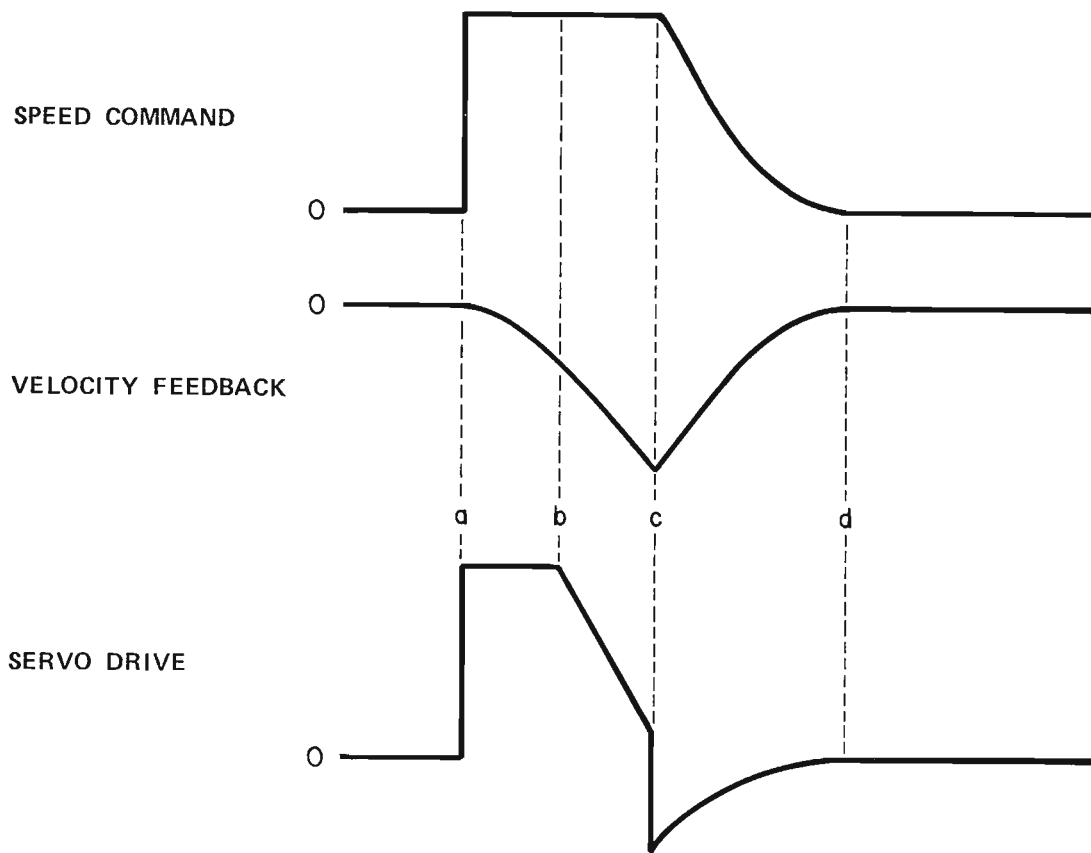
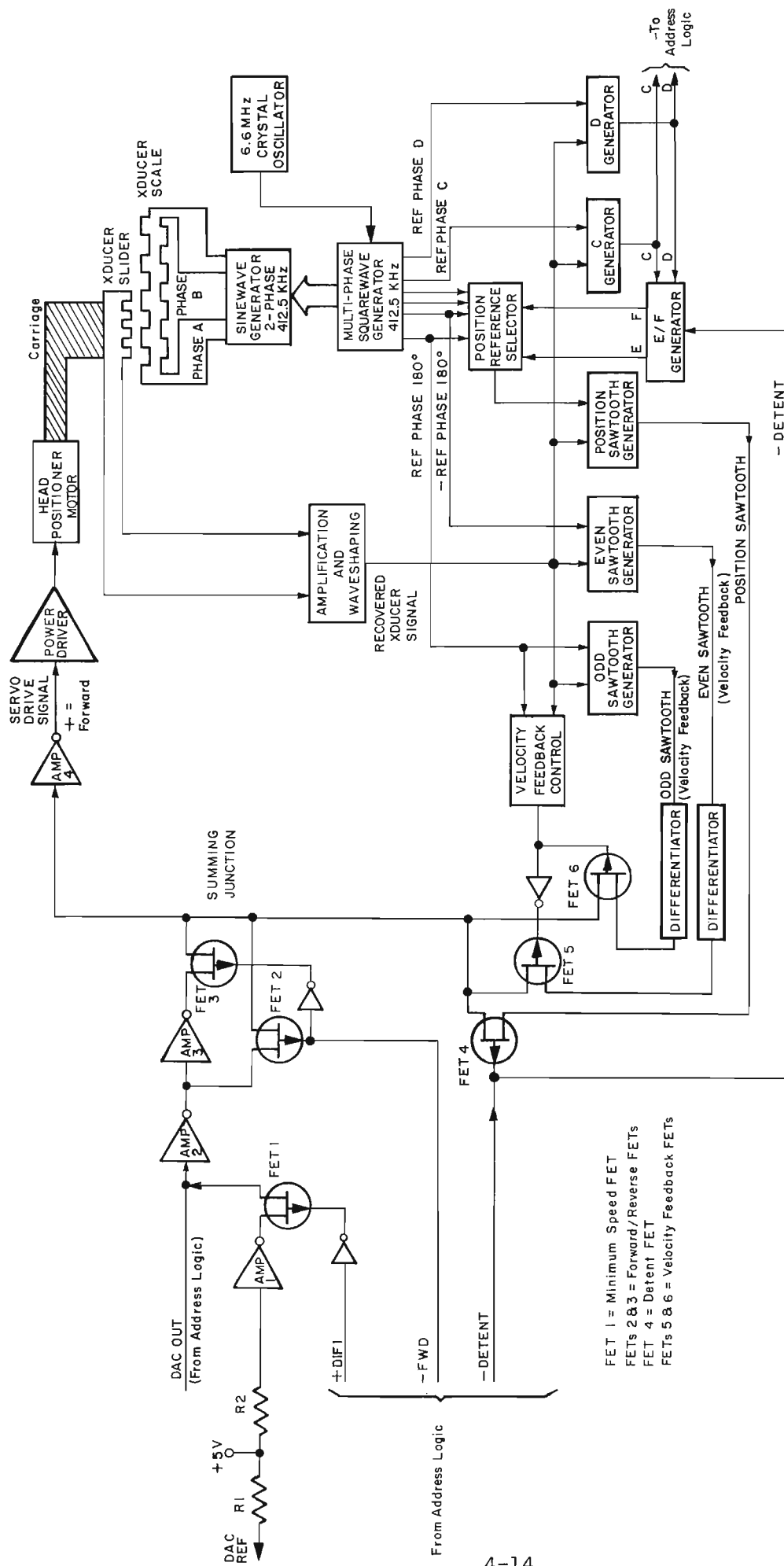


Figure 4-7. SERVO WAVEFORMS



FET 1 = Minimum Speed FET
 FETs 2 & 3 = Forward/Reverse FETs
 FET 4 = Detent FET
 FETs 5 & 6 = Velocity Feedback FETs

Figure 4-8. SERVO SYSTEM EXPANDED BLOCK DIAGRAM

Speed Command

The speed command from the Address Logic is received as signals +DIF 1 and DAC OUT. +DIF 1 is the minimum speed term of the digital speed code. This minimum speed increment is supplied by Amp 1 through FET 1 when +DIF 1 is HI. DAC OUT is an analog current signal whose magnitude is directly proportional to the distance the heads must move from present location to destination location. DAC OUT is at its maximum anytime the distance to go is 256 cylinders or greater. Below 256 cylinders, DAC OUT current gradually diminishes as the heads approach the destination cylinder. The current from the DAC drops to zero when the distance to go reaches one cylinder. Then, as the distance to go drops to zero, +DIF 1 goes LO and turns off the minimum speed increment through FET 1. The DAC REF output from resistor R1 is sent to the DAC as a reference current which establishes the scale factor for DAC output current.

Direction Control

When the -FWD signal is LO, FET 2 is on and FET 3 is off. During head positioning, this produces a (-) polarity at the summing junction, a (+) polarity SERVO DRIVE signal, and forward head motion. When -FWD is HI, FET 2 is off and FET 3 is on, resulting in (+) polarity at the summing junction, (-) polarity SERVO DRIVE, and reverse head motion.

Summing Junction

At the summing junction, the Speed Command input is received through FET 2 or FET 3, the Velocity Feedback is received through FET 5 and FET 6 alternately, and detent control is accomplished through FET 4. The summing junction current signal appears at the output of Amp 4 as the SERVO DRIVE signal.

Head Positioning Transducer

The servo system uses the output of an induction-type printed circuit transducer to develop head position and velocity information. It also decodes this transducer output into cylinder count pulses. These pulses are used by the Address Logic to increment or decrement the Present Address Register.

The two primary coils of this transducer consist of a pair of interleaved conductor patterns. These patterns are printed on an epoxy glass substrate which is bonded to the surface of an aluminum alloy plate. The plate is mounted along the carriage way facing the slider. This primary member of the transducer, referred to as the scale, is stationary. Figure 4-9 shows the location of the transducer components within the disk drive.

The transducer secondary coil also consists of a printed conductor pattern. This member of the transducer, called the slider, is located on the side of the head positioner carriage and moves with the carriage during head positioning. In Figure 4-8, the representation of the transducer scale and slider is a conceptual view only. It does not accurately depict the pattern of the transducer primary and secondary coils.

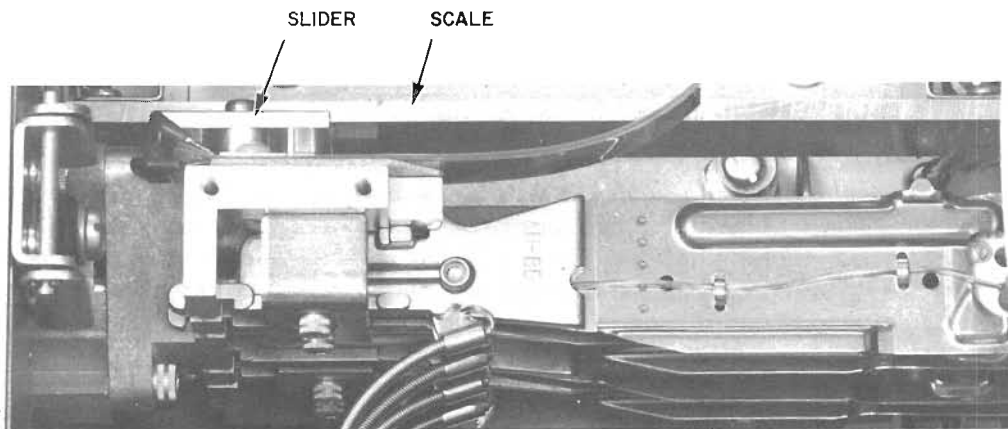


Figure 4-9. POSITION TRANSDUCER

The transducer primary coils are driven by two 412.5 KHz sinewaves, phase-separated by 90° . These two sinewaves are synthesized from selected outputs of a 412.5 KHz multi-phase squarewave generator. An actual waveform of these sinewaves is shown in Figure 4-22.

During head positioning, the motion of the slider with respect to the scale varies the degree of coupling between each of the primary coils and the secondary coil. The output from the secondary coil is a single variable-phase sinewave. This output sinewave undergoes a 360° phase shift during each 4-cylinder traversal by the heads. Figure 4-10 shows this phase shift in four stages as the heads travel a distance of four cylinders forward. During reverse head motion the transducer output signal would shift left instead of right.

The transducer output is amplified and shaped into a variable-phase squarewave identified as RECOVERED XDUCER SIGNAL.

Odd, Even and Position Sawtooth Generators

Figure 4-11 shows the output waveforms of the sawtooth generators during constant velocity head motion. These signals are a product of the phase relationship between the RECOVERED XDUCER SIGNAL and selected reference signals from the Multi-Phase Squarewave Generator. The waveforms shown in Figure 4-11 occur only during head motion, when the RECOVERED XDUCER SIGNAL is shifting phase. When the heads are stationary in the detented position, each of the signals shown in Figure 4-11 remains at a level which coincides with the track centers indicated on the waveforms.

The POSITION SAWTOOTH signal is used to hold the heads on-track during the detent mode. This signal is coupled to the summing junction through FET 4. The detented position, and thus the track center, occurs at the 0 volt potential of the POSITION SAWTOOTH signal. If the heads drift away from track center, the POSITION SAWTOOTH shifts to a polarity which forces the heads back to track center.

The Position Reference Selector sequentially selects four different signals from the Multi-Phase Squarewave Generator and applies them to the Position Sawtooth Generator for phase comparison with the RECOVERED XDUCER SIGNAL. This allows generation of a POSITION SAWTOOTH signal that has a repetition rate equal to the cylinder traversal rate of the head positioner.

The ODD AND EVEN SAWTOOTH signals are used alternately during head positioning to provide velocity feedback to the summing junction. These signals are differentiated and applied to FET 5 and FET 6. The Velocity Feedback Control circuit switches FET 5 and FET 6 on and off alternately to select only the center portion of each sawtooth slope for feedback. This avoids feedback of the sawtooth retrace which is a polarity shift opposite to that desired. Figure 4-11 points out the portion of the ODD AND EVEN SAWTOOTH signals selected for feedback.

C and D Generators

The C and D waveforms shown in Figure 4-11 are produced during head positioning at a rate of one cycle for every four cylinders traversed by the heads. C and D are sent to the Address Logic to generate count pulses for updating the Present Address Register each time a cylinder is crossed.

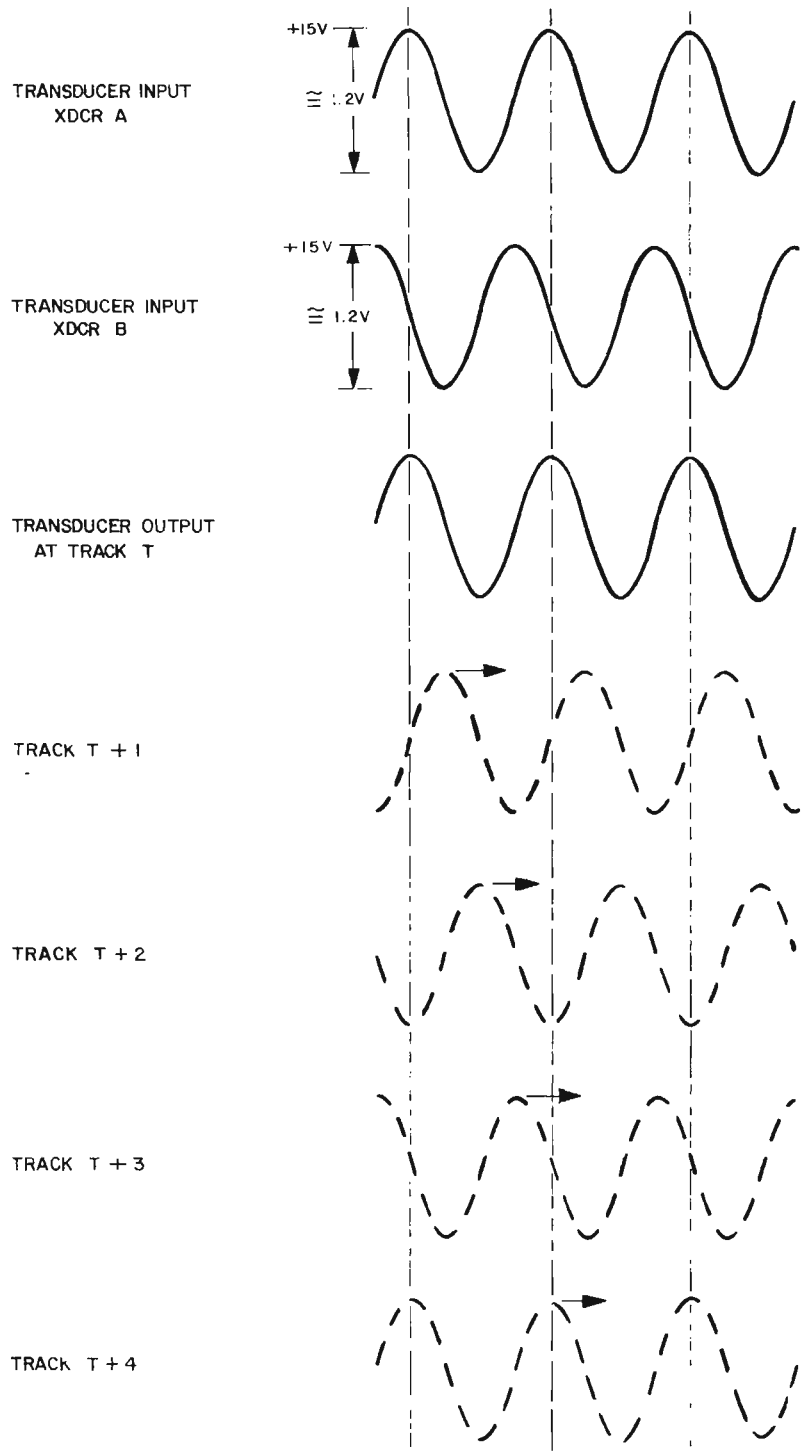
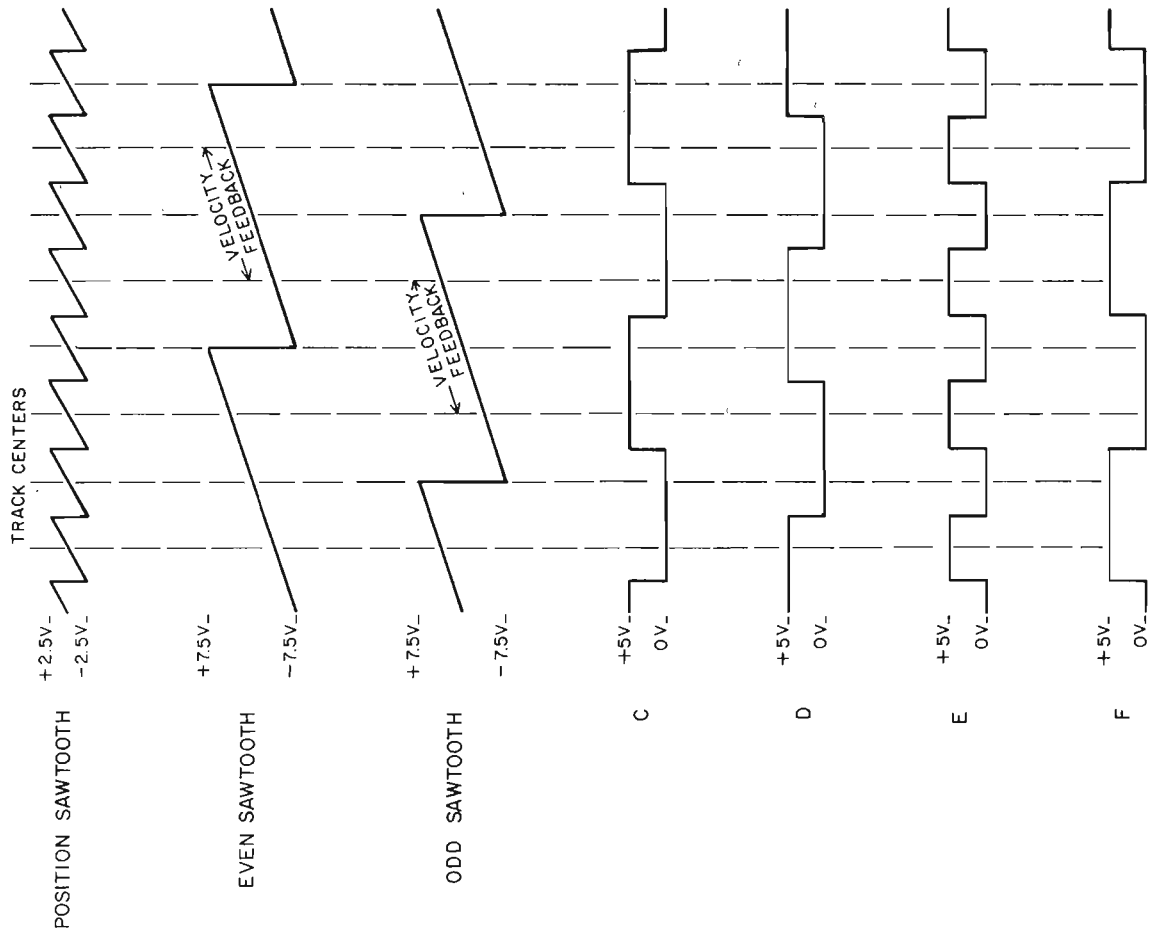


Figure 4-10. TRANSDUCER OUTPUT PHASE SHIFT

FORWARD MOTION — CONSTANT VELOCITY



REVERSE MOTION — CONSTANT VELOCITY

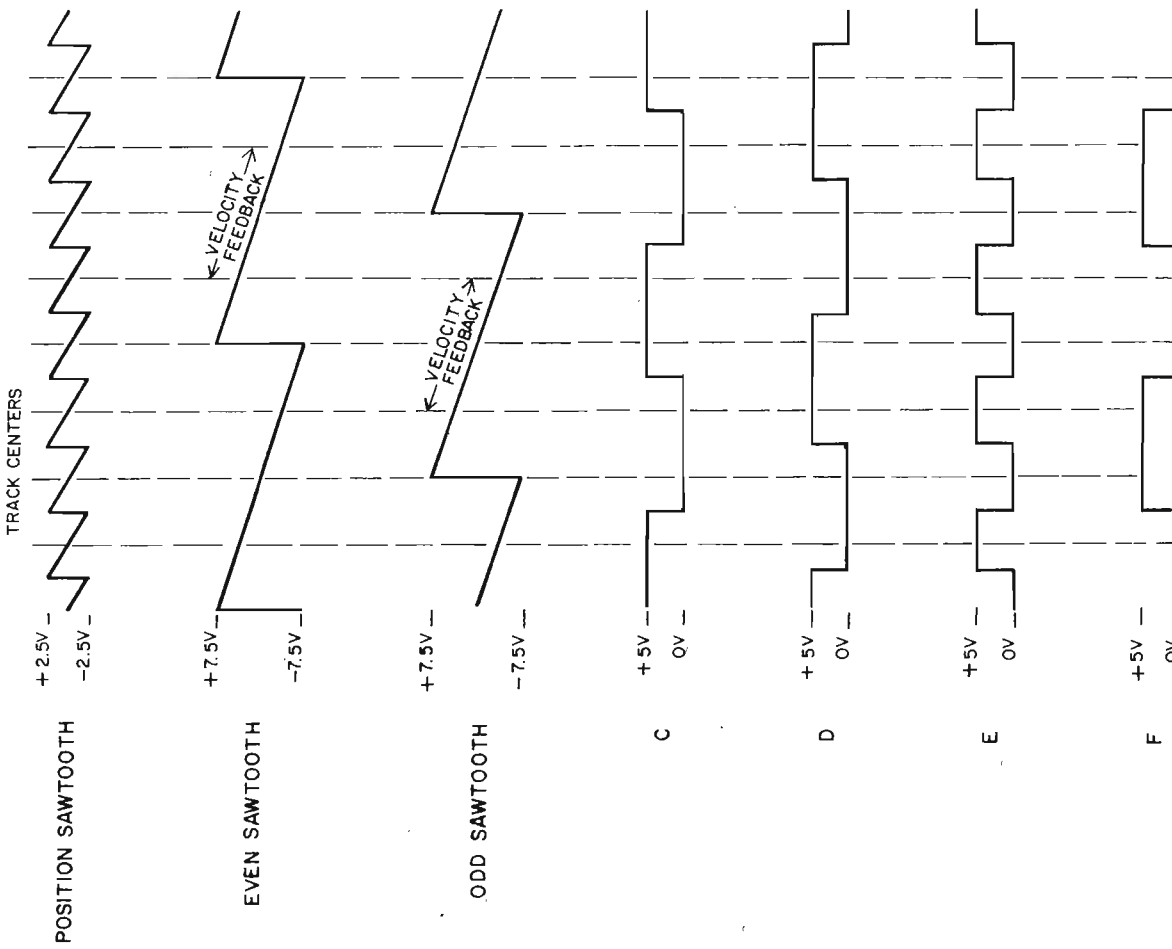


Figure 4-11. VELOCITY AND POSITION WAVEFORMS

A count pulse is produced by the Address Logic at each HI to LO or LO to HI transition of either C or D. During reverse head motion, the D signal leads C by 90°; during forward motion, C leads D by 90°.

E/F Generator

Signals C and D are also sent to the E/F Generator as a timing reference. The E and F signals form a 2-bit binary counter which is used to control the Position Reference Selector. The -DETENT signal disables the E/F Generator during the detent mode.

4.2.5.2 Temperature Compensation

As the operating temperature within the disk drive varies from cool to warm, the recording disks expand slightly. To maintain accurate head-to-track alignment, the Position Transducer Scale is physically linked to the aluminum dust plate which separates the fixed disk and the cartridge. This plate is mounted at only a single point on each side, leaving it free to shift parallel to the head positioner axis during expansion and contraction of the plate. As the recording disks and aluminum plate expand during heating, the transducer scale is shifted outward slightly. As the disks and plate cool, the transducer scale is shifted inward slightly.

4.2.6 Index/Sector Information Control

The hub of each disk contains an index slot which is sensed by a stationary transducer as the slot passes the transducer. The index mark outputs of the transducers, therefore, occur once per disk revolution. The frequency of the lower disk index mark is used by the speed control logic to determine when the spindle has reached proper speed, and to maintain it within +0.2% of that speed. The index mark of the selected disk is also furnished to the controller interface.

In addition to the index slot, the 5440 disk cartridge is also available with equally spaced sector slots cut around the periphery of the disk hub. The more common numbers of sector slots available are 8, 12, 16, 20 or 24. The fixed disk has 24 sector slots in addition to the index slot. The sector slots divide each track into a number of equal segments for disk formatting purposes, as described in Section 3.

The sector slots are sensed by the index transducers, and the resulting sector marks are electronically separated from the index marks. Two separate sector counters count the sector marks from the upper and lower disks during each disk revolution. The 5-bit binary coded output from each sector counter indicates which sector is currently passing under the R/W heads.

The sector marks and sector count for the selected disk are furnished to the controller interface. The sectors for an 8-sector disk are shown in Figure 4-12. For clarity, only one track is shown, with its width greatly exaggerated.

4.2.7 Data Transfer Functions

Figure 4-13 shows a functional block diagram of the Data Transfer PCB.

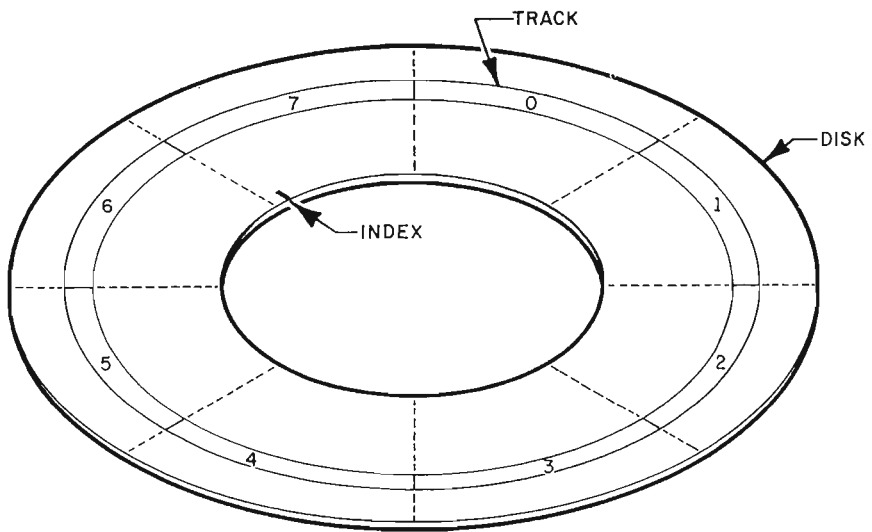


Figure 4-12. DISK SECTOR LAYOUT

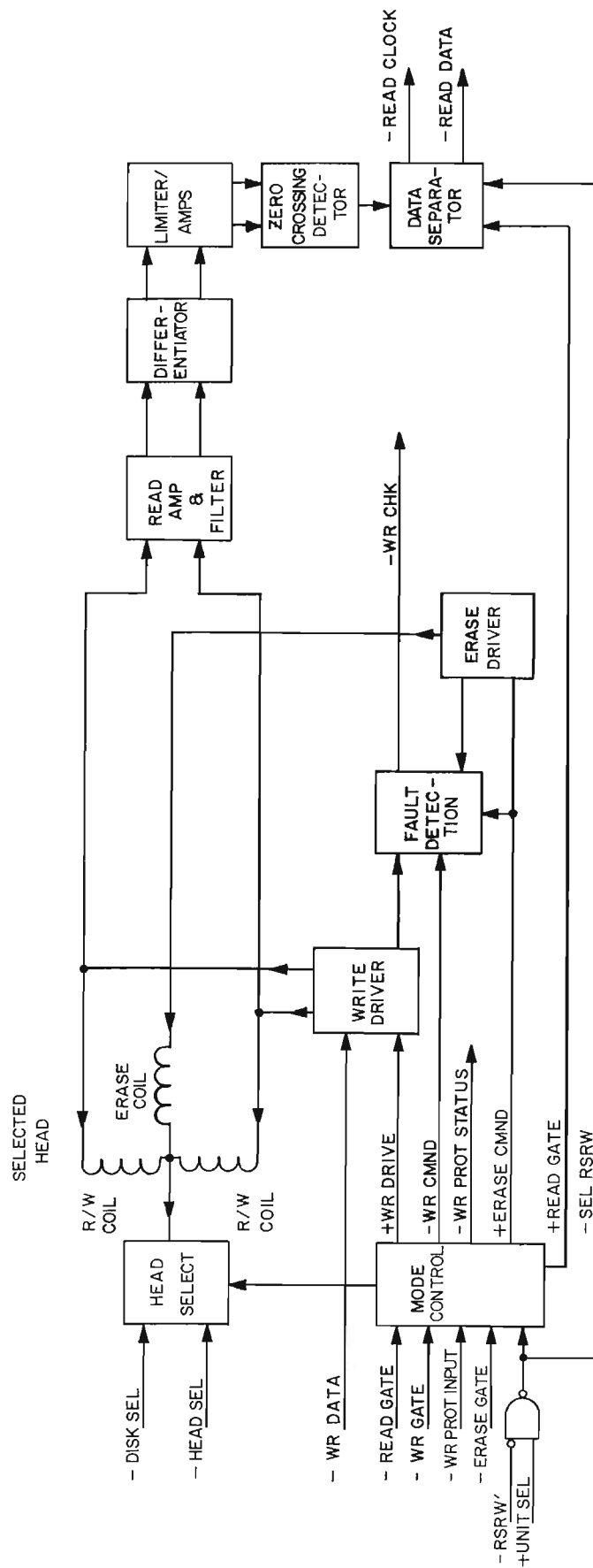


Figure 4-13. DATA TRANSFER FUNCTIONAL BLOCK DIAGRAM

The two primary functions of the Data Transfer System are writing data onto the recording disk and reading data from the disk. The read function is activated by a read command (-READ GATE) from the controller. The write function is activated by a write command (-WRITE GATE) from the controller, but is qualified further by the Write Protect feature.

4.2.7.1 Write Protect

When active, the Write Protect feature inhibits R/W head selection to prevent writing on the disk even if the controller transmits data and -WRITE GATE.

The elements associated with the Write Protect feature are described below.

Internal Write Protect Switches - Two switches mounted on the Data Transfer PCB; one for the upper disk and one for the lower disk. By means of these switches, the Write Protect feature may be totally disabled for either or both disks.

External Write Protect Switch - Illuminated pushbutton switch on front panel. This switch allows the operator to deactivate the Write Protect feature for both disks.

WRITE PROTECT INPUT - from controller. A LO pulse on this line activates the Write Protect feature for either or both disks, in accordance with the settings of the internal write protect switches.

LOAD/RUN Switch - on front panel. By cycling this switch (RUN to LOAD to RUN), the operator can reactivate the Write Protect feature, in accordance with the settings of the internal switches.

Write Protect Indicator - on front panel. This indicator is unlit whenever both disks are not write protected.

4.2.7.2 Read/Write Heads

Figure 4-14 shows the electrical configuration of the read/write and erase coils, and also the physical orientation of the read/write and erase poles in the head assembly. The erase poles are positioned to follow the read/write gap. Erase current is turned on during a write operation to trim the edges of the written track.

4.2.7.3 Head Select

Head selection is performed by the -DISK SELECT and -HEAD SELECT signals according to the codes listed below.

<u>-DISK SELECT</u>	<u>-HEAD SELECT</u>	<u>HEAD SELECTED</u>
LO	LO	(Ø) Top Head, Top Disk
LO	HI	(1) Bottom Head, Top Disk
HI	LO	(2) Top Head, Bottom Disk
HI	HI	(3) Bottom Head, Bottom Disk

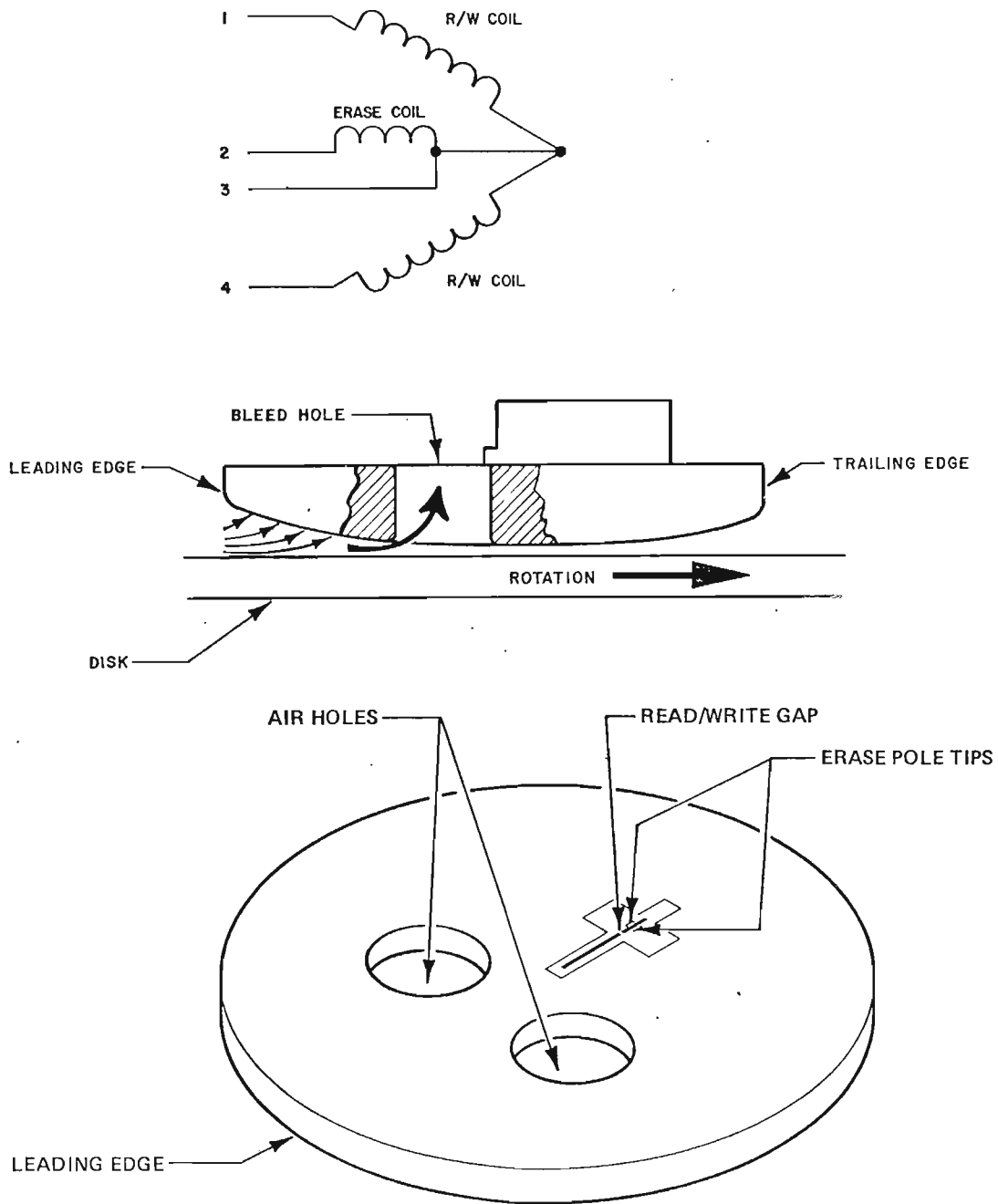


Figure 4-14. READ/WRITE HEADS

Head selection is further controlled by the Mode Control circuitry. If the Write Protect feature is inactive, head selection is enabled whenever the signal -RSRW (-Read to Seek/Read/Write) is LO. If the Write Protect feature is active, head selection is enabled only when -RSRW and -READ GATE are both LO.

4.2.7.4 Mode Control

The Mode Control circuitry receives read, write, erase and protect signals from the controller, and controls the associated circuits accordingly.

4.2.7.5 Write Driver

When enabled by the +WRITE DRIVE signal from Mode Control, the Write Driver accepts information from the controller on the -WRITE DATA interface line. This information consists of multiplexed clock and data pulses; a system known as double frequency recording. Refer to Section 3.5 for a description of double frequency recording.

The Write Driver alternately passes current first thru one R/W coil and then the other, switching coils for each new pulse received. As a result, each pulse produces a head current reversal which is recorded on the disk as a flux transition.

When the +ERASE CMND from Mode Control is HI, the Erase Driver passes current through the erase coil.

4.2.7.6 Read Channel

During a read operation, the R/W coils sense the flux transitions representing recorded clock and data pulses. The retrieved pulses are amplified and then filtered to eliminate high frequency noise.

The Differentiator then converts the peaks of the signals into zero crossings. Further amplification, and limiting, results in a rectangular waveform with edges representing the peaks of the original analog head signal.

The rectangular waveform is applied to a Zero-Crossing Detector which produces a 100 ns output pulse for each edge of the rectangular waveform.

The Data Separator then separates clock and data pulses and puts them onto the -READ DATA and -READ CLOCK interface lines.

4.2.7.7 Data/Clock Separation

4.2.7.7.1 Single-Shot Separator

The standard single-shot data/clock separator may be used with sector mark format but not with address mark format. With the single-shot separator, each clock pulse received from the disk is passed out to the +READ CLOCK line after initiating a data "window". A subsequent data pulse

occurring within this window will be passed out to the +READ DATA line. The data window then terminates prior to receipt of the next clock pulse.

4.2.7.7.2 VFO Separator Option

The optional VFO separator may be used with either sector mark format or address mark format. The VFO separator provides the following features:

- Generates a clock signal that is synchronized with the read data.
- Removes most of the jitter caused by pulse crowding and spindle speed variations.
- Provides closer timing tolerances than the standard single-shot separator.
- Provides missing clock bits for single sector (address mark) format systems.

The VFO separator consists of a phase-locked loop and a data separator. The phase-locked loop provides a stable clock signal which is used to generate a data gate. The data pulse is aligned within this gate.

When -READ GATE goes LO, a 1 usec general reset pulse initializes the VFO separator. The VFO separator is then activated by the first data or clock pulse received from the disk. With continued receipt of data from the disk, the VFO will achieve phase-lock and frequency correction within 20 usec. When phase-lock is first achieved, the data separator may be phased incorrectly, since it cannot distinguish a data bit from a clock bit. To ensure correct phasing, a Zeros Detector circuit looks for a pattern of eight consecutive zeros. Receipt of these zeros from anyplace in the format enables the data separator to determine if it is phased properly, and to reverse its phasing if necessary. As soon as the phasing has been verified, data is gated out to the controller.

It should be noted that when the address mark appears on the interface, the missing clocks will have been filled in by the VFO separator.

4.2.7.8 Fault Detection

The fault detection circuitry is designed to detect the faults listed below. Having detected a fault, this circuitry puts a LO on the -WRITE CHECK interface line, turns on the WRITE CHECK indicator light, turns out the READY indicator light, and deselects all heads.

Fault Conditions:

- Write current without -WRITE GATE = LO.
- No write current with -WRITE GATE = LO.
- Erase current without +ERASE CMND = HI.
- No erase current with +ERASE CMND = HI.
- Multiple head selection.
- Open R/W head coil.

4.3 CIRCUIT DESCRIPTIONS

4.3.1 Input/Output (I/O) PCB (#12025)

Refer to Figure 7-2, I/O PCB Schematic.

The I/O PCB holds the two parallel connected I/O connectors. The Read Clock and Read Data output drivers are located on the I/O PCB to avoid switching relatively high currents on the Data Transfer PCB.

+5V is supplied to the I/O connectors for use by the Terminator. An isolation diode (D1) decouples the internal +5V from the +5V lines of other drives in a daisy-chain system.

4.3.2 Address Logic (A/L) PCB (#12064)

The Address Logic PCB contains the circuits that perform the following functions:

- (1) Hold the present cylinder address in the Present Address Register (PAR).
- (2) Hold the new address from the controller in the New Address Register (NAR).
- (3) Detect invalid new addresses.
- (4) Provide to the head positioner servo an analog current output signal proportional to the distance to go to the new address location.
- (5) Detect when head motion stops, and then issue the RSRW (Ready to Seek, Read or Write) signal or SEEK INCOMPLETE signal.
- (6) Specify direction heads are to move during a seek operation.
- (7) Decode the Unit Select and Attention lines.
- (8) Provide interface buffering for seek control and status lines.

4.3.2.1 New Address Register (NAR)

Refer to Figure 7-3, Address Logic Schematic (Sheet 1).

The NAR consists of nine D-type flip-flops (N40, N50 and D50-5/6). The data inputs to the NAR are controlled by two data selectors (H40 and H50) and a set of input gates.

The NAR input gates are controlled by the +SEL (Select) signal in conjunction with -CAL (Calibrate). When +SEL and -CAL are both HI, the new cylinder address is gated through the input gates to the data selector inputs.

Data selector control is provided by switch SW1 (M75). For 200 tpi operation, the "select" inputs of the data selectors are held HI by switch SW1 being open. This conditions the data selectors to pass their "B" inputs to the NAR. Consequently, the 2-bit goes to NAR input N50-4 and the 256-bit to N40-13. The 1-bit goes directly from input gate K20-14 to FF input D50-2.

For 100 tpi operation, the "select" inputs of the data selectors are held LO by switch SW-1 being closed. This conditions the data selectors to pass their "A" inputs to the NAR. Consequently, the 1-bit goes to NAR input N50-4 and the 128-bit goes to input N40-13. FF D50-5/6 is held set by the LO at D50-4.

The new address is clocked into the NAR 400 nanoseconds after the leading edge of the STROBE pulse from the controller. See Para. 4.3.2.4 for STROBE utilization.

When a Restore command occurs, -CAL goes LO. This simultaneously disables the NAR input gates and raises the output of gate P30-3. As the gate output goes HI the NAR clears to zero.

The six highest bits of the new address are sensed and encoded to detect invalid addresses (addresses greater than 407 in 200 tpi units, and greater than 203 in 100 tpi units). The resultant signal, \rightarrow 407(203), is routed to the Strobe logic, where it enables ADRS ACK (Address Acknowledge) if the address is valid, or LAI (Logical Address Interlock) if the address is invalid. When an invalid address is detected, no NAR clock pulse occurs; consequently, the NAR retains the last valid address.

The RAMP signal is ORed with the bit 8 output of the NAR to provide head positioner velocity control during loading and unloading of the heads. The combination of the bit 8 provided by RAMP plus the DIF 1 speed signal produces a speed command of 9.

The HI RAMP signal also appears to the input of the Full Adder as a new address value of 8, consequently, the head positioner proceeds out to cylinder 8. At cylinder 8 the Ramp FF becomes reset, and since the NAR is holding zeros, a seek to track 0 occurs immediately. See Para. 4.3.2.5 for RAMP signal control.

4.3.2.2 Present Address Register (PAR) and Count Control Logic

Refer to Figure 7-3, Address Logic Schematic (Sheet 1).

The PAR is a 10-bit up/down counter, implemented with cascaded synchronous up/down counters H60, F60 and D60. H60 and F60 hold the lower eight bits of the cylinder address. The ninth and tenth bits are held by D60. Although no valid address utilizes the tenth bit, which has a weight of 512, this bit is summed with a fixed "one" bit in the full adder. This is done to eliminate the possibility of an extra count pulse (due to an overshoot past track zero) from creating a maximum value servo error signal which would force the head positioner to retract at full velocity into the rear end stop.

The count pulses and up/down control signal are decoded from two signals entitled "C" and "D" supplied by the Servo PCB. C and D are derived from the recovered transducer signal which indicates head-to-track positional relationship. Signals C and D each make one complete cycle for every four tracks crossed

by the R/W heads. The count pulses are supplied to the counter through gate E60-8; the UP/DOWN control signal is supplied through gate E60-3.

Refer to Figure 4-15. When the heads are moving forward, the C signal leads the D signal by 90° ; when the heads are moving in reverse, the C signal lags the D signal by 90° . Each transition of C and D generates a count pulse which increments or decrements the PAR.

NOTE: The PAR holds the present address in one's complement form. This allows a difference value to be obtained when the contents of the PAR and NAR are summed in the full adder.

When the head positioner is moving forward, the Up/Down control line is HI as each count pulse occurs, causing the PAR to be decremented by one count for each count pulse. Conversely, when the head positioner is moving in reverse, the Up/Down control line is LO when each count pulse occurs, causing the PAR to be incremented by one count for each count pulse.

The L (Load) input of the PAR is controlled by the -CAL signal. -CAL goes LO during a restore operation or during a retract condition. When -CAL goes LO, the lower nine bit positions of the PAR are loaded with ones through the parallel load inputs (A,B,C and D) of the Present Address Register. With -CAL holding the Load input LO, the PAR Count input (D/U) is disabled. -CAL goes HI at the end of the restore operation or retract condition, thereby enabling the PAR Count input.

The PAR operates the same for 200 tpi and 100 tpi.

4.3.2.3 Servo Speed Control Logic

Refer to Figure 7-3, Address Logic Schematic (Sheet 1).

The Servo Speed Control Logic utilizes a Full Adder, Exclusive-OR Gates, Detent Detection Gates, Speed Code Gates and a Digital-To-Analog Converter (DAC). The three primary functions of these circuits are:

- (1) to produce a speed control current signal (DAC OUT) of variable magnitude proportional to the distance the head positioner must move from the present address to the destination address.
- (2) to provide a signal (-CARRY) which indicates the required direction of head travel.
- (3) to generate a detent signal (-DETENT) which will hold the heads on-track when they arrive at the destination address.

Full Adder

The Full Adder performs the summation of the contents of the NAR and the PAR. Since the PAR holds the one's complement of the present address, the output of the Full Adder represents the number of tracks of difference between the present address and the new address. This is entitled the "distance-to-go".

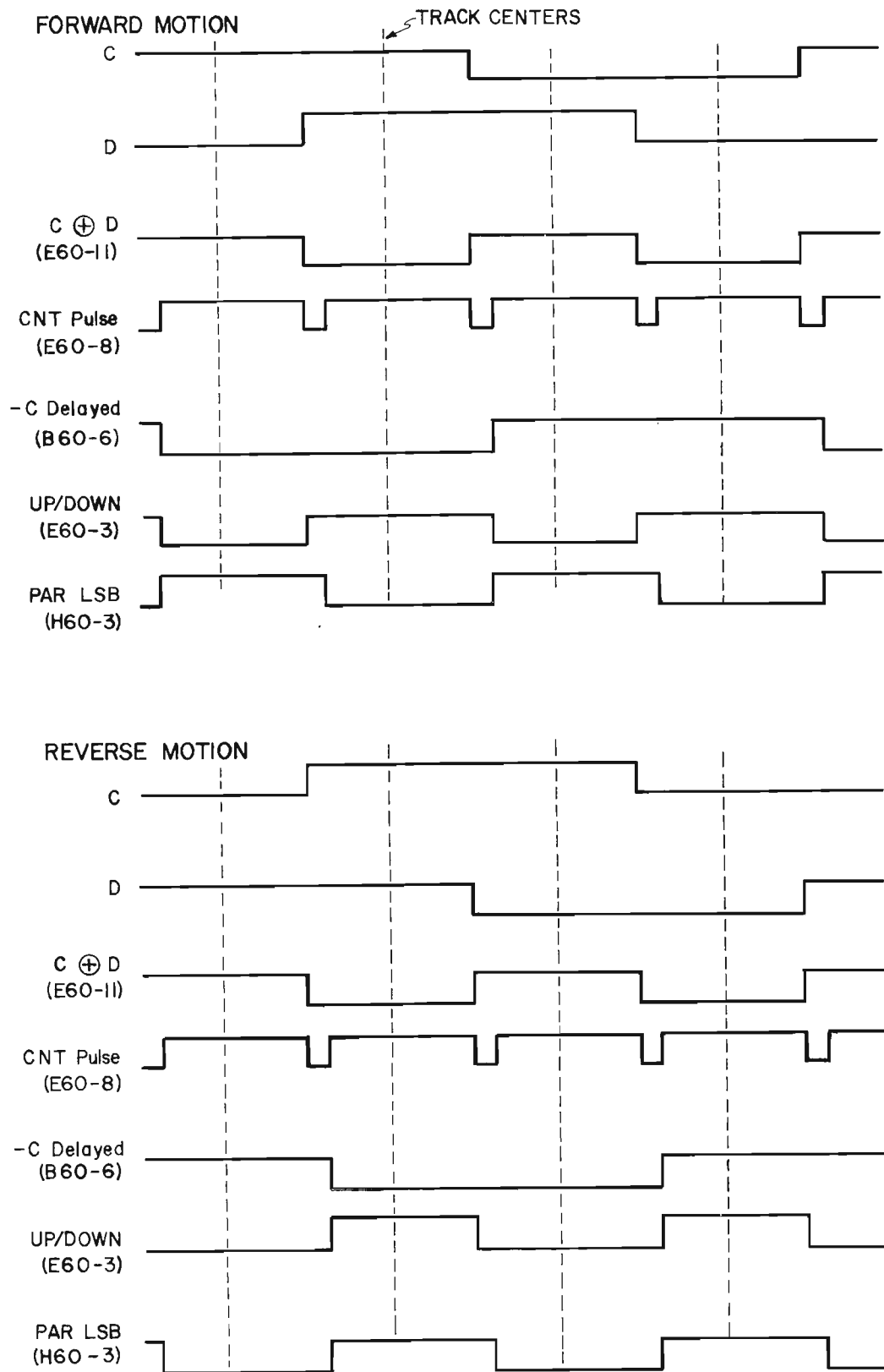


Figure 4-15. COUNT CONTROL WAVEFORMS

As shown by the examples in Figure 4-16, a carry out of the Full Adder occurs only when forward head travel is required to reach the new address. A carry sets Carry FF, D50-9/8. One output of the Carry FF is applied to the carry input of the Full Adder as an end-around carry to complete the summation. This output of the Carry FF is also used to control the X-OR Gates, as described later. The other output of the Carry FF is supplied to the direction control logic as the signal -CARRY. When forward head travel is required, -CARRY will be LO; when reverse head travel is required, -CARRY will be HI.

X-OR Gates

The function of the X-OR (Exclusive-OR) Gates is to ensure that the binary speed code signals to the DAC are in true form rather than complemented form. This is accomplished by inverting the output signals from the Full Adder if necessary. Figure 4-16 shows that for a forward seek, the distance-to-go code out of the Full Adder is in true form. However, since the distance-to-go signals always undergo an inversion in the Speed Code Gates, for a forward seek they must also be inverted by the X-OR Gates so they will be back in true form when they reach the inputs of the DAC.

For a reverse seek, the Full Adder outputs are in complemented form, so an inversion by the Speed Code Gates will put them in true form. Consequently, no inversion by the X-OR Gates is required.

The Carry FF controls the X-OR Gates. When a reverse seek is required, no carry occurs and the exclusive-OR function performs no inversion. However, when a forward seek is required, a carry occurs and causes the X-OR Gates to invert the distance-to-go signals.

Detent Detection Gates

The Detent Detection Gates sense the distance-to-go lines and encode an output signal entitled -DETENT. If any one of the lines being sensed is LO, the heads have not yet reached the new address. In this case, the -DETENT signal is HI. When the heads reach the new address, all of the sensed lines are HI and -DETENT goes LO. This puts the servo into its detent mode to hold the heads on-track.

-DETENT is also controlled by -CAL at gate input B40-3. This allows -CAL to interrupt the detent mode for a restore or retract operation.

Speed Code Gates And DAC

The nine distance-to-go lines from the X-OR Gates are reduced to eight speed code lines by the Speed Code Gates. Lines 2 thru 8 are applied to the DAC, while the minimum speed signal, +DIF 1, is routed to the Servo PCB separately to allow more precise control of the lowest speed increment. The corresponding unused DAC input, A8, is grounded. +DIF 1 is also activated by -CAL for a restore or retract operation.

The lower eight distance-to-go lines are each applied to a separate Speed Code Gate. The ninth, and highest, distance-to-go signal is applied to all of the Speed Code Gates. As a result, any time the highest distance-to-go line (256 for 200 tpi; 128 for 100 tpi) is active, all of the speed code signals will be active, providing maximum DAC current output. After the remaining distance to go drops below 255 tracks (127 for 100 tpi), each succeeding track that

EXAMPLE 1. FORWARD SEEK

			carry	512	256	-	-	-	-	-	-	-	-	1	=	
PAR		0	1	1	1	1	1	1	1	1	1	1	1	1	=	∅
NAR		1	0	0	1	1	0	0	1	0	0				=	1∅∅
Full Add out	1	x	0	0	1	1	0	0	1	0	0			=	1∅∅ (with end-around carry added)	
X-OR out			1	1	0	0	1	1	0	1	1			=	-1∅∅ (first inversion)	
DAC in			0	0	1	1	0	0	1	0	0			=	1∅∅ (second inversion)	

EXAMPLE 2. REVERSE SEEK

			carry	512	256	-	-	-	-	-	-	-	1	=	
PAR		0	1	1	0	0	1	1	0	1	1			=	1∅∅
NAR		1	0	0	0	1	1	0	0	1	0			=	5∅
Full Add out	x	1	1	1	0	0	1	1	0	1			=	-5∅ (no carry)	
X-OR out			1	1	1	0	0	1	1	0	1		=	-5∅	
DAC in			0	0	0	1	1	0	0	1	0		=	5∅	

Figure 4-16. DISTANCE-TO-GO EXAMPLES



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is crossed diminishes the speed code by a value of one. A corresponding reduction in DAC output current occurs at every other track crossing, while +DIF 1 switches at every track crossing. The DAC output provides a current source output (DAC OUT) of 127 discrete current increments proportional to the digital input value. Figure 4-17 shows a simplified DAC OUT current waveform during a long seek. The minimum output current from the DAC is .0156 MA and the maximum is 1.944 MA.

The DAC REF input signal is a reference current which establishes the minimum-to-maximum current range of the DAC.

4.3.2.4 Strobe Logic

In response to a Strobe pulse from the controller, the Strobe logic develops various signals to initiate operations within the Disk Drive, and to provide status signals back to the controller.

Refer to Figure 7-4, Address Logic Schematic (Sheet 2).

When +RSRW is HI and the drive is selected, a -STROBE pulse from the controller will raise the input of one-shot A30-5/6. This one-shot delays the strobe pulse by 400 nanoseconds. At the rise of input A30-10, output A30-12 of the one-shot goes LO for 400 nanoseconds. As output A30-12 goes HI at the end of the 400 nanoseconds, it triggers the second one-shot, A30-13/4. This one-shot produces a 2.1 microsecond HI pulse at output A30-13 and LO pulse at output A30-4.

If the new cylinder address is valid, the HI pulse passes through AND gate B20-11 and produces an -ADRS ACK (Address Acknowledge) pulse. The -ADRS ACK pulse is transmitted back to the controller, and also clocks the new address into the New Address Register. Also in the case of a valid address, when the pulse out of A30-13 clocks LAI FF B30-9/8, the FF sets, or remains set, because its B30-12 input is HI. The LO pulse at one-shot output A30-4 generates an -ATTN pulse through gate F30-6.

If an invalid address appears on the new address input lines, signal ->407 (203) goes LO. This inhibits gate B20-11, preventing an -ADRS ACK pulse, and causes the LAI FF to reset when clocked by the pulse from A30-13. The LO at FF output B30-9 produces an -ATTN signal back to the controller. Simultaneously, the HI at FF output B30-8 produces a LO on the -LAI interface output line. The -LAI condition terminates when the controller transmits a valid address which sets the LAI FF back to its normal state with B30-9 HI.

The -RESTORE signal is provided a separate input to the Strobe logic to allow a restore operation to be initiated even if an abnormal condition within the drive is preventing the Ready to Seek, Read, or Write (RSRW) condition from becoming true.

4.3.2.5 Direction Control, Calibrate And RAMP Logic

Direction Control and Calibrate

The -FWD signal controls direction of head positioner motion. The -CAL signal "calibrates" the Disk Drive by setting the NAR to zeros, the PAR to ones,

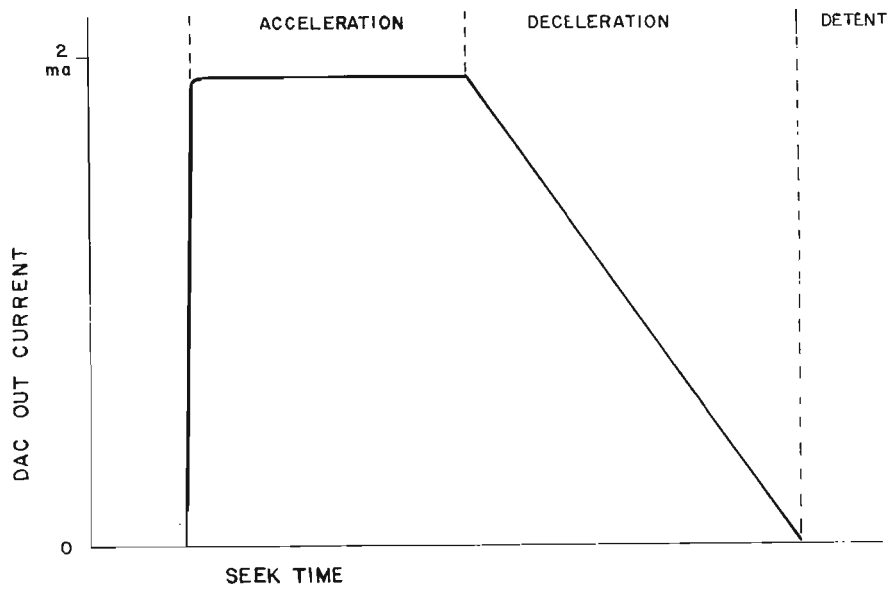


Figure 4-17. DAC OUTPUT CURRENT

and activating +DIF 1 to move the heads to the track 0 or retract position.

Three different situations affect the -FWD and -CAL signals for direction control and calibration:

- 1) For normal seek operations, -FWD is controlled by -CARRY, and -CAL is HI.
- 2) For a retract operation, -RETRACT forces -FWD to go HI (reverse) and -CAL to go LO.
- 3) For a restore operation, the "Calibrate" Latch sets, forcing -CAL to go LO, and allowing direction to be controlled by the OVER TRKS ("heads over tracks") signal.

Refer to Figure 7-4, Address Logic Schematic (Sheet 2).

During normal seek operations, the Calibrate FF, D30-9/8, is reset, and gate inputs D20-9, 11 are HI. Gate input D20-10 is controlled, through gate A40-11, by -CARRY. When -CARRY is LO, -FWD will be LO (forward); and when -CARRY is HI, -FWD will be HI (reverse).

During a retract operation, -RETRACT forces -CAL LO through gate input B20-10, and forces -FWD HI through gate input D20-11.

When a restore operation is initiated, or when -RETRACT goes HI, the Calibrate FF sets. A restore command will set the FF only if -RESTORE is LO, -RETRACT is HI, and a -STROBE pulse occurs.

Two cascaded FF's (H20-5/6, H20-9/8) are used to generate a set pulse for the Calibrate FF when -RETRACT goes HI. Both of these FF's are clocked by the 412.5 KHZ clock. When -RETRACT goes HI, the first positive-going clock transition sets FF H20-5/6. This raises input H20-12 of the second FF so that it becomes set on the next clock pulse. During the single clock period interval between the setting of the first FF and second FF, the two HI inputs to gate K50-8 produce a LO pulse output which serves to set the Calibrate FF.

The Calibrate FF resets on the rising edge of the +OVER TRKS signal. In the case of the Calibrate FF having been set by -RETRACT going HI, the heads are moving out over the disk from the retracted position. When the heads reach the point where +OVER TRKS goes HI, the Calibrate FF resets.

In the case of a restore operation having set the Calibrate FF, +OVER TRKS was already HI and the heads are in reverse motion. The heads continue moving away from the center of the disk until +OVER TRKS goes LO. (See Figure 4-18). At that point, head motion switches to forward and immediately the +OVER TRKS signal goes HI again. This LO to HI transition of +OVER TRKS resets the Calibrate FF and terminates head positioner drive.

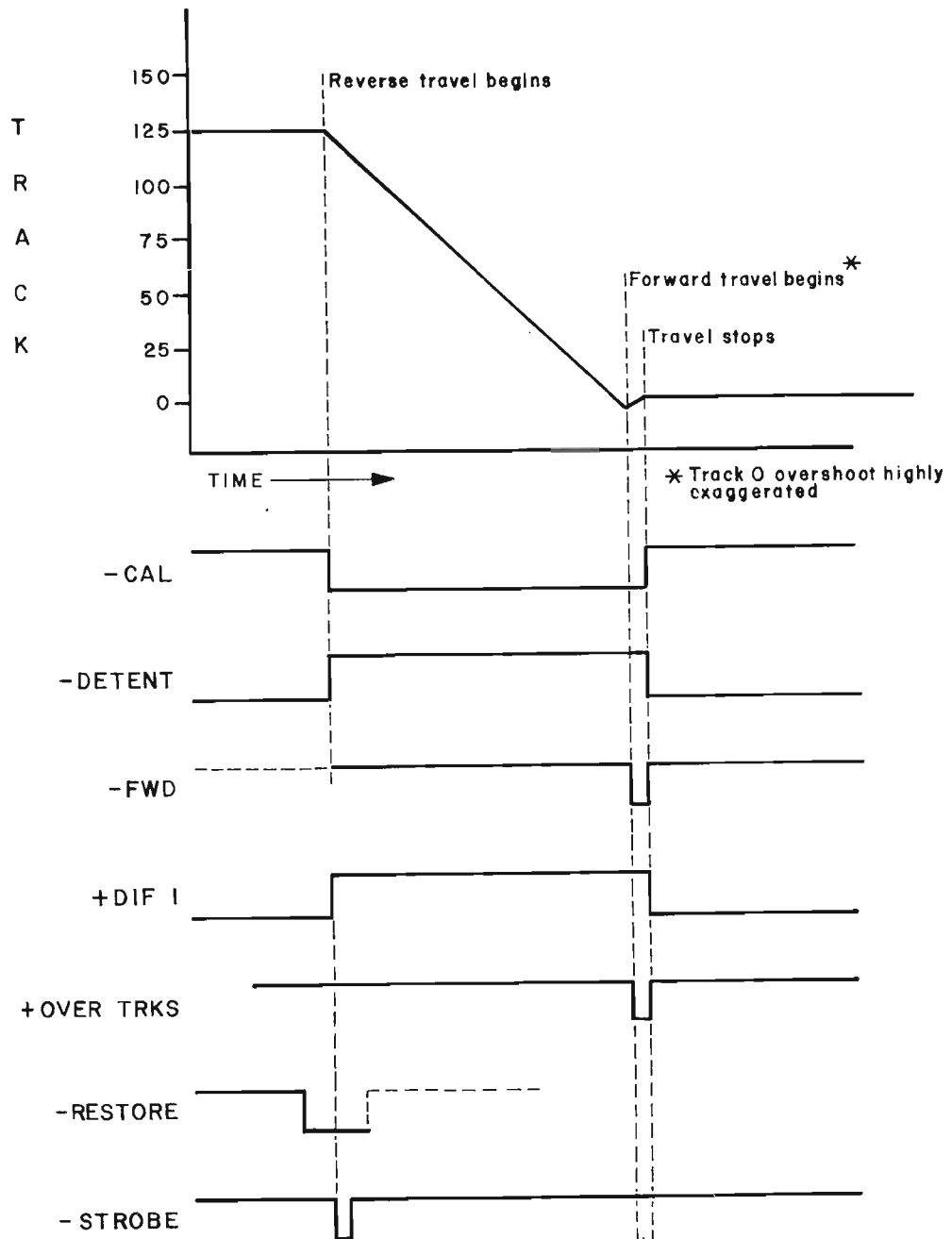


Figure 4-18. RESTORE FROM CYLINDER 125

RAMP Logic

The purpose of the RAMP signal is to provide an adequate speed command for properly loading and unloading the Read/Write Heads. (See Para. 4.3.2.1).

Refer to Figure 7-4, Address Logic Schematic (Sheet 2).

Typical manipulation of the Ramp FF occurs as follows.

When the LOAD/RUN switch is moved from RUN to LOAD, the -RETRACT signal goes LO and sets the Ramp FF (B60-9) thru gate A50-11. +RAMP goes HI and remains HI as the heads retract, unload and stop at the Home position.

When the LOAD/RUN switch is moved back to RUN, the start-up cycle begins. When the brush cycle has been completed and the spindle has reached Speed OK velocity, -RETRACT goes HI and allows the heads to advance and load. Head velocity is controlled by a speed command of 9, as provided by +RAMP (8-bit) and +DIF 1. As the heads cross track 0, the +OVER TRKS signal goes HI, re-setting the Calibrate FF. With -CAL HI, the Present Address Register begins counting as the positioner does a normal seek to cylinder 8. When the heads arrive at cylinder 8, +DETENT goes HI. This, in conjunction with +OVER TRKS being HI, resets the Ramp FF thru gate D20-6. With +RAMP LO, the inputs to the Adder consist of zeros from the New Address Register and a -8 from the Present Address Register; consequently, the head positioner immediately performs a normal seek to track 0.

4.3.2.6 Seek Settling Logic

Refer to Figure 7-4, Address Logic Schematic (Sheet 2).

The seek settling logic generates a 3.1 millisecond delay, beginning from the time the heads reach the desired track to the time -RSRW is allowed to go LO. This delay allows time for the head positioner to settle in the de-tented position before a read or write operation is permitted.

During the coarse positioning phase of a seek operation, -DETENT is HI. This holds counter A20 and FF B30-5/6 reset. When the heads arrive at the desired track, -DETENT goes LO, enabling counter A20. When the counter output reaches 1280, a HI output from gate B20-3 sets FF B30-5/6, causing -RSRW to go LO. The time lapse during the 1280 counts is 3.1 milliseconds. Although of no further consequence, the counter continues to run until -DETENT goes HI at the beginning of the next head movement.

Counter A20 is a TTL compatible MOS device operating at +5 volts.

4.3.2.7 Seek Incomplete

Refer to Figure 7-4, Address Logic Schematic (Sheet 2).

The Seek Incomplete FF, D30-5/6 sets if the +I OK signal goes LO. +I OK represents the time/current product of head positioner motor current. With the Seek Incomplete FF set, the -SEEK INC interface output goes LO and -RSRW goes HI. The Seek Incomplete FF can be reset by a restore command or a head retract signal.

4.3.2.8 Unit Select And Attention

Refer to Figure 7-4, Address Logic Schematic (Sheet 2).

Switches SW-3 and SW-4 serve to identify the disk drive as unit number 1,2,3 or 4. For unit-select decoding, the two switch levels are applied to inputs 10 and 11 of data selector M40. The code presented at these two inputs determines which Select input line must be activated by the controller to select the disk drive.

The coding that determines which Unit Select input and which Attention output are enabled, is listed below.

<u>SW4</u>	<u>SW3</u>	<u>UNIT I.D.</u>
1	1	1
0	1	2
1	0	3
0	0	4

1 = switch closed

0 = switch open

Attention line selection is performed by decoder M50. The ATTN signal is applied to input M50-2 of the decoder. ATTN exits the decoder from one of the four outputs, M50-4,5,6 or 7, depending on the code that is applied to decoder inputs M50-3, 13 by the switch levels.

The polarity of the ATTN output signal is optional by the setting of switch SW2. SW2 determines whether or not an inversion of ATTN occurs in the X-OR gates M30,3,6,8,11. With SW2 closed, the ATTN output signal is HI when active (true). With SW2 open, the ATTN output signal will be LO when active.

4.3.3 Servo (SO) PCB (#12068)

This subsection contains circuit descriptions of the servo system. For a functional description of the servo system, refer to subsection 4.2.5.

4.3.3.1 Speed Command Inputs

Refer to Figure 7-11, Servo PCB Schematic (Sheet 1).

DIF 1

The +DIF 1 minimum speed control signal is inverted and then used for on/off control of FET D40-9. When the FET is turned on, amplifier B18-10 provides a selected amount of current to amplifier input B18-1.

Diode A20 at the source terminal of FET D40-9 serves as a protective device for the FET. All other such configurations in the servo system serve the same function.

DAC OUT

The DAC OUT current signal joins the DIF 1 current increment at amplifier input B18-1. Being a current signal, an accurate scope waveform cannot be obtained at this point. The speed command appears at the output of amplifier B18-12 as a negative voltage signal, as shown in Figure 4-19.

The network of resistors and diodes between output and input of amplifier B18-12 provides gain-curve shaping for the amplifier.

4.3.3.2 Direction Control

The -FWD signal passes through gate B29-3 to control the Reverse FET, D40-16. -FWD is also inverted by A29-8 and passed through gate B29-6 to control the Forward FET, D50-1. For forward motion, FET D50-1 is turned on and FET D40-16 is turned off. For reverse motion, FET D50-1 is off and FET D40-16 is on.

-FWD is gated with -DETENT at gates B29-3 and B29-6. This turns off both the Forward FET and Reverse FET during the detent mode to ensure a zero level SERVO DRIVE signal.

4.3.3.3 SERVO DRIVE Signal

The summation of speed command and velocity feedback occurs at amplifier input D29-1. Since this is a current signal, a valid scope waveform cannot be obtained at this point. SERVO DRIVE appears as a voltage signal at the output of amplifier D29-12. The amplitude of SERVO DRIVE depends on the distance the heads must travel, up to a maximum level at distances of 256 cylinders or greater.

Figure 4-20 shows simplified waveforms of a long forward seek. When the speed command is first applied (point a), SERVO DRIVE rises sharply and levels off at maximum amplitude with amplifier D29-12 saturated. SERVO DRIVE remains at maximum until velocity feedback has increased sufficiently to bring the amplifier out of saturation (point b). Further increase in velocity feedback results in a decrease of SERVO DRIVE.

At point c the distance to go drops below 256 and the speed command begins to decrease. As a result, velocity feedback exceeds the speed command and SERVO DRIVE reverses polarity. The heads decelerate and come to a stop at point d.

For forward motion, SERVO DRIVE is a positive signal; for reverse motion, it is a negative signal.

4.3.3.4 Multi-Phase Squarewave Generator

Refer to Figure 7-12, Servo PCB Schematic (Sheet 2).

The multi-phase generator is composed of two Quadruple D-Type Flip-Flop modules wired as an 8-bit shift register. Clocking is provided by the 6.6 MHz crystal oscillator. Sixteen successive phases of 412.5 KHz squarewave signal

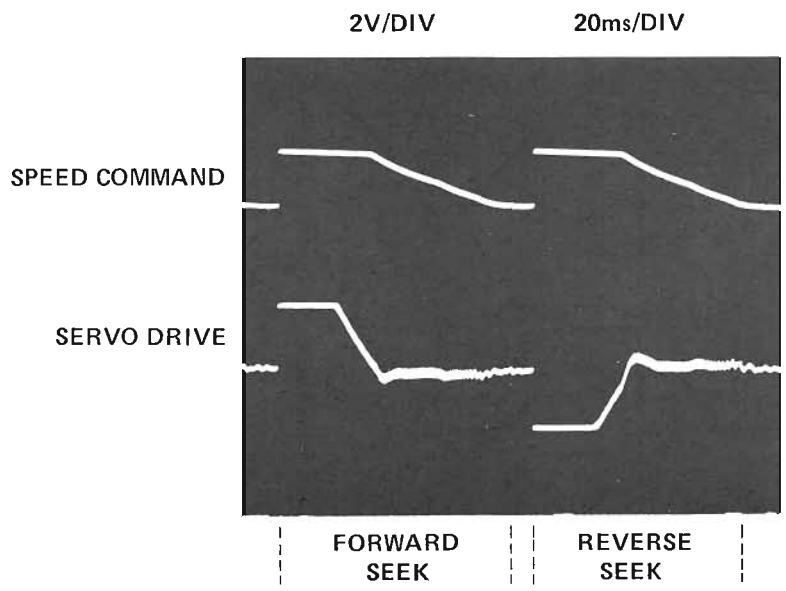


Figure 4-19. SPEED COMMAND AND SERVO DRIVE

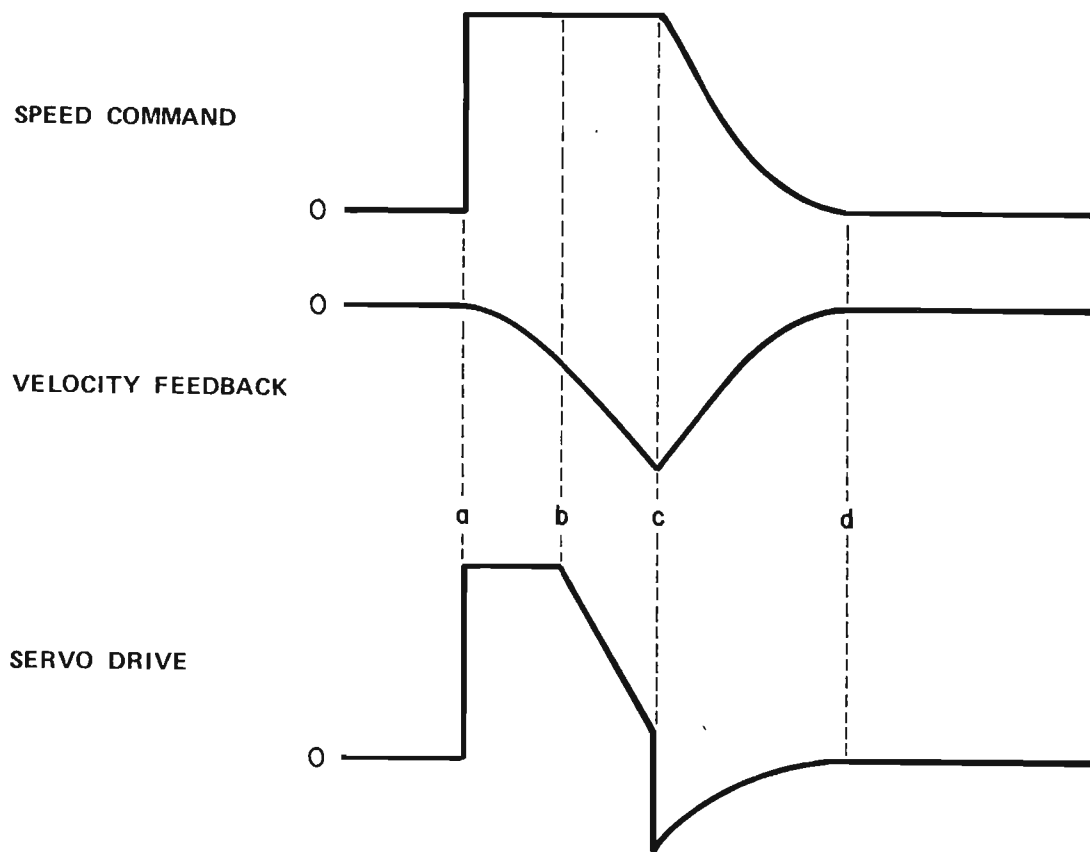


Figure 4-20. SERVO WAVEFORMS

are available at the outputs of the multi-phase generator. The waveforms appearing at the eight non-inverted outputs are shown in Figure 4-21.

4.3.3.5 Position Transducer Inputs

Selected phases from the squarewave generator are applied to two resistor networks to produce the 412.5 KHz XDCR A and XDCR B signals shown in simplified form in Figure 4-21. The resistor values are weighted to produce XDCR signals with a sinusoidal waveshape. After filtering by capacitors P14 and P16, the signals appear as shown in Figure 4-22. XDCR A lags XDCR B by 90° .

4.3.3.6 Position Transducer Output

A single constant-amplitude, variable-phase sinewave signal is induced into the transducer secondary coil. The phase of this signal varies with the degree of coupling between the secondary coil and the XDCR A and XDCR B primary coils. During head travel, the transducer output signal goes through a 360° phase shift for each four tracks crossed.

The transducer output signal is applied to a wide band differential amplifier (H18-8/7) and is further amplified and shaped into a squarewave by voltage comparator K29-12. This variable-phase squarewave signal is entitled RECOV XDUCER.

4.3.3.7 Odd and Even Sawtooth Generators

The following description refers to the Odd Sawtooth Generator circuit but applies also to the Even Sawtooth Generator.

Refer to Figure 7-12, Servo PCB Schematic (Sheet 2).

Flip-flops P72-9/7 and P72-5/6 in the Odd Sawtooth Generator are used to compare the phase relationships between the RECOV XDUCER signal and the reference signal REF PHASE 180° . Figure 4-23 shows the switching waveforms for the two flip-flops for a single head position. As shown, FF output P72-5 goes HI at the falling edge of RECOV XDUCER and goes LO at the falling edge of REF PHASE 180° .

When the heads are moving, the phase relationship between RECOV XDUCER and REF PHASE 180° is constantly changing. This in turn changes the duty cycle (HI time) of the FF P72-5 output signal. Output P72-6 of the flip-flop is applied to an inverter, a buffer (K47) and then to an integrating amplifier circuit (F50-12). The output amplitude from this amplifier is directly proportional to the duty cycle of the signal applied to the capacitor/resistor network at its input.

Figure 4-24 shows the relationship between input duty cycle and output sawtooth slope for forward and reverse head motion. When the heads are moving forward, the duty cycle of the input signal (K47 collector) gradually increases from 0% to 100%. This corresponds to the gradual slope of the sawtooth output. After reaching 100% duty cycle, the input signal instantaneously switches back to 0% duty cycle. This corresponds to the retrace portion of the sawtooth signal. The sawtooth cycle repeats for every four tracks crossed by the heads.

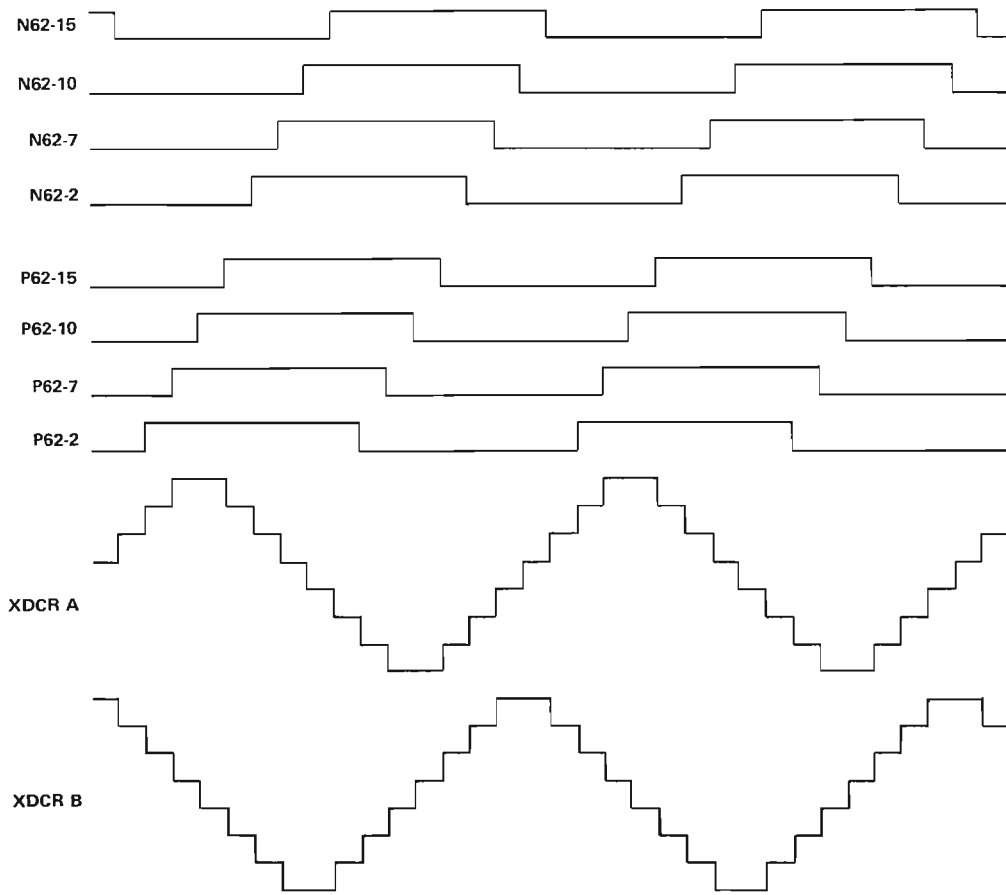


Figure 4-21. XDCR SIGNAL GENERATION

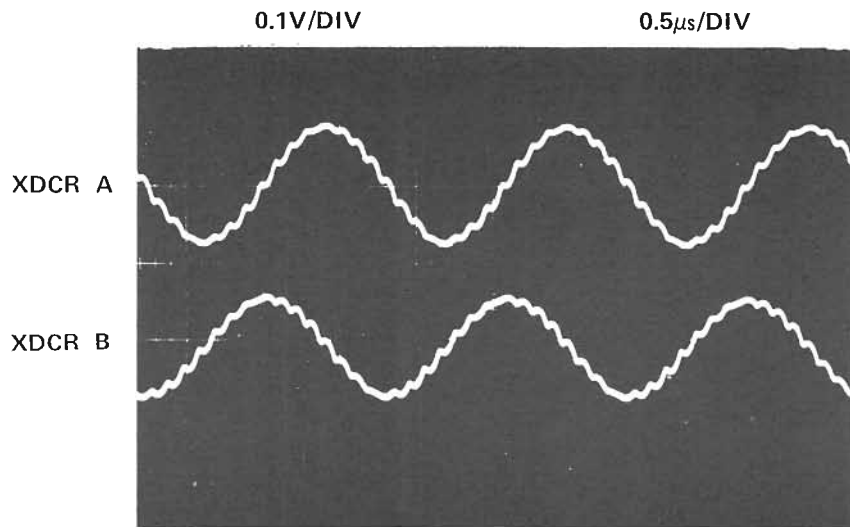


Figure 4-22. XDCR A AND XDCR B

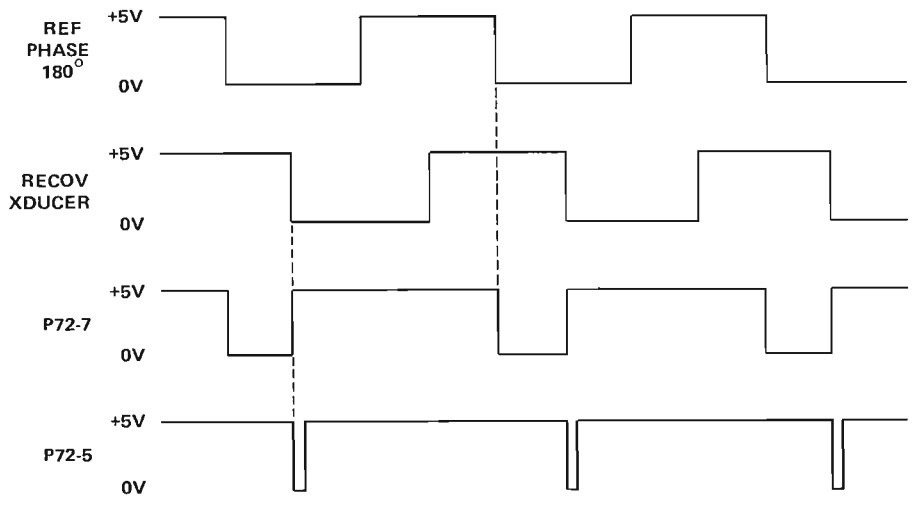


Figure 4-23. ODD SAWTOOTH FLIP-FLOP SWITCHING

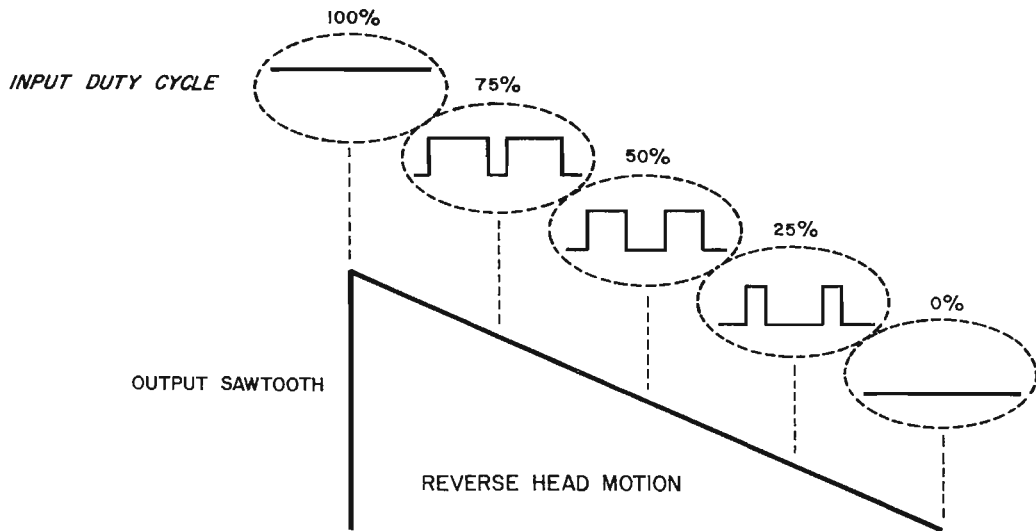
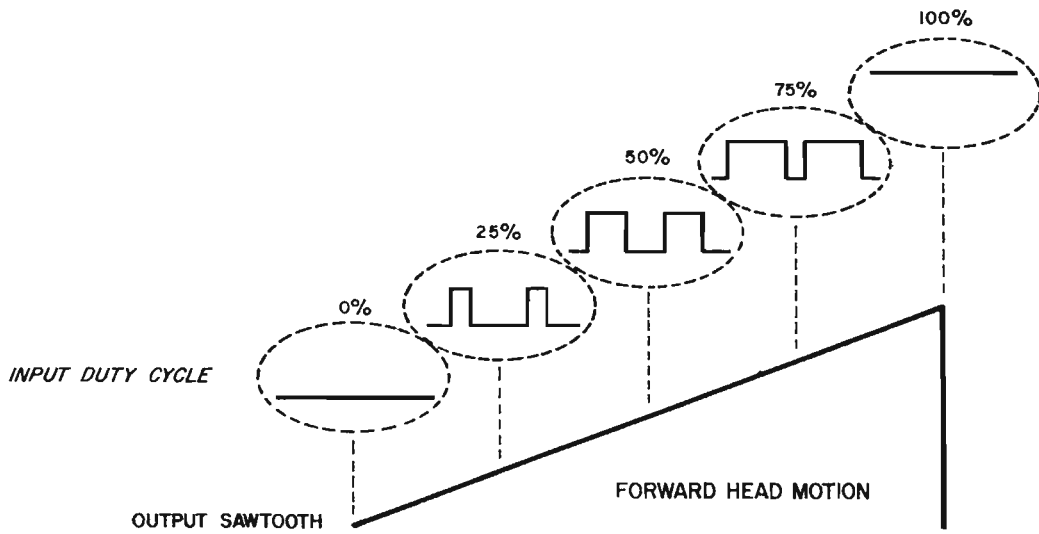


Figure 4-24. SAWTOOTH GENERATION

The Even Sawtooth Generator uses the inversion of REF PHASE 180° as its reference signal. Consequently, EVEN SAWTOOTH and ODD SAWTOOTH are phase separated by 180° .

4.3.3.8 Velocity Feedback

Velocity feedback is achieved by coupling the center slope portions of the Odd and Even Sawtooth signals to the summing junction.

Refer to Figure 7-11, Servo PCB Schematic (Sheet 1).

The ODD SAWTOOTH and EVEN SAWTOOTH signals are each applied to an integrating circuit (Capacitor F37/resistor F38, and capacitor F40/resistor F41). Each of these integrated signals is then applied to two FET switches. One of the FET's connects to the summing junction and the other connects to ground (FET's D50-16 and D40-8 for ODD SAWTOOTH; FET's D50-9 and D40-1 for EVEN SAWTOOTH). On-off control of the feedback FET's is derived from the phase relationship between RECOV XDUCER and REF PHASE 180° .

Figure 4-25 shows the waveforms associated with the Feedback FET control signals. The output of X-OR gate A50-3 is a squarewave whose duty cycle varies with head position. During head travel, the signal at A50-3 produces a triangular waveform at input A72-10 of a voltage comparator. The comparator output signal (A72-7) is an inverted squarewave that switches at the halfway levels of the triangular input signal.

The LO period of inverter output B50-6 coincides with the center portion of the EVEN SAWTOOTH slope. During this period, FET D50-9 is turned on to couple the Even feedback signal to the summing junction. Simultaneously, FET D40-8 is turned on to clamp the Odd feedback line to ground.

The LO period of inverter output B50-4 coincides with the center portion of the ODD SAWTOOTH slope. During this period, FET D50-16 is turned on to couple the Odd feedback signal to the summing junction. Simultaneously, FET D40-1 is turned on to clamp the Even feedback line to ground.

4.3.3.9 C and D

Refer to Figure 7-11, Servo PCB Schematic (Sheet 1).

Signals C and D are produced by the same type of circuit as that used for the feedback FET control signals. The C circuit uses an input reference signal entitled REF PHASE C from the multi-phase squarewave generator. The D circuit uses an input reference signal entitled REF PHASE D from the multi-phase squarewave generator. The switching sequence of C and D for forward and reverse head motion is shown in Figure 4-26.

4.3.3.10 E and F

Refer to Figure 7-11, Servo PCB Schematic (Sheet 1).

Signals E and F are derived from C and D by two D-type flip-flops (A40) and X-OR gate A50-11. The two flip-flops are disabled by a LO -DETENT signal at their clock inputs. When the clock inputs are HI, the flip-flop outputs

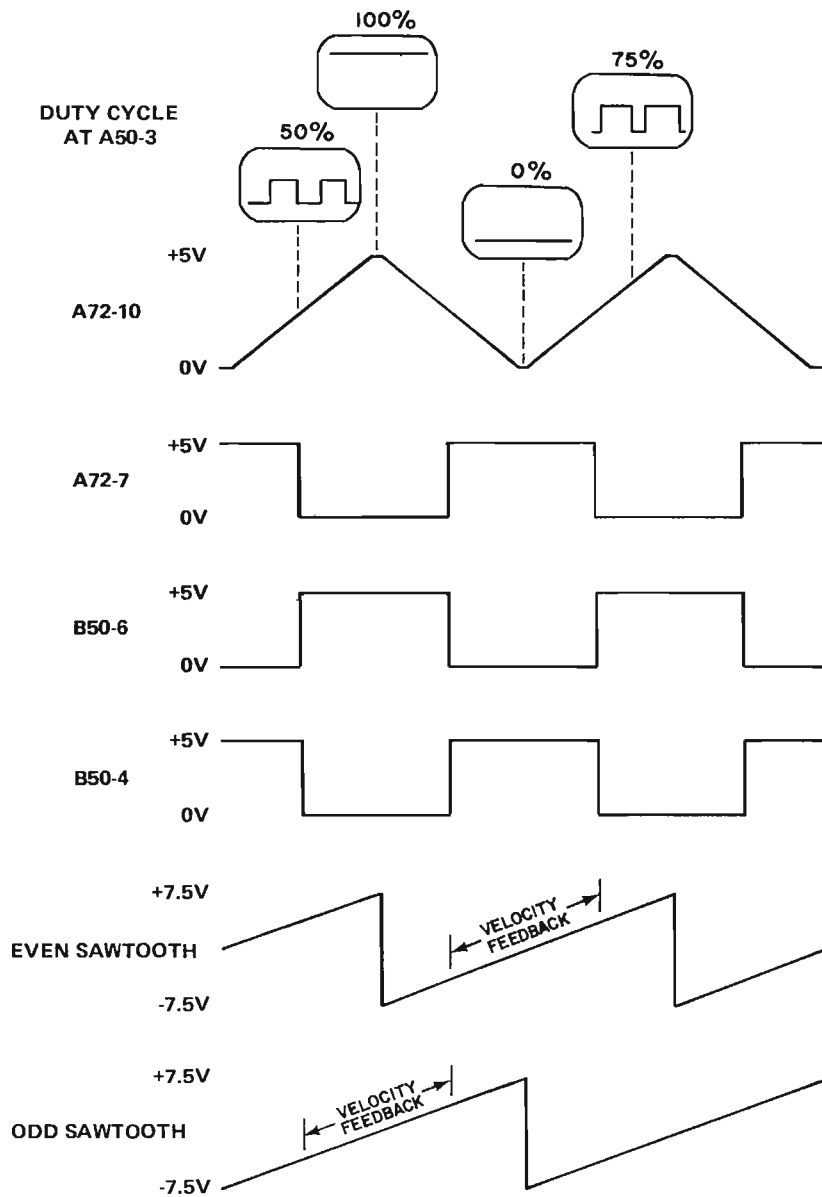
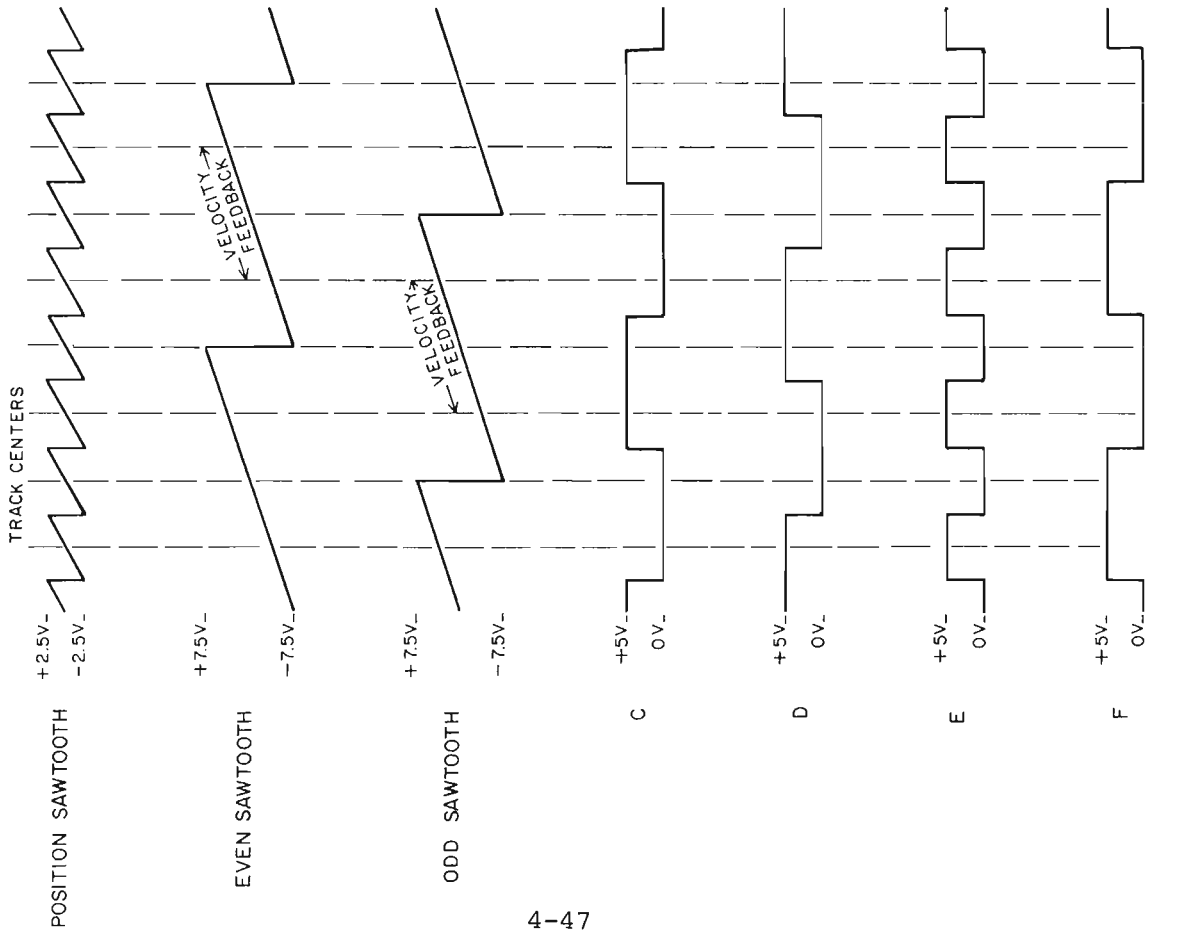


Figure 4-25. FEEDBACK FET SWITCHING SIGNALS

FORWARD MOTION — CONSTANT VELOCITY



REVERSE MOTION — CONSTANT VELOCITY

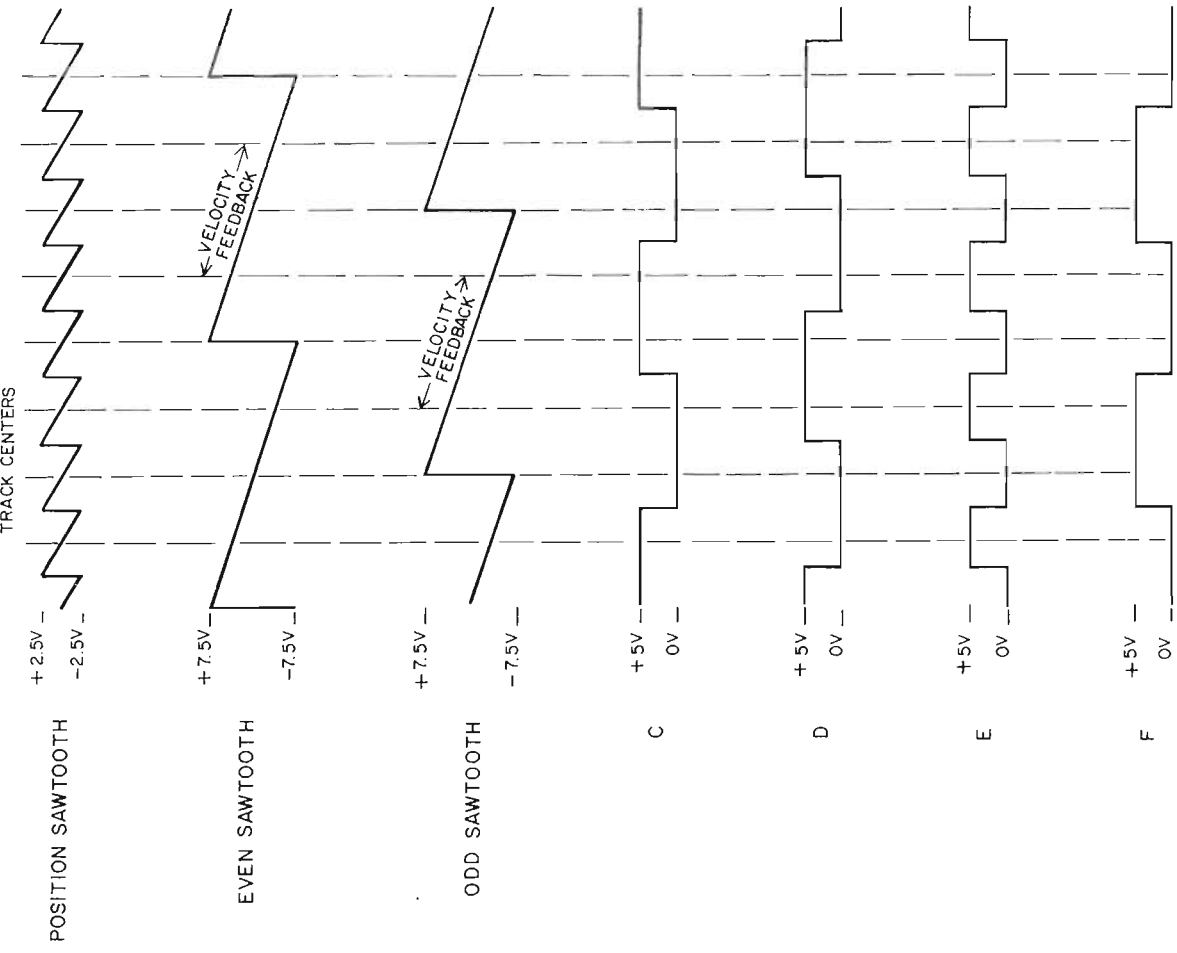


Figure 4-26. VELOCITY AND POSITION WAVEFORMS

follow the C and D signals at the data inputs of the flip-flops. The switching sequence of E and F for forward and reverse head motion is shown in Figure 4-26.

4.3.3.11 Position Sawtooth Generator

The Position Sawtooth Generator operates basically the same as the Odd and Even Sawtooth Generators. Instead of a single reference signal, however, four different reference signals are used, depending on head position. Selection of the reference signal is performed by the Position Reference Selector, M62. Signals E and F control the Selector. E and F provide a 2-bit binary code which advances at each track crossing. As a result, the reference signal that appears at the Selector output (M62-7) changes at each track crossing. This allows generation of a POSITION SAWTOOTH whose repetition rate corresponds to the track crossing rate of head motion. Figure 4-26 shows the relationship of the POSITION SAWTOOTH to various other Servo signals.

4.3.3.12 Detent Mode

Refer to Figure 7-11, Servo PCB Schematic (Sheet 1).

When -DETENT goes LO, the output of inverter B50-12 goes LO and turns on the Position FET, D50-8. The Position FET couples the POSITION SAWTOOTH signal to the summing junction through resistor E47. Any tendency for the heads to drift away from track center will cause the POSITION SAWTOOTH to shift to a polarity which will oppose the drift.

4.3.3.13 +4.5V

Refer to Figure 7-12, Servo PCB Schematic (Sheet 2).

The +4.5V level is used as a reference voltage for the three sawtooth output amplifiers. The +4.5V is produced at the collector of transistor H67. This circuit matches the transistor stages which drive the sawtooth amplifiers. As a result, during thermal variations, the amplifier reference voltage tracks the amplifier signal and ensures a symmetrical output signal.

4.3.3.14 -5V

Refer to Figure 7-12, Servo PCB Schematic (Sheet 2).

-5V for use on the Servo PCB is developed by tracking regulator L29-12. The -5V tracks the +5V supply level which is applied to input L29-1 of the tracking regulator.

4.3.4 Logic (LO) PCB (#12066)

The Logic PCB performs the following functions.

- 1) Separates index and sector marks, and develops a 5-bit sector count output.
- 2) Generates PHASE 1 and PHASE 2 spindle drive signals and performs the necessary frequency adjustments for spindle speed control.

- 3) Develops spindle motor and brush motor enable signals.
- 4) Develops signals for Cartridge Unlock, Servo Release, Reset Write Check, Load/Run status, Retract, Ready status, and "Over Tracks" head location detection.

4.3.4.1 Spindle Drive Control Logic

Refer to Figure 7-5, Logic PCB Schematic (Sheet 1).

The Spindle Drive Latch (M30-6/L40-6) produces the -PHASE 1 ENABLE and -PHASE 2 ENABLE signals that turn the spindle motor on and off. The Spindle Drive Latch is controlled primarily by the Load/Run switch, the +CTG INTERLOCK signal and the -EMERGENCY RETRACT signal.

With the disk drive in the Run mode, the Load/Run Latch (L20-3/L20-6) has a HI at output L20-6 which holds counter K40 reset. The +CTG INTERLOCK signal is HI at gate input L30-5, resulting in a LO at gate output L30-6. The LO at input L40-4 of the Spindle Drive Latch holds latch output L40-6 HI and output M30-6 LO. Consequently, -PHASE 1 ENABLE and -PHASE 2 ENABLE are LO, enabling spindle drive. At this time, FF M40-5/6 is in its set state due to the LO at its preset input, M40-4.

When the Load/Run switch is switched to LOAD, the -LOAD SW signal goes LO and toggles the Load/Run Latch. This produces a LO at gate input L30-4, and allows input L40-4 of the Spindle Drive Latch to go HI. Simultaneously, the LO at inputs 6 and 7 of counter K40 enable it to begin counting SELECTED INDEX pulses. At the sixth index pulse, counter output K40-8 goes HI and clocks FF M40-5/6 to its reset state. The resulting LO at input M30-3 toggles the Spindle Drive Latch, causing -PHASE 2 ENABLE to go HI to turn off the PHASE 2 driver circuit on the P/D PCB. The 6-revolution delay is provided to allow completion of a write operation which may be in progress when the drive is switched to the Load mode.

The Delay Skip Latch avoids this delay if the operator should happen to switch the drive from Load to Run and back to Load before the spindle reaches operating speed. When +SPEED OK is LO, latch output N50-12 goes LO as soon as -RUN goes HI. This immediately clears FF M40-5/6 by the LO at its clear input.

The -PHASE 1 ENABLE signal remains LO during the spindle braking period. After this interval, the -SPINDLE STOPPED signal goes LO and causes -PHASE 1 ENABLE at gate output P20-3 to go HI. This turns off the PHASE 1 driver circuit to avoid overheating the driver while the disk drive is in the Load mode.

The +CTG INTERLOCK signal inhibits spindle drive if the cartridge clamps are not closed.

If an emergency retract or power-on-reset condition occurs, input M30-4 of the Spindle Drive Latch goes LO. This forces output M30-6 HI and turns off spindle drive.

If the Load/Run switch is in the RUN position when -EMERG RETRACT goes LO at gate input P20-13, FF M40-5/6 will be forced from set state to reset state by the LO at its clear input (M40-1). This in turn toggles the Spindle Drive

Latch, making its M30-6 output go LO and turning off spindle drive. As soon as -EMERG RETRACT goes HI again, FF M40-5/6 returns to its set state because its preset input M40-4 is still LO. With M40 set, inputs M30-3, 4, and 5 of the Spindle Drive Latch are all HI. This switches the Latch back to its original state to again enable spindle drive.

4.3.4.2 Brush Drive Control Logic

Refer to Figure 7-5, Logic PCB Schematic (Sheet 1).

With the disk drive in the Load mode and the brushes in their home position, the Brush Switch Latch and Brush Cycle Latch are both in the set state (L20-8 = HI and L30-11 = HI). Start of the brush cycle is inhibited by the LO at gate input L30-9.

When the Load/Run switch is switched to RUN, gate input L30-9 goes HI. As a result, +BRUSH ENABLE goes HI and the brush cycle begins. As the brushes leave their home position, the brush switch toggles to its "OUT" position. This resets the Brush Switch Latch, which in turn resets the Brush Cycle Latch. The brush cycle continues however, because the LO provided by output L20-8 of the Brush Switch Latch to gate input H20-6 keeps the +BRUSH ENABLE signal HI.

At the end of the brush cycle, the brush switch toggles back to its "HOME" position, setting the Brush Switch Latch. The Brush Cycle Latch remains reset until the Load/Run switch is switched from RUN to LOAD. At that time, the Brush Cycle Latch becomes set by the LO at gate output L30-3 in preparation for the next brush cycle.

The Power On Reset (POR) signal resets the Brush Cycle Latch at turn-on.

4.3.4.3 Home and Over Tracks Detectors

The Home and Over Tracks Detectors each consist of a Light-Emitting Diode (LED) and phototransistor mounted on the base plate of the head positioner. A metal shutter is mounted on the carriage assembly. The location of these components is shown in Figure 4-27. The schematic and waveforms of the circuits are shown in Figures 4-28 and 4-29.

When the heads are in the Home position (fully retracted), the shutter blocks light between the LED and phototransistor of the Home Detector. As a result, the phototransistor is nonconductive and the Home Detector output is HI, as shown in Figure 4-29. When the heads begin moving away from the Home position, the shutter allows light to pass and the Home Detector output signal goes LO.

The shutter blocks light through the Over Tracks Detector when the heads are not over the track area of the disks, and passes light when they are. This produces the OVER TRKS DETECTOR waveform shown in Figure 4-29.

4.3.4.4 Logic Control for -RETRACT, -CTG UNLOCK and +SERVO RELEASE

These three signals are each partially controlled by the Home Detector output signal.

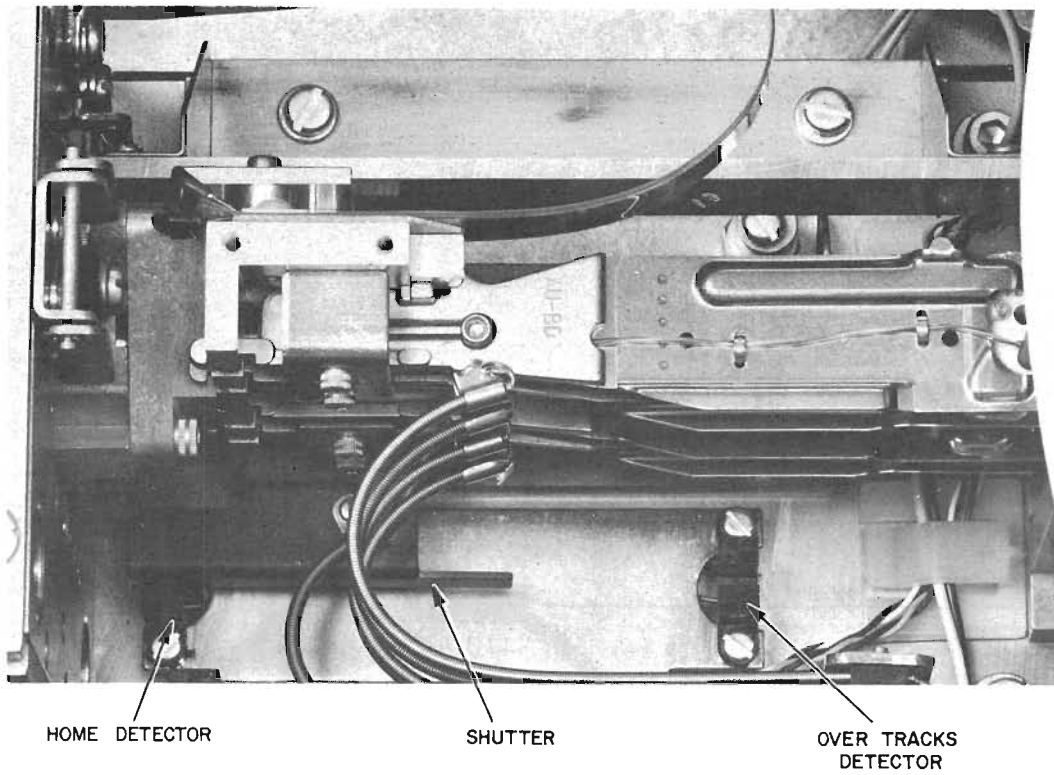


Figure 4-27. HEAD POSITION DETECTORS

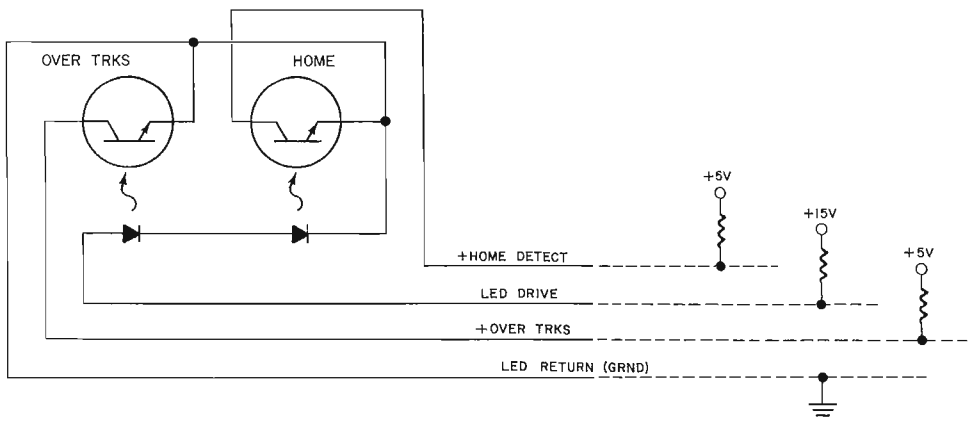


Figure 4-28. HEAD POSITION DETECTOR CIRCUITS

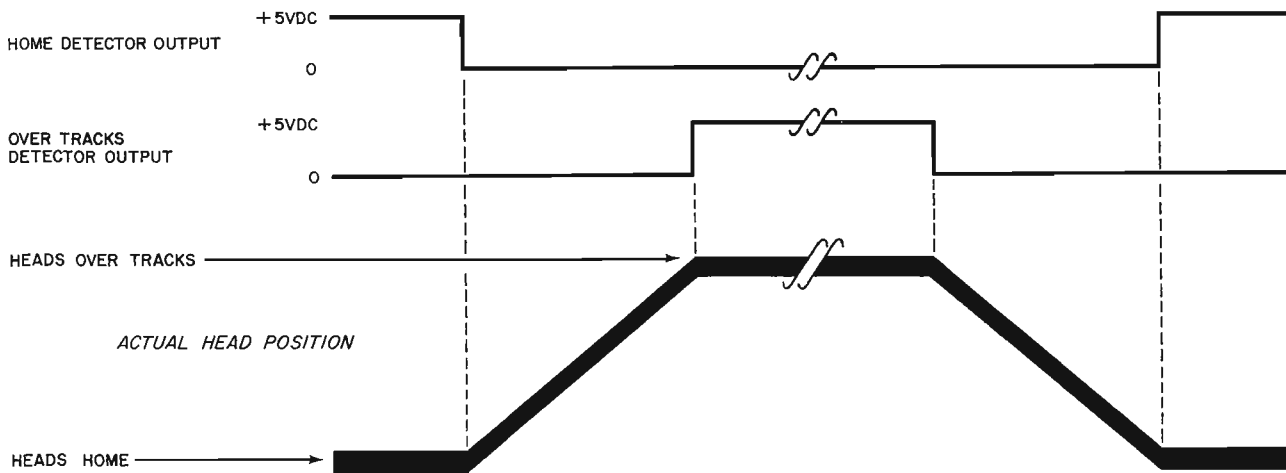


Figure 4-29. HEAD POSITION DETECTOR SIGNALS

-RETRACT

When LO, the -RETRACT signal will force a retract of the heads to the Home position and will hold them there. When -RETRACT goes HI, the heads will advance out to track 0.

Refer to Figure 7-5, Logic PCB Schematic (Sheet 1).

The Retract Latch has two set inputs:

- 1) Input M30-13 goes LO, to set the Latch, if the brushes are not home, or if +SPEED OK is LO; 2) Input M30-1 is a safety factor which sets the Latch to hold the heads retracted if either the Home Selector or Over Tracks Detector malfunctions.

The Retract Latch resets when -HOME goes LO at Latch input L40-12, but only if +BRUSH HOME and +SPEED OK allow Latch input M30-13 to be HI.

-CTG UNLOCK

Refer to Figure 7-5, Logic PCB Schematic (Sheet 1).

The -CTG UNLOCK signal is controlled by gates N20-5 and N30-8. -CTG UNLOCK will go LO only when all of the following conditions exist.

- 1) -PHASE 1 ENABLE = HI at gate input N20-6. This indicates that the spindle is not rotating.
- 2) +BRUSH HOME and +HOME signals are HI at gate inputs N30-10 and N30-9. This indicates that the brushes and heads are not out over the disk where they could cause damage during cartridge removal.

+SERVO RELEASE

Refer to Figure 7-5, Logic PCB Schematic (Sheet 1).

The +SERVO RELEASE signal will be HI as long as +HOME is HI at gate input K30-1, and +RETRACT is HI at gate input K30-2. This inhibits servo drive while the heads are in the home position, until +RETRACT goes LO to advance the heads.

4.3.4.5 Ready Signals and -RESET WR CHK

Refer to Figure 7-5, Logic PCB Schematic (Sheet 1).

Ready Signals

The +READY signal is HI whenever the heads are out of the Home position and there is no write check condition. The -READY IND signal controls the front panel READY indicator light. +FILE READY goes HI when +READY is HI and the unit is being selected by the controller.

-RESET WR CHK

This signal serves two different functions on the Data Transfer PCB. One is to reset the Write Check circuits, and the other is to reestablish the Write Protect condition, in accordance with the setting of the internal write protect switches.

-RESET WR CHK is controlled by the +PHASE 2 ENABLE signal at gate input N30-1, and the -INITIALIZE signal at gate input N30-2. -RESET WR CHK will go LO if either or both inputs go LO. +PHASE 2 ENABLE goes LO whenever the Load/Run switch is changed to LOAD. -INITIALIZE is LO during Power-On Reset and during Emergency Retract.

4.3.4.6 Index and Sector Mark Separation

Note: The frequencies and times used in this description are those associated with 2400 rpm operation. Variations associated with 1500 rpm operation are summarized at the end.

The method used for electronic separation of the index mark from the sector marks is based on the fact that the sector slots are relatively widely separated on the disk hub while the index slot follows close behind one of the sector slots. The separation circuitry establishes a brief "window" following each sector mark. The location of the index slot is such that when the spindle is up to speed the index mark will occur within this window following one of the sector marks.

The following text describes separation of index/sector marks received from the lower transducer, but pertains also to the duplicate circuit for separation of upper index/sector marks. Refer to Figure 7-6, Logic PCB Schematic (Sheet 2).

In the input circuit of voltage comparator A20, resistor D15 serves as the transducer load resistor, resistor D16 and capacitor D18 serve as a noise filter, and diode D17 prevents transient voltage spikes from reaching the input of the comparator where they can cause it to malfunction.

The voltage waveforms for the index/sector separator circuit are shown in Figure 4-30. The trailing edge of each sector mark and index mark triggers one-shot A40-13/4 to produce a 40 microsecond output pulse. FF B40-5/6 is in its reset state as each sector mark is received. This enables the sector mark gate (D40-6) and disables the index mark gate (D40-3). FF B40-5/6 then sets on the trailing edge of the sector mark, enabling the index mark and disabling the sector mark gate. The flip-flop will remain set, and thereby hold the index window open, until it is reset by a LO from the carry output (A50-12) of the Lower Window Counter.

The counter is clocked by a 20.625 KHz signal at input A50-5. Starting from a preset count of 1 (counter input A50-15 is held high), the counter will take a nominal 678.8 microseconds to produce a LO at its carry output. Consequently, the index window is open for 678.8 microseconds. A pulse received during the window period will be passed through gate D40-3 as the index pulse.

The lower index pulses pass from gate D40-3 to the 3A input of the output data selector (H30-11), while the upper index pulses are applied to input 3B. The lower sector pulses pass from gate D40-6, through inverter F40-2, to the

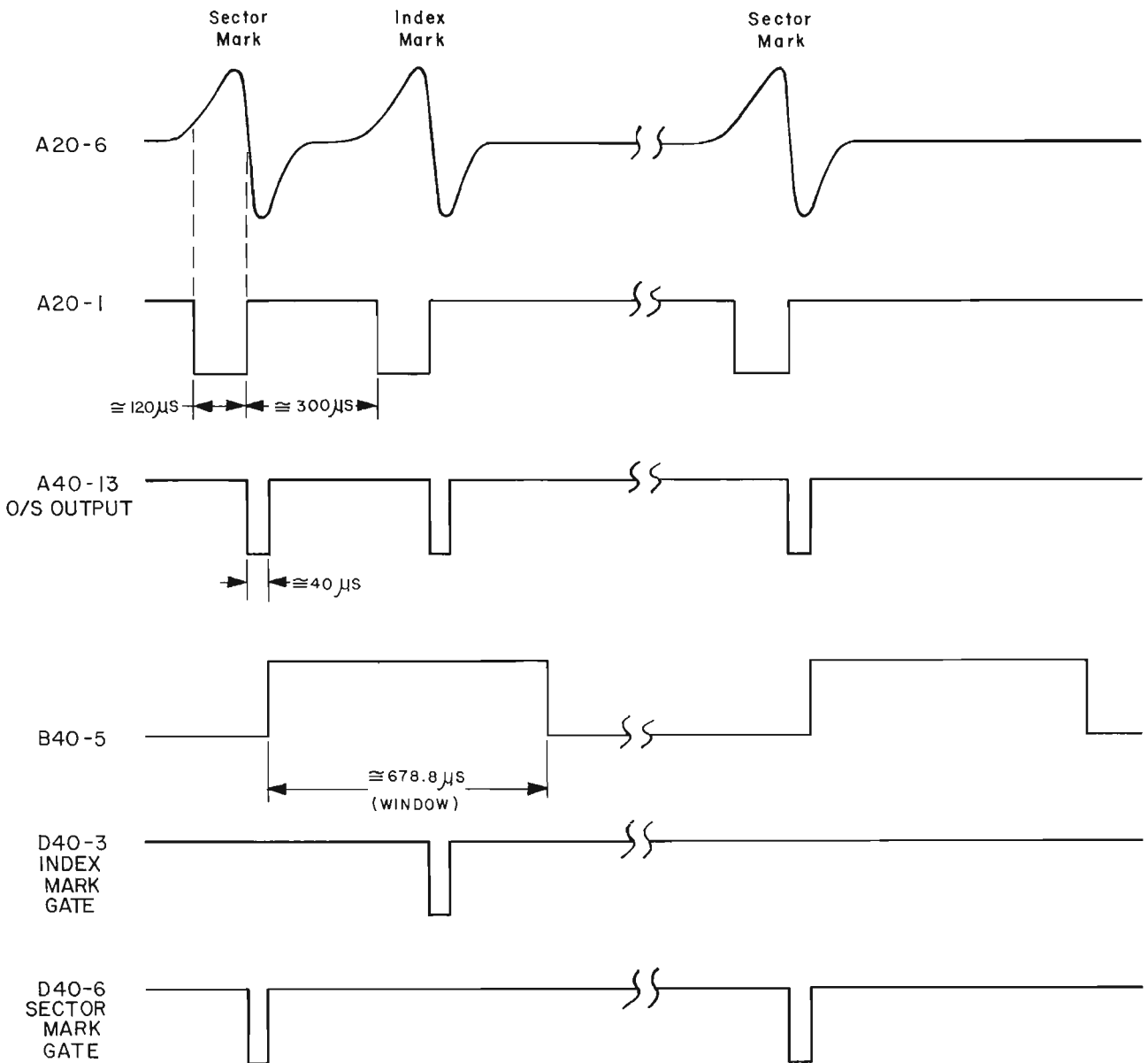


Figure 4-30. INDEX/SECTOR SEPARATION WAVEFORMS (2400 RPM)

2A input of the data selector (H30-5), while the upper sector pulses are applied to the 2B input. The signal +TOP DISK SEL at input H30-1 conditions the data selector to pass either the upper or lower index/sector pulses through to its output.

In units operating at 1500 rpm, the clock signal for counters A50 (lower index) and B50 (upper index) is 33 KHz, resulting in an index window of approximately 1086 microseconds.

Switch SW1-1 (B70) in the upper index circuit is used when a disk with only an index mark is being used. With SW1-1 closed, FF B40-9/8 is held set, which enables gate D40-8 to pass the single pulse received during each disk revolution as the index pulse.

4.3.4.7 Sector Counter

The following description of the lower sector counter pertains also to the upper sector counter which is the same.

Refer to Figure 7-6, Logic PCB Schematic (Sheet 2).

The sector counter consists of the 4-bit binary counter E20 which holds the lower four bits of the sector count, and FF H40-5/6 which holds bit 16. FF D30-5/6 and gate E40-6 serve to reset the counter.

The first sector following the index mark is designated as sector 0. Prior to receiving the index pulse, FF D30-5/6 is in its reset state, enabling counter E20 by the LO at E20-2. The sector counter is incremented by each sector pulse at counter input E20-14.

When the index pulse arrives, FF D30-5/6 is set by the LO at its preset input (D30-4). This produces a HI at the RO₁ input of the counter and enables gate E40-6. The next sector pulse produces a HI pulse at counter input RO₂ and gate input E40-4. With RO₁ and RO₂ both HI, counter E20 resets, while the LO pulse out of gate E40-6 resets H40-5/6. The trailing edge of this same sector pulse clocks FF D30-5/6 reset, producing a LO at counter input RO until the next index pulse sets FF D30-5/6 again.

The four outputs from counter E20 are applied to data selector F30, along with the four outputs from the upper sector counter (E30). The 16-bits, from FF H40-5/6 and H40-9/8, are applied to the other data selector (H30). The data selectors pass either the upper or lower sector counter outputs, depending on the state of the +TOP DISK SEL signal.

All of the sector mark, index mark and sector counter signals sent to the output interface are controlled by the FILE READY signal. This is accomplished in two different ways: 1) data selector F30 is strobed by -FILE READY at its F30-15 input; 2) the signals out of the other data selector (H30) are gated with the +FILE READY signal. H30 is not strobed like F30, because its +SELECTED INDEX output signal is required for internal use without the FILE READY restriction.

4.3.4.8 Spindle Drive Signal Generation

The PHASE 1 and PHASE 2 spindle drive signal frequencies are approximately 80 Hz for 2400 rpm and 50 Hz for 1500 rpm. PHASE II is phased 90°

lagging from PHASE I.

Refer to Figure 4-31.

The input signal to this circuit is a 412.5 KHz square wave derived from the 6.6 MHz crystal oscillator signal on the Servo PCB. K50 serves as a frequency divider that divides the 412.5 KHz by 5 for 2400 rpm, or by 8 for 1500 rpm. The divide factor is controlled by switch SW1-2 at inputs K50-3 and 4.

Note: The remainder of this description will use frequency values associated with 2400 rpm operation. The frequencies associated with 1500 rpm are proportionately lower.

K50 produces an 82.5 KHz signal at its carry output (K50-15). This signal is sent to four different locations: 1) to the Load input (K50-9) of the frequency divider to reset the divider; 2) to the Clock input of the rate multiplier (F50-9); 3) to gate input (E40-2); and 4) to counter input (H50-14.)

Counter L50 provides a divide by 2 function which produces a 41.25 KHz signal at output L50-3. Gated with the 82.5 KHz signal, this produces a 41.25 KHz signal out of gate E40-3 with a pulse duration equal to that of the 82.5 KHz signal. This signal is applied to the "unity" input of the rate multiplier (F50-12). Disregarding the frequency control inputs to the rate multiplier for the moment, the signal at the unity input (F50-12) of the rate multiplier will pass directly to the Y output (F50-6).

The 41.25 KHz signal from the rate multiplier is divided by counter K60. The 80 Hz signal taken from the Q9 output (K60-12) of the counter is gated with -SPINDLE DRIVE to produce the PHASE 1 signal. It is also Exclusive-ORed with the Q8 output of the counter to produce the PHASE 2 signal lagging by 90°.

Counter K60 is an MOS device operating at +5 VDC. The MOS noninverting buffers, M60-2 and M60-4, are used as power buffers.

For 1500 rpm operation, the basic output frequency is 50.354 Hz.

4.3.4.9 Spindle Speed Control

Two functions are necessary to achieve spindle speed control. First, the spindle speed must be monitored to determine whether it is fast or slow. Second, the frequency of the spindle drive signals must be increased or decreased to produce the necessary change in spindle speed.

The following text provides a general description of these functions before presenting circuit details. The frequencies used in the following descriptions are for 2400 rpm operation; for 1500 rpm operation, the frequencies are proportionately lower.

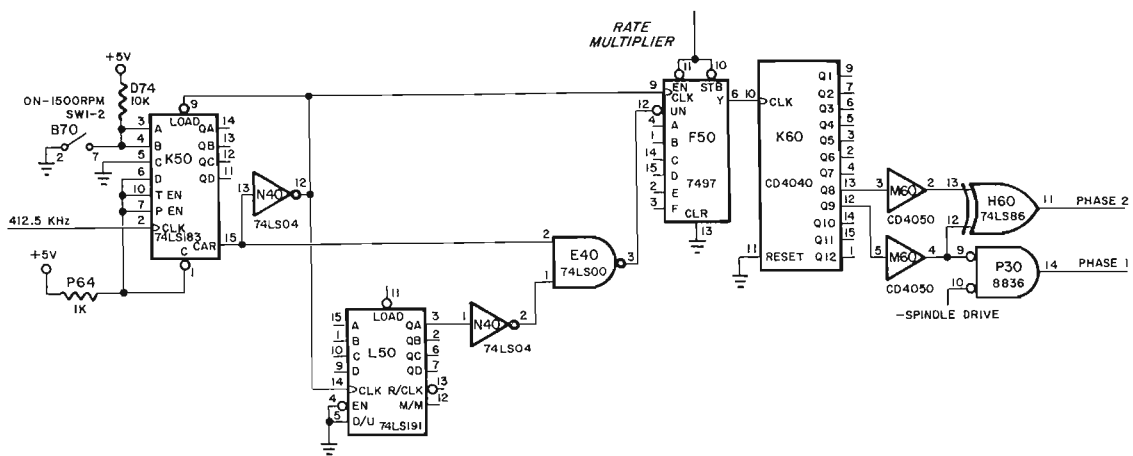


Figure 4-31. SPINDLE DRIVE GENERATION

General

Refer to the block diagram in Figure 4-32.

Spindle speed is monitored by measuring the time lapse between index pulses with the Index Period Counter. If the counter indicates a time lapse exceeding 25 milliseconds, the spindle speed is slow; if the time lapse is less than 25 milliseconds, the spindle speed is fast.

The fast/slow indication is stored by the Fast/Slow FF and applied to a binary up/down counter. If a fast condition exists, the counter will be decremented by one count; if a slow condition exists, the counter will be incremented by one count. After each adjustment of the counter, there is a brief delay to allow the spindle speed to respond before making another adjustment.

The parallel binary outputs from the counter are applied to the rate inputs of the Rate Multiplier, while a basic frequency of 41.25 KHz is applied to the unity input. As the basic signal passes through the Rate Multiplier, additional pulses are inserted into the pulse train according to the binary value at the rate inputs.

If the rate inputs = 0, no pulses are added; if the rate inputs = 63 (maximum for six rate inputs), an additional pulse is inserted for every 8 pulses of the basic signal. Increasing the rate at which pulses are being inserted is equivalent to increasing the frequency and, consequently, increasing the spindle speed. Conversely, reducing the rate at which pulses are being inserted has the opposite effect.

The signal from the Rate Multiplier is applied to a Frequency Divider that produces the PHASE 1 and PHASE 2 output signals. The range of frequency control extends from 80.566 Hz up to 90.65 Hz.

Since the circuit recognizes only "too fast" or "too slow", the spindle speed is constantly being increased or decreased in very small steps to keep it well within $\pm 0.2\%$ of 2400 rpm nominal.

Speed Monitor Circuit

Refer to Figure 7-6 (Logic PCB Schematic, Sheet 2).

The speed monitor function is performed by counter M50 and FF N60-9/8. Counter M50 is clocked by an 82.5 KHz signal from counter output K50-12. On each index pulse, counter M50 resets. The number of counts made between index pulses is dependent on the spindle speed. Starting from 0, counter M50 will take 24.824 milliseconds to reach the count where the Q12 output (M50-1) goes HI with all other Q outputs LO. At 25.018 milliseconds, the Q5 output will go HI with Q12 output still HI. These two separate conditions define "spindle fast" and "spindle slow", i.e., if Q12 = HI and Q5 = LO at index pulse, spindle speed is fast; if Q12 = HI and Q5 = HI at index pulse, spindle speed is slow. Counter M50 is an MOS device operating on +5 VDC. The non-inverting buffers at its outputs are used as power buffers.

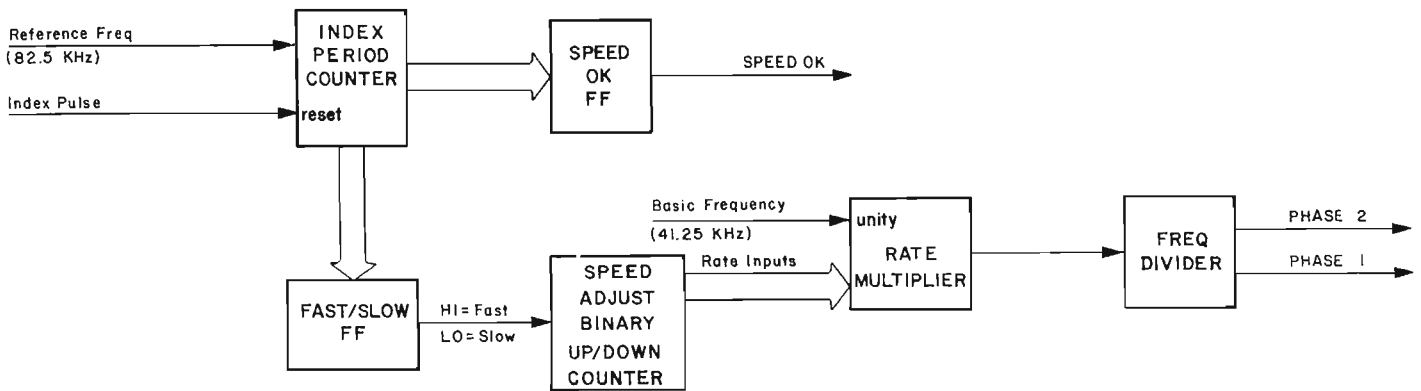


Figure 4-32. SPINDLE SPEED CONTROL BLOCK DIAGRAM

FF N60-9/8 stores the fast/slow indication. The FF is clocked each time the Q5 output of counter M50 goes HI. The Q12 output from M50 is applied to the set input (N60-12) of the FF. If Q5 goes HI with Q12 = HI (slow spindle speed), the FF sets; if spindle speed is fast, FF N60-9/8 will not be set. Output N60-8 of the Fast/Slow FF serves as the fast/slow indicator. N60-8 = HI = spindle fast; N60-8 = LO = spindle slow.

Speed Adjustment Circuit

Refer to Figure 7-6, Logic PCB Schematic (Sheet 2).

The FAST/SLOW signal from FF N60-8 controls the Down/Up inputs of the Speed Adjust Counter (E60/E50). This is an 8-bit binary up/down counter with its upper six bit outputs applied to the rate inputs of the Rate Multiplier.

The enable input (E60-4) of the Speed Adjust Counter is controlled by gate F60-8. Gate inputs F60-9 and 10 provide a $\div 4$ function which enables the Counter for a single count at every 4th index pulse. The gating structure comprised of gates F60-6, H60-3 and H60-6 encodes a signal that prevents overflow and underflow of the Speed Adjust Counter. This is done by disabling the Counter if either of the following conditions occur: 1) FAST/SLOW signal HI calling for a down count but both counters E60 and E50 already at minimum count. Minimum count is indicated by the M/M (Minimum/Maximum) output of both counters being HI and the QD output of both counters being LO; 2) FAST/SLOW signal LO calling for an up count but both counters E60 and E50 already at maximum count. Maximum count is indicated by the M/M output of both counters being HI and the QD outputs also being HI.

Only the six highest bit outputs from the Speed Adjust Counter are applied to the Rate Multiplier (F50). This has the effect of an additional $\div 8$. As a result, the Rate Multiplier input code can be adjusted only once every 32 index pulses. This interval allows time for the spindle speed to respond to a speed adjustment before making further adjustment of the spindle drive frequency.

The 41.25 KHz signal which passes from the unity input (F50-12) to the Y output of the Rate Multiplier is augmented with additional pulses, according to the rate input code. The enable input (F50-11) of the Rate Multiplier is controlled by a $\div 16$ counter output (L50-13). This limits the maximum pulse insertion rate to one inserted pulse for every 8 pulses coming through the unity input of the Rate Multiplier, as shown in Figure 4-33. Counter L50 is clocked by 82.5 KHz, while 41.25 KHz is applied to the unity input of the Rate Multiplier.

With all six rate inputs LO, no additional pulses are inserted, so the Y output frequency equals the unity input frequency of 41.25 KHz. With all six rate inputs HI, the maximum pulse insertion rate occurs, providing a 12.5% frequency increase to 46.4.

Counter K60 divides the basic Rate Multiplier output signal by a factor of 512 down to 80.566 Hz. Gates P30-14 and H60-11 produce PHASE 1 and PHASE 2, with PHASE 2 lagging by 90° . The 12.5% frequency adjust factor provides a PHASE 1/PHASE 2 frequency range of 80.566 Hz to 90.6 Hz. The fact that the minimum frequency is slightly above 80Hz compensates for inherent motor slip.

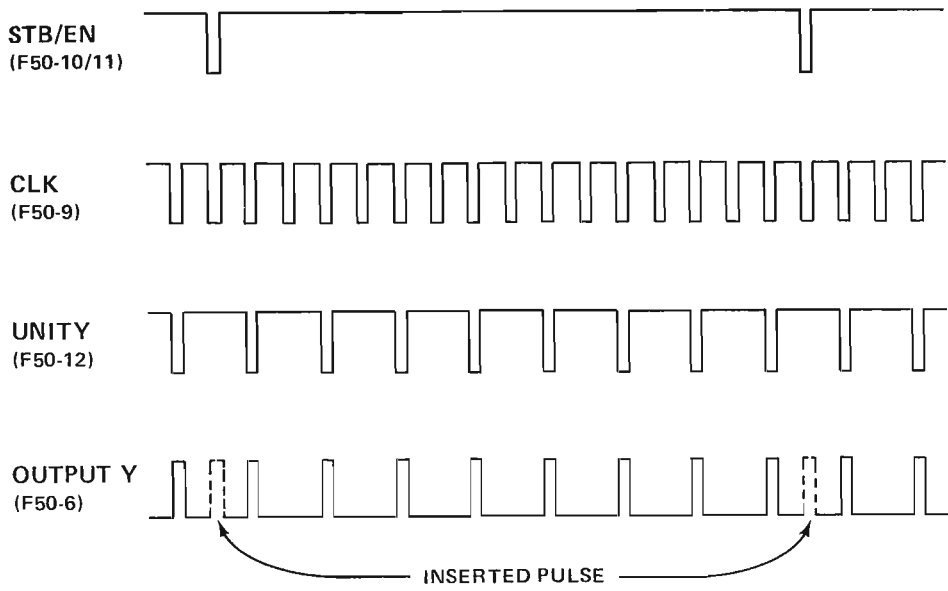


Figure 4-33. RATE MULTIPLIER SIGNALS

SPEED OK

The Q7 and Q12 outputs of the Index Period Counter (M50) are encoded at gate L40-8 for Speed OK sensing. At slow spindle speeds, the long time lapse between index pulses allows the Counter (M50) to reach a count with Q12 = HI and Q7 = HI. When this occurs, the output of gate L40-8 goes LO and inhibits gate L40-3 to disable the Counter clock. The Counter holds this state until the next index pulse resets it to begin counting again. The index pulse also clocks the Speed OK FF (N60-5/6). With input N60-2 LO, the FF remains reset and the +SPEED OK signal remains LO. When spindle speed approaches its nominal value, the Q12 = HI/Q7 = HI condition does not occur before the index pulse; consequently, the Speed OK FF sets.

The output from the Speed OK FF is ANDed with the output from a retriggerable one-shot (D60-13) to produce the +SPEED OK signal. The purpose of the one-shot is to prevent head damage which can occur if the heads are loaded without a cartridge in place. With a cartridge in place and the spindle rotating, the one-shot retriggers on every index or sector mark from the upper disk. The period of the one-shot is 55 ms; consequently, when the spindle is up to speed, the one-shot remains retriggered and its output (D60-13) remains HI. With the one-shot output HI and the Speed OK FF output HI, the +SPEED OK signal goes HI. Without a cartridge in place, there are no sector or index marks to retrigger the one-shot. As a result, +SPEED OK cannot go HI to allow head loading.

- 4.3.5 Data Transfer (D/T) PCB (#12046) - Standard
(#12076) - With VFO Option (200 ns pulse width)
(#12110) - With VFO Option (100 ns pulse width)

These two PCB's are identical except for the data separator circuits which are described separately.

4.3.5.1 Head Selection

Refer to Figure 7-7, Data Transfer PCB Schematic (Sheet 1).

Head selection is performed by the Head Select Decoder (B77). Inputs A and B of the decoder receive the DISK SEL and HD SEL signals. The head select inputs decode as listed below.

<u>-DISK</u> <u>SEL</u>	<u>-HD</u> <u>SEL</u>	<u>HEAD</u> <u>SELECTED</u>
LO	LO	Top Head, Top Disk
LO	HI	Bottom Head, Top Disk
HI	LO	Top Head, Bottom Disk
HI	HI	Bottom Head, Bottom Disk

Inputs C and D of the decoder serve as disable inputs. Head selection is disabled if either input is HI. Input C inhibits head selection anytime -RSRW is HI. If -WR PROTECT CMND is LO, input D allows head selection only when -RSRW and -READ GATE are LO.

Refer to Figure 7-8, Data Transfer PCB Schematic (Sheet 2).

A LO head selection signal from the Head Select Decoder turns on one of the transistors A66, A64, A61, or A57. During a read operation, the conductive transistor connects the R/W coil centertap to +5V thru diode A74. During a

write operation, the -WRITE ENABLE signal turns on transistor A70. This connects the R/W coil centertap to +15V thru transistor A70 and the conductive head select transistor.

4.3.5.2 Mode Control

Refer to Figure 7-7, Data Transfer PCB Schematic (Sheet 1).

READ

The signal -READ GATE is inverted by gate L16-3. +READ GATE is sent to the Data Separator where it enables the Data Separator output when +READ GATE is HI.

WRITE

-WRITE GATE is ANDed with -SEL RSRW at gate M19-2. The resulting signal is ANDed with the -WRITE PROT CMND at gate M65-3.

Four signals are derived from the output of gate M65-3: 1) -WR CMND is sent to the fault detection circuits; 2) -WR ENABLE controls the write bias transistor; 3) -WR CLAMP disables the Read Amp input during a write operation; 4) +WR DRIVE enables the Write Drive circuit.

ERASE

Control of the erase function is option by the setting of switch SW1 (L35). With SW1 open, erase is controlled by -WRITE GATE and -SEL RSRW thru gate M77-3. In this state, the erase function is active whenever the write function is active.

With SW1 closed, erase is controlled by -ERASE GATE from the controller. When write protect is active, the erase command is inhibited at gate M77-11.

Two equivalent signals are derived from the output of gate M77-11:

1) +ERASE DRIVE controls erase coil current thru transistor A73 (See Figure 7-8); 2) +ERASE CMND is sent to the fault detection circuits.

4.3.5.3 Write Protect

Refer to Figure 7-7, Data Transfer PCB Schematic (Sheet 1).

The write protect function is controlled by two identical circuits for the upper and lower disks. The following description refers to the write protect circuit for the upper disk.

When switch S2 is closed, gate M69-3 is disabled and the Upper Protect FF cannot be set. In this condition, the upper disk is unprotected.

When switch S2 is open, gate M69-3 is enabled. In this condition, the Upper Protect FF can be set by either -RESET WR CHK or -WR PROT INPUT. -RESET WR CHK goes LO at power turn-on, during emergency retract, and when the drive is switched from RUN to LOAD. -WR PROT INPUT goes LO on command from the controller. With the Upper Protect FF set, the upper disk is protected.

With switch S2 open, the Upper Protect FF can be reset only by depressing the PROTECT switch on the front panel. This action causes +WR PROT RESET to go HI, resetting the flip-flop.

The output of the Upper Protect FF (N69-13) is gated with +TOP DISK at gate R69-6. Similarly, the output of the Lower Protect FF (N69-7) is gated with -TOP DISK at gate R69-8.

One additional signal which can produce a write protect condition is -WR CHK. By tying -WR CHK directly into gate S69-6, an unqualified write protect condition can be generated to protect recorded data whenever a write check condition occurs, regardless of the settings of the write protect switches.

The grounded-input inverter (P58-10) that ties to gate input S69-5 is reserved for possible future use.

The -WR PROT STATUS output signal to the controller will be LO when either or both disks are protected and the drive is selected.

The Protect Indicator FF (N69-4) produces a significant indication only in its reset state. In this condition, its LO output turns off the PROTECT light to indicate that neither disk is protected. The set state of the Protect Indicator FF, however, is independent of the write protect option switches. Consequently, it is possible for the Protect Indicator FF to be set, and the red light to be lit, even when neither disk is protected.

4.3.5.4 Write Driver

Refer to Figure 7-8, Data Transfer PCB Schematic (Sheet 2).

Assuming -SEL RSRW is LO, each -WR DATA pulse received at gate input M19-11 will produce a corresponding positive pulse at flip-flop input F77-11. The flip-flop toggles on the rising edge of each pulse. The flip-flop outputs alternately switch transistors E49 and E58 on and off. This effectively reverses R/W head current for each new pulse by switching write current back and forth between R/W coils.

Transistor E64 and associated components serve as a constant current source.

When recording on the inner tracks of the disk, the write current is reduced to compensate for the greater bpi density. When the signal -NAR 256 is LO, transistor E68 turns on and shunts some of the write current away from the driver circuit.

4.3.5.5 Fault Detection

Refer to Figure 7-8, Data Transfer PCB Schematic (Sheet 2).

The types of faults detected are listed and described in the paragraphs which follow. For troubleshooting purposes, four D-type flip flops (J70) on the Data Transfer PCB serve to identify the type of fault condition that has occurred.

1) Erase Current Without +ERASE CMND = HI.

2) No Erase Current With +ERASE CMND = HI.

Either of these two faults will produce a HI at the output of the Erase Fault Gate (E77-3). This HI sets the ER Fault FF (J70-14), and also causes a LO at gate output L60-13. The LO at L60-13 produces a HI out of gate M65-11 and a LO out of gate M77-8.

A delay circuit at the input of gate L16-2 retards the responses of this gate, to avoid setting the Write Check Latch (M55-9) on spurious pulses from the write fault detection circuits. When gate output M77-8 goes LO, capacitor L24 must discharge through resistor L25 and diode L22 before gate output L16-2 can go HI.

A HI at L16-2 is inverted, producing a LO at input M55-9 of the Write Check Latch. This resets the latch and establishes the Write Check condition.

3) Write Current Without -WRITE GATE = LO.

4) No Write Current With -WRITE GATE = LO.

Write faults are detected by two different circuits: an AC write fault detector, and a DC write fault detector. The primary purpose of the AC fault detection circuit is to detect a partial loss of AC write current. Typically, this condition is caused by an open in one half of the center-tapped R/W head winding, or failure of one side of the write driver.

A DC write fault is defined as a complete loss of write drive current. The DC and AC write fault detectors both respond to a DC write fault.

DC Write Current is sensed by transistor F54. The output from F54 is sent to the DC WR Fault Gate (E77-6), along with -WR CMND. A HI out of this gate will set the DC Fault FF (J70-11), which produces a LO at TP20. The HI out of gate E77-6 also sets the Write Check Latch (M55-9), in the same manner described earlier.

AC Write Current is sensed by the circuit comprising transistors F53, H55 and H56. Whenever write current pulses are present, an AC signal is coupled through diodes E52 and E53, and capacitor E50. This signal is amplified by transistors F53 and H55, and then converted to a rippled DC level by diode H53 and capacitor H51. This positive level turns on transistor H56, which produces a low output from the circuit.

If current pulses are absent from one of the write drive lines, the signal to the current sense circuit is only one-half its normal frequency. This reduces the DC potential below the turn-on threshold of transistor H56, making the output of the circuit HI.

The output of the AC write current sensing circuit is applied to the AC Write Fault Gate (E77-11) along with -WR CMND. A HI out of this gate will set the AC Fault FF (J70-6), and also set the Write Check Latch (M55-9).

For troubleshooting purposes, it is important to note that the DC fault test point (TP20) and the AC fault test point (TP21) will both be LO during a DC write fault. During an AC write fault, however, only the AC fault test point (TP21) will be LO.

5) Multiple Head Selection Fault

Detection of a multiple head selection fault is accomplished by voltage comparator J50-12 during write, or comparator J50-7 during read. Except for the values of the bias potentials at their inputs, these two circuits operate the same. The bias differences compensate for the fact that during read the head select transistors are tied to +5V, whereas during write they tie to +15V. The operation of comparator J50-12 is described in the paragraphs which follow.

During a normal write operation, the potential at comparator input J50-4 is negative in relation to the reference potential at comparator input J50-5. In this condition, the comparator output is LO, representing no fault.

If a malfunction causes multiple head selection, current flow through resistor J53 increases. As a result, the potential at J54-4 shifts positive in relation to the reference potential at J50-5. When this happens, the comparator output goes HI.

The J59 gates at the comparator outputs select the appropriate output depending on whether it is a write operation or read operation. A HI out of gate J59-3 sets the HD Fault FF and the Write Check Latch.

4.3.5.6 Read Channel

4.3.5.6.1 Head Biasing

Refer to Figure 7-9, Data Transfer PCB Schematic (Sheet 3).

Transistors D61 and D62 serve as a constant current source to forward bias the R/W head diodes (shown in Figure 7-8). This ensures reliable coupling of the read data signals from the heads to the Read Amplifier input.

During a write operation, the signal -WR CLAMP isolates the read amplifier from the R/W heads to prevent saturating the amplifier.

4.3.5.6.2 Read Amplifier and Filter

The differential Read Amplifier consists of transistors B42 and B46, with a constant current source made up by transistors A49 and A53. The gain of this amplifier is approximately 30.

Buffer transistors A45 and B41 drive a low-pass filter network which removes high frequency noise from the signal.

4.3.5.6.3 Differentiator

The Differentiator converts the peaks of the data signals into zero crossings. The gain of this circuit is approximately 20 at 1.25 MHz (all 0's) and 40 at 2.5 MHz (all 1's).

4.3.5.6.4 Limiter-Amplifiers

Following the Differentiator are two stages of amplification and limiting which shape the signal into a rectangular waveform with edges representing the peaks of the original analog head signal. Limiting is accomplished by diodes D26/D27 in the first amplifier and A20/A21 in the second amplifier.

4.3.5.6.5 Zero-Crossing Detector

Each of the two outputs from the Zero-Crossing Detector produces a 100ns positive pulse at the negative edge of its corresponding input signal. Pulse duration is determined by the amount of time it takes capacitor B11 to charge from the current source section of the circuit. When B11 has charged, the OFF transistor turns ON, and the corresponding output goes LO.

4.3.5.6.6A Single-Shot Data Separator - Standard

Refer to Figure 7-10, Data Transfer PCB Schematic (Sheet 4).

The data separation process is controlled by the Separator FF, E25-9/8. For purposes of explanation, assume that the bit about to be received is a 0 (clock pulse without data pulse). The Separator FF is in its reset state, enabling the Clock Gate (F25-11). The first pulse received on the +RAW DATA line passes through the Clock Gate to the Read Clock output line. The resultant LO pulse at the output of the Clock Gate presets the Data Window FF (E25-5/6). This activates the Data Window Timer by turning off transistor J41.

The trailing edge of the LO pulse out of the Clock Gate sets the Separator FF, thereby disabling the Clock Gate and enabling the Data Gate. Meanwhile, capacitor J43 in the Data Window Timer is charging negative through current source J44. When input J39-3 of the voltage comparator becomes more negative than input J39-2, the comparator output goes LO. This LO clears the Data Window FF, which in turn clears the Separator FF and terminates the data window period.

In the foregoing example, no data pulse was received, so the timer simply timed out and closed the window. If a data pulse does occur, the leading edge of the data pulse out of gate F25-8 resets the Data Window FF, which interrupts the Data Window Timer. At the trailing edge of the data pulse, gate output F30-8 goes LO and resets the Separator FF, thereby closing the data window.

Transistor H43 in the Data Window Timer is used to equalize the current drawn by this circuit during its active and inactive states. When transistor J41 is ON, transistor H43 is OFF, and vice versa. This prevents current fluctuations that could couple noise into the low level analog circuits.

Data magnetically recorded on a disk is subject to a phenomenon known as "pulse-crowding". This necessitates lengthening the data window if the previous data bit was a 0 (clock pulse without data pulse). By turning on current source J45, the charge current available to capacitor J43 is reduced, thereby lengthening its charge time.

For the Unseparated Data Option, switch S4 is closed. This enables the Data Gate to pass both data and clock pulses onto the +READ DATA interface line.

4.3.5.6.6B VFO Data Separator - Optional (#12110)

Refer to Figure 7-19, VFO Data Transfer PCB Schematic (Sheet 4).

The VFO data separator may be divided into the following functional groups:

- Start and Reset Logic - consisting of the Start Clear O/S (F35-6), VCO Enable FF (H35-9), and associated circuitry.
- Phase Lock Loop - consisting of the Lag FF (K36-9/8), the Lead FF (K36-5/6), the Lag/Lead Reset FF (H35-5/6), the Bidirectional Current Source (K45, K49, K46, K50), the VCO (Voltage Controlled Oscillator - E23), and associated circuitry.
- Data/Clock Separator - consisting of flip-flops H25, K16, L16, and associated circuitry.
- Data/Clock Phase Detection and Selection - consisting of the Phase Detect Counters (H15, H16), the Phase Select FFs (L26), and the Phase Selector (E16).

Start Clear Logic

When +READ GATE goes HI, the Start Clear O/S (F35) generates a 1 usec LO pulse to clear the VCO Enable FF, the Lag and Lead FFs, and the Phase Select FFs. Following this initial clear, the Lag/Lead Reset FF sets on receipt of the first clock or data pulse. This releases the forced clear condition of the Lag and Lead FFs. Meanwhile, the pulse received passes through a 100 ns delay line (F44) and sets the VCO Enable FF. The resulting HI from H35-9 enables gate F25-8 to pass the VCO output to the CLK input of the Lag FF.

Phase Lock Loop

After a small additional delay by inverters L36-2 and L36-4, the data or clock pulse is applied to the CLK input of the Lead FF.

If the VCO signal and data/clock pulses are synchronized, the Lead FF and Lag FF will set at exactly the same time. This raises both inputs to gate K26-3 simultaneously, clearing the Lag/Lead Reset FF, which, in turn, immediately clears both the Lead FF and Lag FF.

If the data/clock pulse is leading the VCO, the Lead FF will set before the Lag FF. Conversely, if the data/clock pulse is lagging the VCO, the Lag FF will set before the Lead FF. When the second flip-flop sets, both flip-flops are immediately cleared. The duration of time between the setting of the Lag and Lead flip-flops represents the degree of phase error between the data/clock signal and VCO.

In the case of a lead error, the LO level at output K36-6 of the Lead FF turns on transistor K46 of the Bidirectional Current Source. This draws the top end of capacitor E44 towards a positive potential as the capacitor charges positive. The actual potential reached depends on the length of time that the Lead FF remains set. This positive potential is applied to the top end of

varicap E33 in the VCO circuit. The increased voltage across the varicap lowers its capacitance and thereby increases the VCO frequency. As the lead error diminishes, the potential applied to the varicap diminishes. When the VCO and data/clock signal lock into phase, the error potential applied to the top end of the varicap will be 0 volts nominal.

A lag error will produce just the opposite effect, by turning on transistor K50 in the Bidirectional Current Source. Capacitor E44 charges negative and reduces the potential across the varicap, thereby decreasing the VCO frequency.

Phase lock and frequency correction are accomplished most quickly by reading a series of 1-bits. The pulse frequency for 1s is twice the frequency for 0s, thus allowing closer control of the lag and lead error voltages to avoid frequency overshoot during the initial frequency correction.

Voltage Controlled Oscillator (VCO)

The major components of the VCO are the tank circuit comprised of coil E28 and varicap E33, transistor E23, and the feedback path provided by gate F25-6.

The free-running frequency of the VCO is 5.08 MHz nominal, and is obtained when the top end of the varicap is at 0 volts and the bottom end is at approximately -7 volts. The free-running frequency is adjusted by the 5K pot, E39.

An increase of potential across the varicap reduces its capacitance and increases VCO frequency. A decrease of potential produces the opposite effect.

Zener diode E13 and capacitor E14 provide an isolated +5V supply for the VCO.

Data/Clock Separator

FF H25-9/8 switches at 1/2 VCO rate. The alternate HI/LO outputs of this flip-flop steer the data pulses and clock pulses into FFs K16-9/8 and L16-9/8. Which FF will receive the data pulses and which the clock pulses is indeterminate, since it depends on the phasing of the Data/Clock FF (H25-9/8) when phase lock occurs. However, during a single read operation, all of the clock pulses will go through one of these two FFs and all of the data pulses will go through the other. The Phase Selector (E16) will ensure that the clock pulses end up at the +READ CLOCK output and the data pulses end up at the +READ DATA output. The waveforms in Figure 4-34 show one example of data/clock signal separation, wherein the data pulses are passing through FFs K16-9 and K16-5, and the clock pulses are passing through FFs K16-9 and L16-5.

Data/Clock Phase Detection and Selection

The two channels through the data/clock separator are monitored by two binary counters (H15 and H16). Counter H15 clocks on the output of FF L16-9 and clears on the output of FF K16-8. Conversely, counter H16 clocks on the output of FF K16-9 and clears on the output of FF L16-8. With this configuration, a counter is incremented by each pulse on one of the channels and cleared by any pulse on the other channel.

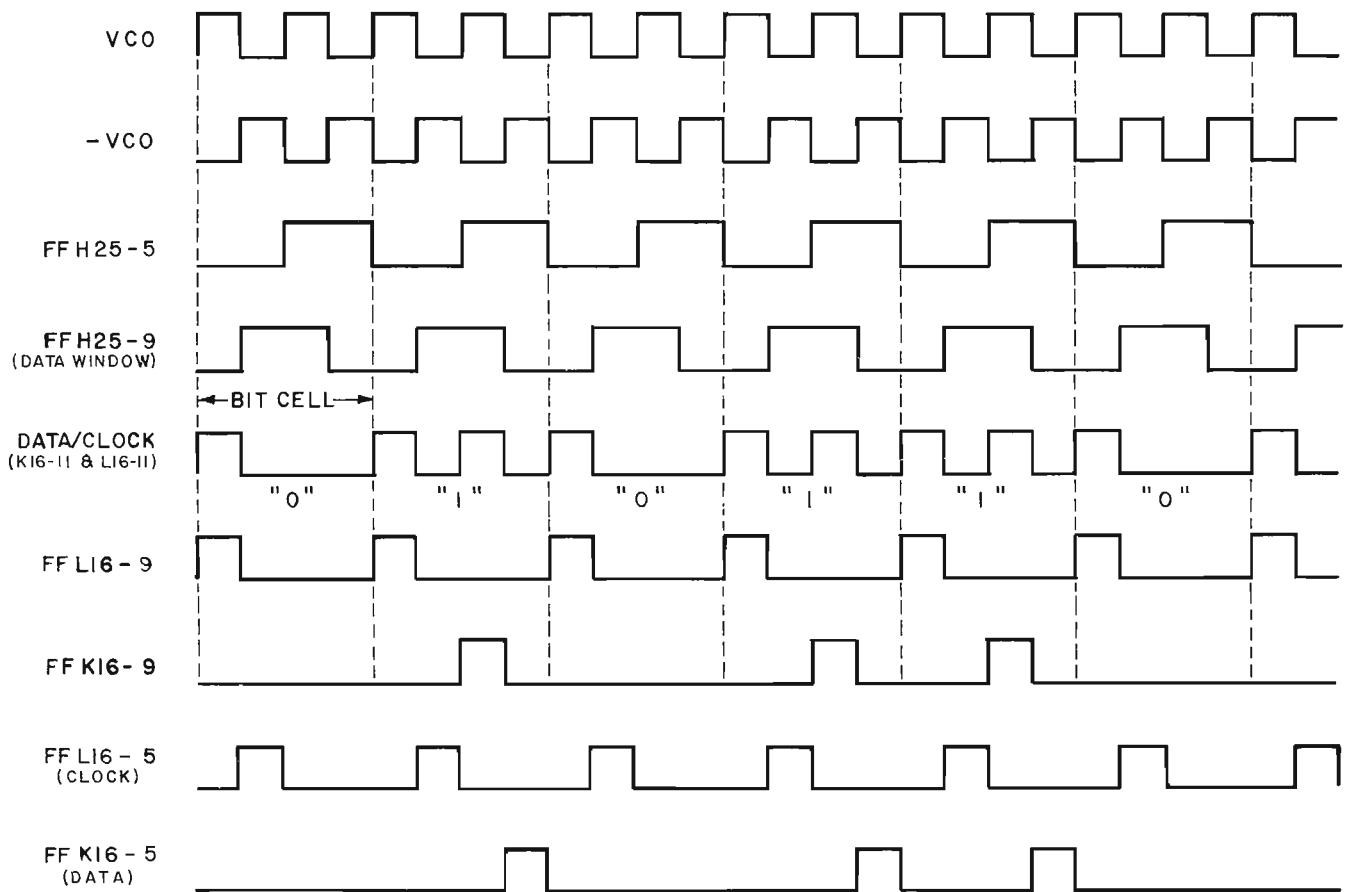


Figure 4-34. VFO DATA SEPARATION

When eight consecutive zeros appear in the format, eight clock pulses will pass through one of the channels while no pulses pass through the other channel. On the eighth pulse, the QD output of one of the counters goes HI. This clocks either FF L26-5/6 or FF L26-9/8 to its set state. The resulting LO at Phase Selector input E16-15 enables the Phase Selector. At input E16-1 of the Phase Selector, a HI will allow the B inputs to pass to outputs 1Y and 2Y, whereas a LO will allow the A inputs to pass. By this selection process, the clock pulses pass to the +READ CLK output line, and the data pulses pass to the +READ DATA output line.

4.3.6 Power Driver (P/D) PCB (#12062)

The Power Driver PCB contains the following circuits.

- (1) Spindle Motor Drive Circuits
- (2) Braking Timer Circuit
- (3) Head Positioner Motor Drive Circuits
- (4) Voltage Sense And Emergency Retract Circuits
- (5) Cartridge Unlock Circuit

4.3.6.1 Spindle Motor Driver

The spindle motor is an AC induction motor with two stator windings phased 90 electrical degrees apart. Drive for the motor requires a nominal 48 volt AC signal applied to each stator winding, with the Phase 1 signal leading the Phase 2 signal by 90°. The rotational rate is proportional to the frequency of excitation, which is slightly above 80 Hz for 2400 RPM and slightly above 50 Hz for 1500 RPM. Rotor slip is compensated for by the speed control logic on the Logic PCB which provides automatic frequency control to hold the disk speed within $\pm 0.2\%$ of its nominal value. Braking of the motor is accomplished by applying a DC signal to the Phase 1 winding and turning off the Phase 2 winding drive. Power dissipation in the motor and driver circuits is limited through the use of a switching current regulator.

PHASE 1 and PHASE 2 are the square wave input signals for the two driver circuits. The -PHASE 1 ENABLE and -PHASE 2 ENABLE signals enable or disable the inputs to the spindle motor driver circuits.

A block diagram of the driver for a single stator winding is shown in Figure 4-35. The driver consists of two input amplifiers, four current switches, a current sense resistor, four "free wheeling" diodes and two current feedback circuits. Circuit operation is described in the following paragraphs.

The input amplifiers convert the PHASE 1 squarewave input signal into two complementary trapezoidal waveforms, entitled PHASE 1A and PHASE 1B, with amplitudes of +15V and -15V when the motor is being driven. The PHASE 1 signals are in quadrature (different by 90°) with the Phase 2 signals. During the LOAD function of the disk drive, the outputs of the input amplifiers are held at 0V \pm .8V, turning off the current drivers and permitting no current to flow in the stator winding.

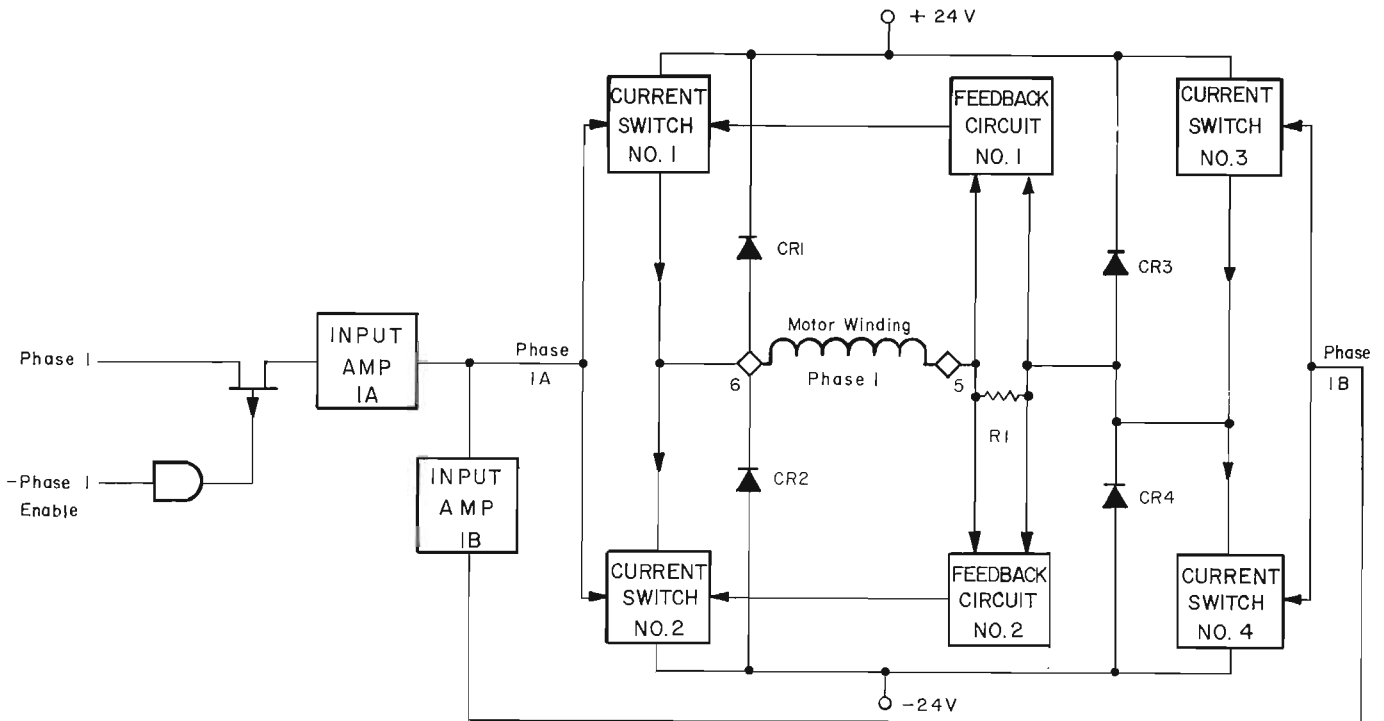


Figure 4-35. SPINDLE MOTOR PHASE I DRIVER

During the positive level of PHASE 1A, current switch 1 is turned on, applying +24V to motor winding terminal 6. Simultaneously, the negative level of PHASE 1B turns on current switch 4. As current builds up in the motor winding, a voltage appears across the current sense resistor (R1) proportional to the current in the motor winding. When this voltage reaches approximately 0.7V, the action of current feedback circuit 1 causes current switch 1 to turn off. The voltage at terminal 6 then switches from +24V to approximately -24V, where it is limited by the clamping action of diode CR2. As the decreasing current flow through the current sense resistor reaches the lower feedback threshold, current switch 1 is again turned on, repeating the cycle. This action continues as long as the PHASE 1A signal remains positive and PHASE 1B remains negative, limiting the current to an average of 4 amperes. Current switch 2, current feedback circuit 2, diode CR1 and the current sense resistor perform this current limiting function during the alternate half cycle of PHASE 1A and PHASE 1B.

Additional current limiting at approximately 4.7A is provided in the circuitry of current switches 3 and 4 to protect the power devices from overstressing in the event of a component failure.

CAUTION

Probing of the Power Driver Board with power applied should be avoided because of the danger of accidental shorts which may destroy a power stage. Operation of the Driver Circuits with a non-inductive dummy load will result in excessive dissipation in the switching current regulator circuit due to the increases switching frequency.

No adjustments are required to the Spindle Motor Driver circuits and no restrictions apply to the input signal duration as long as the power devices are correctly mounted on the Heat Sink. The action of the switching current regulator reduces the device dissipation since the devices are in saturation, dissipating little power, or cut off, dissipating no power. The primary power dissipation occurs while the device is switching.

Pertinent waveforms are shown in Figure 4-36. The PHASE 1A voltage waveform shows the typical trapezoidal input waveform as a solid line and its minimum limit as a dotted line. The motor winding terminal 5 waveform indicates the expected signal at this terminal, corresponding to the PHASE 1A waveform shown. The motor winding terminal 5 waveform indicates the expected voltage at this terminal as the motor builds up speed. As the motor speed increases, the back EMF of the motor limits the current to an average value of approximately 1.5A, and the switching current regulator operates, if at all, only on a peak current. Motor current is indicated in the lower waveform.

4.3.6.2 Braking Timer

Refer to Figure 7-13, Power Driver PCB Schematic (Sheet 1).

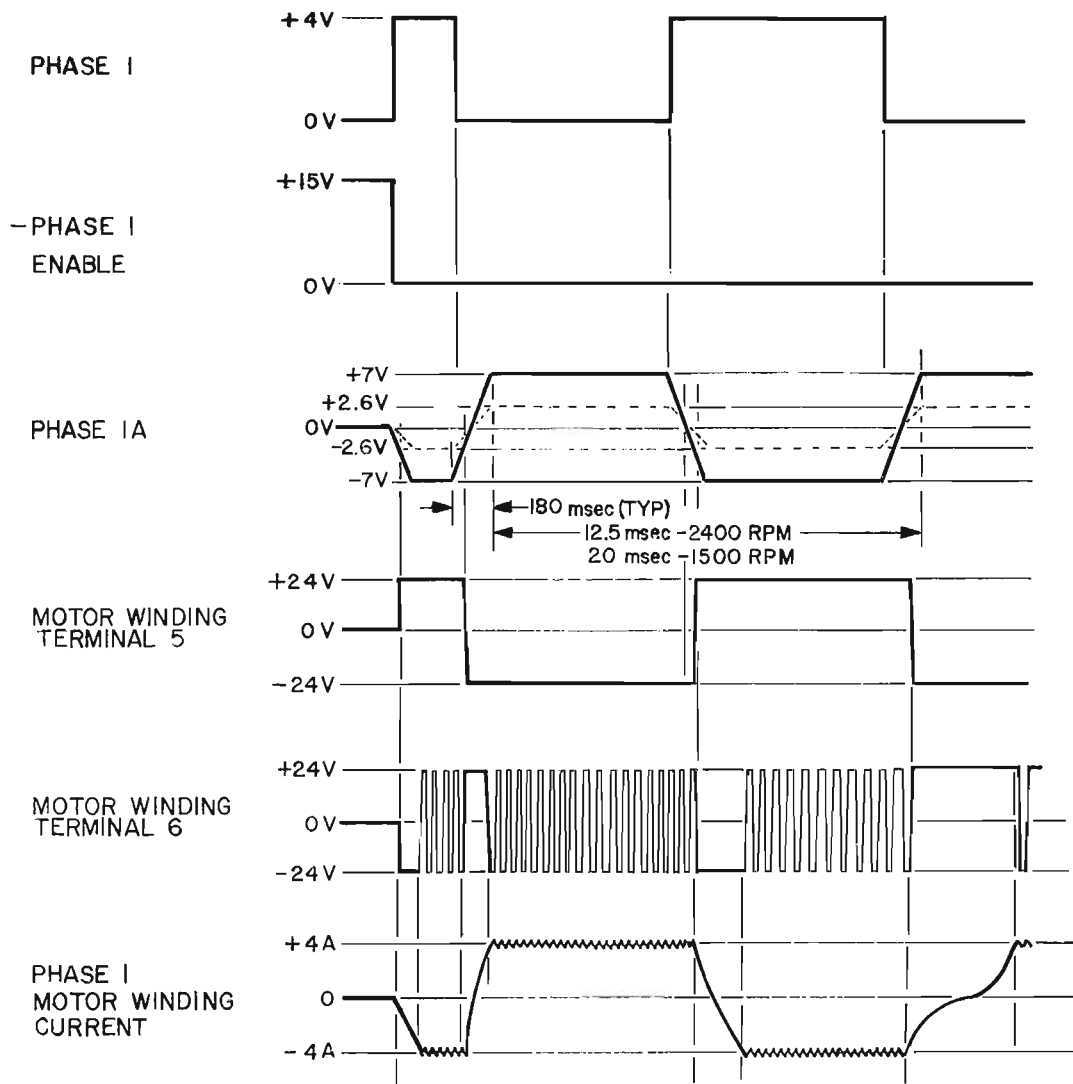


Figure 4-36. SPINDLE DRIVER WAVEFORMS

The braking timer (K15) establishes the 30 second time interval during which dynamic braking is applied to the spindle motor when the disk drive is switched from RUN to LOAD. During that time, a DC signal of +7 volts is applied to Phase 1A, -7 volts to Phase 1B, 0 volts to Phase 2A and 0 volts to Phase 2B. This results in a continuous HI at gate output F21-3, and capacitor K22 begins charging through resistor K20. When the voltage on K22 reaches the threshold level of the timer, after approximately 30 seconds, the output of the timer (-SPINDLE STOPPED) goes from HI to LO. By this time the spindle has stopped rotating. -SPINDLE STOPPED is sent to the Logic PCB where it turns off PHASE 1 which is no longer needed for braking.

-SPINDLE STOPPED is HI during the Run mode and 30 seconds into the Load mode.

4.3.6.3 Positioner Motor Driver

Refer to the Servo Driver portion of Figure 6-14, Power Driver PCB Schematic (Sheet 2).

Current for the head positioner motor is provided by a network similar to current switch 3 and current switch 4 of the spindle motor driver circuit. The major functional difference in this network is that the current developed for small signals is directly proportional to the amplitude of the drive signal. For large signals, the current is limited to approximately 7A by feedback from the current sense resistor (B47) to the Feedback Summation Amplifier. Currents of this magnitude for longer than 32 milliseconds cause a "SEEK INCOMPLETE" signal to be generated. A block diagram indicating the functional divisions of the positioner motor driver is shown in Figure 4-37. These divisions are: (1) an Input Amplifier, (2) a Servo Release circuit to release the head positioner from servo control, (3) a Feedback Summation Amplifier to limit motor current by negative feedback, (4) a Power Driver to provide adequate drive current for the positioner motor, (5) an Emergency Retract Driver to retract and unload the heads if an out-of-tolerance voltage condition is detected, (6) a voltage Check circuit to produce an emergency retract command if a supply voltage failure occurs, and (7) an Over-Current Detector circuit.

The SERVO DRIVE signal is an analog signal generated on the Servo (SO) Board. When positive, the SERVO DRIVE signal turns on the positive driver network. When the heads are detented (held stationary over a track), any motion of the heads away from the detent position causes the SERVO DRIVE signal to generate an opposing signal. Since positive drive current causes the positioner carriage to move toward the spindle, attempting to manually move the positioner carriage toward the spindle will cause negative drive current to flow in the motor. The amount of current flowing will be proportional to the amount of force applied, up to the limit of 7 amperes.

The servo driver may be released from control by the SERVO DRIVE signal by two different means: (1) by a HI SERVO RELEASE signal, which occurs when the positioner is in the home position and no -RETRACT signal is present; and (2) by manual operation of the Servo Release switch. Head crash will occur if the spindle is stopped with the heads over the disk; consequently, the Servo Release switch should not be used if spindle power is off.

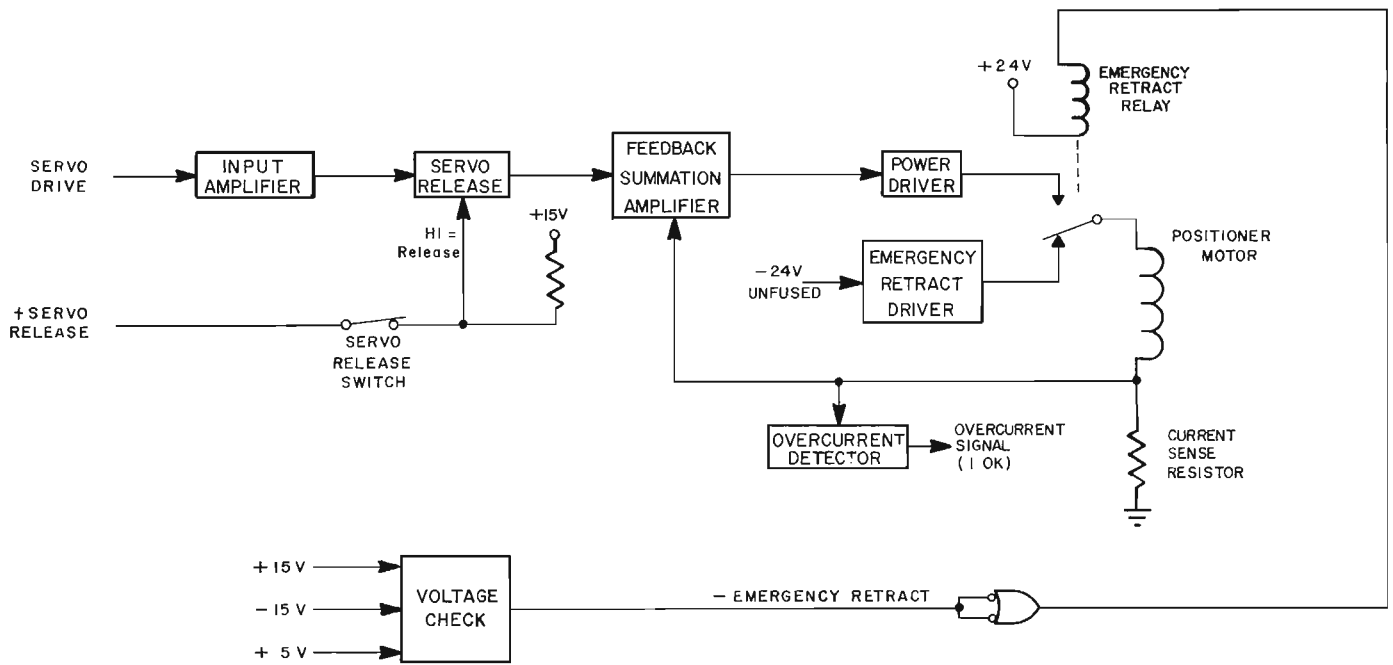


Figure 4-37. HEAD POSITIONER DRIVER BLOCK DIAGRAM

When the spindle motor drive is off, -PHASE 2 ENABLE turns off transistor E59 to remove +24 volt power from the positioner driver transistor. This eliminates the possibility of head and disk damage caused by the positioner being driven over the disk in the event of a positioner driver transistor failure.

The overcurrent integrator has a time constant of 47 milliseconds and the overcurrent detector a threshold of 0.54 volt. The resulting time constant for the combination of the integrator and the detector for a full current condition (7A) is 32 milliseconds for currents of either polarity. At the end of the time constant, the overcurrent signal will go low. Lower current values cause longer delay times, and values less than 2.7A are below the threshold of the detector circuit.

4.3.6.4 Voltage Check And Emergency Retract

Refer to Figure 7-14 Power Driver PCB Schematic (Sheet 2).

The purpose of these circuits is to perform an emergency retract operation in the event of a failure or out-of-tolerance condition of any of the supply voltages.

The voltage check circuit senses the +15 VDC, -15 VDC and +5 VDC. This also indirectly includes the +24 VDC and -24 VDC, since +15V and -15V are derived from them. The +15 VDC and -15 VDC are monitored for both overvoltage and undervoltage. The +5 VDC is monitored for undervoltage by the voltage monitor circuit on the Power Driver PCB, while overvoltage protection is provided by a circuit in the +5 VDC power supply. If a failure or out-of-tolerance condition occurs, the output signal (-EMERGENCY RETRACT) of the voltage check circuit goes LO.

The emergency retract circuit utilizes a relay and the unfused -24V power supply to retract the heads when the -EMERGENCY RETRACT signal goes LO. When this occurs, relay A30 is deenergized by the HI output of gate F21-5. This disconnects the positioner motor from the servo driver output and connects it to the emergency retract driver. Darlington E38 is biased "on" by the charge current of capacitor D54, which produces a drive current of about 3A for approximately 15 milliseconds. This drive current accelerates the positioner to a velocity sufficient to overcome the head-unload ramp resistance. Resistor B75 maintains a lower level of drive current after initial acceleration of the head positioner.

4.3.6.5 Cartridge Unlock Driver

Refer to Figure 7-14, Power Driver PCB Schematic (Sheet 2).

The cartridge unlock solenoid driver is controlled by the -CTG UNLOCK signal. When -CTG UNLOCK is HI, the driver transistor is off and the solenoid remains in its deenergized locked position. When -CTG UNLOCK goes LO, capacitor F15 begins charging and the driver transistor conducts heavily, providing pull-in current to the solenoid. As the capacitor charges, conduction through the driver transistor decreases and its emitter voltage rises. When the emitter voltage has risen to +12 volts, current flow through the driver transistor levels off and remains constant, supplying holding current for the solenoid.

4.3.6.6 +24V Regulator

The +24V Regulator (M7) provides overvoltage protection for the front panel indicator lamps.

4.3.7 Power Supply Assembly (#19033)

4.3.7.1 General Characteristics

The internal power supply assembly of the Model 44B performs the following functions:

- 1) Produces the DC voltages required by the disk drive circuits:

+24 VDC/-24 VDC/-24 VDC UNFUSED
+15 VDC/-15 VDC
+5 VDC

- 2) Produces an "AC OK" signal to indicate the status of AC input power.
- 3) Provides on-off control and power for the brush motor.
- 4) Provides power for the fan motor.

The Model 44B power supply is adaptable to any one of four different AC input voltages: 100, 120, 220 or 240 VAC at 49 to 61 Hz. The disk drive is set for the appropriate input voltage by a small 4-position voltage selector printed circuit card. This card is located in the fuse compartment near the on-off switch at the rear of the machine. To adapt the drive to a different input voltage, the selector card is simply pulled out, turned to the desired position (as indicated on the card), and reinserted.

4.3.7.2 Theory of Operation

Refer to Figure 7-15.

- 1) +24 VDC/-24 VDC/-24 VDC UNFUSED

The circuit to develop these voltages consists of a standard bridge rectifier with center-tapped transformer winding and capacitive filter. No regulation is required. The +24 VDC and -24 VDC are both fused at 15 A. In addition, a -24 VDC UNFUSED output is provided to drive the emergency head retract circuit.

- 2) +15 VDC/-15 VDC

These two voltages are derived from the +24 VDC and -24 VDC by an integrated voltage regulator, H24. The regulator senses the voltage across the sensing resistors, H32 and H33, and controls the series pass transistors, H10 and E10 accordingly.

- 3) +5 VDC

The +5 VDC supply includes a standard bridge rectifier circuit with capacitive filtering at its output.

Overvoltage Protection - Overvoltage protection is provided by a silicon controlled rectifier (SCR) at E63. When overvoltage occurs, the SCR fires, shorting the rectifier output and causing the 7 A fuse, A42, to open.

The overvoltage protection circuit consists of the SCR, capacitors E37 and E40, resistor E39, diode E41 and 5-volt zener diode E42. The resistor, diode and zener form a voltage divider network, with the positive end of the resistor connected to the SCR gate. As long as the rectifier output voltage remains below approximately 6.5 volts, the voltage across the resistor will be less than 0.8 volt, since the voltage drop across the zener and diode E41 is constant at approximately 5.7 volts. Any increase in the rectifier output appears across the 100 Ohm resistor and is applied to the SCR gate. If the gate voltage reaches about 1.25 volts, the SCR fires, drawing heavy current and opening the 7 A fuse.

Capacitors E37 and E40 prevent firing of the SCR by transients reflected by the load.

Voltage Regulation - Regulation of the +5 VDC is accomplished by an integrated regulator (D30) which varies the voltage dropped across a series pass transistor (B62) to compensate for changes in the output voltage.

The integrated regulator is connected as a positive voltage regulator with foldback current limiting. The regulator compares the +5 VDC output voltage, applied to pins 3 and 4, with an internal reference voltage. If the +5 VDC drops, the regulator increases the drive to the base of transistor H60, which in turn increases drive to transistor B62. This reduces the voltage dropped across transistor B62, to compensate for the drop in the +5 VDC output voltage.

The amplitude of the +5 VDC output is adjustable by means of the 500 Ohm potentiometer at D31. This pot varies the internal reference voltage of the integrated regulator.

Current Limiting - The foldback current limiting circuit consists of a 0.01 Ohm current sensing resistor at D48, operational amplifier E30, the integrated regulator at D30, the series pass transistor B62, and associated circuitry.

The voltage across the current sensing resistor is applied to pins 2 and 3 of the operational amplifier, which has an amplification factor of about 10. The output at pin 1 is applied to a voltage divider consisting of resistors E24 and E25. The top of resistor E24 connects to the current limit input at pin 2 of the regulator. When the voltage between pins 2 and 3 of the regulator exceeds 0.65 volts, the regulator turns off the Darlington amplifier. This causes the series pass transistor to become a high impedance, reducing the current to approximately 2.5 A. This action occurs when the +5 VDC load current reaches about 7A.

The four diodes at pin 4 of the operational amplifier set the negative Vc at -2.8 volts.

4) AC OK

The central element of the AC OK circuit is a type 555V timer connected as a retriggerable one-shot. The values of resistor E16 (39K Ohms) and capacitor D24 (1 mfd.) are selected to produce a one-shot time interval equivalent to slightly more than one AC cycle.

During each negative half cycle of AC at transformer terminal 9, a negative pulse is coupled through capacitor D15 and resistor D21. Each of these negative pulses retriggers the one-shot at input D20-2 to renew the time interval, and also turns on transistor E13 to discharge capacitor D24. As a result, the +AC OK output of the one-shot at D20-3 remains HI.

Upon loss of AC power, the negative pulses no longer occur. As a result, capacitor D24 continues to charge. After a period of time equal to slightly more than one AC cycle, the potential at the positive end of capacitor D24 will have reached the time-out threshold of the one-shot. At that point, the output of the one-shot (+AC OK) will drop.

Diode E18 limits the negative excursion of the retrigger pulses to 0.7 volt.

5) Brush Motor

The 24 volt brush motor is switched on and off by triac B15. When +BRUSH ENABLE is HI, transistor B24 turns on. This raises the gate potential of the triac and turns it on. With the triac turned on, the brush motor is effectively connected across terminals 6 and 7 of the transformer.

6) Fan Motor

The 24 volt fan motor connects directly across terminals 6 and 7 of the transformer.



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SECTION 5

MAINTENANCE

5.1 GENERAL MAINTENANCE INFORMATION

5.1.1 Maintenance Requirements

Reduced preventive and corrective maintenance are inherent in the Model 44B Disk Drives. Alignments are simple to perform and infrequently required (see paragraph 5.6.1). Spindle speed and head position are controlled electronically, with a minimum amount of mechanical hardware. As a result of this design, normal preventive maintenance is reduced to cleaning and air-filter replacement, as described in Paragraph 5.4.

5.1.2 Maintenance Instructions

The Model 44B user should consult Paragraph 5.2 of this manual, compare the lists with his existing or projected tools and test equipment, and determine the level of maintenance capability he intends to maintain. Preventive maintenance is described in 5.4, while corrective maintenance is covered by 5.5. Prior to performing any alignment or maintenance, the user should familiarize himself with the location of assemblies in the Model 44B, as shown in Paragraph 5.3. Particular attention is invited to Paragraph 5.7.1, which gives the location, within this section, of instructions for replacement of the various parts and assemblies.

5.1.3 Maintenance Precautions

To avoid damage to the Model 44B or an associated disk cartridge, observe the following precautions during maintenance:

1. Electronic detenting holds the head carriage in position when power is applied. Do not attempt to move the carriage by hand unless the spindle is rotating at operating speed and the servo release switch is in the release position. This switch is located on the Power Driver PCB. With the spindle stationary, or rotating below operating speed, head crash will occur if the R/W heads are moved out over the disks.
2. Never connect or disconnect any cable assembly to or from the Model 44B with AC power applied.
3. When the lower disk is exposed, avoid scratching, nicking, fingerprints or other contact with the coated surface of the disk.
4. Keep the Model 44B as clean as possible. When the drive is open for maintenance but is not actually being worked on, protect it from dust with a lint-free cover. The assembled disk drive should never be stored without either a cartridge dust cover or a plastic bag in place.
5. When the top cover is in place, the drive should be left in the RUN mode whenever possible. This will insure that clean air will be drawn through the filter and supplied to the interior of the disk drive.

6. Before defeating interlocks to remove cartridge with power off, ensure that the brushes and R/W heads are fully retracted.

5.2 REQUIRED TOOLS, TEST EQUIPMENT, AND SPARES

5.2.1 Levels of Maintenance

This paragraph (5.2) describes the tools, test equipment, and spares required for preventive and corrective maintenance of a Model 44B Disk Drive. For brevity, common hand tools are not listed in the manual. Preventive maintenance of the drive is simple, and it is assumed that all users will perform such maintenance themselves. Corrective maintenance capability varies greatly between organizations. Some Model 44B users may have a trained service force, spare drives, and complete facilities, whereas others may be limited to circuit-board replacement. Consequently, the corrective maintenance described in this manual is divided into three levels, each requiring successively more extensive test equipment, spares, and technical capability of personnel. The test equipment and spares are listed separately in 5.2.3 for the different levels. For corrective maintenance beyond the user's capability, contact Diablo Customer Service. As used in this manual, the corrective maintenance levels are as follows:

1. LEVEL 1 - minimum corrective maintenance. Substitution of circuit boards. Simple component replacements and adjustments, not requiring significant disassembly of the drive.
2. LEVEL 2 - Level 1 maintenance plus replacement and alignment of R/W heads. Component replacement requiring limited disassembly of some parts of the drive.
3. LEVEL 3 - Level 2 plus major disassembly, reassembly, and alignment.

In the following lists, all parts numbers shown are Diablo part numbers.

5.2.2 Preventive Maintenance Items

The following items should be available to each person servicing a disk drive on a scheduled basis:

- a. Head cleaning pads, 91% isopropyl alcohol (Texpads, or equivalent) P/N 99000-01
- b. Air filters, P/N 19052
- c. Touch-up lacquer, P/N 99004-01 (gray), -02 (brown), -03 (white) (1 bottle each)
- d. Adhesive tape
- e. Tongue depressors
- f. Cotton swabs
- g. Metal cleaner, P/N 70677 (bottle)

5.2.3 Corrective Maintenance Items

5.2.3.1 Level 1 Maintenance

- a. Pluggable PCB's (1 each)
- b. Extender board: P/N 41241
- c. Power transistors, (3 each type)
- d. Lamp, miniature flange, 28V; P/N 10545-01 (12)
- e. Disk Cleaning Brush, P/N 16082
- f. Oscilloscope, vbw \geq 50 MHz, vds \geq 100 mV/cm, sweep speed \geq 50 ns/cm

5.2.3.2 Level 2 Maintenance

- a. All Level 1 maintenance items.
- b. Diablo Model 500 Exerciser/Tester.
- c. Alignment cartridge, P/N 70306 (100 tpi), 70709 (200 tpi), or 71299 (200 tpi; required for head positioner azimuth adjustment).
- d. Set of R/W Head Assemblies, P/N 25129-01, -02 (200 tpi); 25128-01, -02 (100 tpi, 2400 rpm); 25127-01, -02 (100 tpi, 1500 rpm).
- e. R/W Head Alignment Filter Plugs (2), P/N 41262.
- f. Head Cable Extenders (4), P/N 41261.
- g. Plastic feeler gauges (1 set).
- h. Torque screwdriver, P/N 99001.
- i. Allen wrench, 9/64, for torque screwdriver.

5.2.3.3 Level 3 Maintenance

- a. All Level 2 maintenance items.
- b. Spindle Assembly, P/N 19161.
- c. Head Positioner Assembly, P/N 19003.

5.3 LOCATION OF ASSEMBLIES

Figure 5-1 shows some of the major assemblies of the Model 44B. The locations of the PCB's within the Card Cage are shown in Figure 5-2.

5.4 PREVENTIVE MAINTENANCE

5.4.1 Preventive Maintenance Philosophy

The principle of maximum machine available time governs the preventive maintenance recommendations contained herein. Unless a preventive maintenance procedure increases overall machine available time, it is not recommended. Except for the procedures recommended in Paragraph 5.4.2, no maintenance or adjustment should be performed on a drive that is operating satisfactorily.

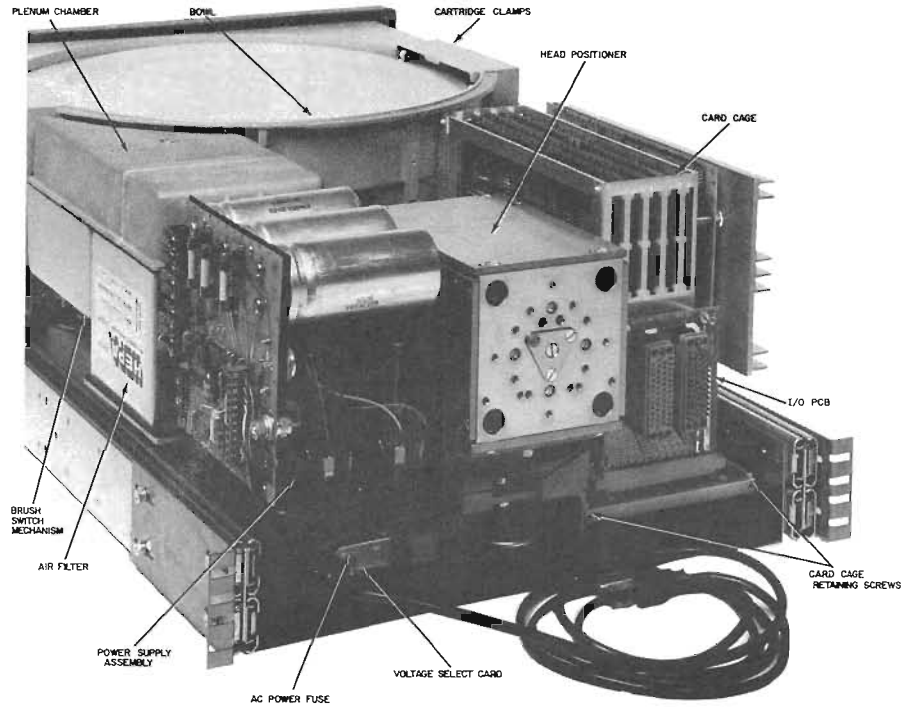


Figure 5-1. LOCATION OF ASSEMBLIES

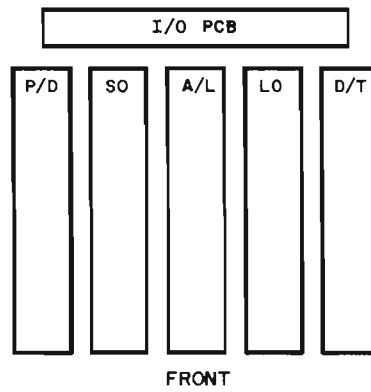


Figure 5-2. CARD CAGE PCB LOCATIONS

5.4.2 Preventive Maintenance Procedures

Table 5-1 summarizes the recommended preventive maintenance procedures, and is based on a one-shift-per-day operation in a normal office environment. Operation in an abnormally dirty environment, a high frequency of cartridge changing, or multi-shift operation would increase the frequency of preventive maintenance required. In addition to the maintenance listed in Table 5-1, the base plate should be wiped with a lint-free cloth and vacuumed whenever the bowl is removed.

Table 5-1.
Preventive Maintenance Action

Interval	Action	Paragraph
Semi-annually	Clean and inspect R/W Heads	5.4.2.1
Semi-annually	Clean and inspect magnetic ring	5.4.2.2
Semi-annually	Replace air filter	5.4.2.3

Prior to performing any of the preventive maintenance procedures listed in Table 5-1, ensure that there is no disk cartridge installed, and that power to the Model 44B is off. See Paragraph 5.6.2(2) for removal of disk cartridge with power off. Remove the top cover as described in 5.7.1.1

5.4.2.1 Cleaning of R/W Heads

In order to clean the R/W heads, the card cage must be pulled back to provide access to the lower heads. To accomplish this, proceed as follows:

1. Unplug the R/W head connectors from the D/T PCB.
2. Remove the two card cage retaining screws shown in Figure 5-1.
3. Slide the card cage rearward enough to allow access to the R/W heads.

Access to the lower heads is now possible when the head carriage is all the way to the rear. Clean both lower heads by rubbing lightly with a pad soaked with 91% isopropyl alcohol (Texpad, or equivalent). The pad should be wrapped around a tongue depressor, so that light to moderate pressure can be exerted. Use a lint-free wiper to remove alcohol residue. Clean the upper heads in a similar manner.

Complete removal of all contamination from the heads is mandatory, including fingerprints.

5.4.2.2 Cleaning and Inspection of the Magnetic Ring

Use adhesive tape to remove any particles from the magnetic ring at the top of the Spindle Assembly. If there is any sign of corrosion on the magnetic clutch surface, remove the corrosion as follows:

1. Using a very small quantity of metal cleaner (P/N 70677) on the end of a cotton swab, rub the clutch surface (see Figure 5-3) until the corrosion is lifted. Exercise care to ensure that fluid does not run between the magnet and the clutch.

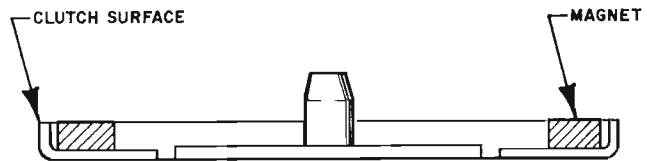


Figure 5-3. CLUTCH SURFACE AND MAGNET

2. Clean the clutch surface with an alcohol pad.
3. Repeat Steps 1 and 2 until all traces of corrosion are removed.
4. Thoroughly clean clutch surface and sides with alcohol. Exercise caution to ensure that the clutch surface is not touched with fingers after performing this step.

5.4.2.3 Replacing the Air Filter

To replace the air filter, first remove the plenum chamber (see Figure 5-1), which is held in place with two screws. Exercise caution so that the gasket around the sealing edges of the plenum chamber is not damaged. The air filter and pad can now be lifted straight up. Install a new air filter and pad, observing the air-flow direction printed on the filter label (arrow up), and replace the plenum chamber. Ensure that both gaskets are well-seated on their sealing edges.

5.5 CORRECTIVE MAINTENANCE

5.5.1 Corrective Maintenance Philosophy

The corrective maintenance philosophy involves two periods - the warranty period and the postwarranty period. While the Model 44B warranty is in effect, corrective maintenance by the user should normally be limited to circuit board replacement; if equipment malfunction cannot be cured by PCB replacement, Diablo should be contacted for technical assistance or to return the unit for repair.

5.5.2 General Troubleshooting Techniques

The recommended first step in troubleshooting is to identify in which of the following categories the malfunction falls:

- Model 44B problem
- Non-Model 44B problem
- Interchangeability problem

If all indications are normal except for the presence of non-intermittent data errors, the problem is probably one of disk pack interchangeability. The alignment of the Read/Write heads may be off. In this case, verify machine alignment by performing the adjustments described in Paras. 5.6.4.3, 5.6.4.4, and 5.6.4.5.

If the problem is not one of disk interchangeability, it should then be determined if the Model 44B is malfunctioning or if the problem is actually originating externally to the disk drive. Check the cartridge seating, verify that all cable connections (including the terminator) are properly made, and that correct signals are being presented to the Model 44B interface. Check that the card cage retaining screws are properly installed. If malfunctioning persists, turn off the AC power, disconnect the I/O cable, and turn on and verify DC power.

Load a cartridge onto the disk drive, and attempt to place the drive in the RUN mode. If the spindle does not start, the problem is with the disk drive, and trouble in the Logic PCB, Power Driver PCB, or mechanical interlocking is indicated. Also, the +5V fuse may be blown.

If the spindle starts, either the READY or CHECK light should come on within one minute, and the corresponding output at the interface connector should be true if the unit is selected.

CHECK light ON indicates trouble in the "write" or "read" circuitry. The READY light on indicates that the cartridge is properly seated, the spindle speed is correct, and heads are loaded.

If neither light comes on within one minute, power or other internal difficulty is indicated.

The Model 44B is designed so that each PCB has well-defined functions, as described in Section 4 of this manual. The interchange of PCBs should be used to isolate faulty PCBs.

5.5.3 Head Crash

A "head crash" (head touches disk surface) is usually detectable audibly. If this occurs, both the disk and the "crashed" head must be replaced as described in 5.7, in addition to rectification of the cause of the head crash. (NOTE: The vast majority of head crashes are due to contamination caused by careless handling and careless operation of the drive, and by failure to replace the air filter at the recommended intervals, see 5.1.3.)

5.6 ADJUSTMENTS

5.6.1 Adjustment Requirements

Table 5-2 shows the conditions under which adjustments are normally required. Except under these conditions, no adjustment should be attempted unless equipment malfunction indicates a definite need for a specific adjustment.

Several of the adjustments described in 5.6 require the use of an alignment cartridge. Instructions in this manual do not pertain to the use of alignment cartridges other than the Diablo Systems cartridge. When using the cartridge for making adjustments on disk drives with the Write Protect Option installed, Write Protect should be set to prevent inadvertent writing on the disk.

In several of the adjustment procedures, the use of a programmable tester (exerciser), while not mandatory, greatly facilitates the adjustments. Where use of the exerciser is specified, the Model 44B user may choose to provide the same interface signals by some other means.

Removal of the top cover, as described in 5.7.1.1, constitutes the first step of each of the adjustments described herein. For simplicity, however, the removal procedure is not cited in each adjustment.

	Adjustments Required								
	Lower Head, Cartridge	Upper Head, Cartridge	Lower Head, Fixed	Upper Head, Fixed	Track 0 Sensor	Carriage Azimuth	Upper Index Transducer	Lower Index Transducer	Brush Mechanism
Replaced									
Lower Head, Cartridge	X								
Upper Head, Cartridge	X	X							
Lower Head, Fixed Disk			X	X					
Upper Head, Fixed Disk				X					
Head Positioner	X	X	X(1)	X(1)	X	X			
Spindle	X	X	X(1)	X(1)	X	X	X	X	
Bowl	X	X	X(1)	X(1)	X		X	X	X
Upper Index Transducer	X	X	X(1)	X(1)	X		X		
Lower Index Transducer	X	X	X(1)	X(1)	X		X	X	
Fixed Disk	X	X	X(1)	X(1)	X		X		

Notes: (1) - No method available for checking adjustment. Dump data from fixed disk before disassembly and reload it after reassembly.

Table 5-2. ADJUSTMENT REQUIREMENTS

5.6.2 Defeat of Interlocks

Some of the adjustment procedures described herein require defeat of one or both interlocks, particularly if the disk drive is being adjusted while installed in a rack. Defeat of the interlocks is accomplished as described below.

CAUTION: Before defeating the cartridge clamp interlock to remove the cartridge with power off, ensure that the R/W heads and brushes are fully retracted.

1. Open the drawer with the power off.
2. Opening the cartridge clamps: With the top cover removed, the cartridge clamps can be spread under any conditions of power, head position, or brush position by manually moving the cartridge clamp interlock link forward. This is most easily accomplished by pulling forward on the link pin of the cartridge interlock solenoid located beneath the bowl on the left side.
3. Operating the Spindle with drawer open and no cartridge installed: The spindle motor can be operated by manual operation of the cartridge interlock switch located inside of the left hand cartridge clamp.

5.6.3 Level 1 Adjustments

There are no adjustments to be performed under Level 1 Maintenance.

5.6.4 Level 2 Adjustments

5.6.4.1 Brush Mechanism Adjustment

1. Lower the front panel to the maintenance position as described in 5.7.1.6.
2. Loosen the three hex head screws which fasten the brush motor plate to right front corner of the baseplate.
3. Remove the plenum chamber by removing the two plenum chamber holding screws.
4. Exerting a light clockwise pressure on the upper brush arm, measure the clearance between the brush bristles and the bowl wall. If the clearance is not $.062 \pm .031$, loosen the jam nut on the eccentric (A) in Figure 5-4, and rotate the eccentric until proper brush-to-wall clearance is obtained. Tighten the jam nut.
5. If the brush motor arm is not in the position as shown in Figure 5-4, manually rotate the brush motor arm clockwise to that position. Insure that the pin is detented in the rear end of the slot in the brush mechanism link, as shown in Figure 5-4.

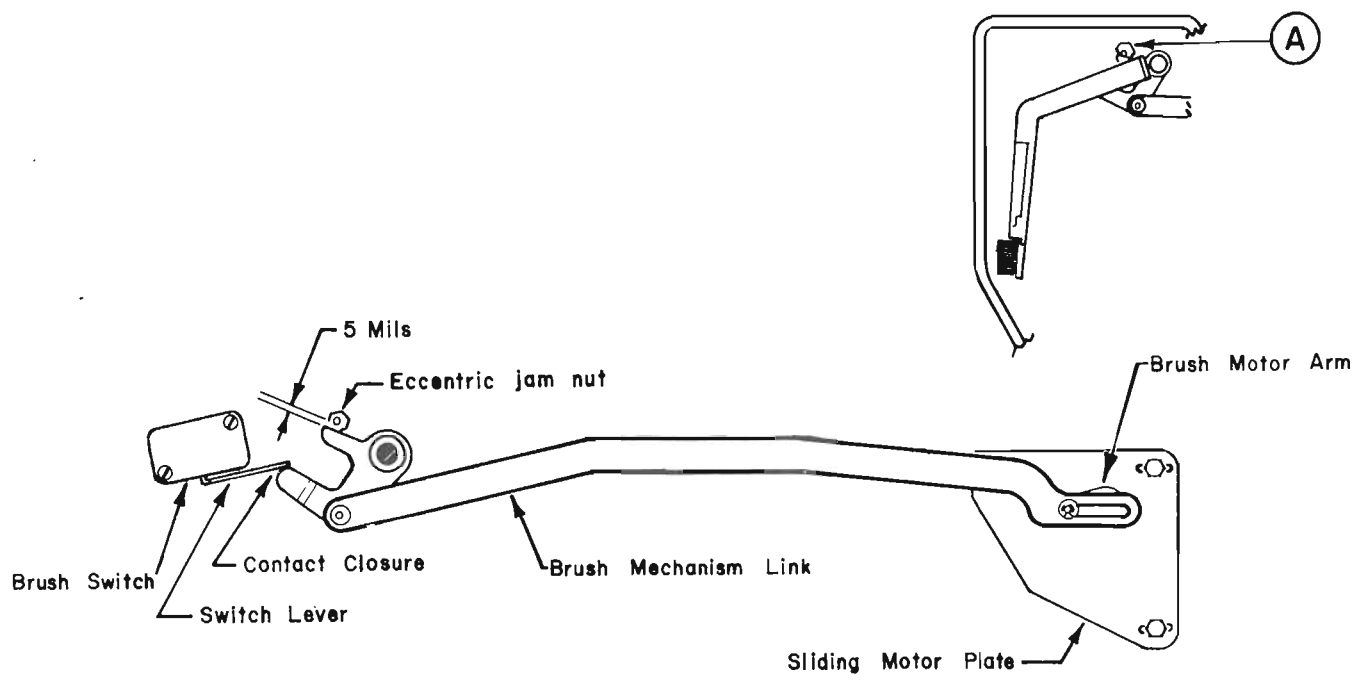


Figure 5-4. BRUSH MECHANISM ADJUSTMENTS

6. Slide the brush motor plate backward or forward to set the clearance between the eccentric and the brush lever to $0.005 \pm .004$. Tighten the three brush motor plate screws.
7. Loosen the two screws holding the brush switch. With the brush mechanism still in the position described in Ste 5, adjust the switch lever to be depressed $.030 \pm .005$ beyond the "make" point. Tighten the two screws.
8. With the cartridge interlock defeated as described in 5.6.2(3), place the drive in the RUN mode, and check for proper operation of the brush mechanism. Brushes should make one cycle and then stop.

5.6.4.2 Lower Index Transducer Adjustment

Place the drive in the RUN mode, and observe the signal at pin 12 of the Logic PCB. The amplitude of the positive peaks should be between 400 and 1200 mV. If the signal falls outside this range, proceed as follows:

1. Place the drive in the LOAD mode and, when able, remove the upper disk cartridge.
2. Remove the lower disk per instructions in section 5.7.2.2.
3. Using a plastic feeler gauge, verify transducer lamination-to-sector ring clearance of $.008" \pm .003"$, as shown in Figure 5-5. If the clearance is out of tolerance, loosen screws A, and add or remove shims (P/N 16358) as required. Retighten screws A just enough to secure the transducer and still allow slight lateral movement.
4. Align the transducer/lamination center line with the spindle hub center, and move the transducer in or out radially until the inner edge of the lamination is approximately even with the base of the sector slots as observed through one of the holes in the hub.
5. Place the drive in the RUN mode, and observe the signal. Being careful not to greatly disturb its radial alignment with spindle center, move the transducer gently in and out to produce optimum signal level.
6. Hold the transducer in this position and carefully tighten screws A. Recheck the signal for proper level, and readjust as necessary.

5.6.4.3 Adjustment of R/W Heads

5.6.4.3.1 Upper Heads

NOTE

The disk drive must be rack mounted or placed on a stable surface and the Track 0 adjustment must be checked before attempting these adjustments.

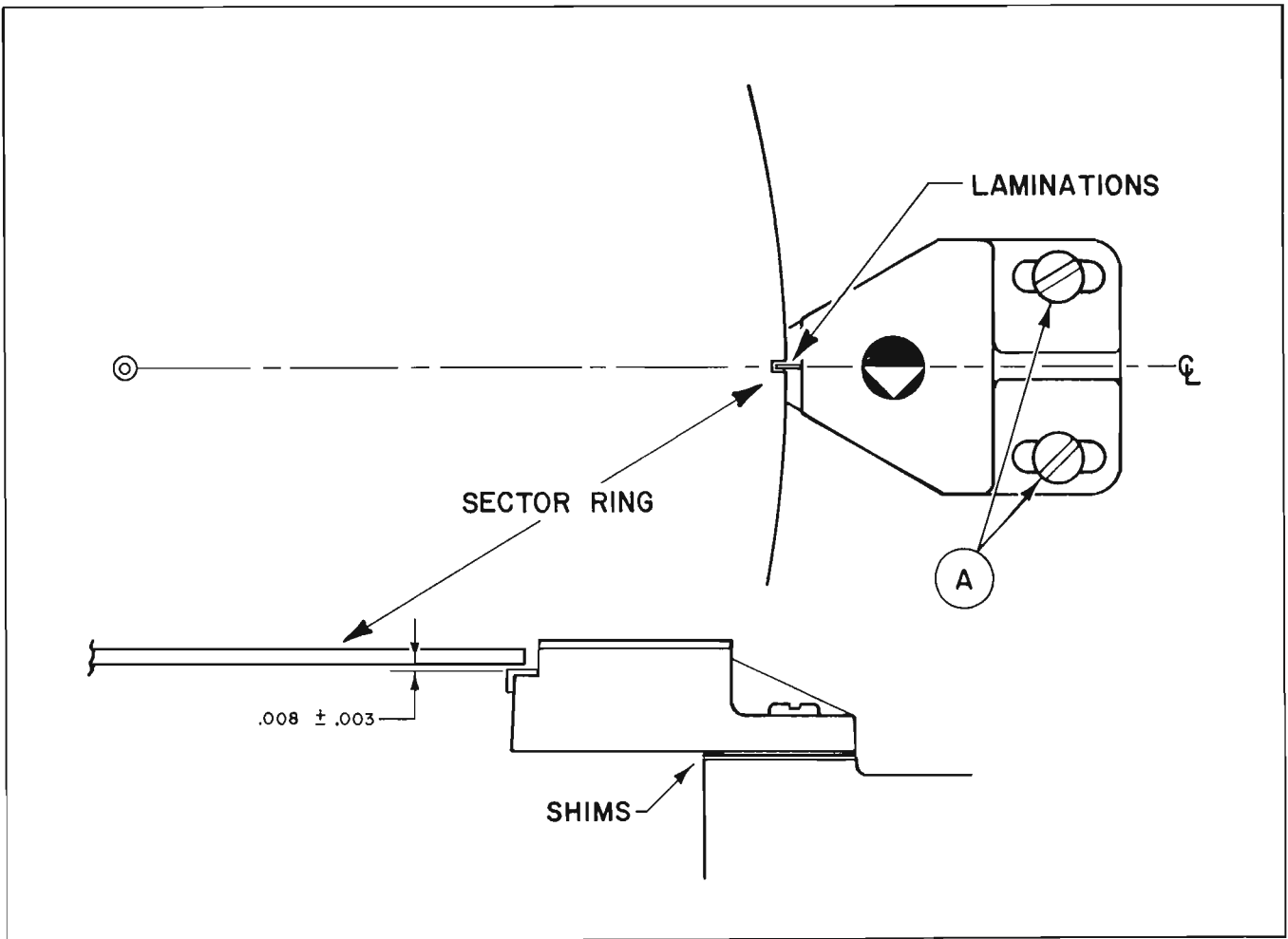


Figure 5-5. LOWER INDEX TRANSDUCER ADJUSTMENT

To adjust the upper heads, an exerciser or other means of positioning the heads to a desired track, an alignment cartridge, oscilloscope, torque screwdriver and R/W Head Alignment Filter are needed. The procedure for adjustment is as follows:

1. Install the alignment cartridge, and then proceed with the alignment, observing the temperature stabilization criteria outlined below.

CAUTION

Thoroughly clean all cartridge/spindle mating surfaces using head cleaning pads listed in 5.2.2. Be certain the cartridge is Write Protected. If Write Protect option is not installed, disable write function at controller or CPU.

Temperature Stabilization

The alignment cartridge shall be temperature stabilized to the disk drive operating temperature prior to attempting alignment.

CAUTION

Only after the disk drive has been temperature stabilized can the alignment cartridge stabilization be accomplished.

Drive Temperature Stabilization

The Model 44B Disk Drive is temperature stabilized after two hours of head-loaded operation from a cold start-up in the recommended machine operating environment.

Alignment Cartridge Temperature Stabilization

The time required for temperature stabilization of the alignment cartridge is dependent upon the cartridge storage environment.

- Storage in the Drive Operating Environment - if the cartridge storage temperature is essentially the same as the recommended machine operating environment, the cartridge shall be allowed to run in the drive with heads loaded for 15 minutes prior to attempting the alignment procedure.
- Storage in Other Than The Drive Operating Environment - if the cartridge storage temperature is essentially different from the recommended drive operating environment, the cartridge shall be allowed to run in the drive with heads loaded for 30 minutes. After this initial period the cartridge shall be removed, reinstalled, and the drive operated with heads loaded for an additional 15 minutes prior to attempting the alignment procedure.

2. Move the card cage to the head cleaning position as described in section 5.4.2.1, then set up the oscilloscope as follows:
 - Set oscilloscope to differential mode (ADD and INVERT).
 - Connect channel 1 to TP-A33 and channel 2 to TP-A36 of the D/T PCB. This provides a differentiated read signal.
 - Trigger on negative (leading) edge of upper Index (-SELECTED INDEX MARK) at TP-F75 on Logic PCB.
 - Set vertical scale for channels 1 and 2 to 50 mV/Div.
 - Set horizontal scale to 2ms/Div-100 tpi, or 1ms/Div-200 tpi.
3. Position the heads to track 073 (100 tpi) or 146 (200 tpi).

NOTE

Head positioning cannot be done manually.
Slew the heads into position using the
CPU or an exerciser.

4. Locate the four Head Plugs on the D/T PCB. Physically select the upper disk R/W head to be checked/aligned, and install the R/W Alignment Filter between its head plug and companion connector on the D/T PCB. These plugs are oriented from the top down: upper head/upper disk; lower head/upper disk. The lower two plugs are for the lower disk heads.
5. Electronically select the head chosen in step #4 above, by CPU or by grounding the -DISK SELECT input. If the upper head is to be checked, also ground the -HEAD SELECT input. Removing this ground later will select the lower head.
6. Observe the alignment signal presentation on the oscilloscope.
7. A. 100 tpi alignment description (using Alignment Cartridge P/N 70306). If the head being checked is properly aligned, the oscilloscope presentation will be approximately as shown in Figure 5-6, with the time between zero crossings for both loops being equal.
B. 200 tpi alignment description (using Alignment Cartridge P/N 70709 or 71299). Observe the oscilloscope pattern, and refer to Figure 5-7 and 5-8.

The oscilloscope pattern should consist of two sinusoidal traces and an alignment marker. When the head is properly aligned, the pattern should resemble that shown in Figure 5-7. A misaligned head will produce a pattern similar to that shown in Figure 5-8.

8. If the head(s) requires alignment, proceed as follows: (Note: If both heads require alignment, the upper head must be adjusted first.)

Lower Head Only

- a. Slightly loosen the screw holding the lower head assembly clamp.

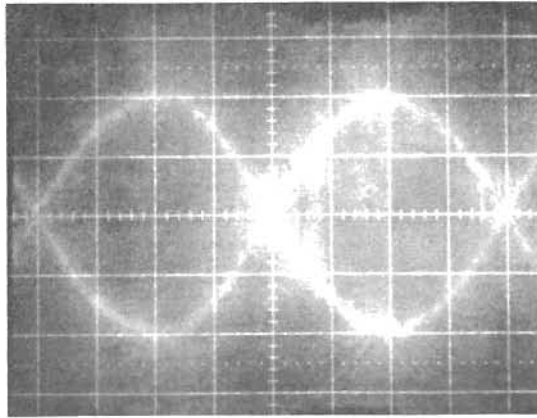


Figure 5-6. 100 TPI HEAD PROPERLY ALIGNED

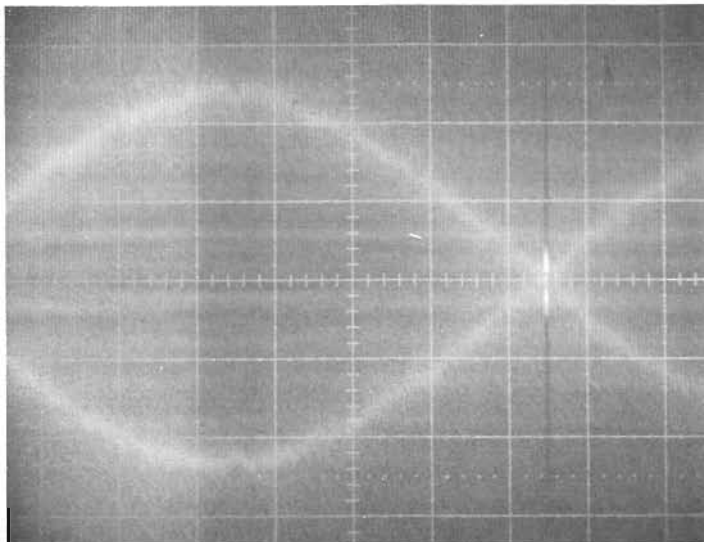


Figure 5-7. 200 TPI HEAD PROPERLY ALIGNED

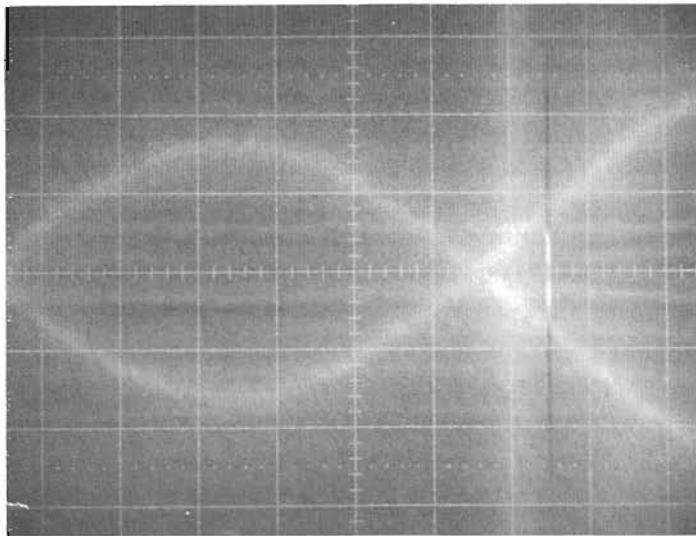


Figure 5-8. 200 TPI HEAD MISALIGNED

- b. Position a screwdriver at the point indicated in Figure 5-9, and manually move the head assembly in or out to obtain the correct alignment waveform.
- c. Torque the lower head assembly clamp screw to 95 inch ounces.

Upper Head

- a. Slightly loosen the two screws holding both head assembly clamps.
- b. Position a screwdriver at the point indicated in Figure 5-9, and manually move the head assembly in or out to obtain the correct alignment waveform.
- c. Torque the upper head assembly clamp screw to 95 inch ounces.
- d. Check alignment of lower head and adjust as necessary.
- e. Torque the lower head assembly clamp screw to 95 inch ounces.

NOTE

As the screw is tightened, the head may move slightly. If necessary, readjust the head position, allowing for any head movement caused by tightening the screw. The upper head must be adjusted first.

9. Switch the unit from RUN to LOAD to retract the heads, and then return to the RUN mode of operation.
10. Reposition the R/W heads back to the alignment track, and recheck the alignment of the heads. Repeat the adjustment procedure as necessary.
11. Remove the R/W Head Alignment Filter.

5.6.4.3.2 Lower Heads

Since disk interchangeability is not affected by the lower heads, the adjustment consists of merely moving the card cage to the head-cleaning position as described in 5.4.2.1, inserting a $.050 \pm .005$ shim between the head mounting plate and the carriage roller plate, tightening the set screw to 95 inch ounces, and removing the shim. This adjustment is shown in Figure 5-10.

5.6.4.4 Upper Index Transducer Adjustment

Install an alignment cartridge (100 tpi-P/N 70306, 200 tpi-P/N 70709 or 71299). Place the drive in the RUN mode, and observe the signal at pin 10 on the Logic PCB. The amplitude of the positive peaks should be between 165 and 450 mV for narrow sector slots, or between 300 and 1000 mV for wide sector slots. If the signal falls outside the appropriate range, proceed as follows:

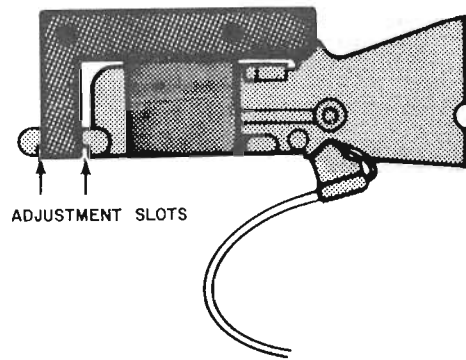


Figure 5-9. HEAD ADJUSTMENT

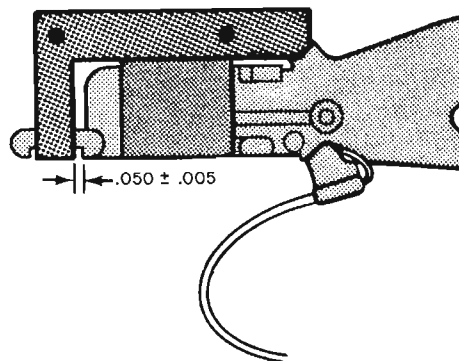


Figure 5-10. HEAD ADJUSTMENT - LOWER SET

1. Place the drive in the LOAD mode and, when able, remove the alignment cartridge.
2. Verify the transducer lamination-to-sector ring clearance of $.008" \pm .003"$ by laying a straight-edge across the spindle hub and checking the gap between its lower edge and the top of the lamination with a plastic feeler gauge. If the clearance is out of tolerance, loosen the hold-down screws (same as screws A in Figure 5-5), and add or remove shims (P/N 16358) as required. Retighten the screws just enough to secure the transducer and still allow slight lateral movement.
3. Align the transducer/lamination center line with the spindle hub center, and move the transducer in or out radially until the tip of the lamination clears the outside of the spindle hub flange by approximately $3/64"$. Tighten the hold-down screws a little.
4. Reinstall the alignment cartridge, switch from LOAD to RUN mode and, when able, recheck the signal level. If the signal is in tolerance, the cartridge may be removed and the hold-down screws tightened firmly. If the signal is not in tolerance, repeat step 3 - moving the transducer radially a small amount either in or out each time until optimum signal level is achieved.

NOTE

A disk hub and sector ring, retrieved from a defective disk cartridge and used here in a manner similar to the procedure outlined for the lower transducer, will appreciably shorten the time needed to achieve a proper signal level.

5. Locate the index transducer base plate, which is screwed to the outside front of the bowl assembly at the centerline. This plate, shown in Figure 5-11, has four hex-head fastening screws ("A") and a slotted-head adjustment screw ("B").
6. Slightly loosen the four fastening screws just enough to permit side movement of the transducer base plate.
7. Install the alignment cartridge, place the drive in the RUN mode, and select the upper disk.
8. Using the exerciser, seek to track 5 (100 tpi) or track 10 (200 tpi).
9. Using the leading edge (negative-going) of the index pulse at TP-F75 of the Logic PCB as a trigger, observe the signal at TP-A33 or TP-A36 of the D/T PCB. This signal is shown in Figure 5-12. Note the long pulse followed by a long burst of signal. The long pulse is the read gate.

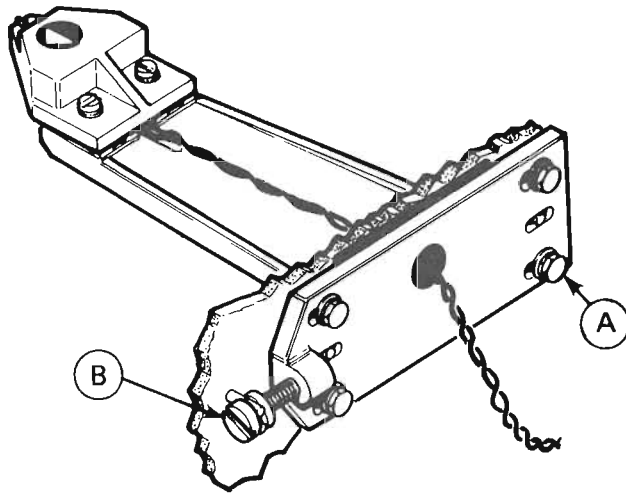


Figure 5-11. UPPER INDEX TRANSDUCER ADJUSTMENT

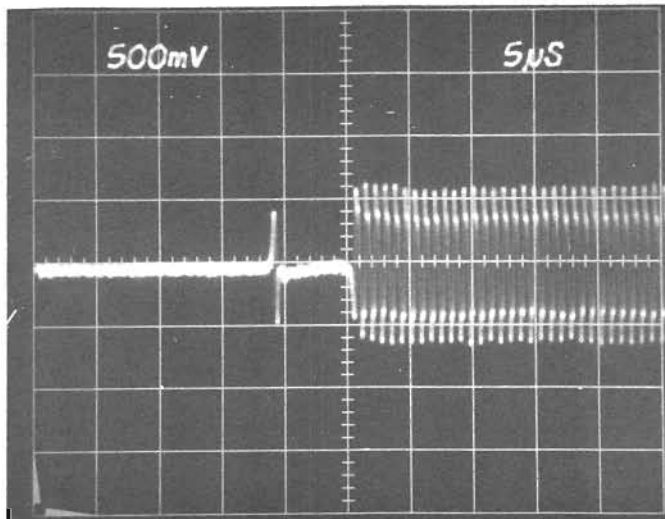


Figure 5-12. INDEX TO DATA BURST WAVEFORM

10. Using the adjustment screw, position the index transducer so that the leading edge of the read gate occurs 18.8 usec after the leading edge of the index mark. (Note: for 1500 rpm drives the proper setting is 30 usec \pm 5 usec). Do not tighten the fastening screws yet.
11. Alternately selecting each of the upper heads, adjust the index transducer so that the read gate is symmetrical around the 18.8 usec point (30 usec for 1500 rpm). Pulse separation between the heads shall not exceed 6.25 usec (10 usec for 1500 rpm).
12. Tighten the four fastening screws, observing that tightening the screws does not result in misalignment.
13. Return the front panel to the operating position.

5.6.4.5 Track Zero Adjustment

Precautions:

- The track 0 adjustment should be performed only after the disk drive is installed in its intended operating location (rack or desk top).
- Do not lean or place objects on the disk drive while taking readings for track 0 adjustment. Any such unusual forces will slightly bow the baseplate and cause erroneous adjustment.
- The track 0 sensor is affected by ambient light, especially the red wavelengths. Maintain a low level of daylight and incandescent light during track 0 adjustment. Reasonable levels of fluorescent light are acceptable.

Track Zero Adjustment requires the use of an alignment cartridge, exerciser, and oscilloscope.

1. Adjust the upper disk R/W heads for .050" gap (same as lower disk heads), as shown in Figure 5-10.
2. Set exerciser WRITE switch to OFF position to prevent writing on alignment cartridge.
3. Adjust scope Ch 1 and Ch 2 for ground reference on display centerline.
4. Set scope as follows:

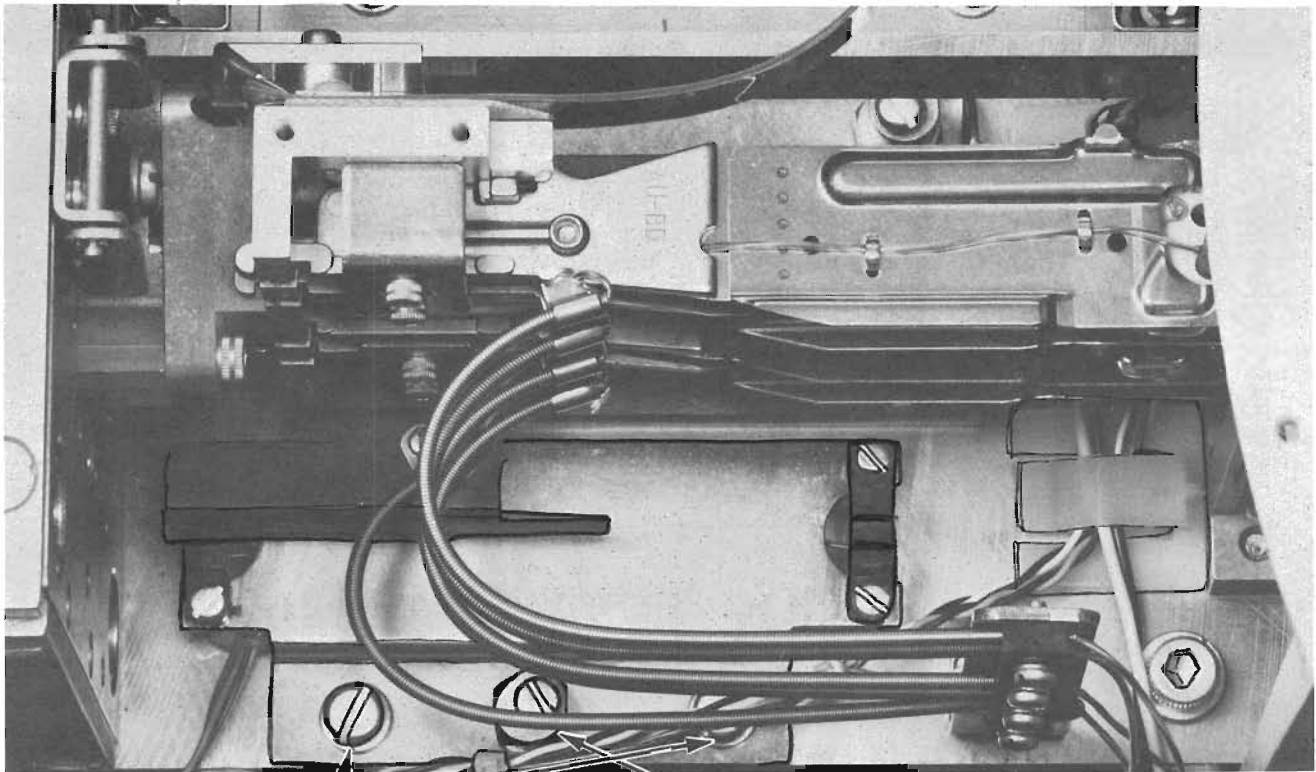
Main Trigger Amplifier

Mode -	NORMAL
Coupling -	DC
Source -	EXT
Time Base -	2 ms

Vertical Amplifiers

Vertical Deflection - Ch 1:	50mV/cm
Ch 2:	2V/cm

5. Set SW-1 on Logic PCB to ON position (Index Only).
6. Install alignment cartridge and set Load/Run switch to RUN. Allow 15 minutes for drive and cartridge to thermally stabilize.
7. Connect Ch 1 scope probe to TP-A33 on D/T PCB, and Ch 2 scope probe to P30-3 on LO PCB.
8. Trigger scope externally on positive (leading) edge of +OVER TRKS DET signal (pin 14 of LO PCB).
9. With exerciser, seek to tracks around track 10 until burst pattern shown in Figure 5-14 is obtained.
10. If adjustment is required, slightly loosen track 0 sensor assembly screws and eccentric lock screw. (Refer to Figure 5-13.)
11. Note track address where burst pattern is obtained, and adjust track 0 eccentric accordingly:
 - Track address < 10 - Turn eccentric clockwise
 - Track address > 10 - Turn eccentric counterclockwise
12. Perform a seek to track 0. The Ch 2 signal (-OVER TRKS) should produce a single positive pulse as the actuator reaches track 0.
13. Move Ch 1 scope probe to TP-H72 (POSITION SAWTOOTH) of Servo PCB.
14. With exerciser, perform continuous 10-track seek-restore operations.
15. Scope Setup:
 - Ch 1 vertical at 2V/cm.
 - Adjust horizontal position so sawtooth crosses its 0 volt level at a vertical graticule line.
16. Adjust track 0 sensor assembly so that -OVER TRKS (Ch 2) goes high halfway through negative portion of sawtooth slope (see Figure 5-15). Figure 5-16 shows actual scope waveform obtained during this adjustment.
17. Tighten track 0 assembly screws and eccentric lock nut while observing scope waveforms to see that adjustment does not change.
18. Move Ch 1 scope probe back to TP-A33 on D/T PCB and recheck for burst pattern at track 10.
19. Return SW-1 on Logic PCB to OFF position.
20. Recheck R/W head alignment if track 0 setting was changed.



TRACK 0 ASSEMBLY SECURING SCREWS

ECCENTRIC AND LOCK SCREW

Figure 5-13. TRACK 0 SENSOR ADJUSTMENT

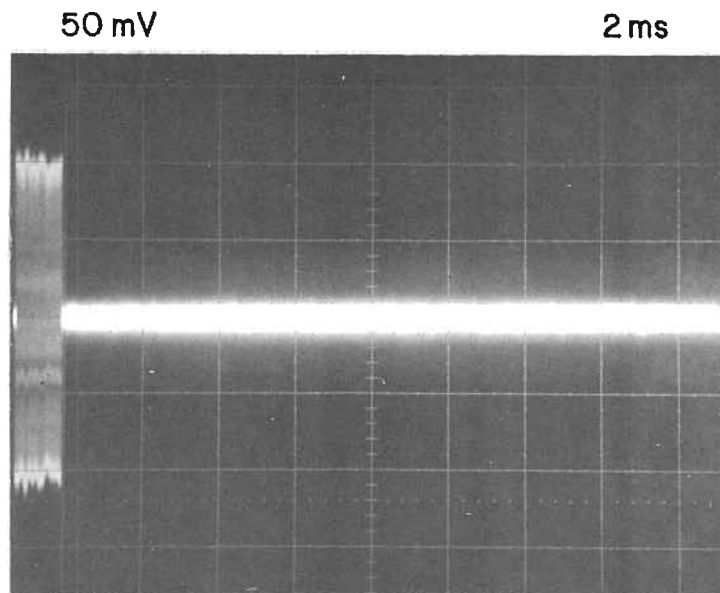


Figure 5-14. TRACK 10 DATA BURST

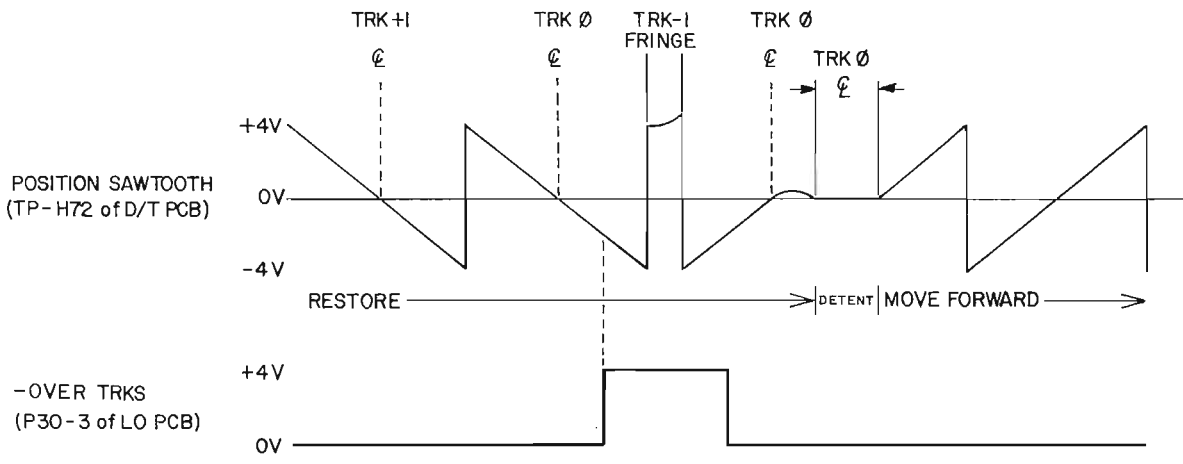


Figure 5-15. TRACK 0 WAVEFORMS

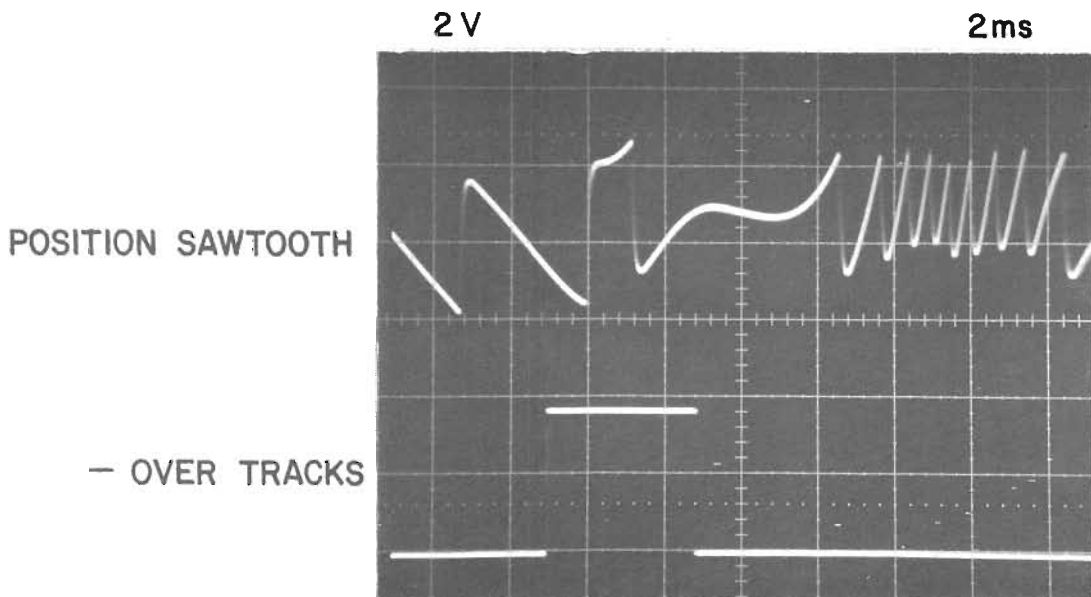


Figure 5-16. TRACK 0 WAVEFORMS PHOTO

5.6.5 Level 3 Adjustments

5.6.5.1 Head-Positioner Azimuth Adjustment

NOTE: This adjustment is performed with disk drive set for 200 tpi/2400 rpm operation. For 100 tpi/1500 rpm drives, set SW-1 on A/L PCB to 200 tpi, and SW-2 on LO PCB to 2400 rpm. Ensure that the switches are returned to original settings after adjustment is completed.

Check Procedure:

1. Trigger scope externally on negative-going edge of index at TP-F75 of the Logic PCB.
2. Measure the Index-to-Data burst times for both upper disk heads at track 10 and track 402. (Time between the index negative edge and first peak of isolated pulse - see Figure 5-12.) The time difference among the four measurements must be less than 6.0 usec. If >6.0 usec, perform the following adjustment procedure:

Adjustment Procedure:

1. Break holding torque of screw holding rear of positioner base plate.
2. Loosen two screws holding front end of positioner base plate.
3. Loosen temperature compensation arm screw.
4. Use large screwdriver to shift positioner to left or right.
5. Verify index-to-data burst on both upper disk heads is within 6 usec at track 10 and track 402.
6. Secure the three head positioner screws and repeat index-to-data burst verification.
7. Check track-zero adjustment according to 5.6.4.5, and adjust if necessary.

5.7 REMOVAL/REPLACEMENT OF ASSEMBLIES AND PARTS

5.7.1 Level 1 Removal/Replacement

5.7.1.1 Top Cover

The top cover is held in place by four securing screws, on the top surface around the rear periphery of the bowl.

5.7.1.2 Removal of Cartridge with Power Off

1. Ensure that the head cartridge is in the fully retracted position.

2. To insure that the brushes are fully retracted, locate the brush lever and eccentric on the right side of the drive. Rotate the brush lever clockwise until it hits the eccentric, if it is not already in that position.
3. Spread the cartridge clamps as described in 5.6.2(2), and remove the cartridge.

5.7.1.3 Card-Cage PCB's

Location of the Card Cage is shown in Figure 5-2.

LO PCB, A/L PCB, SO PCB - These PCB's may be directly unplugged from the Mother PCB.

D/T PCB - Before pulling this board out, disconnect the four R/W head plugs from the board.

P/D PCB - Loosen the two screws that secure the PCB to the card cage, and disconnect the two-piece connector before attempting to pull the PCB out of its Mother PCB connector.

5.7.1.4 I/O PCB

Loosen the two screws that secure the I/O PCB to the card cage, and pull the board out of its connector.

5.7.1.5 Power Supply

1. Remove yellow wires from TB1-6 & 7.
2. Remove black wires from TB1-2 & 7.
3. Unplug connector J7 from Mother PCB.
4. Remove two screws from rear of drive holding power supply.

To reinstall the power supply, reverse the removal procedure.

5.7.1.6 Front Panel Components

Front panel components are accessible for removal or replacement by removing the two hexagon socket screws which hold the front panel in position. Access to these screws is through two holes, one on each side of the bowl, as shown in Figure 5-17. To permit the front panel to swing freely, two lower screws, one on each side, may require loosening. These screws are located between the front panel and the lower section of the slide inner member. The front panel now swings down partially, giving access to components mounted on the rear of the front panel. Some components mounted on the pan or baseplate are also accessible by lowering the front panel.

5.7.1.7 Front Panel

1. Lower the panel to the maintenance position as described in 5.7.1.6.

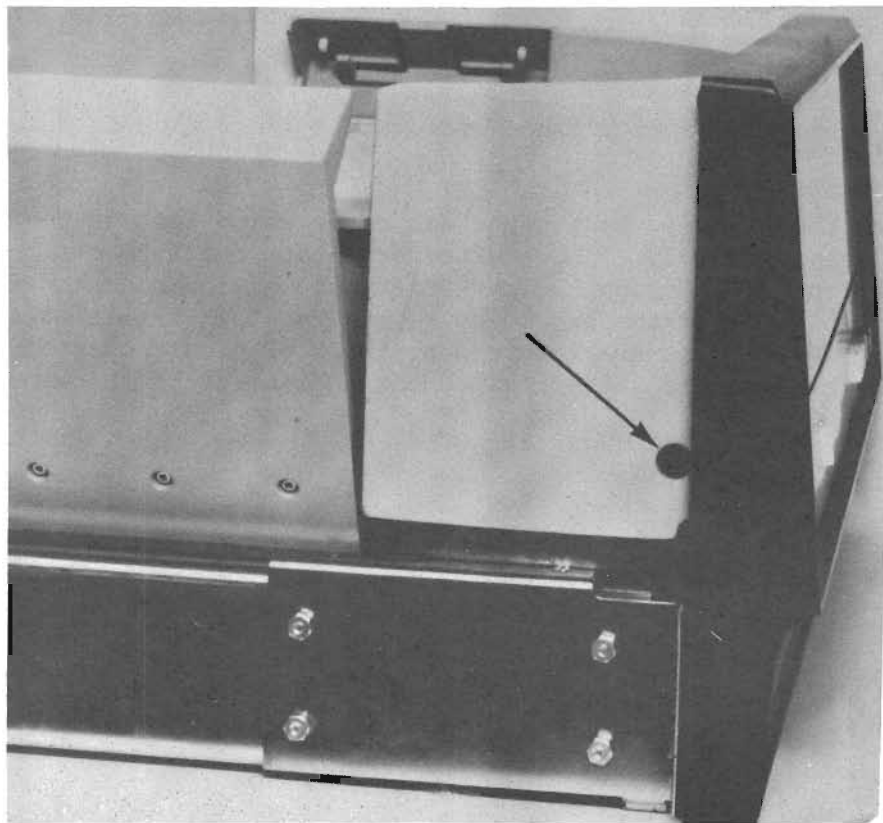


Figure 5-17. FRONT PANEL RETAINING SCREW ACCESS

2. Disconnect the wires from the panel lamps and switches.
3. Unfasten the cable clamps from the front panel.
4. Remove the two hexagon socket screws which hinge the front panel to the pan.

To replace the front panel, perform the preceding operations in reverse order. If necessary, adjust the two set screws in the front handle stiffener so that the drawer handle is approximately flush with the face of the front panel, and so that the side latches work properly. If proper adjustment is not possible using only the set screws, the striker plate may need adjustment.

5.7.1.8 Card Cage Assembly

1. Disconnect R/W head plugs from D/T PCB.
2. Disconnect connector J1 from P/D PCB.
3. Disconnect all cable connectors from Mother PCB.
4. Remove two screws at rear of card cage holding it in place.
5. Slide card cage assembly out of disk drive.

5.7.1.9 Brushes

For access to the lower brushes, remove the fixed disk as described in 5.7.2.2.

To remove the brushes, loosen the set screw which fastens the brush lever to the brush mechanism shaft. Rotate the brush arm out into the bowl for easy access to the brushes. Loosen the set screw holding the brush in the arm, and remove the brush. Follow the procedure in reverse for installing a new brush. Ensure that the brush arms are returned to their original position prior to tightening the brush lever set screw. Check adjustment of the brushes according to 5.6.4.1.

5.7.1.10 Slide Assemblies

Each slide assembly is fastened to the pan by two screws. With the slide fully extended these screws can be seen on the lower track to the front and in the middle. To remove the slide assembly, simply remove the two screws.

5.7.2 Level 2 Removal/Replacement

5.7.2.1 R/W Heads

If lower heads are to be removed or installed with the lower disk in place, care must be taken to avoid damaging the heads or disk.

5.7.2.1.1 Removal

1. Remove R/W head clamps.

2. Slide head out sideways.

5.7.2.1.2 Installation

1. Insert head assembly into the carriage and clamp loosely.
2. Adjust the head(s) as described in 5.6.4.3.

5.7.2.2 Lower Disk

5.7.2.2.1 Removal

1. Lower the front panel to the maintenance position as described in 5.7.1.6.
2. Remove the cartridge retainer assemblies according to 5.7.3.2.
3. Disconnect the cartridge interlock switch connector.
4. Remove the six screws holding the lower disk cover to the inside of the bowl. Remove the lower disk cover.
5. The upper index transducer assembly is held to the front outside surface of the bowl by four screws as shown in Figure 5-11. Detach the index transducer assembly and withdraw it from the bowl recess far enough so that the lower disk can be removed without striking it. Ensure that the assembly is withdrawn straight forward, so that the adjusting screw and fork are not damaged.
6. Disconnect the cartridge interlock switch connector, and pivot the cartridge clamp rearward.
7. Remove the temperature compensation arm from the position transducer assembly.
8. Remove the eight screws holding the spindle clamp ring. This ring holds the lower disk to the spindle assembly.
9. Remove the lower disk, being careful not to scratch the disk surface. Avoid touching the surface of the disk. If the disk is to be re-installed, or otherwise reused, store it in a manner that will protect its recording surfaces.

5.7.2.2.2 Installation

During installation of the lower disk, exercise caution to ensure that the disk's recording surfaces remain free of contamination, including fingerprints.

1. Using pads soaked in 91% isopropyl alcohol, thoroughly clean all the disk surfaces and also the spindle surface on which the disk seats. Polish the disk to remove all alcohol residue.
2. Place the disk on the spindle, ensuring that it is properly seated. Place the spindle clamp ring on the disk, grooved side down.

3. Line up the eight screw holes, and install the screws. Do not tighten the screws more than finger tight.
4. Snug-up two opposite screws. Use very light torque; this is not final tightening.
5. Snug-up two more opposite screws 90° from the first two.
6. Snug-up the remaining four screws in opposite pairs as in steps 4 and 5.
7. Following the sequence given in the preceding three steps, tighten the spindle clamp ring screws. Only moderate torque is required.
8. Replace the upper index transducer. Do not tighten the mounting screws.
9. Reinstall the temperature compensation arm to the position transducer assembly.
10. Reinstall the lower disk cover, ensuring that the cut-out for the upper index transducer is properly oriented.
11. Reinstall the cartridge retainer assemblies.
12. Adjust the upper index transducer as described in 5.6.4.4.
13. Close the front panel and reinstall the two front panel retaining screws.

5.7.2.3 Brush Motor

5.7.2.3.1 Removal

1. Lower the front panel to the maintenance position as described in 5.7.1.6.
2. The brush motor is located at the right front corner of the base plate. Disconnect the brush mechanism link by removing the nut from the pin that holds the link to the brush motor crank arm. The head of the pin is slotted to allow holding it while the nut is being removed. Retain the washers and spring for reinstallation on the pin.
3. Disconnect the brush motor wires.
4. Remove the three screws which fasten the brush motor plate to the baseplate. Remove the brush motor assembly.

5.7.2.3.2 Installation

1. Perform the steps listed in 5.7.2.3.1(2) through (4) in reverse, but do not tighten the three brush motor mounting plate screws.
2. Adjust the brush mechanism as described in 5.6.4.1.

3. Return the front panel to the operating position.

5.7.2.4 Index Transducers

5.7.2.4.1 Upper Index Transducer

1. Lower the front panel to the maintenance position as described in 5.7.1.6.
2. Remove the cartridge clamps as described in 5.7.3.2.
3. Remove the six screws holding the lower disk cover to the inside of the bowl. Remove the lower disk cover.
4. Unplug the upper index transducer connector at Mother PCB connector J14.
5. The upper index transducer leads pass through a grommet in the transducer base plate. Push the grommet out into the bowl, and pass the leads and connector through the grommet hole in the base plate.
6. Remove the two screws which hold the transducer to the transducer arm. Remove the transducer and shims, saving the shims for use with the replacement transducer.

To install the upper index transducer, follow the preceding steps in reverse order. Perform the upper index transducer adjustments described in 5.6.4.4.

5.7.2.4.2 Lower Index Transducer

1. Remove the lower disk as described in 5.7.2.2.
2. Unplug the lower index transducer connector at Mother PCB connector J13.
3. The lower index transducer leads pass through a grommet in the bottom of the bowl. Push the grommet up into the bowl, and draw the leads and connector up through the grommet hole in the bowl.
4. Remove the two screws which hold the transducer to the bowl. Remove the transducer and shims, saving the shims for use with the replacement transducer.

To install the lower index transducer, follow the preceding steps in reverse order. Perform the lower index transducer adjustment described in 5.6.4.2.

5.7.3 Level 3 Removal/Replacement

5.7.3.1 Bowl Assembly

5.7.3.1.1 Removal

1. Remove the lower disk as described in 5.7.2.2.1.

2. Remove the plenum chamber and air filter by removing the two plenum chamber holding screws. Observe the precautions stated in 5.4.2.3.
3. Unfasten all cable clamps from side of bowl.
4. Loosen the set screw which fastens the brush lever to the brush mechanism shaft.
5. Disconnect the brushes retract-switch wires.
6. Unplug both index transducers from the Mother PCB.
7. Remove the lower index transducer as described in 5.7.2.4.2.
8. Remove the upper index transducer as described in 5.7.2.4.1.
9. Remove the four recessed hexagon screws which fasten the bowl to the base plate.
10. Lift the bowl straight up and off, manually guiding the brush lever off the brush mechanism shaft.

5.7.3.1.2 Installation

1. Perform the steps listed in 5.7.3.1.1 in reverse. While tightening the four screws which fasten the bowl to the base plate, twist the bowl in a counterclockwise direction as far as possible and torque the screws to 120 ± 5 inch pounds. When placing the brush lever on the brush mechanism shaft, ensure that the flat of the shaft is toward the brush lever set screws.
2. Perform the adjustments required by Table 5-2.

5.7.3.2 Cartridge Retainer Assembly

Remove the two Allen screws holding the cartridge clamp mechanism. When removing the lefthand cartridge clamp, first disconnect the wires leading to the cartridge interlock switch.

5.7.3.3 Baseplate-Mounted Components

To remove or reinstall the cartridge interlock linkage, or other components mounted on the top surface of the base plate, remove the bowl as described in 5.7.3.1 for access to these components.

5.7.3.4 Spindle Assembly

1. On the underside of the pan, remove the rectangular access plate.
2. Through the access hole, remove the static ground strap assembly.
3. Loosen the two set screws on the fan collar.
4. Remove the Bowl Assembly as described in 5.7.3.1.

5. Disconnect the four-conductor cable bundle from the Power Driver PCB.
6. Remove the three screws which fasten the spindle to the base plate, and lift the spindle off.

The Spindle Assembly is installed by reversing the preceding steps. When installing the spindle, ensure that the machined base plate ridge on which the spindle rests is clean, and that the spindle is firmly seated on the ridge.

5.7.3.5 Head Positioner

1. Unplug connectors J8, J9 and J11 from the Mother PCB.
2. Unplug the R/W head plugs from the D/T PCB.
3. Unplug the 2-conductor plug from the P/D PCB, and separate these two conductors from the other wires leaving the P/D PCB.
4. Remove the two Allen screws at the front end of the head positioner base plate.
5. Remove the one Allen screw at the rear underside of the head positioner.
6. Lift the positioner out of the disk drive.

To reinstall the head positioner, reverse the removal procedure, and then perform the azimuth adjustment (5.6.5.1) and R/W head alignment (5.6.4.3).



SECTION 6

APPENDICES

6.1 OPTIONS

Table 6-1 lists the options available for the Model 44B Disk Drive.

TABLE 6-1

<u>FEATURE</u>	<u>STANDARD</u>	<u>OPTIONAL</u>	<u>OPTION NO.</u>
Fixed Disk Sectoring	---	Index Only	44B-01
		8 Sector	44B-08
		12 Sector	44B-12
		14 Sector	44B-14
		16 Sector	44B-16
		20 Sector	44B-20
		24 Sector	44B-24
ATTENTION Signal	High Active	Low Active	490
Track Density	200 tpi	100 tpi*	491
Spindle Speed	2400 rpm	1500 rpm** (available only with 100 tpi)	492
Data Separator	Single-Shot Separator	VFO Separator*** 100ns pulse width	493-01
		VFO Separator*** 200ns pulse width	493-02
Installation	Rack Mounting	Desk Top Version	496
Unit Select Identification	Unit #1	Unit #2, 3 or 4 (See Sec. 4.3.2.8 for switch settings)	Specify Unit #
Input Voltage	100-120 VAC	220-240 VAC	220-240 VAC

* At 100 tpi, total storage capacity is 50 megabits.

** At 1500 rpm, the bit transfer rate is 1562 MHz and average latency is 20 ms.

*** The VFO option permits the Model 44B to be used with System 3 type format, or other systems in which missing clock pulse formats occur.

6.2 ACCESSORIES

Table 6-2 lists the accessories available for the Model 44B Disk Drive.

TABLE 6-2

<u>ACCESSORY NO.</u>	<u>ACCESSORY</u>
400	Type 5440 cartridge with index mark only
	Type 5440 cartridge:
402-08	8 sector
-12	12 sector
-14	14 sector
-16	16 sector
-20	20 sector
-24	24 sector
436	I/O Terminator
	I/O Cable Assembly:
435-05	5 feet
-07	7 feet

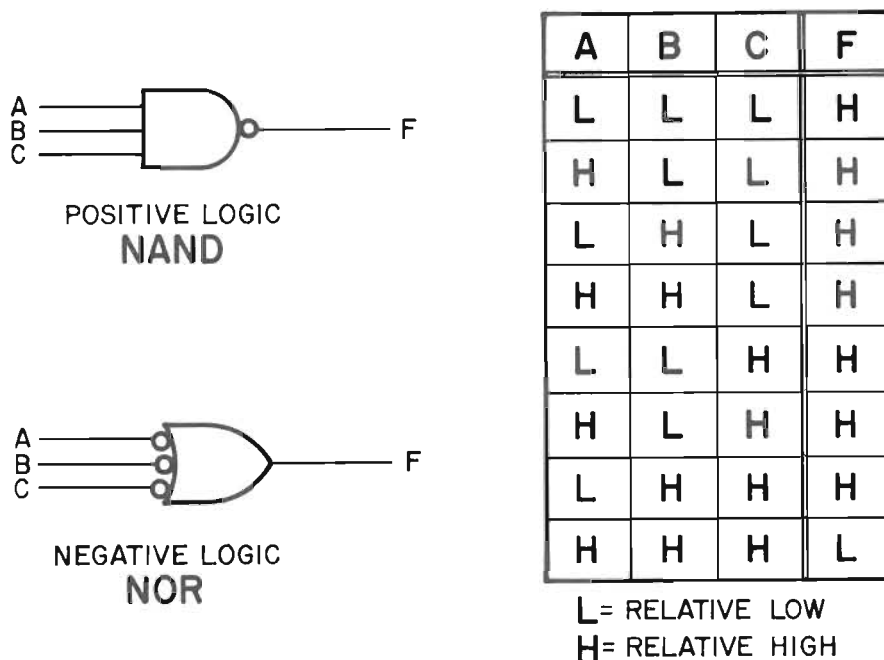
CIRCUIT DIAGRAMS AND CONVENTIONS

7.1 DIABLO CIRCUIT DIAGRAM CONVENTIONS

7.1.1 Functional Logic

Diablo Systems logic diagrams are primarily intended for use by field service personnel as troubleshooting aids and by system design engineers as sources of design theory information. As such, the first responsibility of a set of logic diagrams is to illustrate a design's principles of operation. Diablo Systems logic diagrams emphasize the functions performed by the logic elements in a design rather than the kinds of devices used to implement the function.

For example, a NAND gate may appear on a Diablo Systems logic diagram as either a positive logic AND function with the output inverted (NAND) or as a negative logic OR function with the inputs inverted (NOR).



This practice runs contrary to some logic drawing standards, which require the use of the NAND symbol for both functions. But, in Diablo Systems diagrams, different symbols are used to distinguish between the two functions because the functional elements of a design are considered to be more relevant to the design theory than symbolic representation of the kinds of devices used.

This functional approach to logic symbology is basic to the logic documentation conventions employed by Diablo Systems. The conventions that govern logic symbology and signal nomenclature are explained below. Other information concerning drawing standards that may help the reader interpret Diablo Systems logic diagrams is also included.

7.1.2 Signal Nomenclature

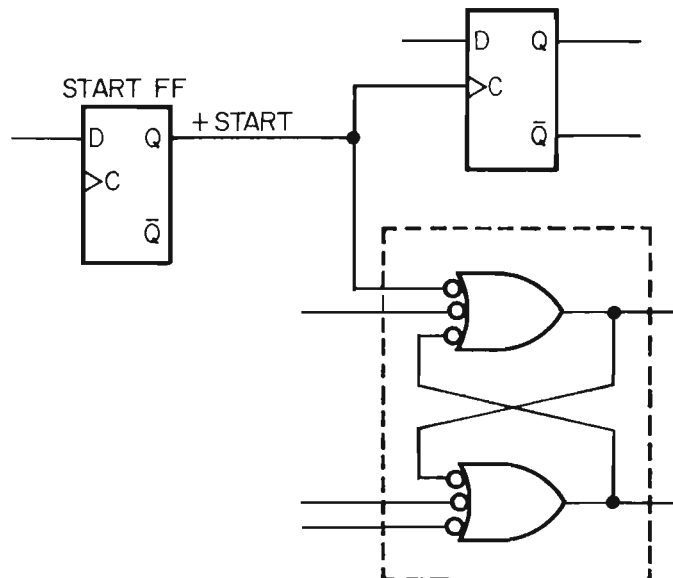
The active level of each logic signal is assigned a descriptive name. A signal is considered active when it either causes or represents some logic event that is significant to the progress of an operation. Consequently, the name given a signal usually provides one of two kinds of information:

- (1) Describes the effect that signal's active level has on the logic it feeds; for example, "-LOAD 'XXX' BUFFER" is the name of the signal that clocks data into the 'XXX' buffer.
- (2) Represents a condition or event that develops elsewhere in the logic; for example, "'XXX' READY" is the name of the signal that is active whenever the 'XXX' logic is able to accept a new command.

A + or - sign generally precedes each signal name to identify which of the two voltage levels used in the logic system is considered to be that signal's active level. The + sign represents the relatively higher logic level, and the - sign the relatively lower level. This means relatively higher or lower with respect to each other; the signs do not indicate signal polarity with respect to ground.

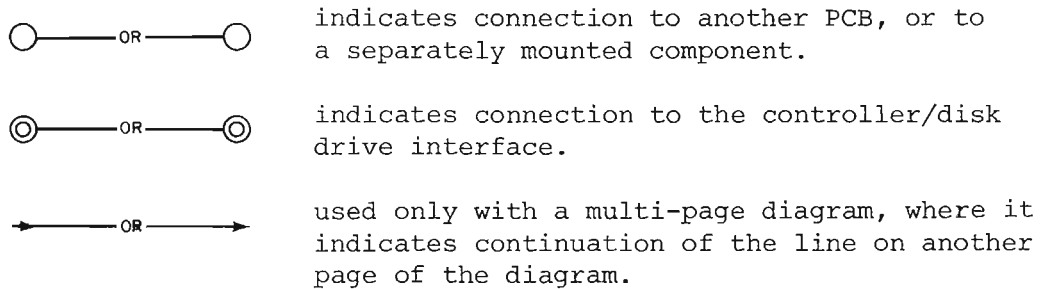
The actual voltage levels represented by the signs will depend on the logic family being used. For example, in TTL circuits, the signal identified by "'XXX' READY" is active when it is at 0 volts (nominal) and inactive at +4 volts (nominal).

Sometimes a signal serves as the input to both positive and negative logic elements. Ordinarily in such cases, the sign preceding the signal name agrees with the active level indicated at the output of the logic element that produced the signal. An example of this is illustrated by the following sketch.



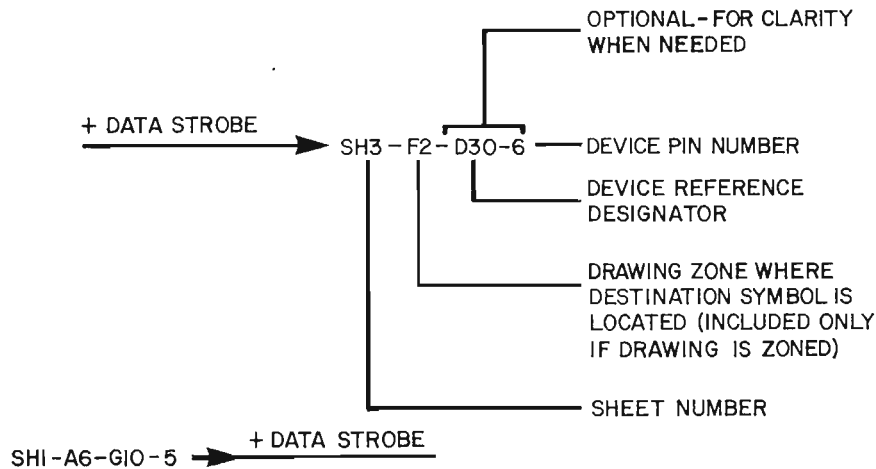
7.1.3 Diagram Input/Output Symbol

Inputs to, and outputs from, each PCB circuit diagram are represented by one of the symbols shown below.



7.1.4 Interpage Referencing

When a circuit diagram requires more than one page, an interpage reference scheme is used at the points on each diagram page where the signal lines enter and leave the page. The reference scheme used includes the following information.



7.1.5 Logic Symbology

The logic function symbols used in Diablo Systems logic diagrams conform closely to those set forth in MIL-STD-806.

Most small scale integration (SSI) circuits are represented by function symbols.

Medium scale integration (MSI) devices, such as shift registers and read-only memories (ROM), may be represented by rectangles with functional labels.

Since both positive and negative logic conventions can appear in a single set of diagrams, the unfilled circle negation symbol specified by MIL-STD-806 is used to distinguish between low-true and high-true signals.

A circle drawn at an input to a symbol indicates that the input is active at its relatively lower potential. The absence of a circle at an input means that the input is logically active at its relatively higher potential. The presence or absence of a circle at a symbol output has similar meaning for the active level of that output.

Usually, all logic symbols are drawn with inputs on the left and outputs on the right. Some device symbols (e.g. one-shots, J-K flip-flops) show some inputs and other external connections on the top and/or bottom of the symbol for clarity. Also, drawing layout restrictions occasionally require that some symbols be drawn with a vertical orientation so that signal flow through them is from top to bottom. However, logic symbols are never drawn with inputs on the right side or outputs on the left; nor are they drawn with inputs and outputs on the same side.

The component identifiers used on Diablo Systems logic diagrams, such as "flip-flop G23", are the grid coordinate codes for locating the components on the printed circuit board. Textual reference to a device, such as a flip-flop, will usually further identify the device by its output terminal number, particularly where a multi-device component is involved.

7.2 INTEGRATED CIRCUIT REFERENCE

(AVAILABLE AT A LATER DATE)

7.3 CIRCUIT DIAGRAMS

The list below indexes the circuit diagrams which follow. The assembly number listed corresponds to the assembly number that is silk-screened onto the PCB assembly.

A revision history appears on the back of each diagram.

<u>Figure No.</u>	<u>Title</u>	<u>Assembly No.</u>
7-1	Interconnection Diagram	19030
7-2	Input/Output PCB Schematic	12025
7-3	Address Logic PCB Schematic - Sheet 1	12064
7-4	Address Logic PCB Schematic - Sheet 2	12064
7-5	Logic PCB Schematic - Sheet 1	12066
7-6	Logic PCB Schematic - Sheet 2	12066
7-7	Data Transfer PCB Schematic - Sheet 1	12046
7-8	Data Transfer PCB Schematic - Sheet 2	12046
7-9	Data Transfer PCB Schematic - Sheet 3	12046
7-10	Data Transfer PCB Schematic - Sheet 4	12046
7-11	Servo PCB Schematic - Sheet 1	12068
7-12	Servo PCB Schematic - Sheet 2	12068
7-13	Power Driver PCB Schematic - Sheet 1	12062
7-14	Power Driver PCB Schematic - Sheet 2	12062
7-15	Power Supply Schematic	19033
7-16	VFO Data Transfer PCB Schematic - Sheet 1	12076-(200ns)/ 12110-(100ns)
7-17	VFO Data Transfer PCB Schematic - Sheet 2	12076-(200ns)/ 12110-(100ns)
7-18	VFO Data Transfer PCB Schematic - Sheet 3	12076-(200ns)/ 12110-(100ns)
7-19	VFO Data Transfer PCB Schematic - Sheet 4	12110-(100ns)
7-20	VFO Data Transfer PCB Schematic - Sheet 4	12076-(200ns)

NOTE: The VFO Data Transfer PCB Assembly is produced in two versions:

- (1) PCB Assembly #12076, with 200 ns output pulse width.
- (2) PCB Assembly #12110, with 100 ns output pulse width.

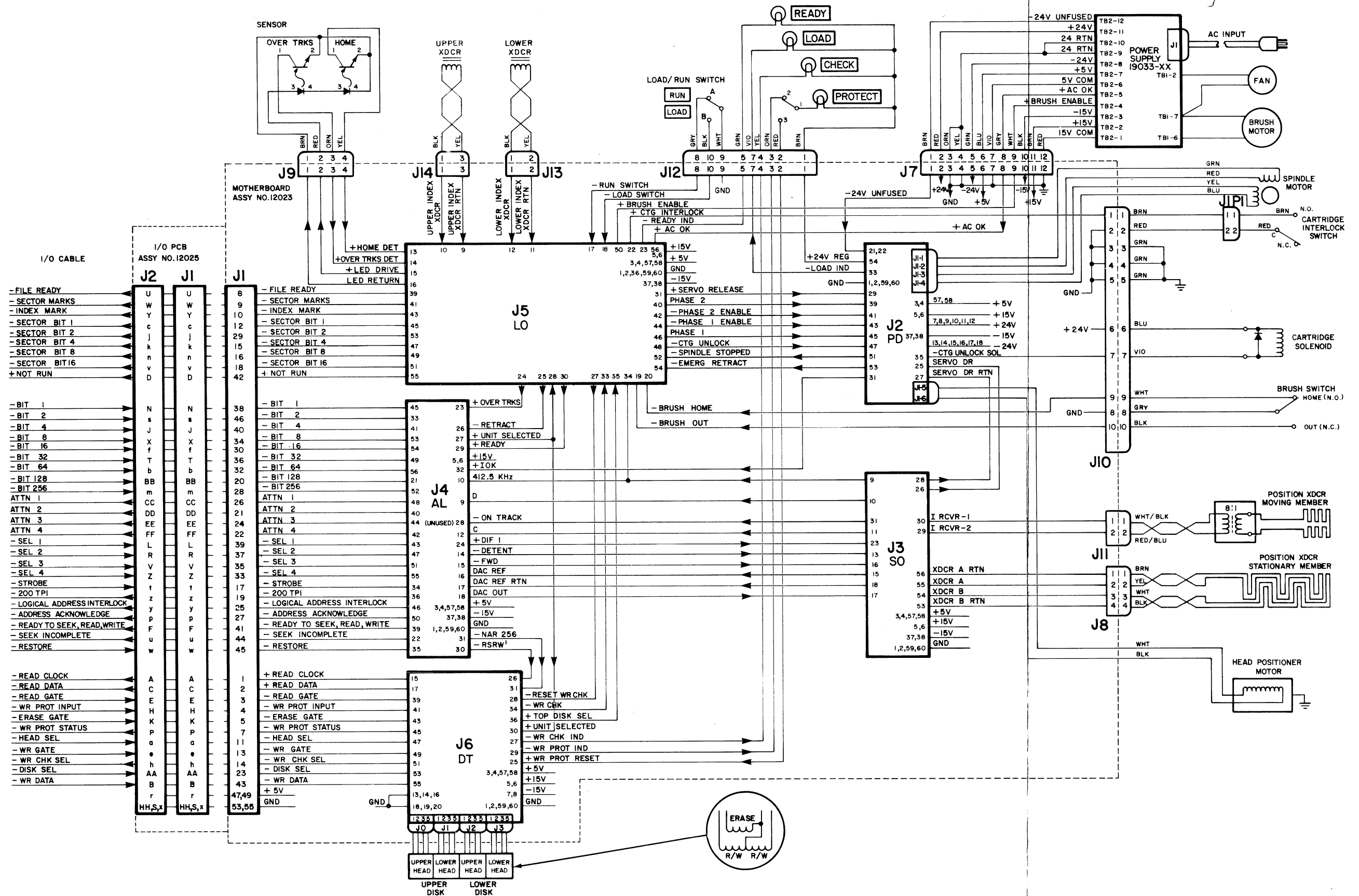


FIGURE 7-1. INTERCONNECTION DIAGRAM #19033

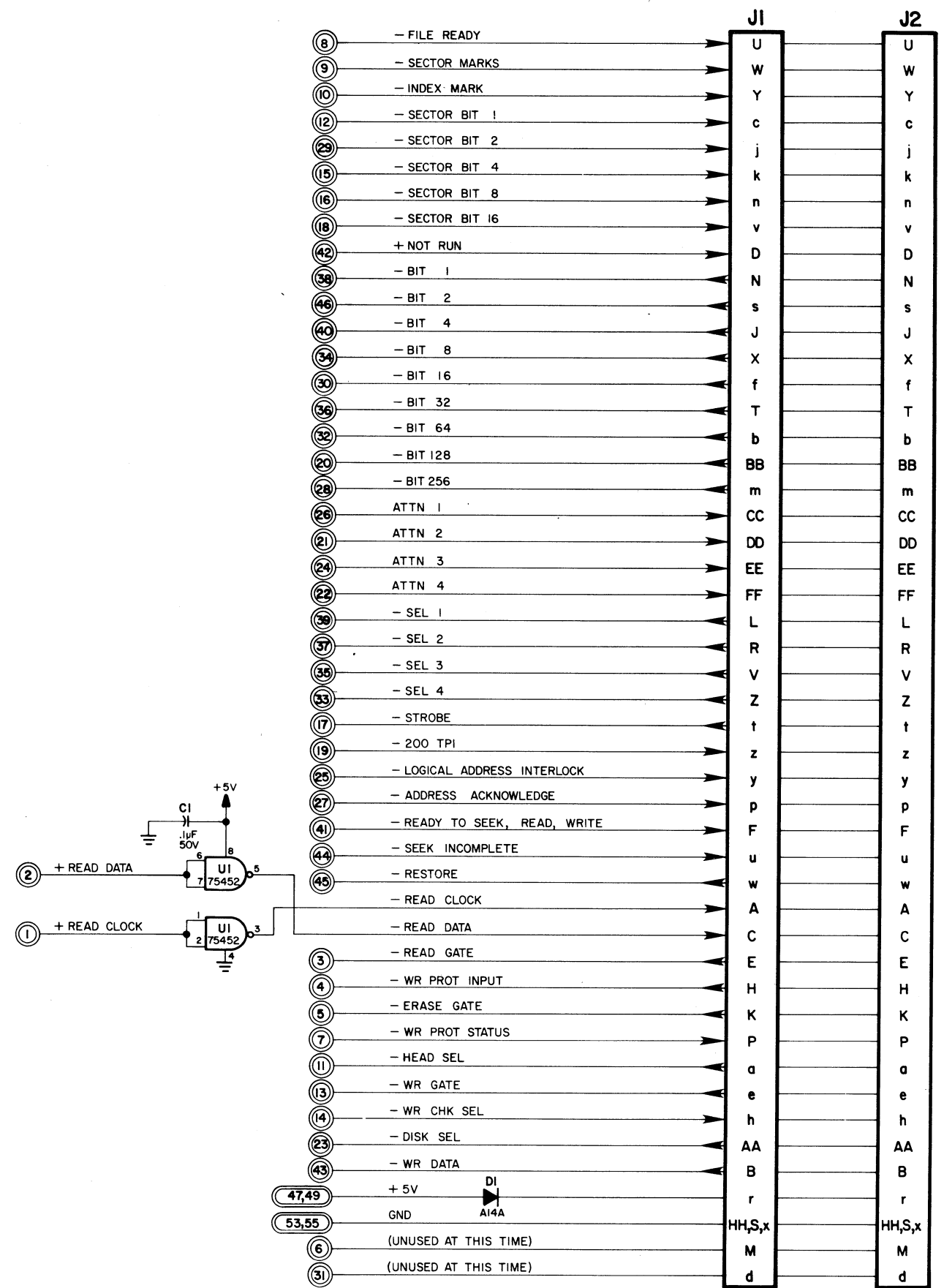
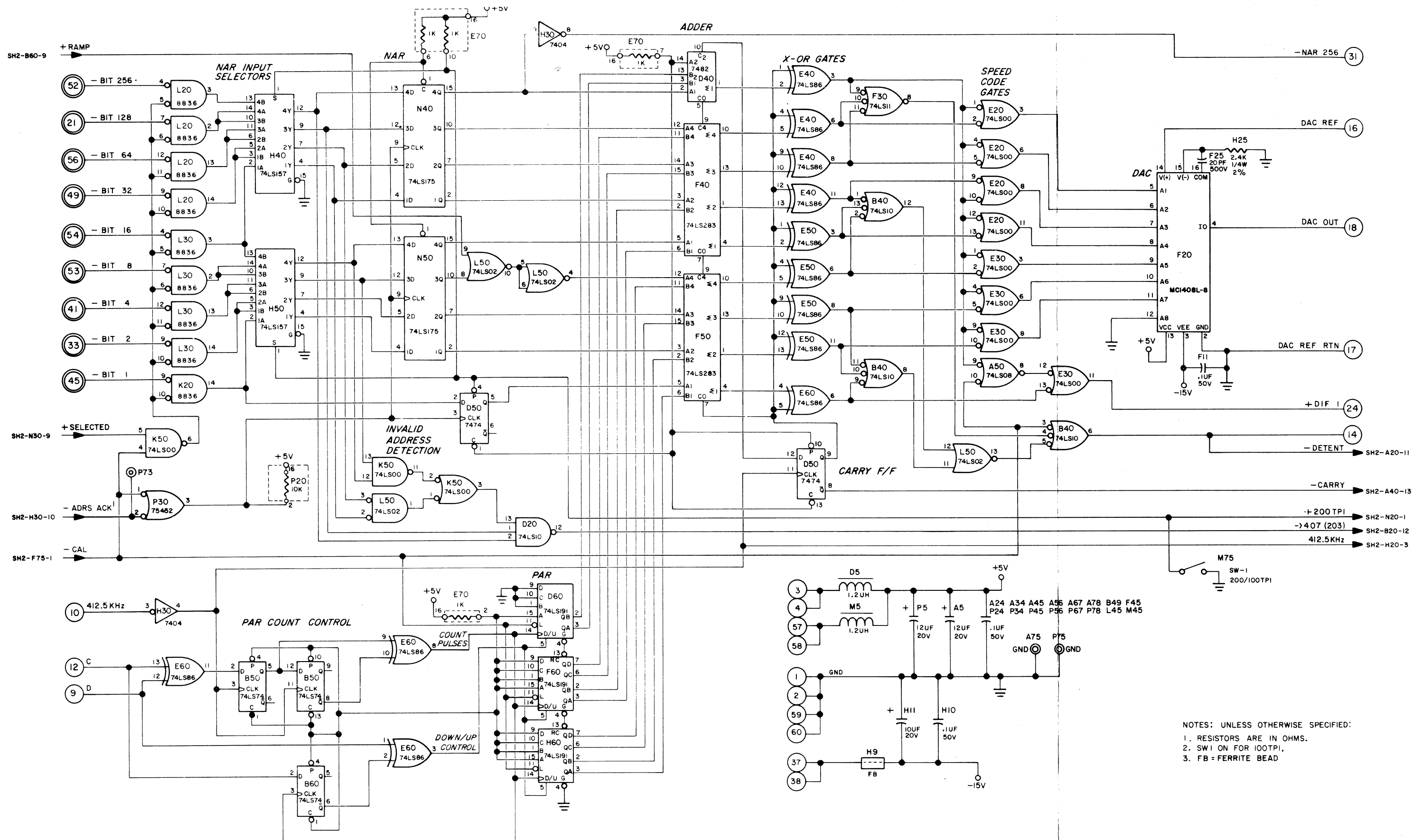
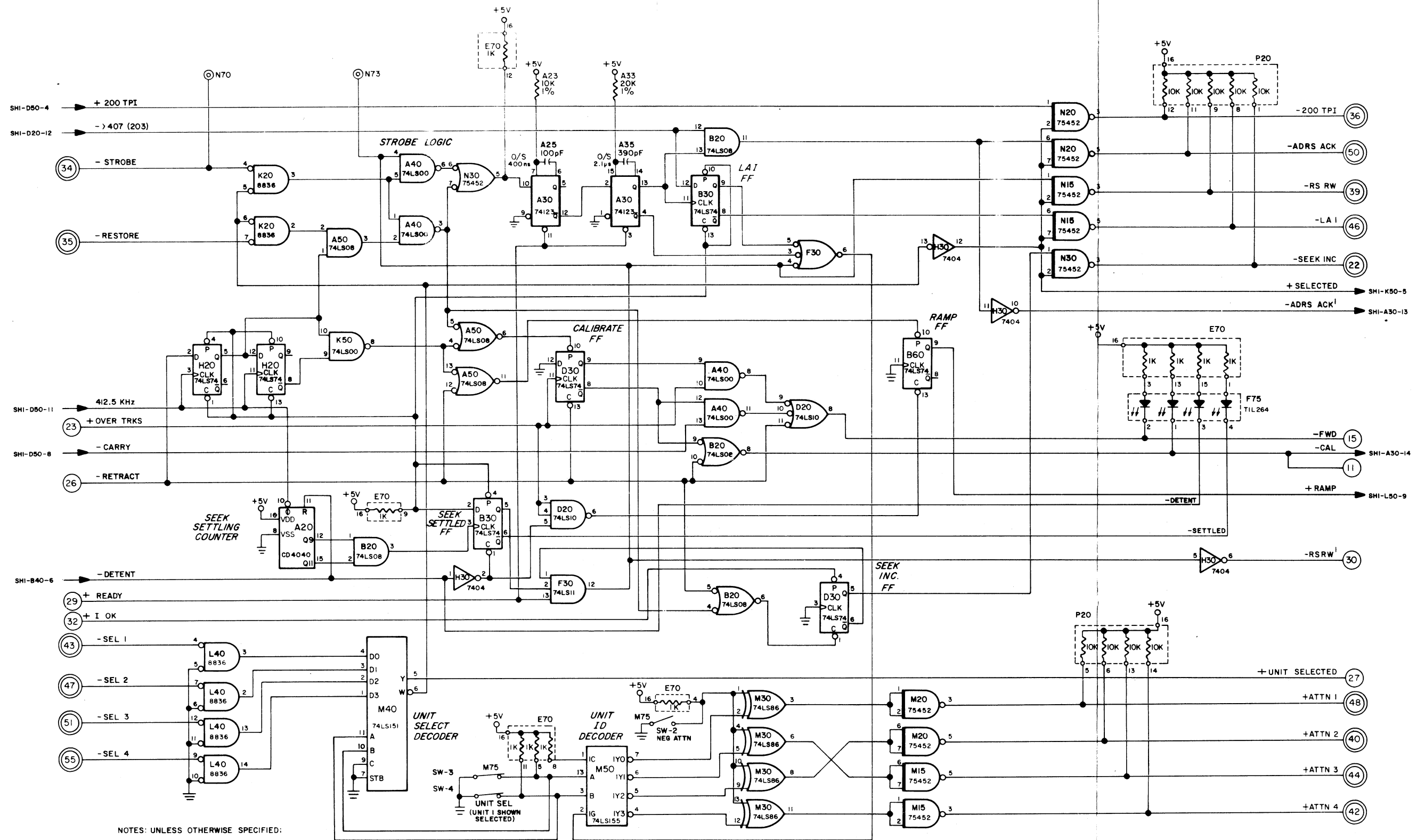


FIGURE 7-2. INPUT/OUTPUT
PCB SCHEMATIC
#12025



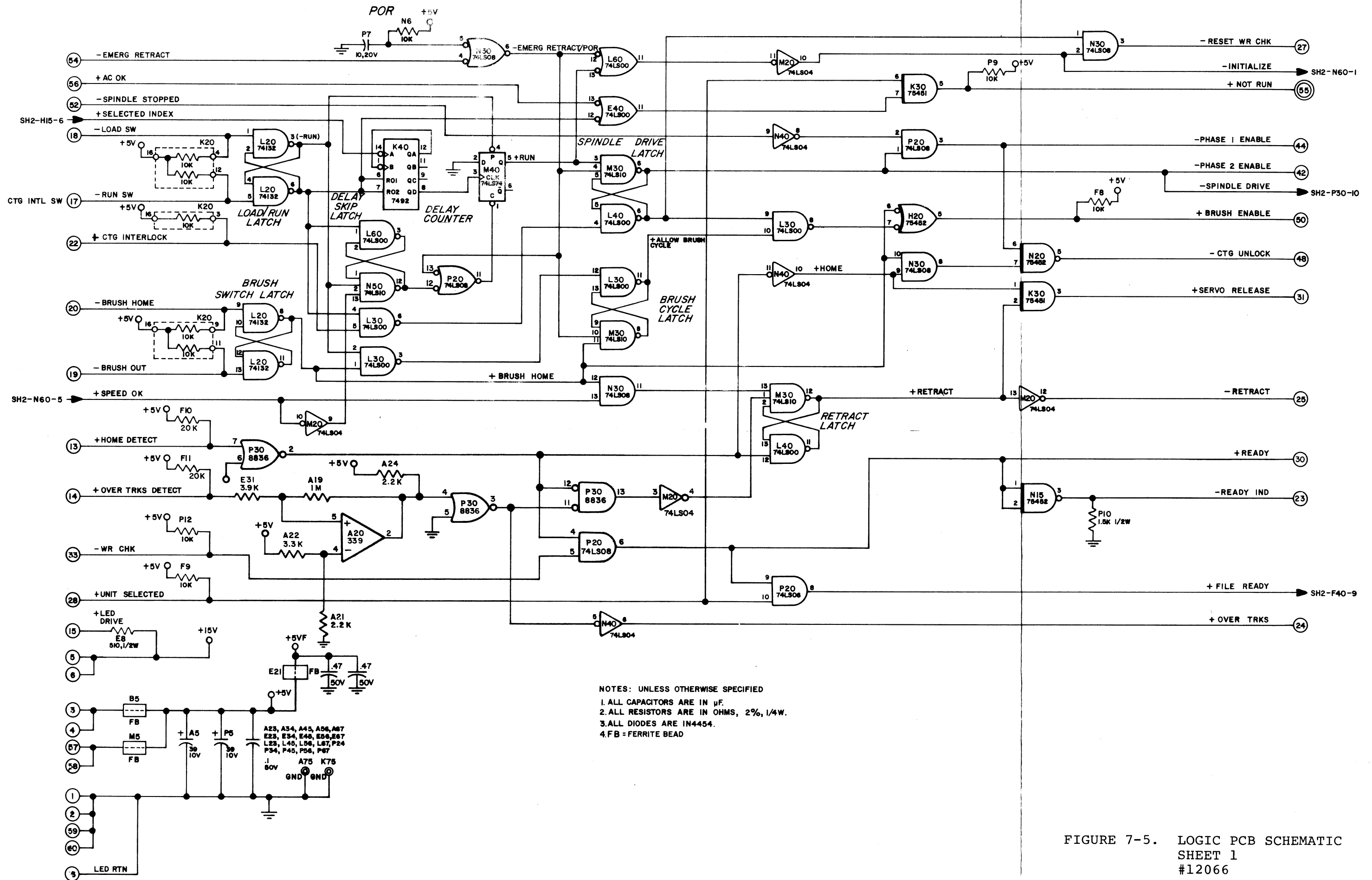
NOTES: UNLESS OTHERWISE SPECIFIED:
 1. RESISTORS ARE IN OHMS.
 2. SW-1 ON FOR 100TPI,
 3. FB = FERRITE BEAD

FIGURE 7-3. ADDRESS LOGIC PCB SCHEMATIC - SHEET 1 #12064



- NOTES: UNLESS OTHERWISE SPECIFIED:
- RESISTORS ARE IN OHMS
 - LED 1 'ON' - CALIBRATE
LED 2 'ON' - FORWARD
LED 3 'ON' - DETENT
LED 4 'ON' - SETTLED
 - SW3 SW4
ON ON - FILE 1
ON OFF - FILE 2
OFF ON - FILE 3
OFF OFF - FILE 4
 - SW2 ON FOR NEG. ATTN.

FIGURE 7-4. ADDRESS LOGIC
PCB SCHEMATIC - SHEET 2
#12064

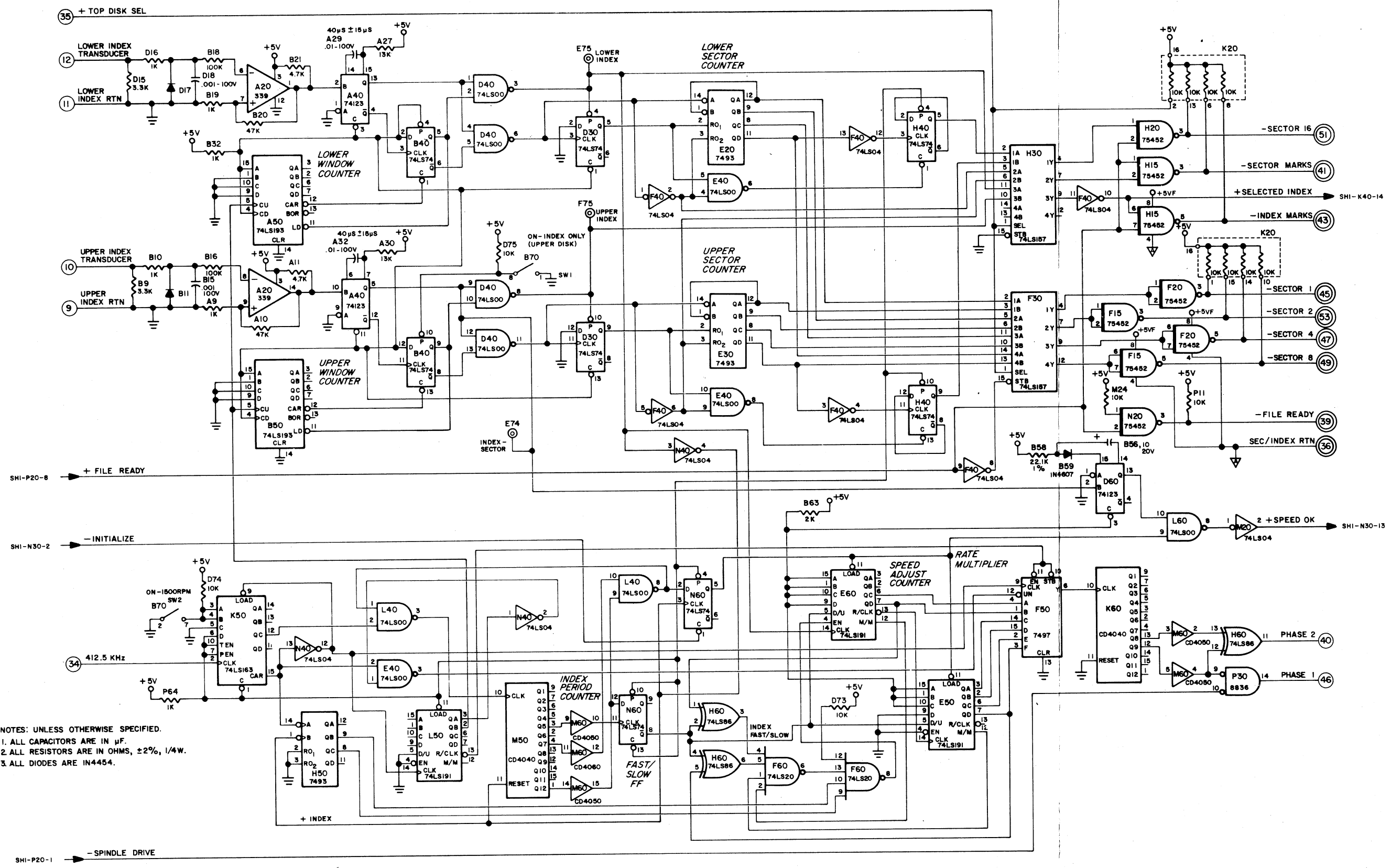


NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL CAPACITORS ARE IN μ F.
 2. ALL RESISTORS ARE IN OHMS, 2%, 1/4W.
 3. ALL DIODES ARE IN4454.
 4. FB = FERRITE BEAD

FIGURE 7-5. LOGIC PCB SCHEMATIC SHEET 1 #12066

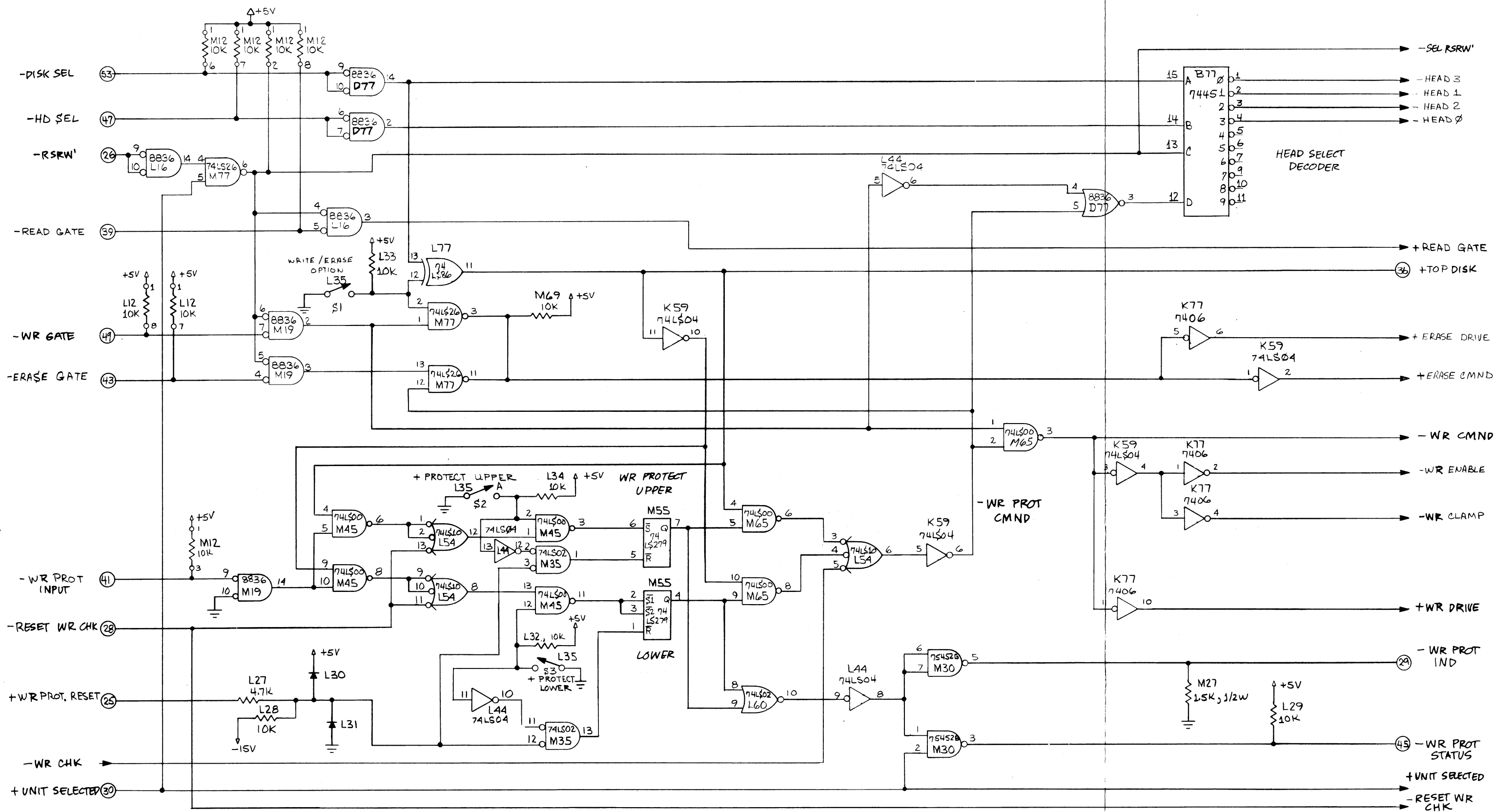
REVISION HISTORY - #12066 LOGIC PCB ASSEMBLY

Rev. XD-K XECO #108 Comparator A20-2 and associated circuitry added to +OVER TRKS DETECT line to improve effectiveness of track 0 adjustment procedure.



NOTES: UNLESS OTHERWISE SPECIFIED.
 1. ALL CAPACITORS ARE IN μ F.
 2. ALL RESISTORS ARE IN OHMS, $\pm 2\%$, 1/4W.
 3. ALL DIODES ARE IN4454.

FIGURE 7-6. LOGIC PCB SCHEMATIC SHEET 2 #12066



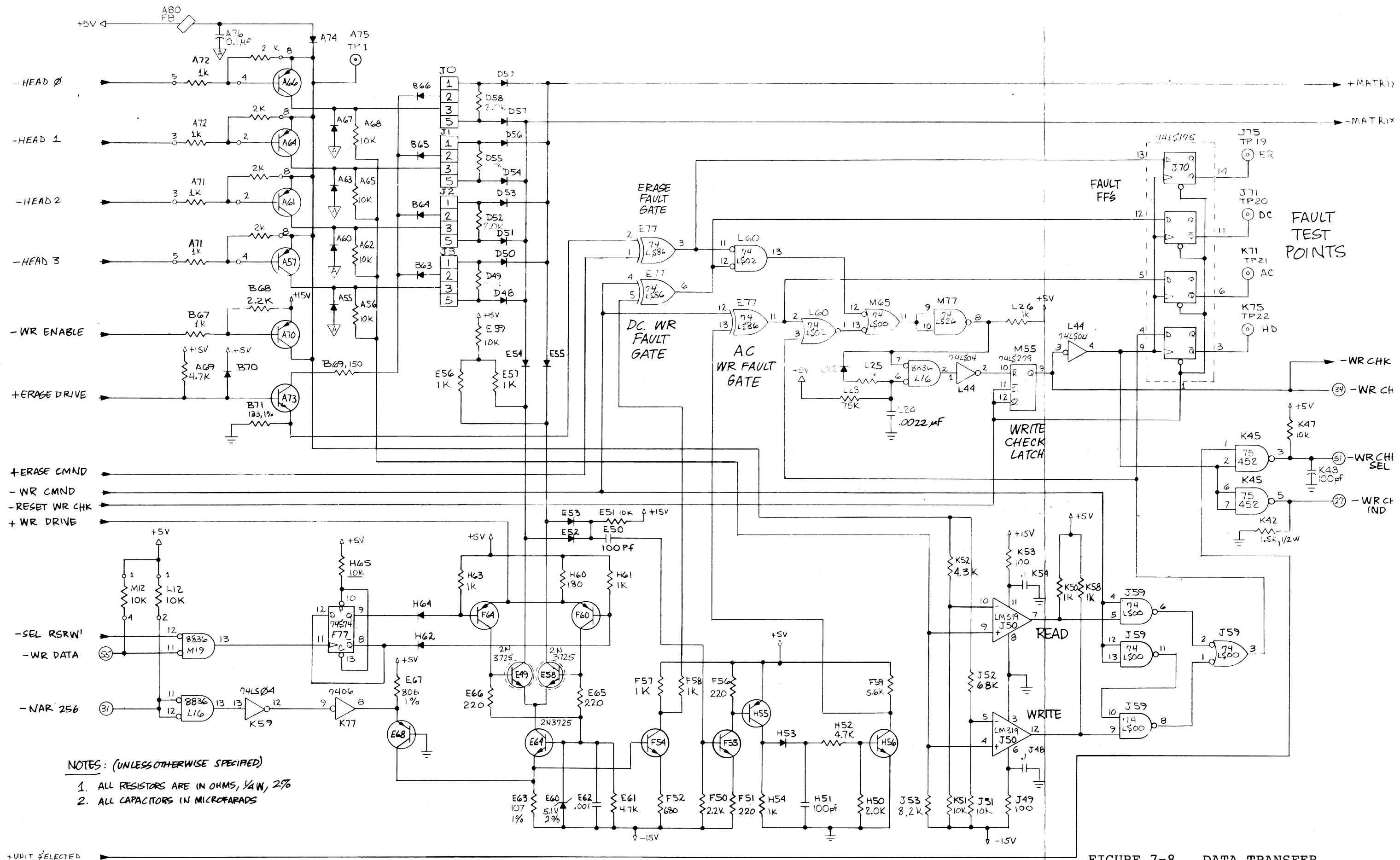
NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE IN OHMS, 1/4W, 2%
2. ALL CAPACITORS ARE IN MICROFARADS
3. OPEN SWITCH TO TIE ERASE FUNCTION TO WRITE GATE.

FIGURE 7-7. DATA TRANSFER PCB SCHEMATIC - SHEET 1 #12046

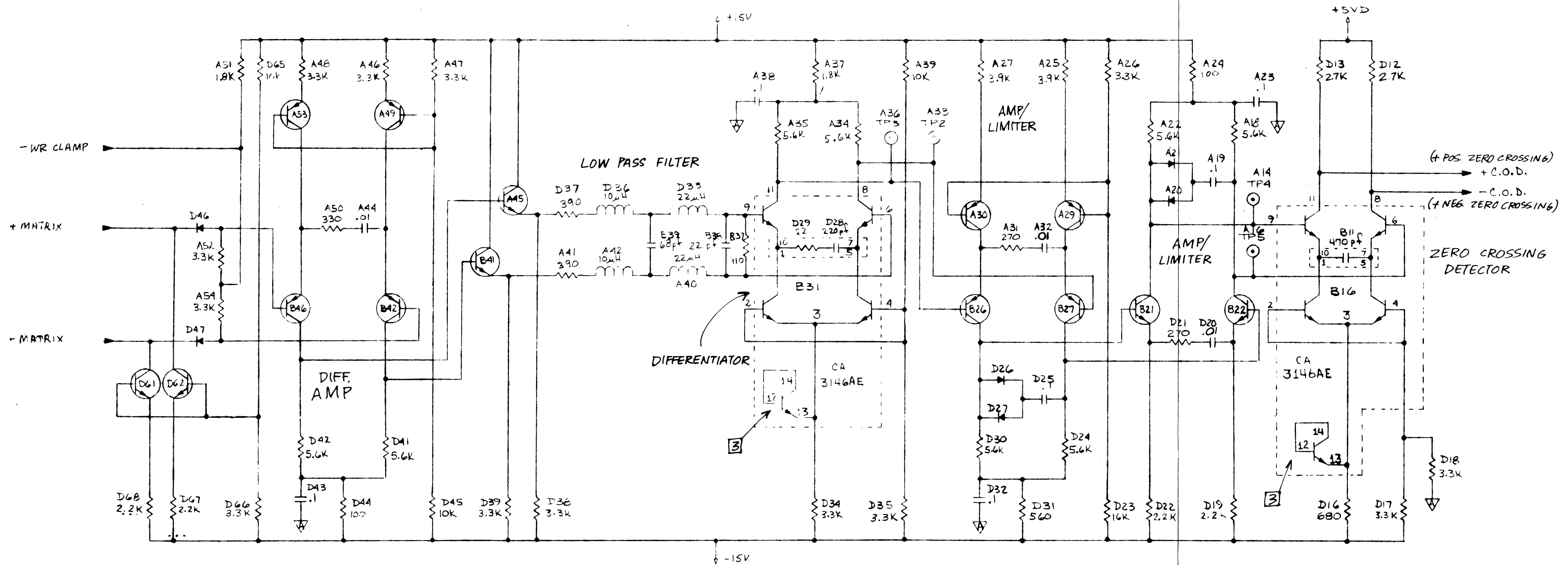
REVISION HISTORY - #12046 DATA TRANSFER PCB ASSEMBLY

Rev. XD-F XECO #110 Capacitor L24 changed from .001 to .0022 (Schematic sht. 2)
Capacitors A32 and D20 changed from .1 to .01 (Sch. sht. 3)
Resistors D12 and D13 changed from 6.8K to 2.7K (Sch. sht. 3)



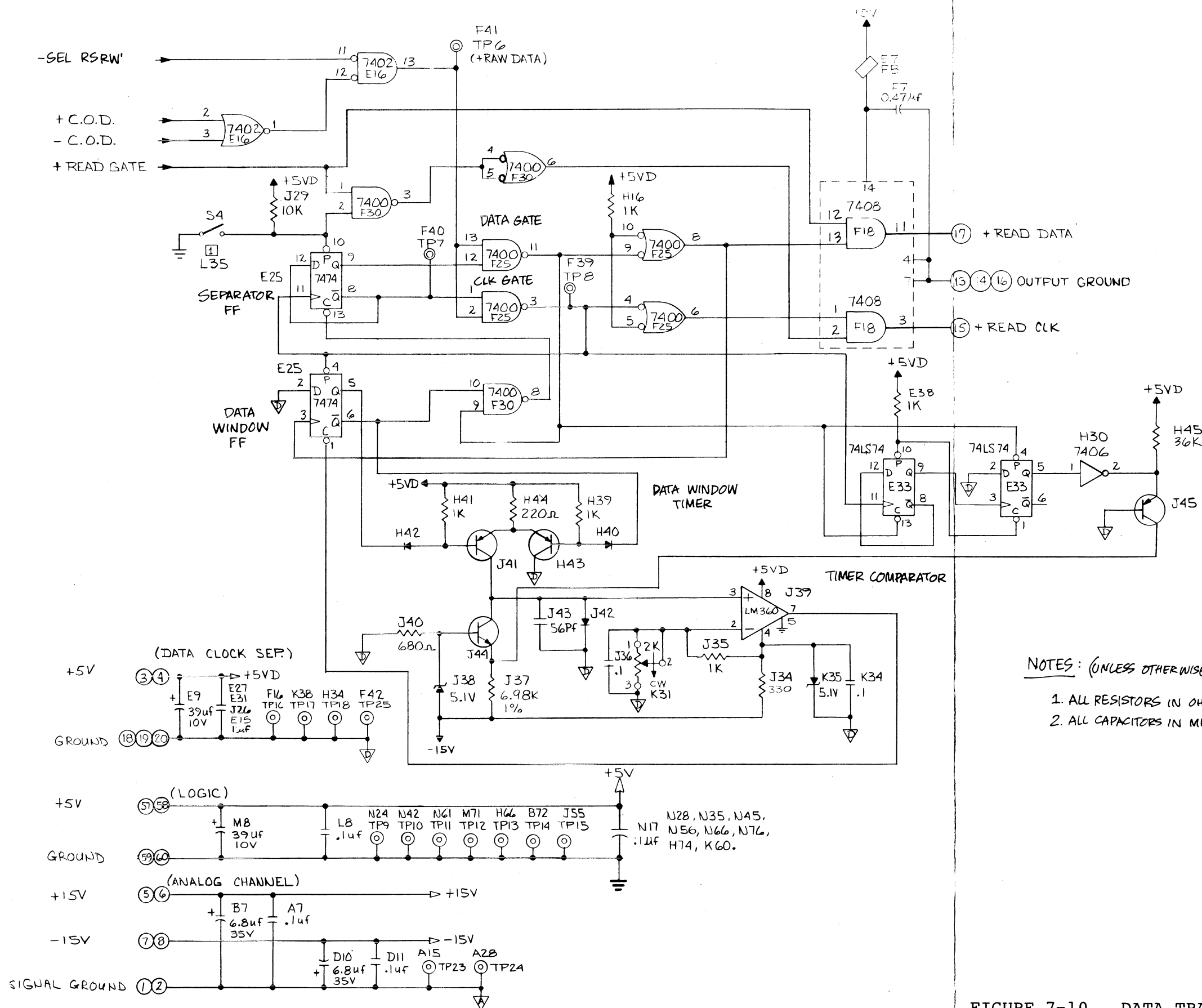
NOTES: (UNLESS OTHERWISE SPECIFIED)
 1. ALL RESISTORS ARE IN OHMS, 1/4W, 2%
 2. ALL CAPACITORS IN MICROFARADS

FIGURE 7-8. DATA TRANSFER PCB SCHEMATIC - SHEET #12046



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS IN OHMS, 1/4 W, 2%
 2. ALL CAPACITORS IN MICROFARADS
 3. UNUSED TRANSISTOR SHORTED TO PREVENT SUBSTRATE BIASING.

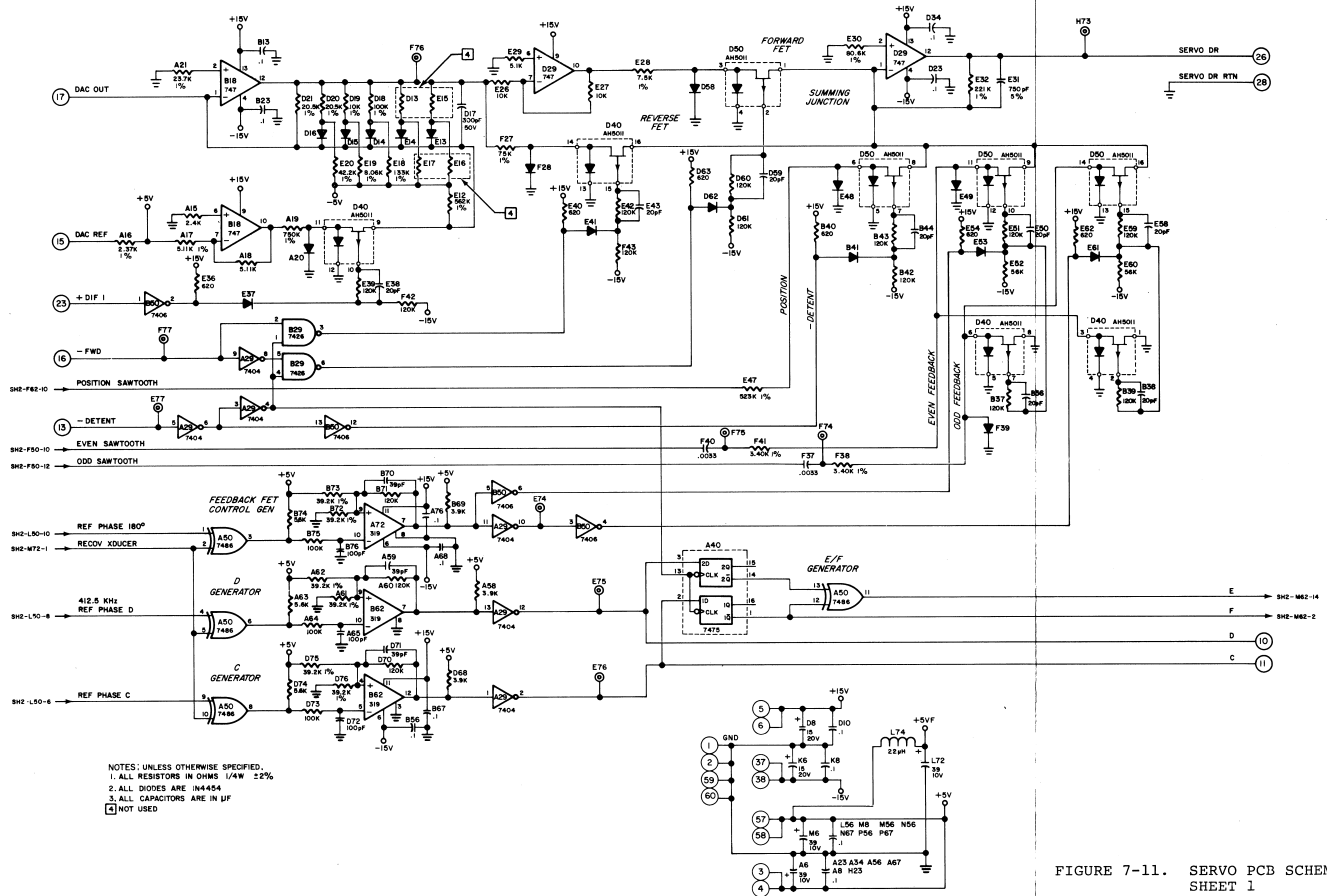
FIGURE 7-9. DATA TRANSFER
PCB SCHEMATIC - SHEET 3
#12046



NOTES: (UNLESS OTHERWISE SPECIFIED)

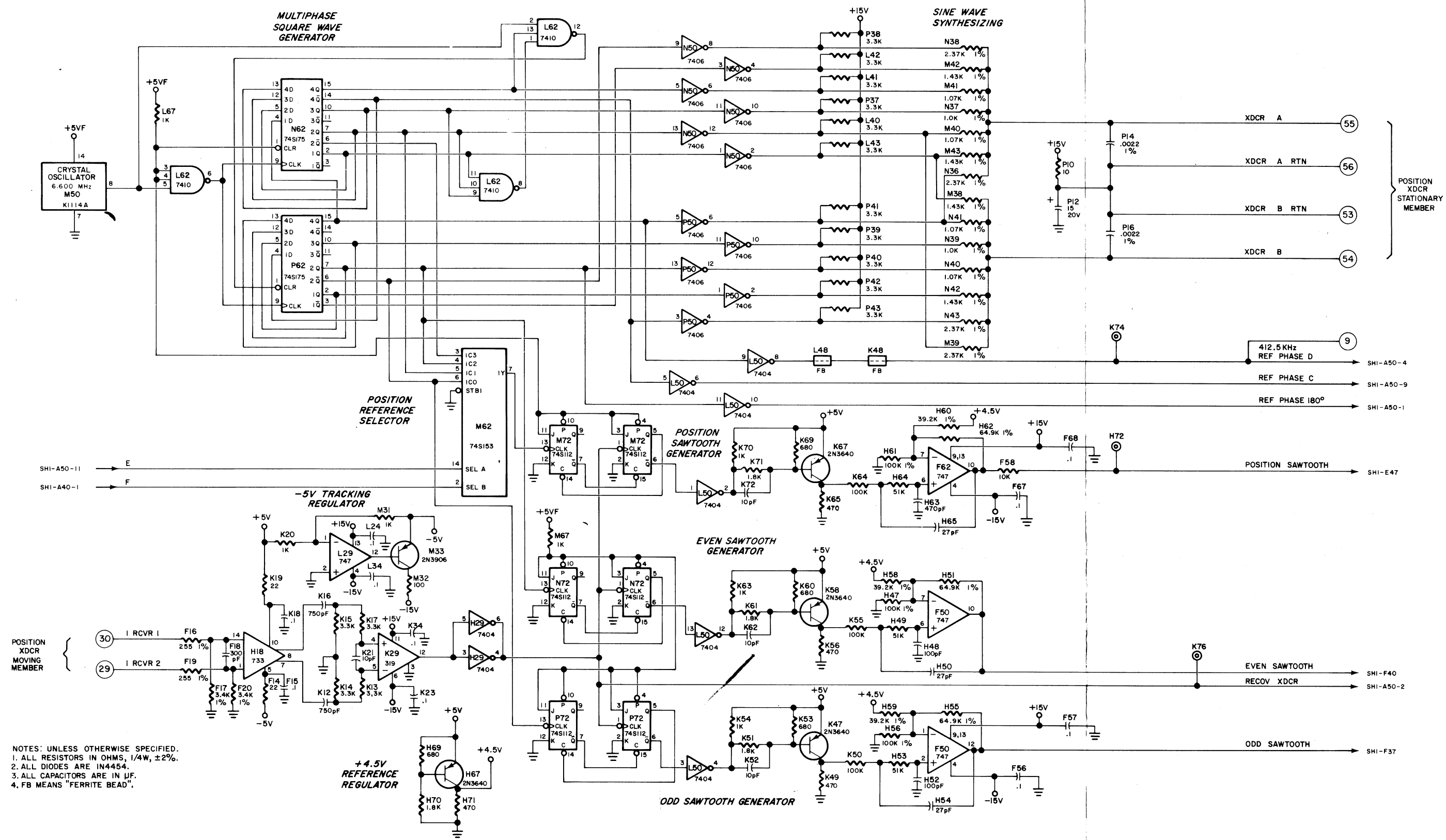
1. ALL RESISTORS IN OHMS, $k\Omega$, $M\Omega$, 2%
2. ALL CAPACITORS IN MICROFARADS

FIGURE 7-10. DATA TRANSFER PCB SCHEMATIC - SHEET 4 #12046



NOTES: UNLESS OTHERWISE SPECIFIED.
 1. ALL RESISTORS IN OHMS 1/4W ±2%
 2. ALL DIODES ARE 1N454
 3. ALL CAPACITORS ARE IN UF
 4. NOT USED

FIGURE 7-11. SERVO PCB SCHEMATIC SHEET 1 #12068



NOTES: UNLESS OTHERWISE SPECIFIED.
 1. ALL RESISTORS IN OHMS, 1/4W, ±2%.
 2. ALL DIODES ARE IN4454.
 3. ALL CAPACITORS ARE IN UF.
 4. FB MEANS "FERRITE BEAD".

FIGURE 7-12. SERVO PCB SCHEMATIC SHEET 2 #12068

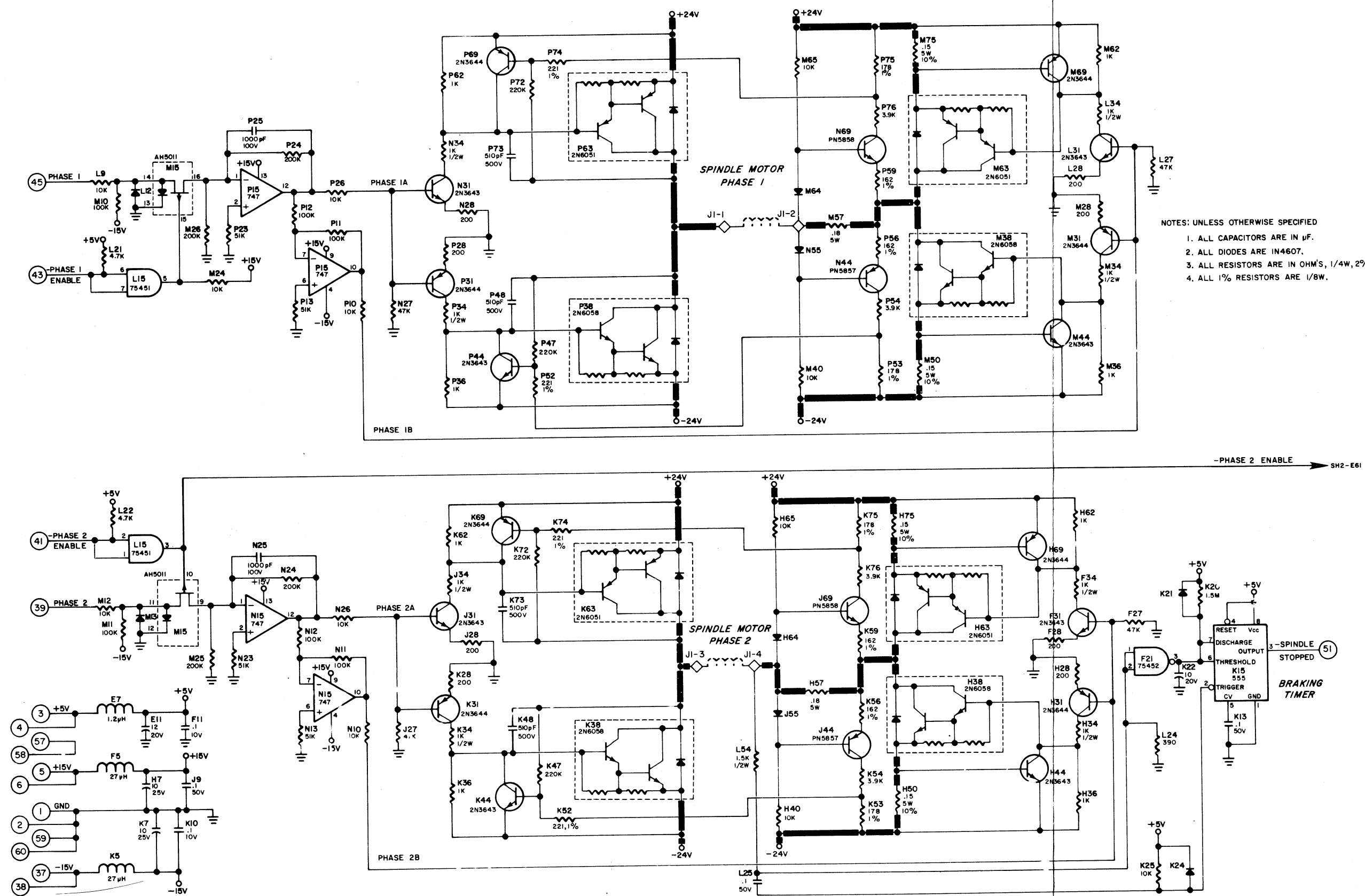


FIGURE 7-13. POWER DRIVER PCB SCHEMATIC - SHEET 1 #12002

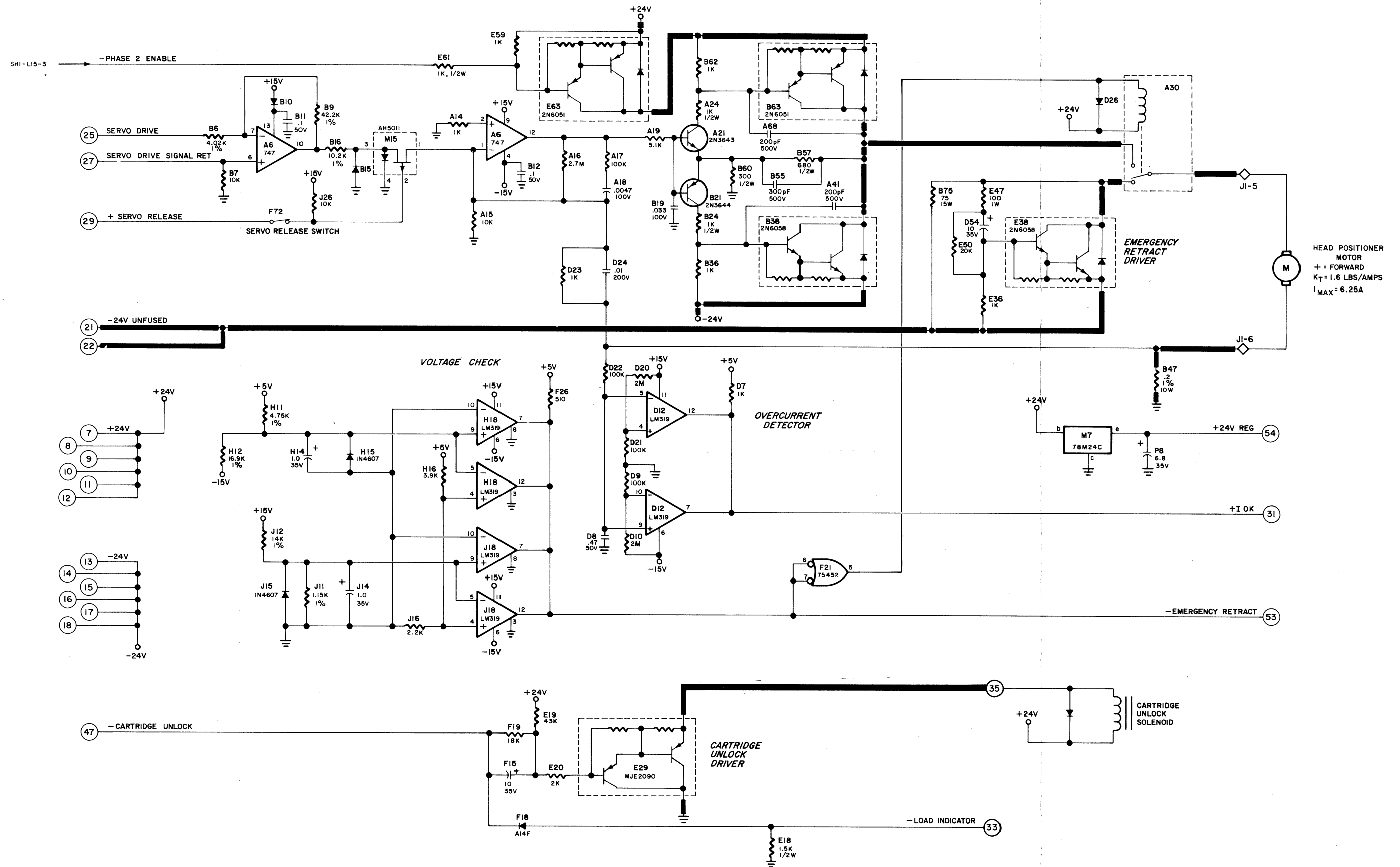


FIGURE 7-14. POWER DRIVER PCB SCHEMATIC - SHEET 2 #12062

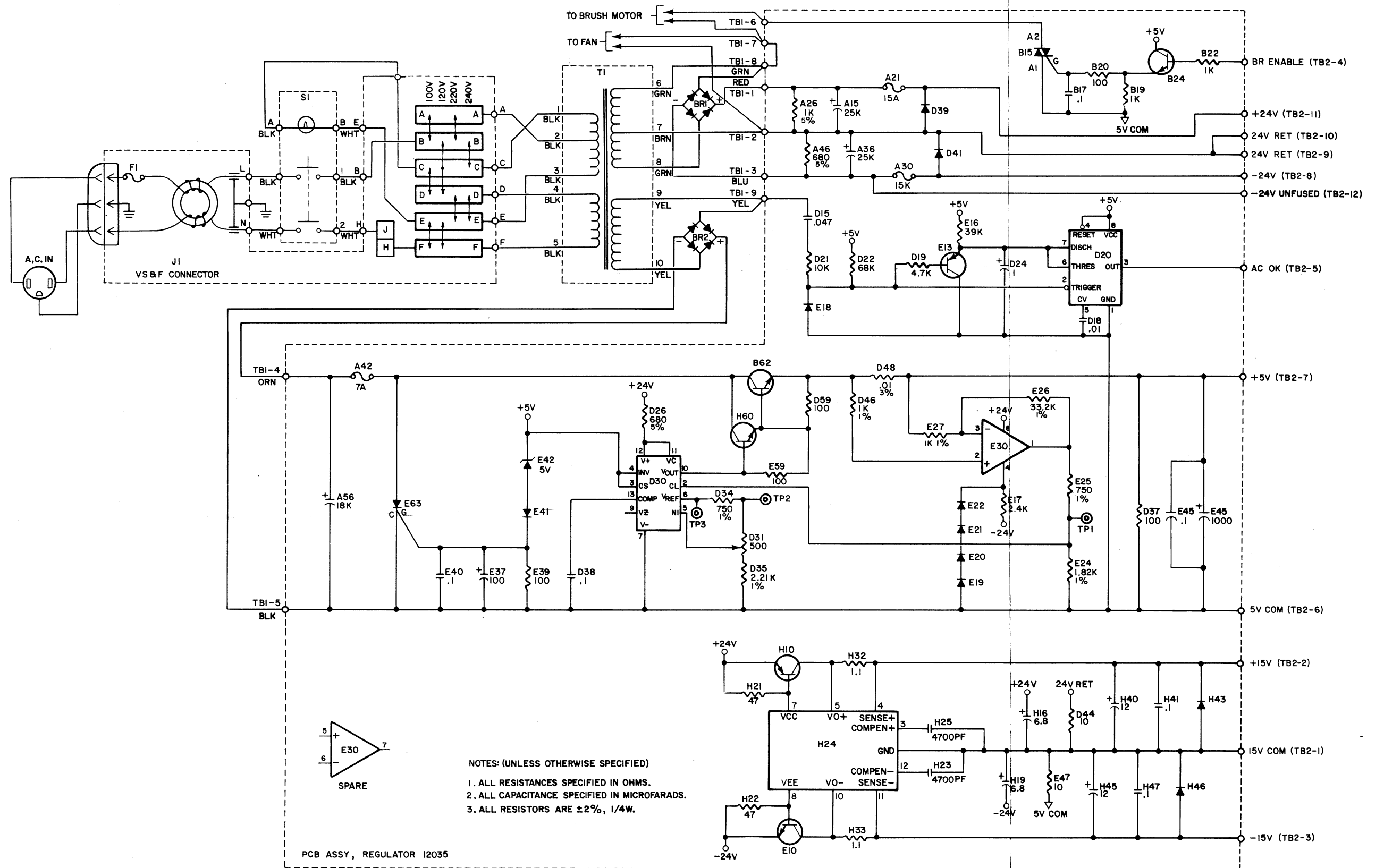
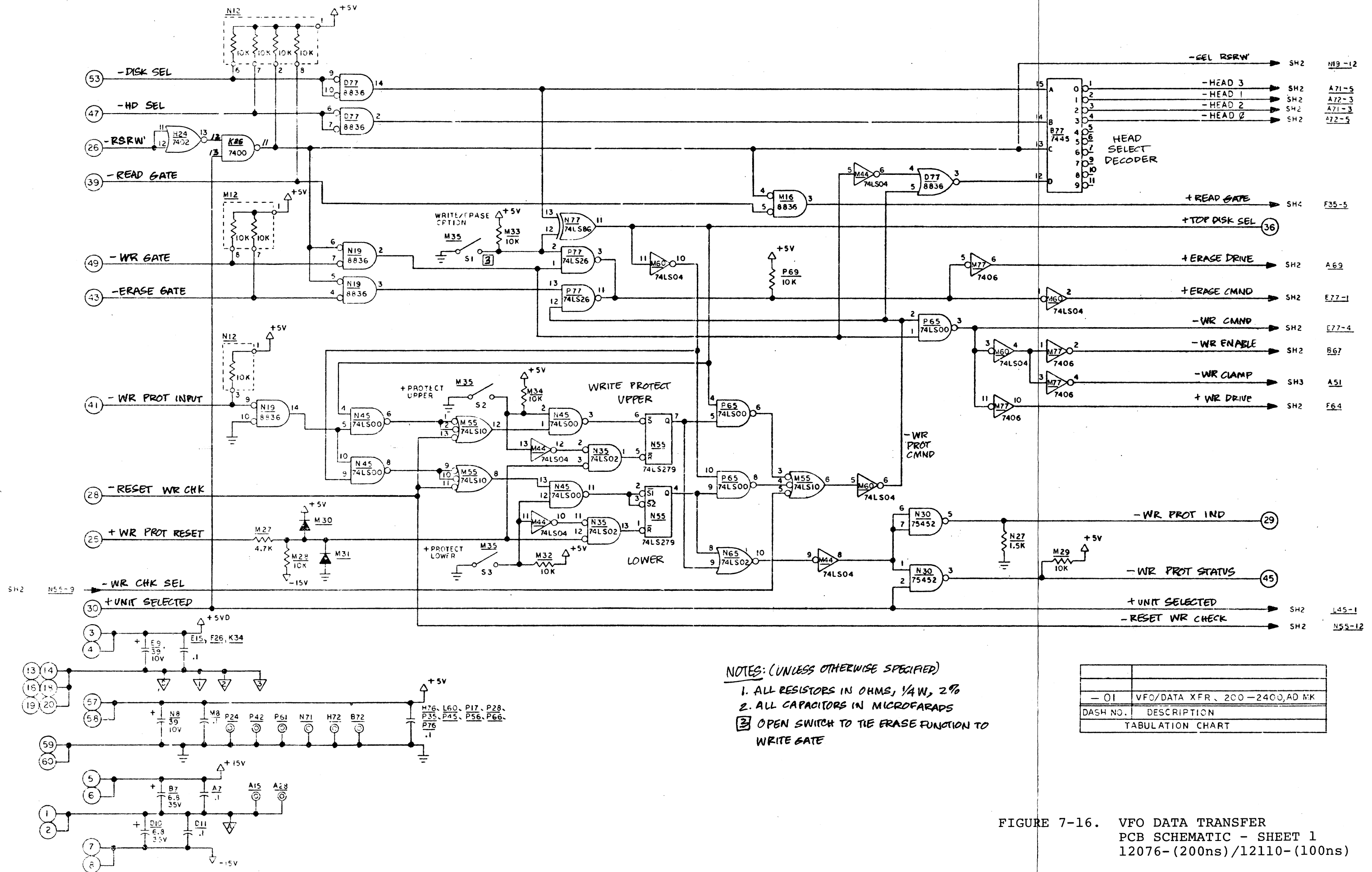


FIGURE 7-15. POWER SUPPLY SCHEMATIC #19033



NOTES: (UNLESS OTHERWISE SPECIFIED)
 1. ALL RESISTORS IN OHMS, 1/4W, 2%
 2. ALL CAPACITORS IN MICROFARADS
 3. OPEN SWITCH TO TIE ERASE FUNCTION TO WRITE GATE

- 01	VFO/DATA XFR, 200-2400, AD MK
DASH NO.	DESCRIPTION
	TABULATION CHART

FIGURE 7-16. VFO DATA TRANSFER
 PCB SCHEMATIC - SHEET 1
 12076-(200ns)/12110-(100ns)

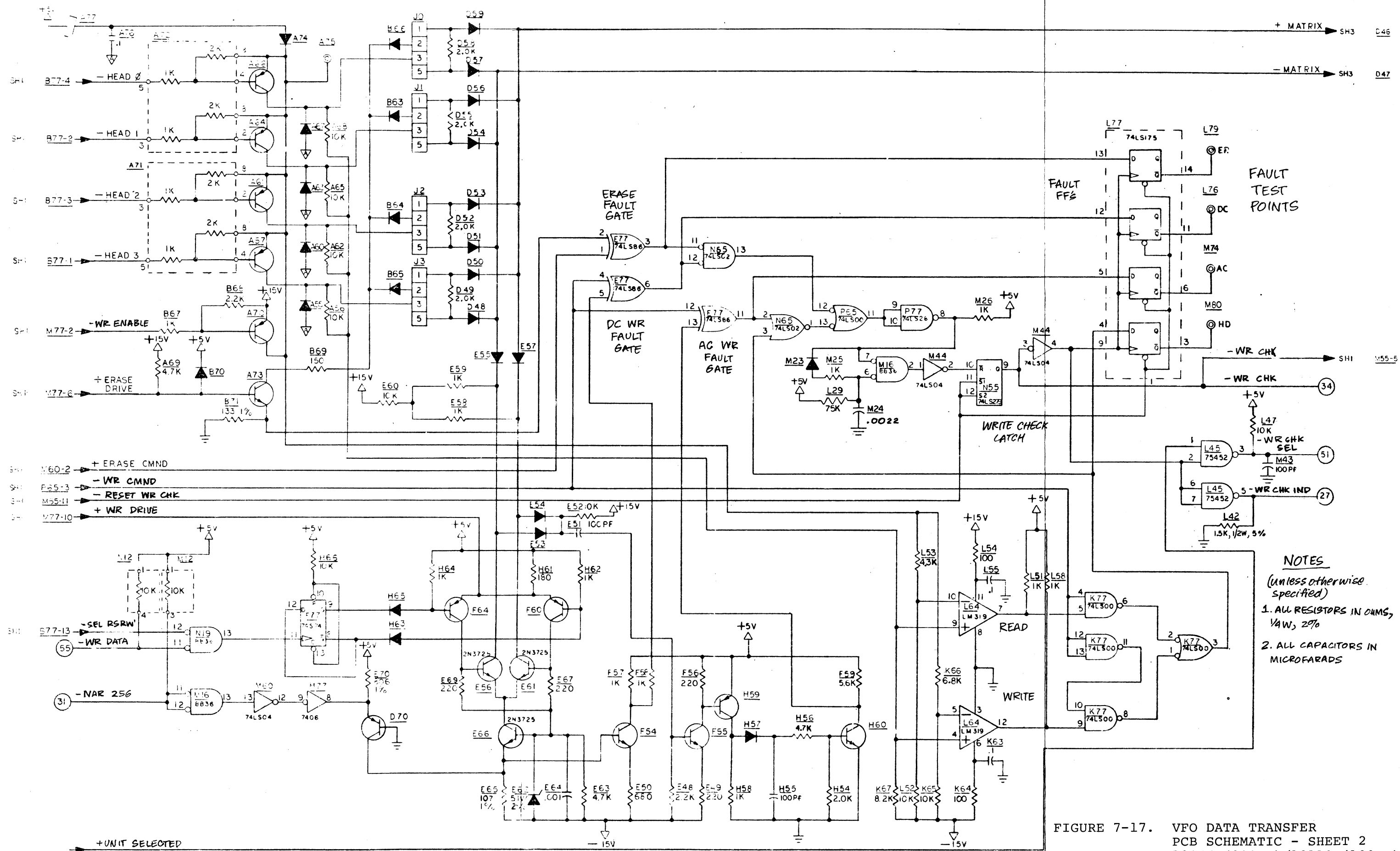
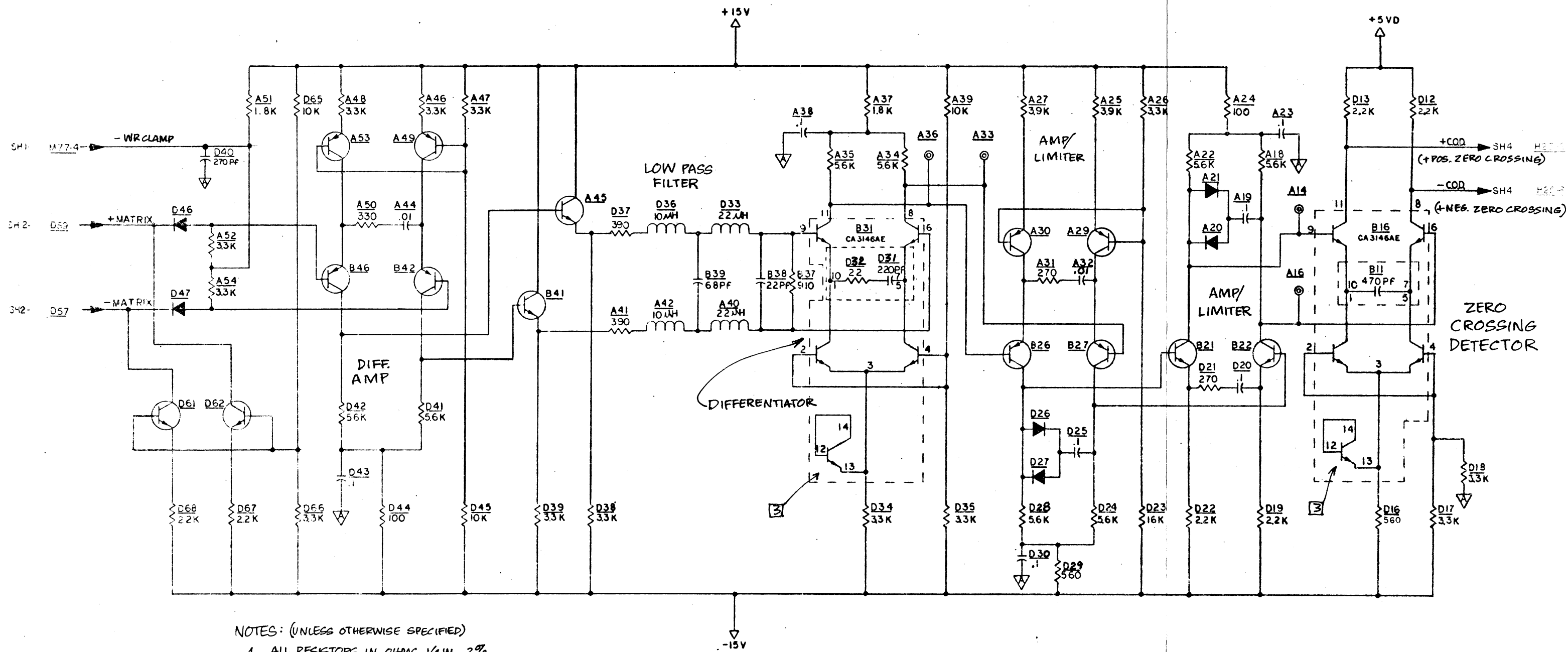


FIGURE 7-17. VFO DATA TRANSFER PCB SCHEMATIC - SHEET 2 12076-(200ns)/12110-(100ns)



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL RESISTORS IN OHMS, μ A/W, 2%
 2. ALL CAPACITORS IN MICROFARADS.
 3. UNUSED TRANSISTOR SHORTED TO PREVENT SUBSTRATE BIASING.

FIGURE 7-18. VFO DATA TRANSFER
PCB SCHEMATIC - SHEET 3
12076-(200ns)/12110-(100ns)

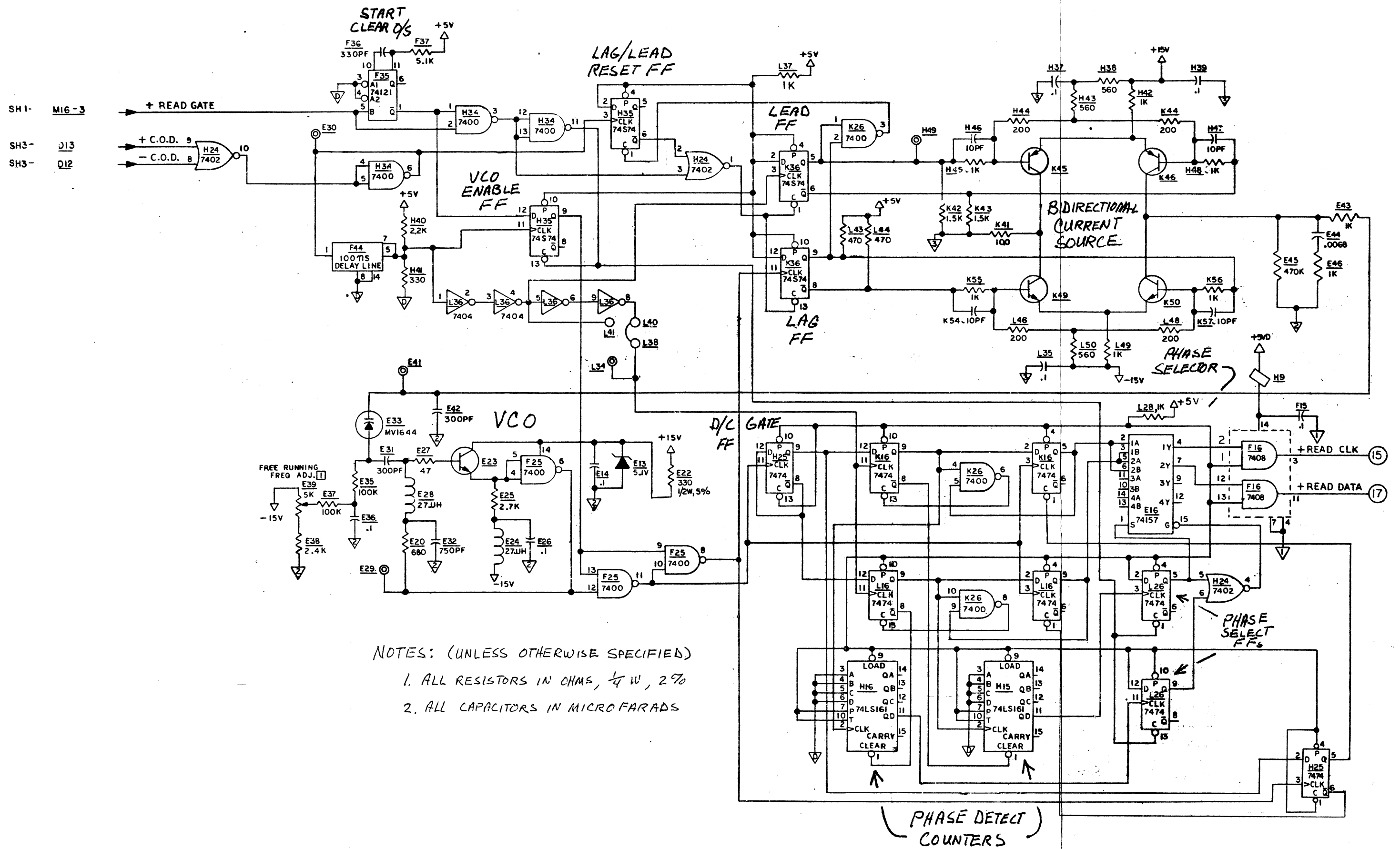
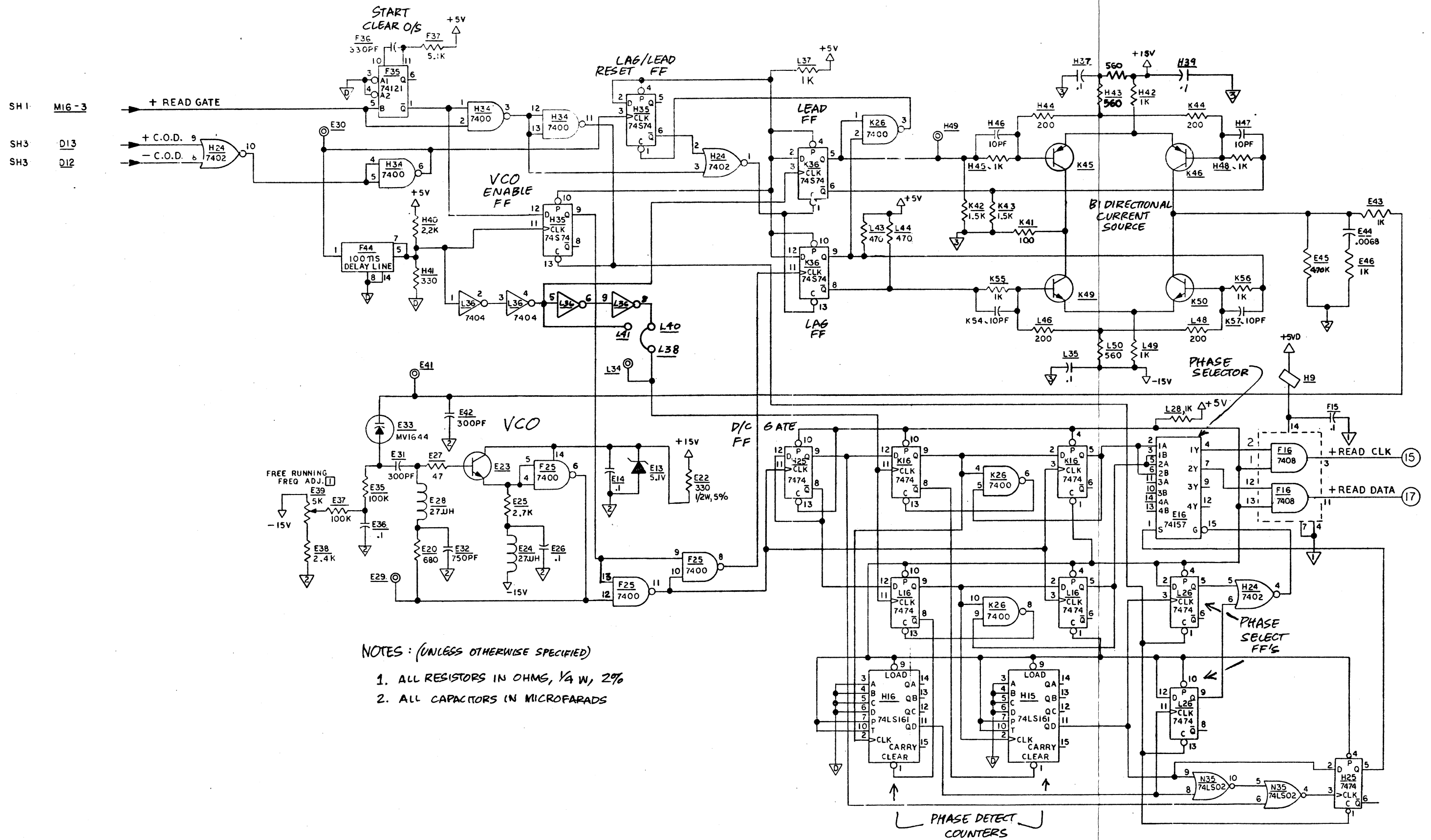


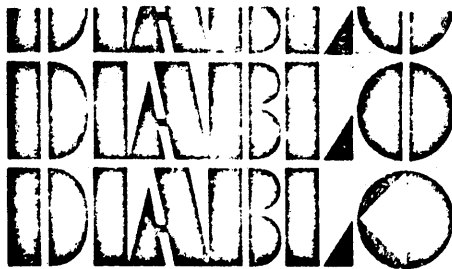
FIGURE 7-19. VFO DATA TRANSFER
 PCB SCHEMATIC - SHEET 4
 #12110-(100ns)



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS IN OHMS, 1/4 W, 2%.
2. ALL CAPACITORS IN MICROFARADS.

FIGURE 7-20. VFO DATA TRANSFER PCB SCHEMATIC - SHEET 4 #12076-(200ns)

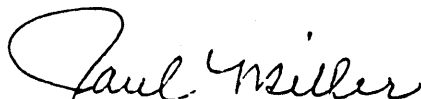


June 7, 1977

FIELD SERVICE AID #9

TO: Model 44B Disk Drive Customers
FROM: Diablo Customer Service
SUBJECT: Revisions 'A' and 'B' to the Maintenance Manual

Attached are revisions 'A' and 'B' to the Model 44B Disk Drive Maintenance Manual (Preliminary), Publication No. 81903-00. Revision 'A' was included in March, 1977 shipments and revision 'B' will be included in June, 1977 shipments.


Paul Miller, Manager
Technical Publications
Customer Service

kc

Feb. '77

DATE



24500 Industrial Blvd.
Hayward, California 94545
Phone: (415) 783-3910

Diablo Systems Incorporated

A Xerox Company

Model 44B Disk Drive Maintenance Manual (Preliminary)
Publication No. 81903-00

Rev. A

PUBLICATION BEING REVISED

PLEASE ENTER THE FOLLOWING REVISIONS AND/OR CORRECTIONS IN YOUR COPY OF THIS MANUAL:

- Page 3-4 3.2.2.1 Input Lines
Write Data and Clock - Change 2nd sentence to read:
"Pulse width must be within the range of 100 to 150 nanoseconds."
- Page 3-5 Write Protect Input - Change 2nd sentence to read:
"If both of the write protect option switches are open,..."
- 3.2.2.2 Output Lines
File Ready - add asterisk to 3rd line of list as follows:
"LOAD/RUN switch in RUN position*"
- Add the following note at the end of File Ready paragraph:
"*When the File Ready line is LO and the Load/Run switch is changed from Run to Load, File Ready remains LO for .125 to .150 second and then goes HI."
- Page 3-7 3.2.2.2 Output Lines
Not Run - Change to read:
"This line immediately goes HI when the drive switches from the Run mode to the Load mode. The controller can use this indication to avoid starting any new read/write activity until the Run mode is reestablished. Meanwhile, the File Ready line continues LO for an additional 125 to 150 milliseconds to allow completion of any read/write action already in progress.
- The use of this line is optional, without any effect on other operations of the drive."
- Page 3-8 Figure 3-1 Output Driver - Read Clock and Read Data.
Delete 1K resistor and +5V.
- Figure 3-2 Output Driver Circuit
Change 1K to 10K and add note:
"75451 used for NOT RUN line to avoid inversion."
- Page 5-17 Four places on page, change head clamp screw torque from 95 inch ounces to 125 inch ounces.

Page 6-1

Table 6-1 Options
Add options and footnote listed below:

<u>Feature</u>	<u>Standard</u>	<u>Optional</u>	<u>Option No.</u>
Fixed Disk Sectoring	----	32 Sector	44B-32
Write Protect:			
Fixed Disk	Off	On	494
Cartridge	Off	On	495
Series 30 Compatibility**	----	----	498

** The Series 30 Compatibility option includes the features listed below. Any one or combination of these features is also available separately upon request.

	<u>Standard</u>	<u>Optional</u>
1) Index Mark	40us pulse	5us pulse
2) LAI Signal	DC level	5us pulse occurring 30us after STROBE
3) ADRS ACK Signal	1.2us pulse	5us pulse occurring 30us after STROBE



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ADDEND A

PAGE 1 OF 4

April '77
DATE

ADDENDA

Model 44B Disk Drive Maintenance Manual (Preliminary)
Publication No. 81903-00 Rev. B

PUBLICATION BEING REVISED

PLEASE ENTER THE FOLLOWING REVISIONS AND/OR CORRECTIONS IN YOUR COPY OF THIS MANUAL:

- Page 3-5 3.2.2.1 Input Lines
Write Protect Input - Add following sentence:
"Since this line is not gated by Unit Select, the pulse is applied simultaneously to all drives in a daisy chain."
- 3.2.2.2 Output Lines
Address Acknowledge - Change 2nd sentence to read:
"An -ADDRESS ACKNOWLEDGE signal (1 microsecond LO)..."
- Page 3-6 3.2.2.2 Output Lines
Seek Incomplete - Change 2nd sentence to read:
"This signal level will be maintained until receipt of a RESTORE command and STROBE, or until the drive is switched to LOAD and back to RUN."

Write Check - Change item (2.) to read:
"2a. WRITE GATE LO without DC write current."
"2b. WRITE GATE LO without AC write current."
- Page 3-7 3.2.2.2 Output Lines
NOT RUN - Change to read:
"This line goes HI when the drive switches from Run Mode to Load Mode, or when +AC OK goes LO to indicate loss or turn-off of AC power."
- Page 4-26 4.3.7.8 Fault Detection
In list of "Fault Conditions", change 2nd item to read:
".No DC write current with -WRITE GATE = LO."
".No AC write current with -WRITE GATE = LO."
- Page 4-32 4.3.2.4 Strobe Logic
In 2nd paragraph:
Change "2.1 microsecond" to "1 microsecond."
- Page 4-50 4.3.4.3 Home and Over Tracks Detectors
Add following sentence at end of 3rd paragraph:
"Comparator A20 (shown in Figure 7-5) establishes a stable switching threshold for the OVER TRKS DETECT signal."
- Page 4-53 4.3.4.4 -RETRACT
In 2nd paragraph item "2)":
"Home Selector" should be "Home Detector".

Model 44B Disk Drive Maintenance Manual (Preliminary)
Publication No. 81903-00 Rev. B

April '77

DATE

- Page 4-56 4.3.4.7 Sector Counter
4th paragraph, last sentence:
"RO" should be "RO₁".
- Page 4-76 4.3.6.3 Positioner Motor Driver
In 1st sentence:
Change "Figure 6-14" to "Figure 7-14".
- Pages 4-79 Discard old pages 4-79 thru 4-81.
thru 4-81 Insert new pages 4-79 thru 4-90.
- Page 5-3 5.2.3.2 Item h.
Change P/N 99001 to P/N 70342.
- Page 5-12 5.6.4.2 Lower Index Transducer Adjustment
Change 2nd sentence to read:
"The amplitude of the positive peaks must be at least +400mV and the amplitude of the negative peaks must not exceed -1500mV. The positive pulse must occur first."
- Page 5-15 Step 2.
Change 1st sentence to read:
"Set the oscilloscope as follows:"
- Following step 3 add step "3a" to read:
"Unfasten the head lead clamp bracket (visible in lower right corner of Figure 5-13) from the head positioner chassis. Remove the two card cage retaining screws and carefully slide the card cage rearward to allow side access to the head clamps."
- CAUTION
- "To avoid head lead damage, seek operations must not be performed while the card cage is positioned rearward. When the card cage is returned to its forward position check that all connectors are properly seated onto the Mother PCB connectors."
- Page 5-17 5.6.4.4 Upper Index Transducer Adjustment
Change 3rd sentence to read:
"The amplitude of the positive peaks must be at least +300mV for narrow (0.20") sector slots, and the amplitude of the negative peaks must be no greater than -1500mV for wide (0.80") sector slots. The positive pulse must occur first. If the signal falls outside the specified limit, proceed as follows:"
- Page 5-19 5.6.4.4 Step 9.
Change 1st sentence to read:
"9. Using the leading (negative-going) edge of the index pulse at TP-F75 (12065 artwork) or TP-E76 (12065-01/-02 artwork) as a trigger, observe the signal at TP-A33 or TP-A36 of the D/T PCB."

Page 5-25

5.6.5.1

"Check Procedure" Step 1., Change to read:

"1. On Logic PCB, trigger scope externally on negative-going edge of index pulse at TP-F75 (12065 artwork) or TP-E76 (12065-01/-02 artwork)."

"Adjustment Procedure" Step 3., Change to read:

"3. Loosen two screws holding temperature compensation arm to dust plate."

Page 6-1

6.1 OPTIONS

Change Option No. 498 - Series 30 Compatability - to read as follows:

	<u>Standard</u>	<u>Optional</u>
1) Index/Sector Marks	40usec pulse	5+2 usec pulse
2) LAI Signal	DC level	5+2 usec pulse occurring 35+10 usec after STROBE leading edge.
3) ADRS ACK Signal	1usec pulse	5+2 usec pulse occurring 35+10 usec after STROBE leading edge.
-RSRW Signal	Hi within 1usec of STROBE leading edge.	Goes HI 35+10 usec after STROBE leading edge.

Page 7-6 Insert attached new page. Discard old page 7-6.

Figure 7-1 Change diagram number from "#19033" to "19030".

Figure 7-3A Insert attached new page.

Figure 7-4A Insert attached new page.

Figure 7-3B Insert attached new page.

Figure 7-4B Insert attached new page.

Figure 7-5 Insert attached revised page. Discard old Figure 7-5.

Figure 7-6 Insert attached revised page. Discard old Figure 7-6.

Figure 7-5A Insert attached new page.

Figure 7-6A Insert attached new page.

Figure 7-5B Insert attached new page.

Figure 7-6B Insert attached new page.

April '77
DATE

Figure 7-10 Add Note 3 as follows:

"3. K31 Adjustment: With all zeros data pattern, adjust K31 to produce a period of 320nsec from leading edge at test point F41 to leading edge at test point F40."

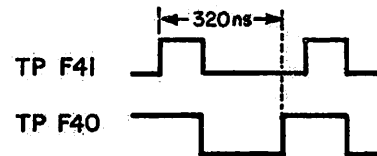


Figure 7-13 Insert attached revised page. Discard old Figure 7-13.

Figure 7-14 Change "-I OK" to "+I OK".
Change resistors D10, D20 from 2.7M to 2M.

Figure 7-13A Insert attached new page.

Figure 7-14A Insert attached new page.

Figure 7-19 Add Note 3 as follows:

"3. E39 Adjustment: With -READ GATE held HI, adjust E39 to produce 5.08MHz at test point E29."

4.3.6.6 +24V Regulator

The +24V Regulator (M7) provides overvoltage protection for the front panel indicator lamps.

4.3.6A Power Driver (P/D) PCB - No. 12062-01

For Power Driver PCB No. 12062 refer to 4.3.6.

The Power Driver PCB contains the following circuits.

- (1) Spindle Motor Drivers
- (2) Braking Timer
- (3) Head Positioner Motor Driver
- (4) Voltage Sense and Emergency Retract Circuits
- (5) Cartridge Unlock Circuit

4.3.6.1A Spindle Motor Driver

The spindle motor is an AC induction motor with two stator windings phased 90 electrical degrees apart. Drive for the motor requires a nominal 48 volt AC signal applied to each stator winding, with the Phase 1 signal leading the Phase 2 signal by 90°. The rotational rate is proportional to the frequency of excitation, which is slightly above 80 Hz for 2400 RPM and slightly above 50 Hz for 1500 RPM. Rotor slip is compensated for by the speed control logic on the Logic PCB which provides automatic frequency control to hold the disk speed within $\pm 0.5\%$ of its nominal value. Braking of the motor is accomplished by applying a DC signal to the Phase 1 winding and turning off drive to the Phase 2 winding. The spindle stops rotating approximately 15 seconds after the Load/Run switch is set to LOAD. Power dissipation in the motor and driver circuits is limited through the use of switching current regulators.

The driver circuits for Phase 1 and Phase 2 are identical, consisting of bridge power drivers with switching current regulation. A block diagram of the Phase 1 driver is shown in Figure 4-38, and pertinent waveforms are shown in Figure 4-39. Circuit operation is described in the following paragraphs.

When the disk drive is in the Load mode, the Enable FET is off. The output of the Input Amp is held at 0V $\pm 0.8V$, turning off the Current Drivers and permitting no current flow through the motor winding.

The Enable FET turns on when the output of the Enable Gate is LO. The Input Amp converts the PHASE 1 TTL signal into a trapezoidal waveform that switches between +15V and -15V. When the Amp output swings positive, Current Driver 1 turns on, turning on Current Switch 1 and also turning on Current Driver 4 through the Coupling Resistor. Current Driver 4 then turns on Current Switch 4. As a result, approximately 48 volts is applied across the motor winding, with terminal J1-1 at +24V nominal and terminal J1-2 at -24V nominal.

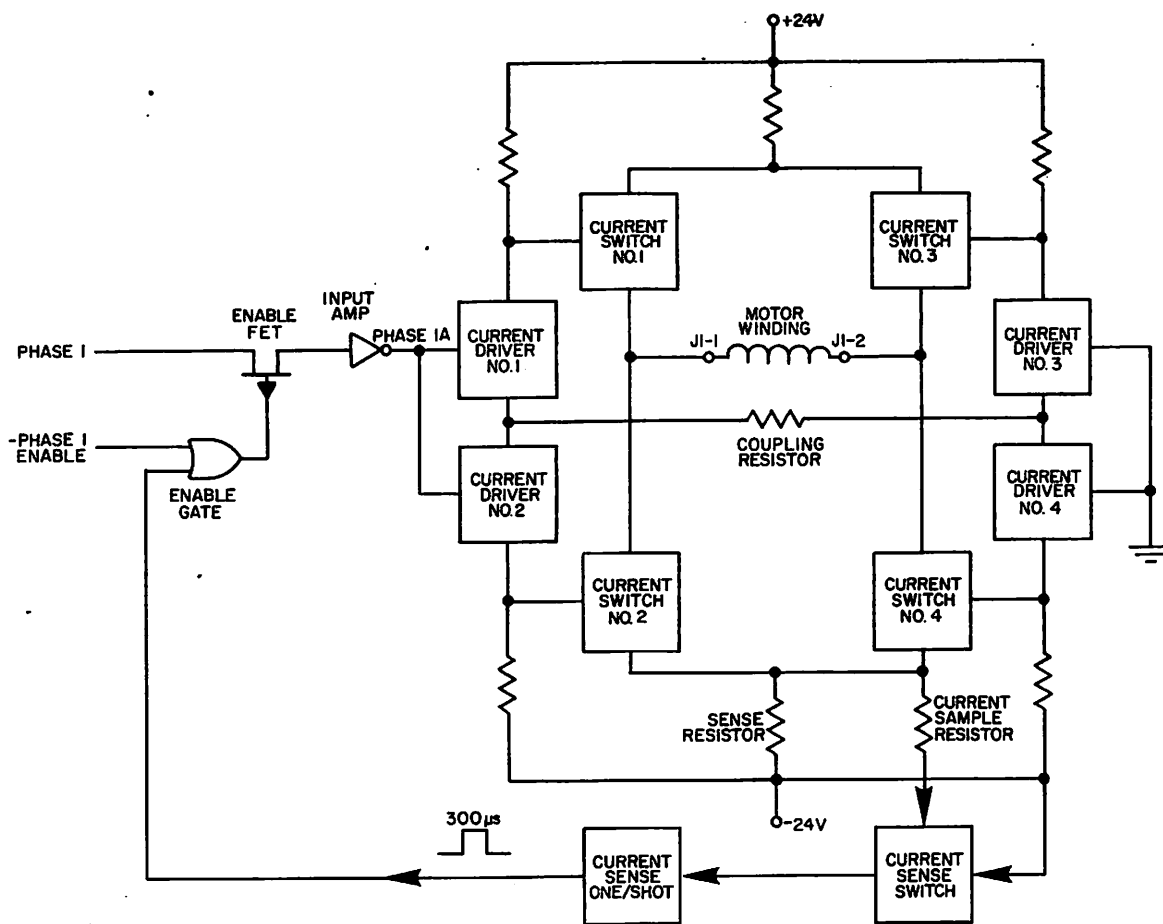


Figure 4-38. SPINDLE MOTOR PHASE 1 DRIVER
(Power Driver No. 12062-01)

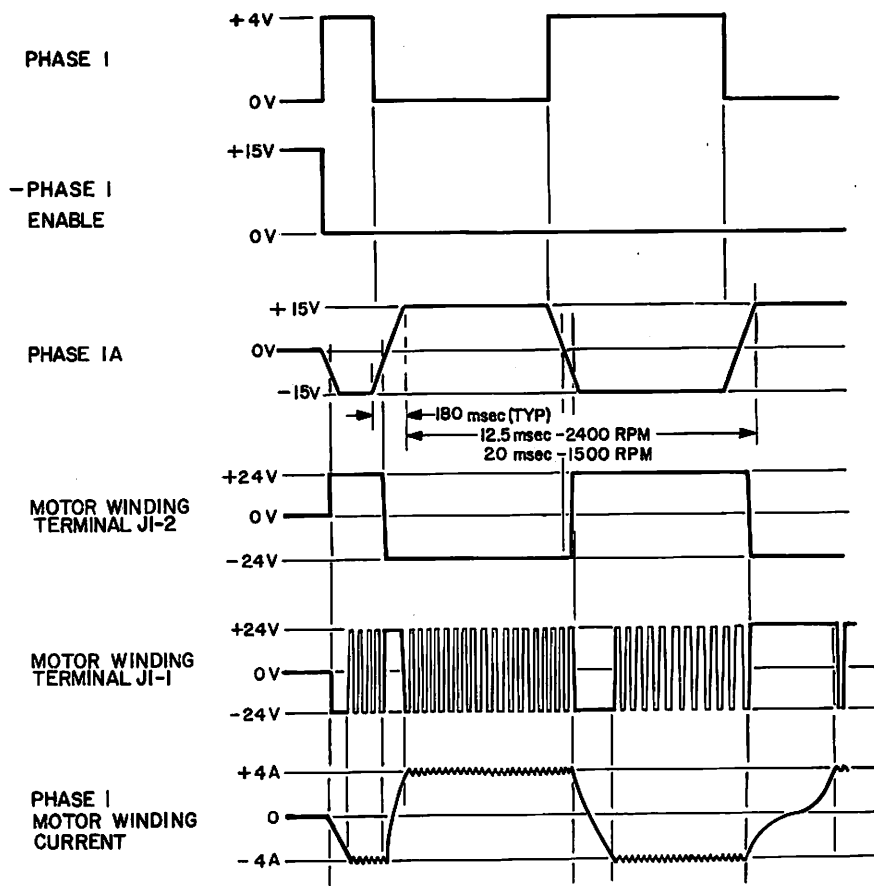


Figure 4-39. PHASE 1 SPINDLE DRIVER WAVEFORMS DURING STARTUP

As current builds up in the motor winding, a voltage develops across the Sense Resistor proportional to the current in the motor winding. When this voltage approaches 0.7V, the Current Sense Switch turns on and triggers the Current Sense One-Shot. The pulse output from the One-Shot turns off the Enable FET. The Input Amp output goes to 0v and the Current Drivers and Switches turn off. After 300 usecs. (+111 usecs.), the Current Sense One-Shot resets, the Enable FET turns on again and Current Drivers 1 and 4 and Current Switches 1 and 4 turn on again. Current again begins to build up in the motor winding and the current limiting cycle repeats. The current limiting circuitry is designed to trigger at 4A of motor current.

During the next half cycle of PHASE 1, the Input Amp output swings negative. Current Drivers and Current Switches 1 and 4 turn off, and Current Drivers and Current Switches 2 and 3 turn on. This reverses the voltage polarity applied across the motor winding and reverses the direction of current flow through the winding. The current limiting circuitry continues to function as it did during the previous half cycle of PHASE 1.

As motor speed increases, the counter emf of the motor limits the current to an average value of approximately 4A. In a disk drive set up for a spindle speed of 2400 RPM, the switching current regulators are normally active only during spindle acceleration and braking, when counter emf is insufficient to limit motor current adequately. In a disk drive set up for 1500 RPM operation, the switching current regulators operate for a portion of every half cycle of PHASE 1 and PHASE 2. Due to the lower speed and slower switching rate, motor current builds to a higher value at 1500 RPM than at 2400 RPM.

The spindle motor driver circuits are capable of continuous operation as long as the power devices are properly mounted on the heat sink. The switching current regulator minimizes power dissipation, since the devices dissipate little power when saturated, and no power when cut off. Primary power dissipation occurs while the device is switching.

No adjustments are required to the Spindle Motor Driver circuits.

CAUTION

Probing of the Power Driver PCB with power applied should be avoided because of the danger of accidental shorts which may destroy a power stage. Operation of the driver circuits with a non-inductive dummy load will result in excessive power dissipation in the switching current regulator circuits due to the increased switching frequency.

4.3.6.2A Braking Timer

Refer to Figures 4-40 and 4-41. Braking timer L15 establishes the 22+6 second time interval during which dynamic braking is applied to the spindle motor when the disk drive is switched from RUN to LOAD. During braking, the PHASE 1 signal is held HI and PHASE 2 is disabled. This results in a continuous HI at gate output F21-3, and capacitor L22 begins charging through resistor L20. When the potential on L22 reaches the threshold level of the timer, the output of the timer (-SPINDLE STOPPED) goes from HI to LO. By this time the spindle has stopped rotating. -SPINDLE STOPPED is sent to the Logic PCB where it turns off PHASE 1 which is no longer needed for braking.

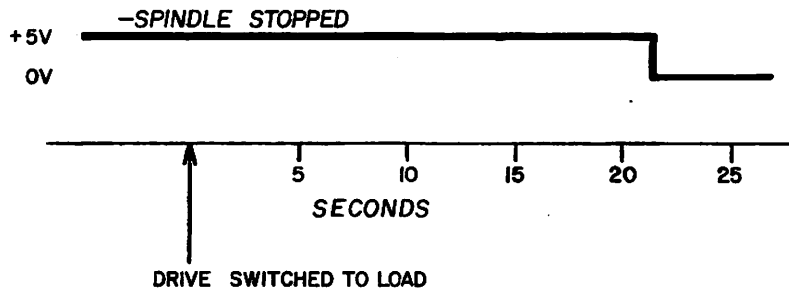


Figure 4-40. -SPINDLE STOPPED TIMING

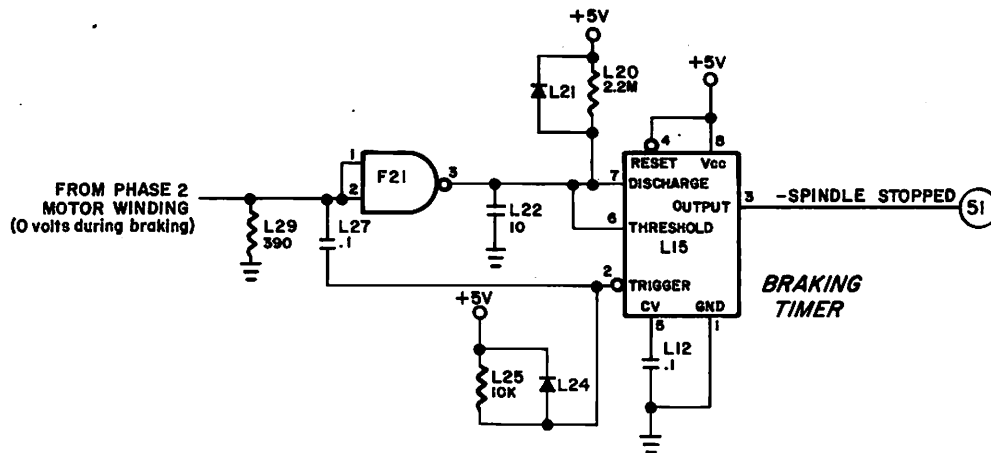


Figure 4-41. SPINDLE BRAKING TIMER

4.3.6.3A Positioner Motor Driver

A block diagram indicating the functional divisions of the positioner motor driver is shown in Figure 4-42. These divisions are: (1) an Input Amplifier, (2) a Servo Release circuit to release the head positioner from servo control, (3) a Current Limit Amplifier to limit motor current by negative feedback, (4) a Power Driver to provide adequate drive current for the positioner motor, (5) an Emergency Retract Driver to retract and unload the heads if an out-of-tolerance voltage condition is detected, (6) a Voltage Check circuit to detect supply voltage failures, and (7) an Overcurrent Detector circuit.

Refer to the Servo Driver portion of Figure 7-14A. The Power Driver for the head positioner motor consists of a positive driver B63 (forward motion) and a negative driver E63 (reverse motion). The drive current developed for small input signals is directly proportional to the amplitude of the signal. For large input signals, the drive current is limited to approximately 6.25A by negative feedback from the current sense resistor B43 to the Current Limit Amplifier. Currents of this magnitude for longer than 32 milliseconds cause a "SEEK INCOMPLETE" signal to be generated.

SERVO DRIVE is an analog signal generated on the Servo PCB. When positive, the SERVO DRIVE signal turns on the positive driver network. When the heads are detented (held stationary over a track), any motion of the heads away from the detent position causes the SERVO DRIVE signal to generate an opposing signal. Since positive drive current causes the positioner carriage to move toward the spindle, attempting to manually move the positioner carriage toward the spindle will cause negative drive current to flow in the motor. The amount of current flowing will be proportional to the amount of force applied, up to the limit of 6.25 amperes.

The servo driver may be released from control by the SERVO DRIVE signal by two different means: (1) by a HI SERVO RELEASE signal, which occurs when the positioner is in the home position and no -RETRACT signal is present; and (2) by manual operation of the Servo Release switch. Head crash will occur if the spindle is stopped with the heads over the disk; consequently, the Servo Release switch should not be used if spindle power is off.

The overcurrent integrator has a time constant of 47 milliseconds and the overcurrent detector a threshold of 0.8 volt. The resulting time constant for the combination of the integrator and the detector for a full current condition (6.25A) is 32 milliseconds for currents of either polarity. At the end of the time constant, the overcurrent signal will go LO. Lower current values cause longer delay times, and values less than 1.6A are below the threshold of the detector circuit.

4.3.6.4A Voltage Check and Emergency Retract

Refer to Figure 4-43. The purpose of these circuits is to perform an emergency retract operation in the event of a failure or out-of-tolerance condition of any of the supply voltages.

The voltage check circuit senses the +15 VDC, -15 VDC and +5 VDC. This also indirectly includes the +24 VDC and -24 VDC, since +15V and -15V are derived from them. The +15 VDC and -15 VDC are monitored for both overvoltage and undervoltage. The +5 VDC is monitored for undervoltage by the voltage check circuit on the Power Driver PCB, while overvoltage protection is provided

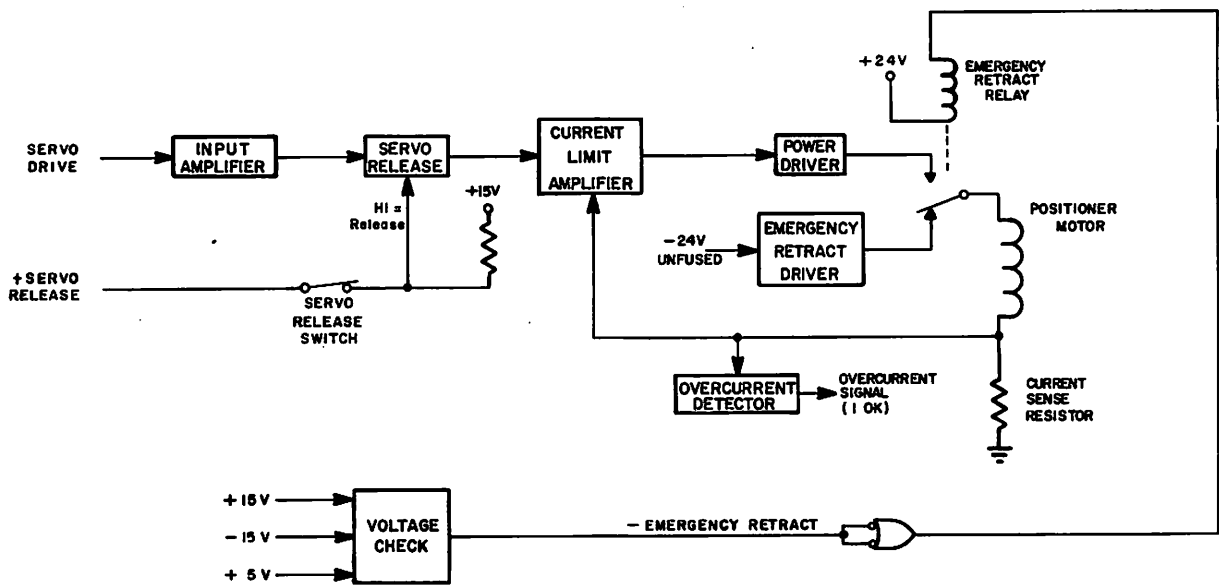


Figure 4-42. HEAD POSITIONER DRIVER
(Power Driver No. 12062-01)

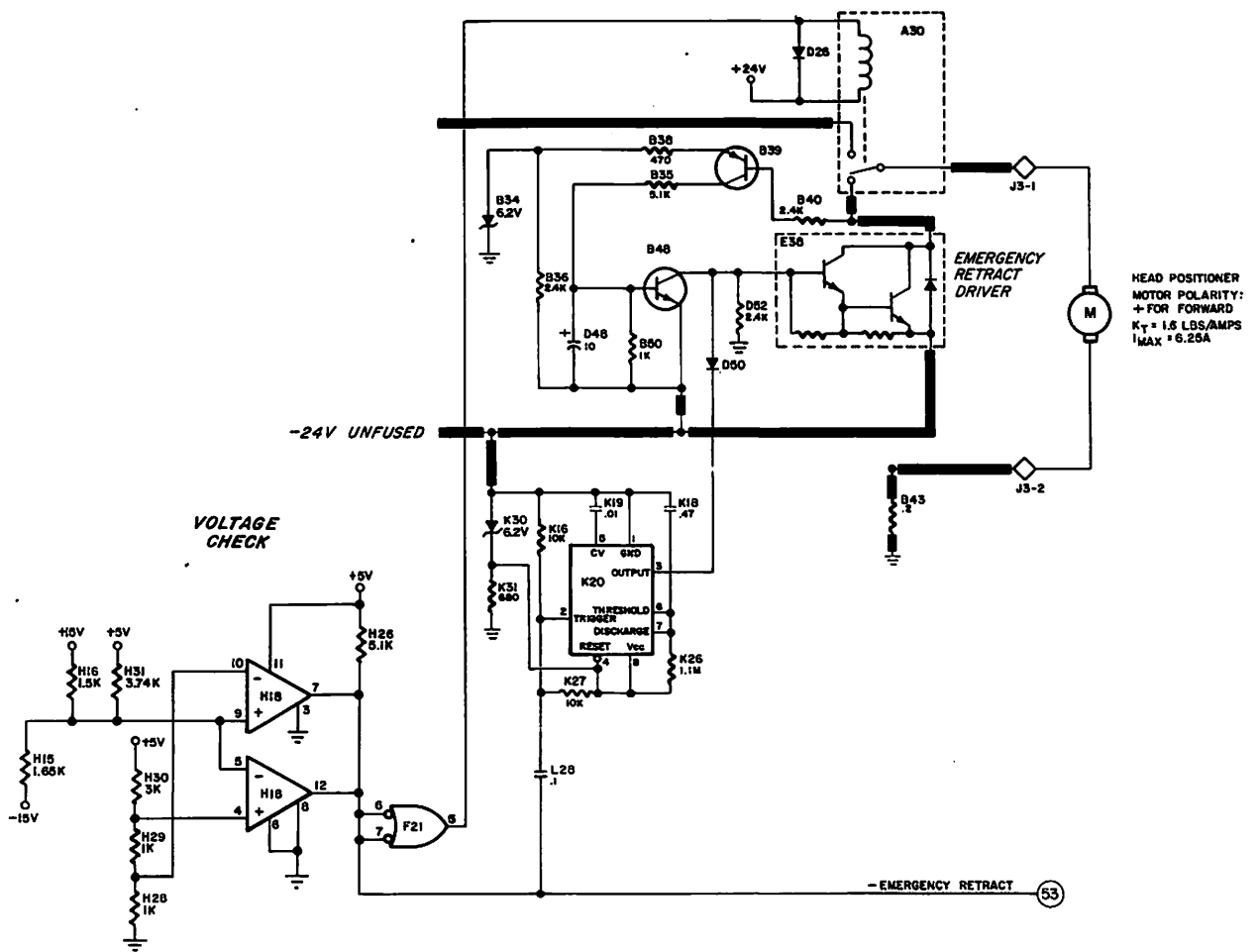


Figure 4-43. VOLTAGE CHECK AND EMERGENCY RETRACT
(Power Driver No. 12062-01)

by a circuit in the +5 VDC power supply. If a failure or out-of-tolerance condition occurs, the output signal (-EMERGENCY RETRACT) of the voltage check circuit goes LO.

The emergency retract circuit utilizes a relay and the unfused -24V power supply to retract the heads. When the -EMERGENCY RETRACT signal goes LO, the output of power gate F21-5 turns off and deenergizes relay A30. This disconnects the positioner motor from the servo driver output and connects it to the emergency retract driver. As -EMERGENCY RETRACT goes LO, a negative pulse is coupled through capacitor L28 and triggers timer K20-3. Timer output K20-3 goes HI and allows the retract driver transistor E38 to turn on. Transistors E38, B39 and B48 function as a switching current regulator to provide a controlled current of about 3A to the positioner motor. This current accelerates the positioner carriage to a velocity sufficient to overcome the ramp resistance as the heads unload. The retract current is maintained until the timer times out (approximately 500 msec.) or until the -24V supply has decayed to the point where the retract driver turns off. During this time, the positioner carriage is actively held in the home (retracted) position by the retract current.

4.3.6.5A Cartridge Unlock Driver

Refer to Figure 7-14A. The cartridge unlock solenoid driver is controlled by the -CTG UNLOCK signal. When -CTG UNLOCK is HI, the driver transistor is off and the solenoid remains in its deenergized locked position. When -CTG UNLOCK goes LO, capacitor F15 begins charging and the driver transistor conducts heavily, providing pull-in current to the solenoid. As the capacitor charges, conduction through the driver transistor decreases and its emitter voltage rises. When the emitter voltage has risen to +12 volts, current flow through the driver transistor levels off and remains constant, supplying holding current for the solenoid.

4.3.6.6A +24V Regulator

The +24V Regulator M25 provides overvoltage protection for the front panel indicator lamps.

4.3.7 Power Supply Assembly (#19033)

4.3.7.1 General Characteristics

The internal power supply assembly of the Model 44B performs the following functions:

- 1) Produces the DC voltages required by the disk drive circuits:

+24 VDC/-24 VDC/-24 VDC UNFUSED
+15 VDC/-15 VDC
+5 VDC

- 2) Produces an "AC OK" signal to indicate the status of AC input power.
- 3) Provides on-off control and power for the brush motor.
- 4) Provides power for the fan motor.

The Model 44B power supply is adaptable to any one of four different AC input voltages: 100, 120, 220 or 240 VAC at 49 to 61 Hz. The disk drive is set for the appropriate input voltage by a small 4-position voltage selector printed circuit card. This card is located in the fuse compartment near the on-off switch at the rear of the machine. To adapt the drive to a different input voltage, the selector card is simply pulled out, turned to the desired position (as indicated on the card), and reinserted.

4.3.7.2 Theory of Operation

Refer to Figure 7-15.

- 1) +24 VDC/-24 VDC/-24 VDC UNFUSED

The circuit to develop these voltages consists of a standard bridge rectifier with center-tapped transformer winding and capacitive filter. No regulation is required. The +24 VDC and -24 VDC are both fused at 15 A. In addition, a -24 VDC UNFUSED output is provided to drive the emergency head retract circuit.

- 2) +15 VDC/-15 VDC

These two voltages are derived from the +24 VDC and -24 VDC by an integrated voltage regulator, H24. The regulator senses the voltage across the sensing resistors, H32 and H33, and controls the series pass transistors, H10 and E10 accordingly.

- 3) +5 VDC

The +5 VDC supply includes a standard bridge rectifier circuit with capacitive filtering at its output.

Overvoltage Protection - Overvoltage protection is provided by a silicon controlled rectifier (SCR) at E63. When overvoltage occurs, the SCR fires, shorting the rectifier output and causing the 7 A fuse, A42, to open.

The overvoltage protection circuit consists of the SCR, capacitors E37 and E40, resistor E39, diode E41 and 5-volt zener diode E42. The resistor, diode and zener form a voltage divider network, with the positive end of the resistor connected to the SCR gate. As long as the rectifier output voltage remains below approximately 6.5 volts, the voltage across the resistor will be less than 0.8 volt, since the voltage drop across the zener and diode E41 is constant at approximately 5.7 volts. Any increase in the rectifier output appears across the 100 Ohm resistor and is applied to the SCR gate. If the gate voltage reaches about 1.25 volts, the SCR fires, drawing heavy current and opening the 7 A fuse.

Capacitors E37 and E40 prevent firing of the SCR by transients reflected by the load.

Voltage Regulation - Regulation of the +5 VDC is accomplished by an integrated regulator (D30) which varies the voltage dropped across a series pass transistor (B62) to compensate for changes in the output voltage.

The integrated regulator is connected as a positive voltage regulator with foldback current limiting. The regulator compares the +5 VDC output voltage, applied to pins 3 and 4, with an internal reference voltage. If the +5 VDC drops, the regulator increases the drive to the base of transistor H60, which in turn increases drive to transistor B62. This reduces the voltage dropped across transistor B62, to compensate for the drop in the +5 VDC output voltage.

The amplitude of the +5 VDC output is adjustable by means of the 500 Ohm potentiometer at D31. This pot varies the internal reference voltage of the integrated regulator.

Current Limiting - The foldback current limiting circuit consists of a 0.01 Ohm current sensing resistor at D48, operational amplifier E30, the integrated regulator at D30, the series pass transistor B62, and associated circuitry.

The voltage across the current sensing resistor is applied to pins 2 and 3 of the operational amplifier, which has an amplification factor of about 10. The output at pin 1 is applied to a voltage divider consisting of resistors E24 and E25. The top of resistor E24 connects to the current limit input at pin 2 of the regulator. When the voltage between pins 2 and 3 of the regulator exceeds 0.65 volts, the regulator turns off the Darlington amplifier. This causes the series pass transistor to become a high impedance, reducing the current to approximately 2.5 A. This action occurs when the +5 VDC load current reaches about 7A.

The four diodes at pin 4 of the operational amplifier set the negative Vc at -2.8 volts.

4) AC OK

The central element of the AC OK circuit is a type 555V timer connected as a retriggerable one-shot. The values of resistor E16 (39K Ohms) and capacitor D24 (1 mfd.) are selected to produce a one-shot time interval equivalent to slightly more than one AC cycle.

During each negative half cycle of AC at transformer terminal 9, a negative pulse is coupled through capacitor D15 and resistor D21. Each of these negative pulses retriggers the one-shot at input D20-2 to renew the time interval, and also turns on transistor E13 to discharge capacitor D24. As a result, the +AC OK output of the one-shot at D20-3 remains HI.

Upon loss of AC power, the negative pulses no longer occur. As a result, capacitor D24 continues to charge. After a period of time equal to slightly more than one AC cycle, the potential at the positive end of capacitor D24 will have reached the time-out threshold of the one-shot. At that point, the output of the one-shot (+AC OK) will drop.

Diode E18 limits the negative excursion of the retrigger pulses to 0.7 volt.

5) Brush Motor

The 24 volt brush motor is switched on and off by triac B15. When +BRUSH ENABLE is HI, transistor B24 turns on. This raises the gate potential of the triac and turns it on. With the triac turned on, the brush motor is effectively connected across terminals 6 and 7 of the transformer.

6) Fan Motor

The 24 volt fan motor connects directly across terminals 6 and 7 of the transformer.

7.2 INTEGRATED CIRCUIT REFERENCE

(AVAILABLE AT A LATER DATE)

7.3 CIRCUIT DIAGRAMS

The list below indexes the circuit diagrams which follow. The Assembly No. corresponds to the assembly number silk-screened onto each PCB assembly. The Artwork No. corresponds to the part number of the bare PCB. This part number is etched directly on the PCB.

A revision history appears on the back of each diagram.

<u>Figure No.</u>	<u>Title</u>	<u>Assembly No.</u>	<u>Artwork No.</u>
7-1	Interconnection Diagram	19030	
7-2	Input/Output PCB Schematic	12025	
7-3	Sheet 1 - Address Logic PCB Schematic	12064	12063
7-4	Sheet 2 -		
7-3A	Sheet 1 - Address Logic PCB Schematic	12101	12063/12100
7-4A	Sheet 2 -		
7-3B	Sheet 1 - Address Logic PCB Schematic	12101-XX	12100-01
7-4B	Sheet 2 -		
7-5	Sheet 1 - Logic PCB Schematic	12066	12065
7-6	Sheet 2 -		
7-5A	Sheet 1 - Logic PCB Schematic	12066	12065-01
7-6A	Sheet 2 -		
7-5B	Sheet 1 - Logic PCB Schematic	12066-XX	12065-01/12065-02
7-6B	Sheet 2 -		
7-7	Sheet 1 - Data Transfer PCB Schematic	12046	
7-8	Sheet 2 -		
7-9	Sheet 3 -		
7-10	Sheet 4 -		
7-11	Sheet 1 - Servo PCB Schematic	12068	
7-12	Sheet 2 -		
7-13	Sheet 1 - Power Driver PCB Schematic	12062	
7-14	Sheet 2 -		
7-13A	Sheet 1 - Power Driver PCB Schematic	12062-01	
7-14A	Sheet 2 -		
7-15	Power Supply Schematic	19033	
7-16	Sheet 1 - VFO Data Transfer Schematic	12076-(200ns)/ 12110-(100ns)	
7-17	Sheet 2 -		
7-18	Sheet 3 -		
7-19	Sheet 4 -	12110-(100ns)	
7-20	Sheet 4 -	12076-(200ns)	

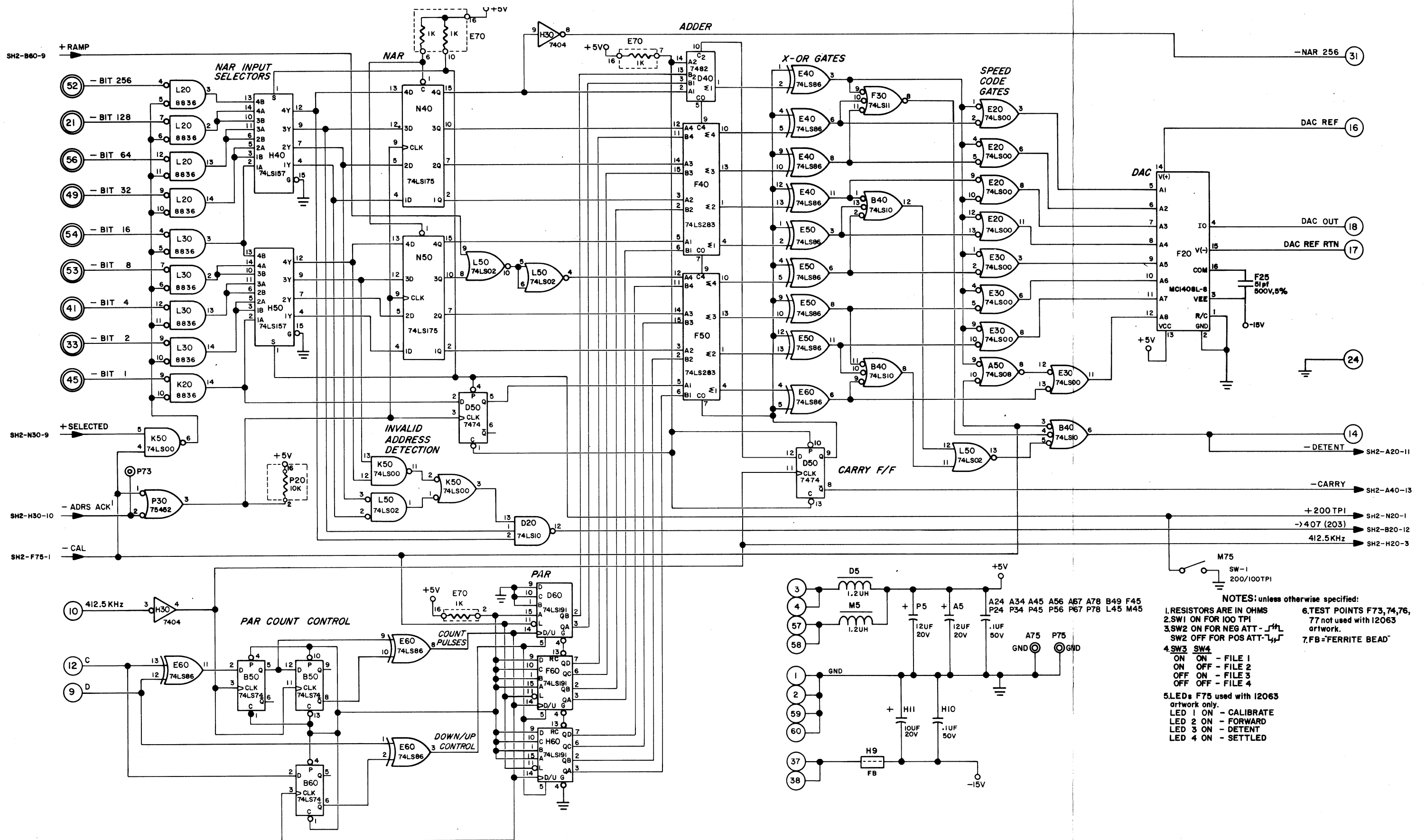


FIGURE 7-3A. ADDRESS LOGIC PCB SCHEMATIC - SHEET 1 #12101 (Artwork 12100 or Modified 12063)

REVISION HISTORY - ADDRESS LOGIC PCB No. 12101
(PCB Artwork No. 12100, or 12063 modified for 12101 PCB
Assembly)

<u>Rev.</u>	<u>XECO</u>	<u>Artwork 12063 (modified)</u>
XD-B	099	Speed code bit 1 goes to DAC F20 instead of becoming DIF 1.
		<u>Artwork 12100</u>
XD-A	082	Releases schematic and assembly for new artwork.
XD-C	107	Document change.
XD-D	126	Bill-of-material change.

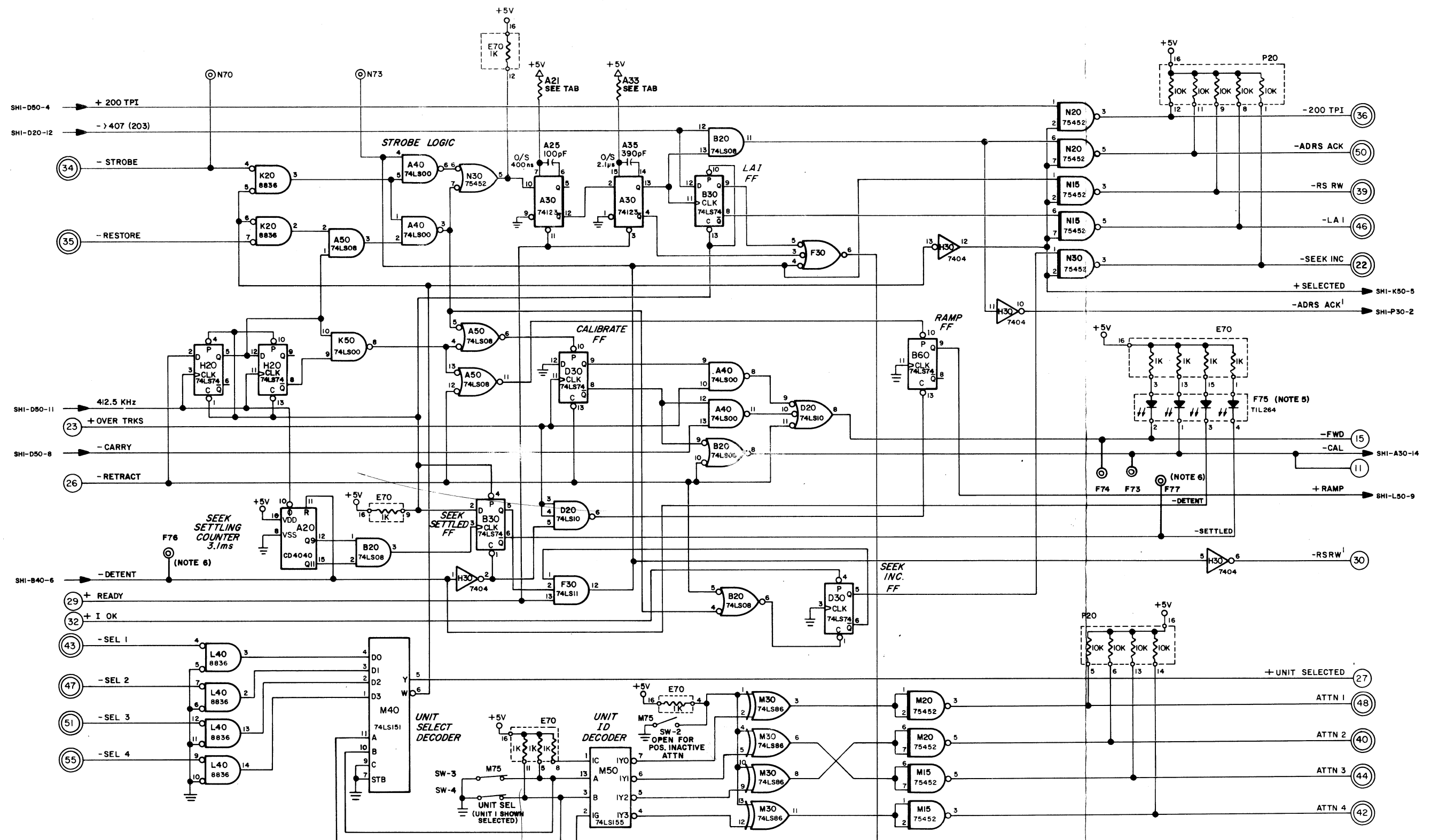


FIGURE 7-4A. ADDRESS LOGIC
PCB SCHEMATIC - SHEET 2
#12101
(Artwork 12100 or Modified 12063)

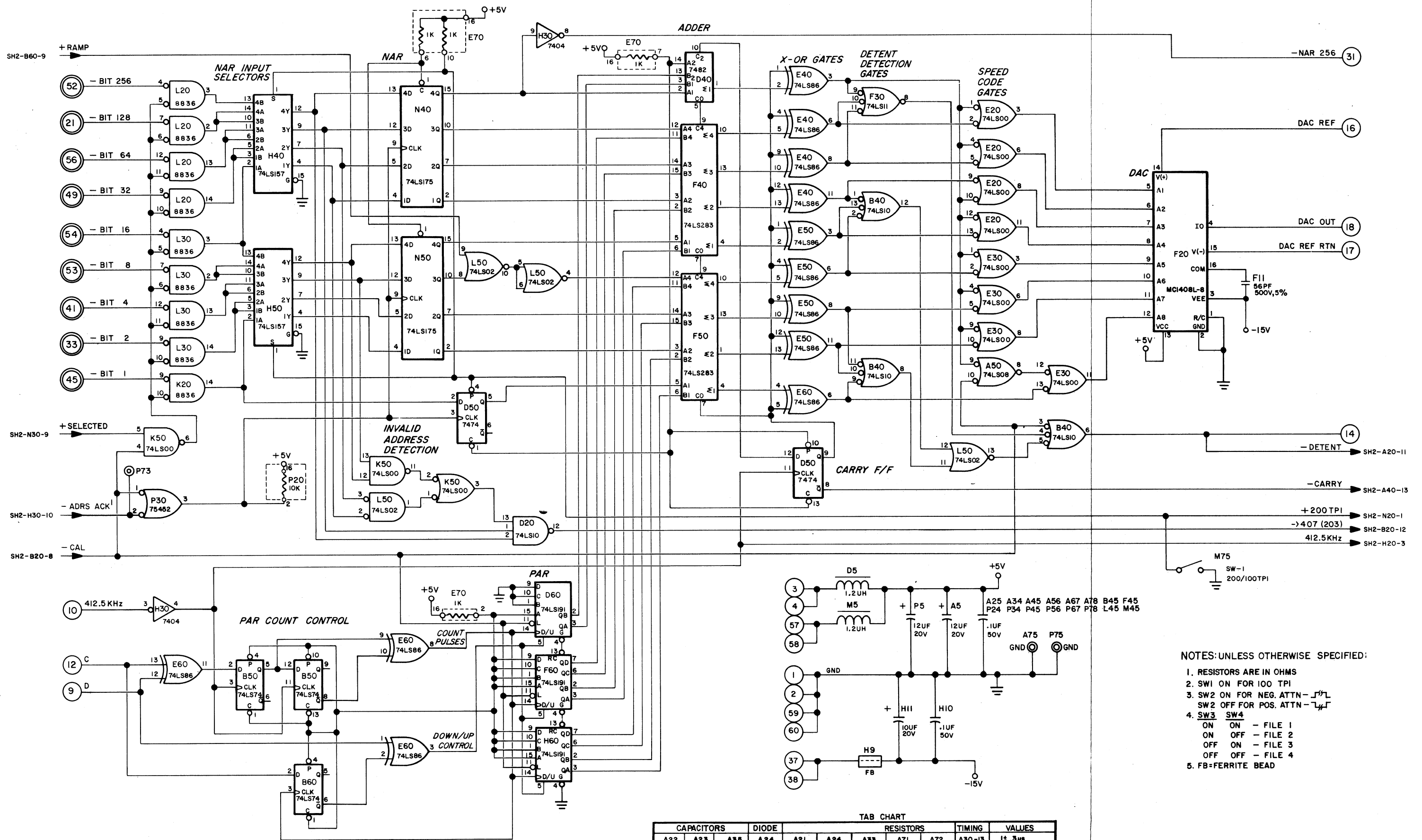


FIGURE 7-3B. ADDRESS LOGIC PCB SCHEMATIC - SHEET 1 #12101-XX (Artwork 12100-01)

REVISION HISTORY - ADDRESS LOGIC PCB No. 12101-XX
(PCB Artwork No. 12100-01)

Rev. XECO

XD-E 100 1) Releases schematic and assembly for artwork
 12100-01 covering PCB assemblies 12101-01, -02.
 2) Gate B70-11 added in -RETRACT line.

XD-F 141 A22 listing in Tab Chart corrected.

Rev. ECO

A 2097 ECO release of schematic and assembly for 12101-01,
 -02, -03.

B 2219 Inputs to Attention gate F30-6 altered for interface
 compatability with Model 44A. Gate K20-13 and inverter
 H30-6 added.

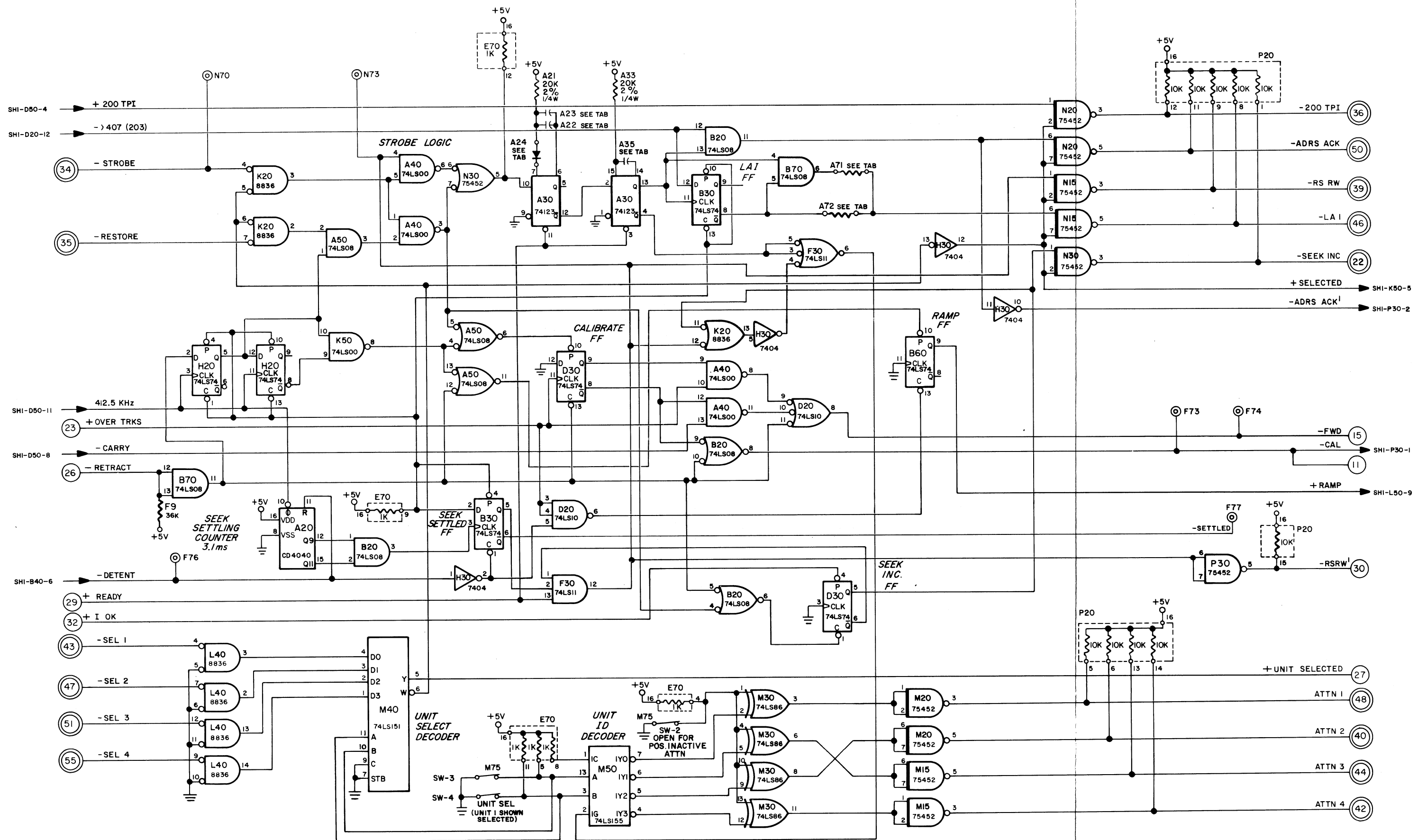


FIGURE 7-4B. ADDRESS LOGIC
PCB SCHEMATIC - SHEET 2
#12101-XX
(Artwork 12100-01)

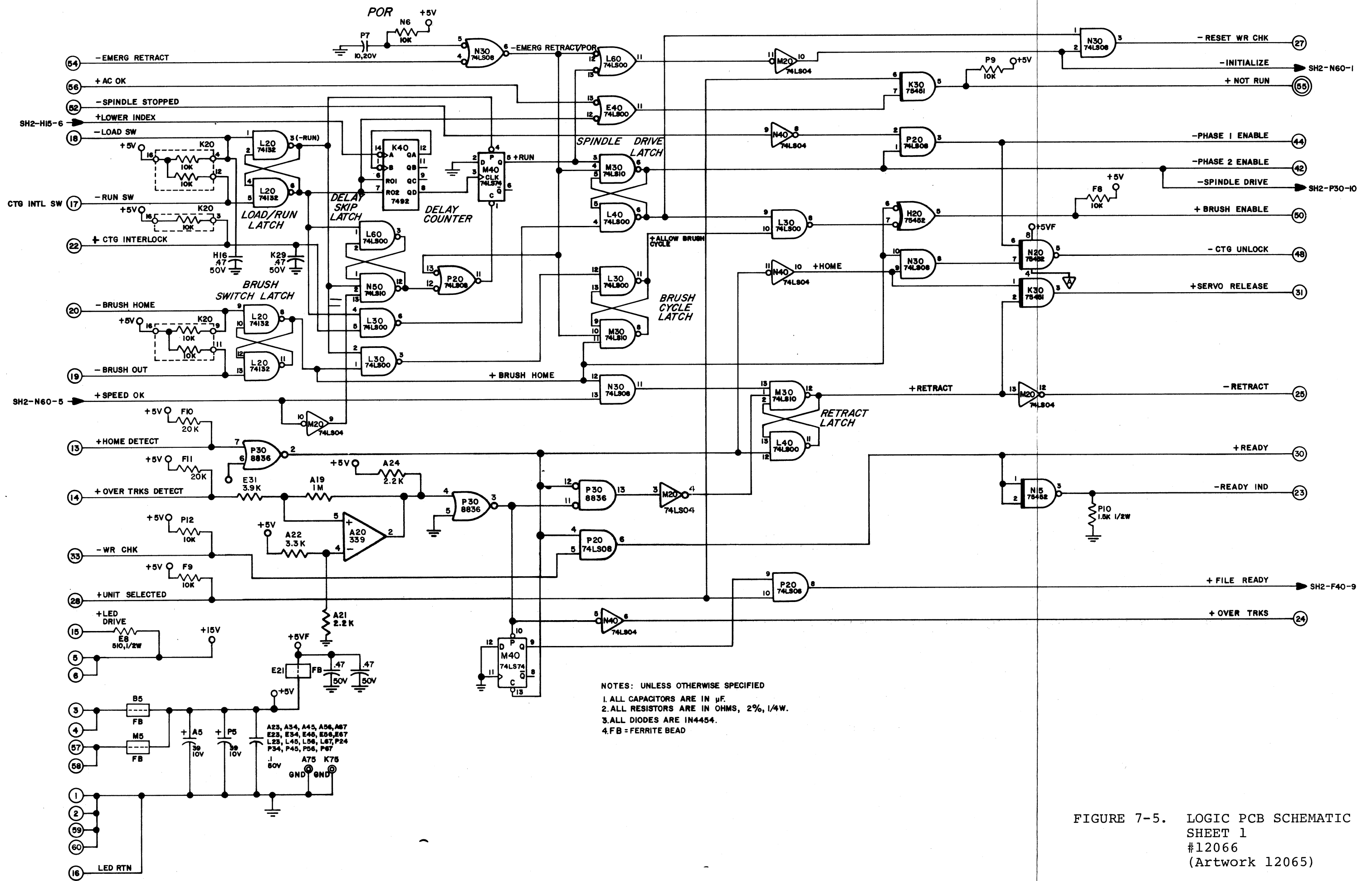


FIGURE 7-5. LOGIC PCB SCHEMATIC SHEET 1
 #12066
 (Artwork 12065)

REVISION HISTORY - LOGIC PCB No. 12066
(PCB Artwork No. 12065)

<u>Rev.</u>	<u>XECO</u>	
XD-E	073	Schematic and assembly of earliest version shipped.
XD-F	083	Gate N50-6 and inverter N40-8 added to Speed OK F/F clear input to prevent heads loading at low RPM after emergency retract.
XD-H	103	Add jumper to replace missing trace. No functional effect.
XD-L	113	1) Comparator A20-2 added to OVER TRKS DETECT circuit. 2) Delay Counter K40 clock changed from SELECTED INDEX to LOWER INDEX.
XD-M	124	Schematic correction to OVER TRKS comparator A20-2 circuit.
XD-R	149	1) Updates index transducer amps to match Rev. level A of 12066-XX using 12065-02 artwork. 2) Diode replaced by resistor at position B59 in D60 O/S circuit.
XD-W	197	FF M40-9/8 added to prevent false File Ready for turn-key applications.

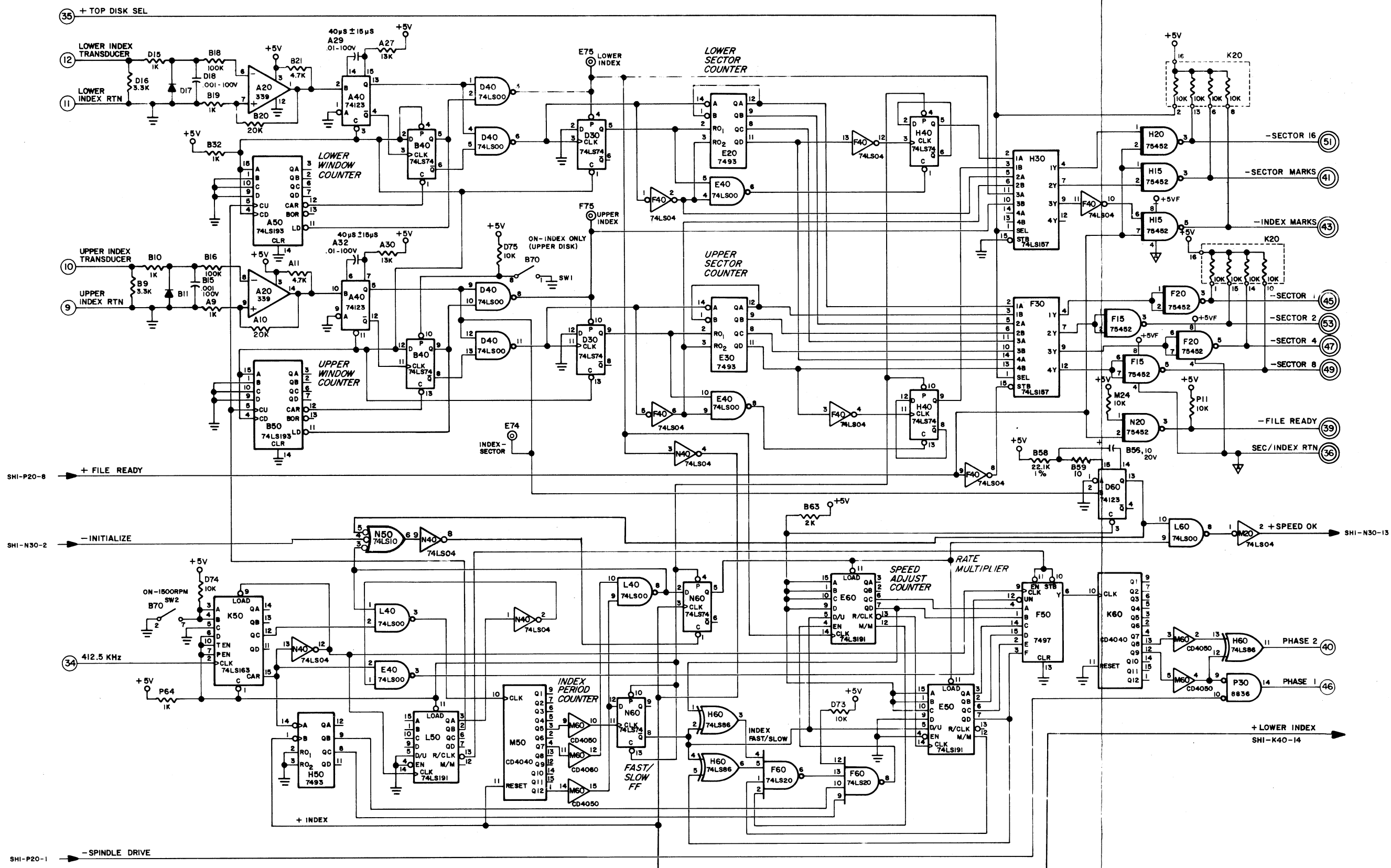
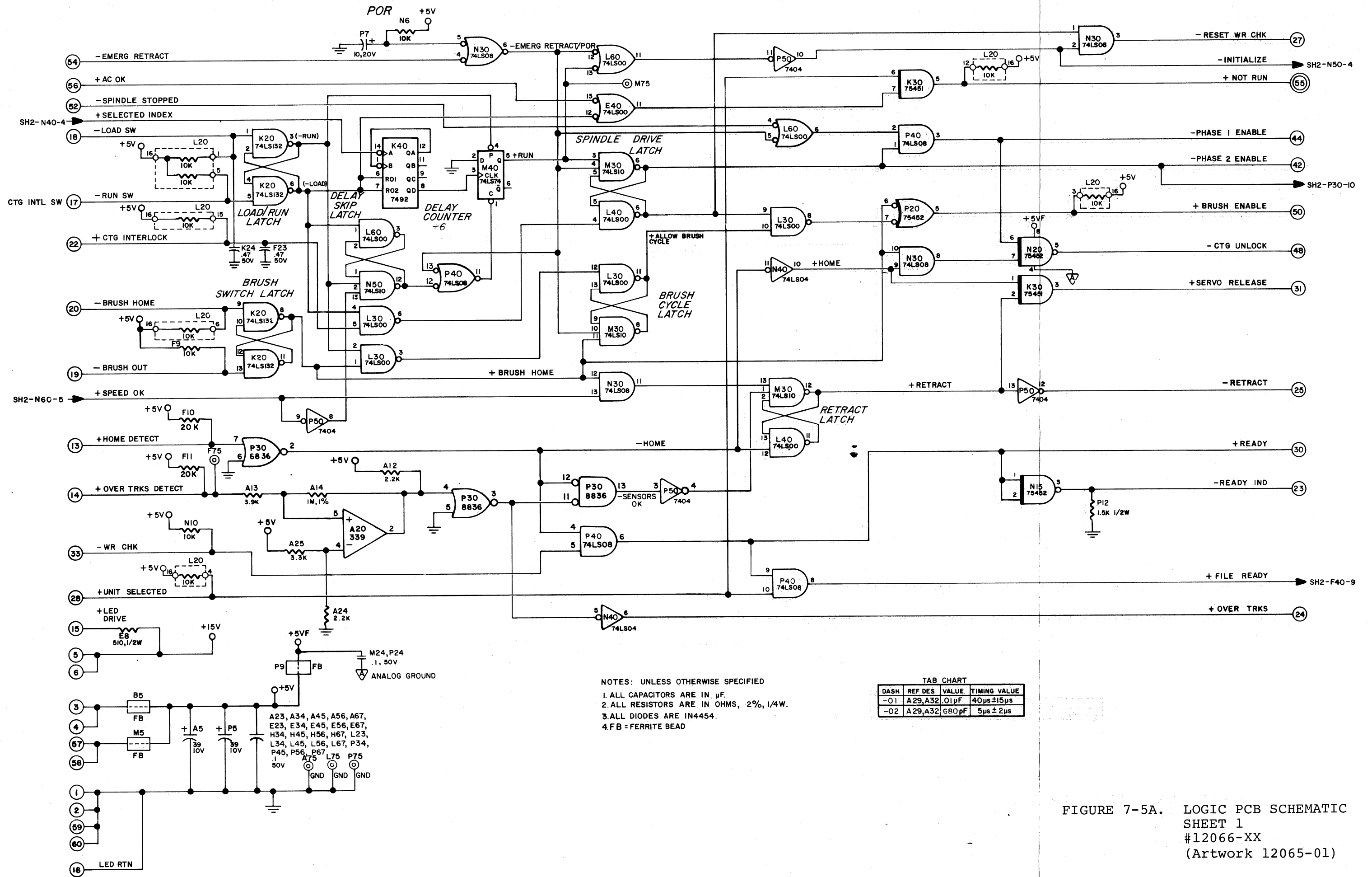


FIGURE 7-6. LOGIC PCB SCHEMATIC SHEET 2 #12066 (Artwork 12065)



NOTES: UNLESS OTHERWISE SPECIFIED
 1. ALL CAPACITORS ARE IN µF.
 2. ALL RESISTORS ARE IN OHMS, 2%, 1/4W.
 3. ALL DIODES ARE IN4454.
 4. FB = FERRITE BEAD

TAB CHART

DASH	REF DES	VALUE	TIMING VALUE
-01	A29,A32	0.1µF	40µs±15µs
-02	A29,A32	680pF	5µs±2µs

FIGURE 7-5A. LOGIC PCB SCHEMATIC SHEET 1 #12066-XX (Artwork 12065-01)

REVISION HISTORY - LOGIC PCB No. 12066
(PCB Artwork No. 12065-01)

For later revision levels using #12065-01 artwork, see Figures 7-5B
and 7-6B.

<u>Rev.</u>	<u>XECO</u>	
XD-G	086	Release of schematic and assembly for artwork 12065-01.
XD-J	104	1) Delay Counter K40 clock changed from SELECTED INDEX to LOWER INDEX. 2) TP F75 changed from HOME DETECT to OVER TRKS DETECT.
XD-K	108	Comparator A20-2 added to OVER TRKS DETECT circuit.
XD-N	125	Schematic correction to OVER TRKS Comparator A20-2 circuit.
XD-S	150	1) Resistors A10/B20 in index transducer amps changed from 47K to 20K. 2) In D60-13 O/S circuit, diode B59 replaced by resistor.

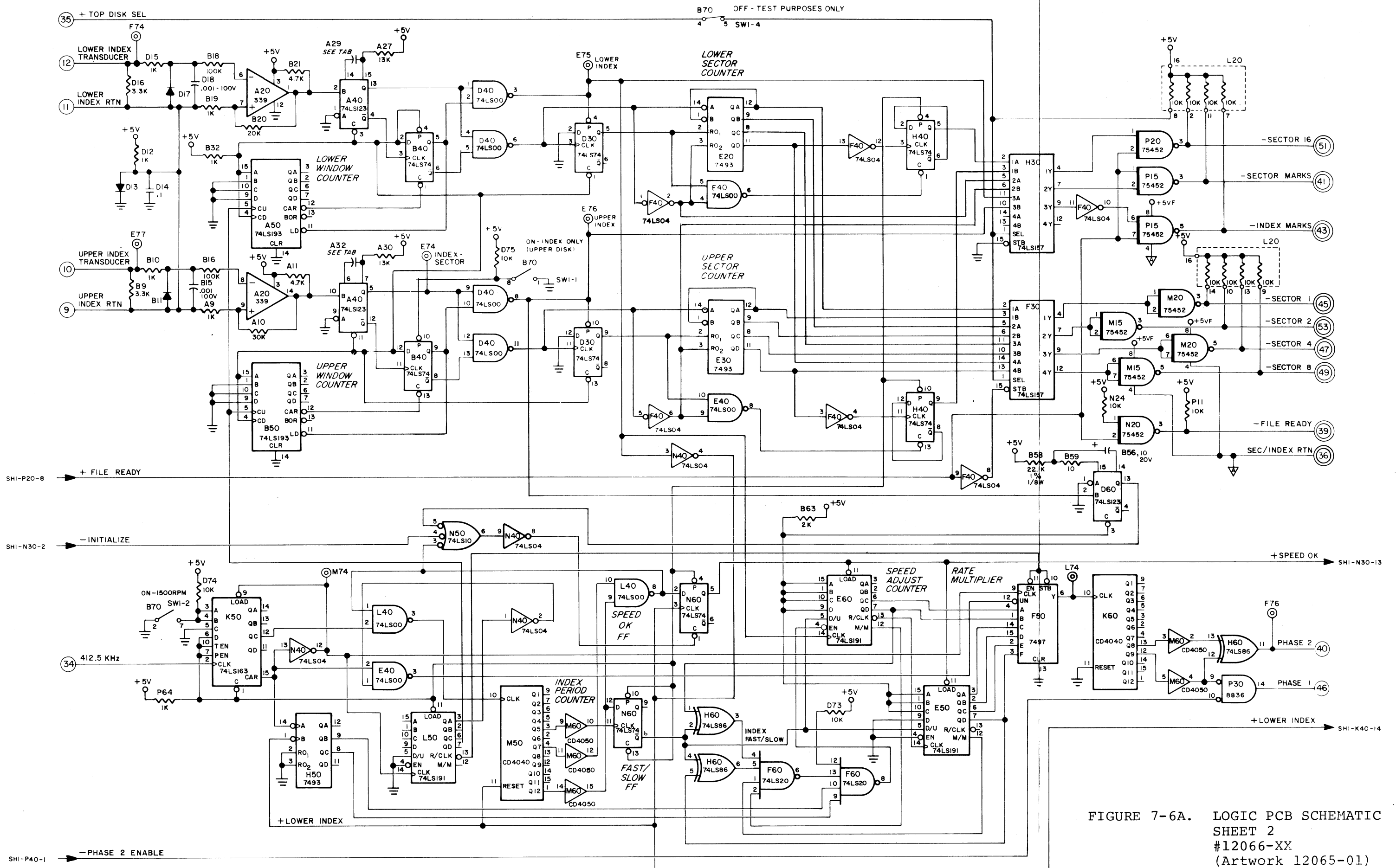


FIGURE 7-6A. LOGIC PCB SCHEMATIC SHEET 2 #12066-XY (Artwork 12065-01)

SHI-P40-1 - PHASE 2 ENABLE

SHI-P20-8 + FILE READY

SHI-N30-2 - INITIALIZE

SHI-N30-13 + SPEED OK

SHI-K40-14 + LOWER INDEX

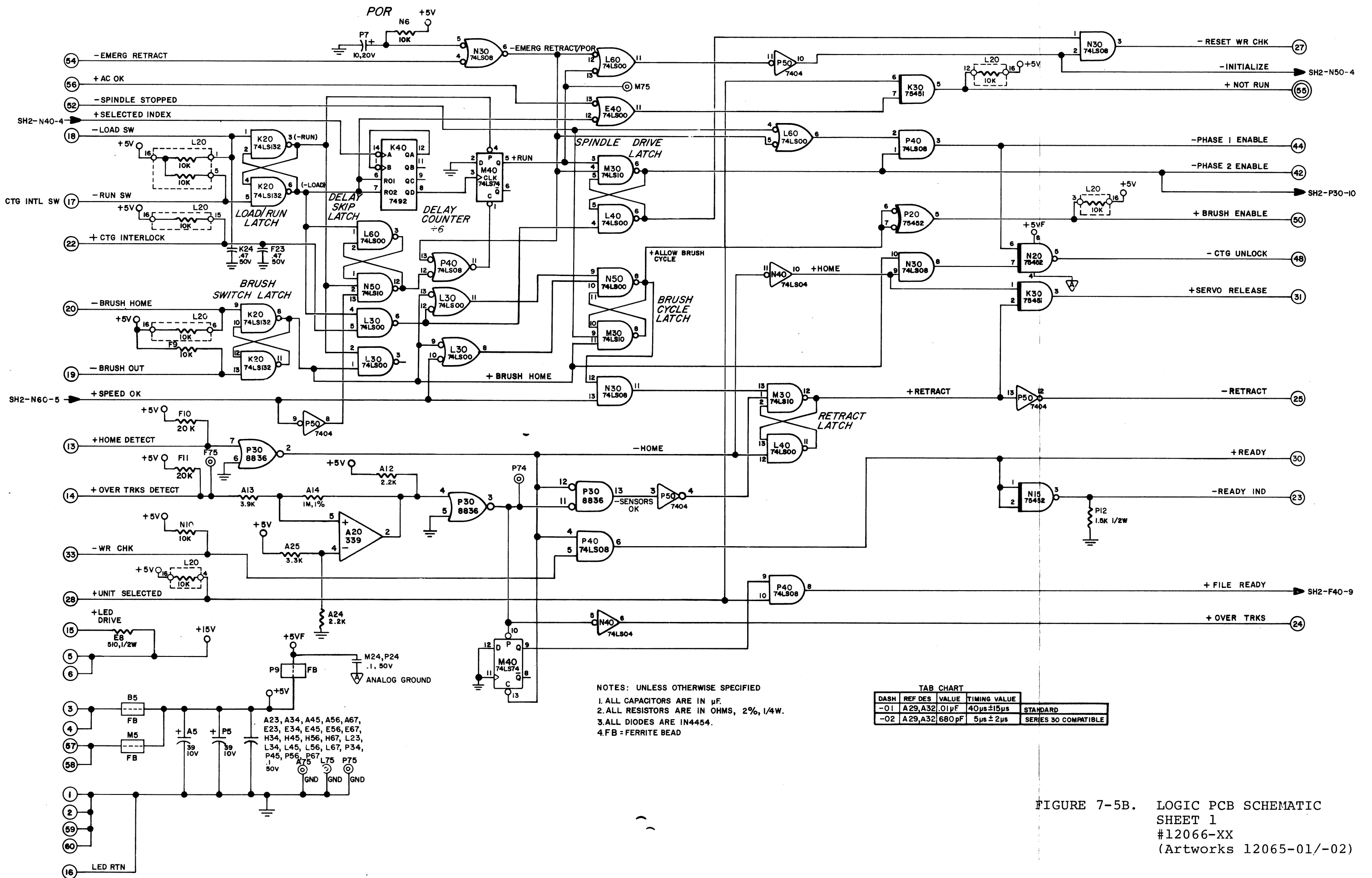


FIGURE 7-5B. LOGIC PCB SCHEMATIC SHEET 1 #12066-XX (Artworks 12065-01/-02)

REVISION HISTORY - LOGIC PCB No. 12066-XX

For earlier Rev. levels using 12065-01 artwork, see Figures 7-5A and 7-6A.

<u>Rev.</u>	<u>XECO</u>	<u>Artwork 12065-01</u>
XD-V	176	1) Resistor A10 in Upper Index Transducer amp changed from 20K to 30K. 2) Brush Enable circuit changed.
XD-X	198	FF M40-9/8 added to prevent false File Ready for turn-key applications.

<u>Rev.</u>	<u>ECO</u>	<u>Artwork 12065-02</u>
C	2220	Earliest version shipped
D	2283	FF M40-9/8 added to prevent false File Ready for turn-key applications.

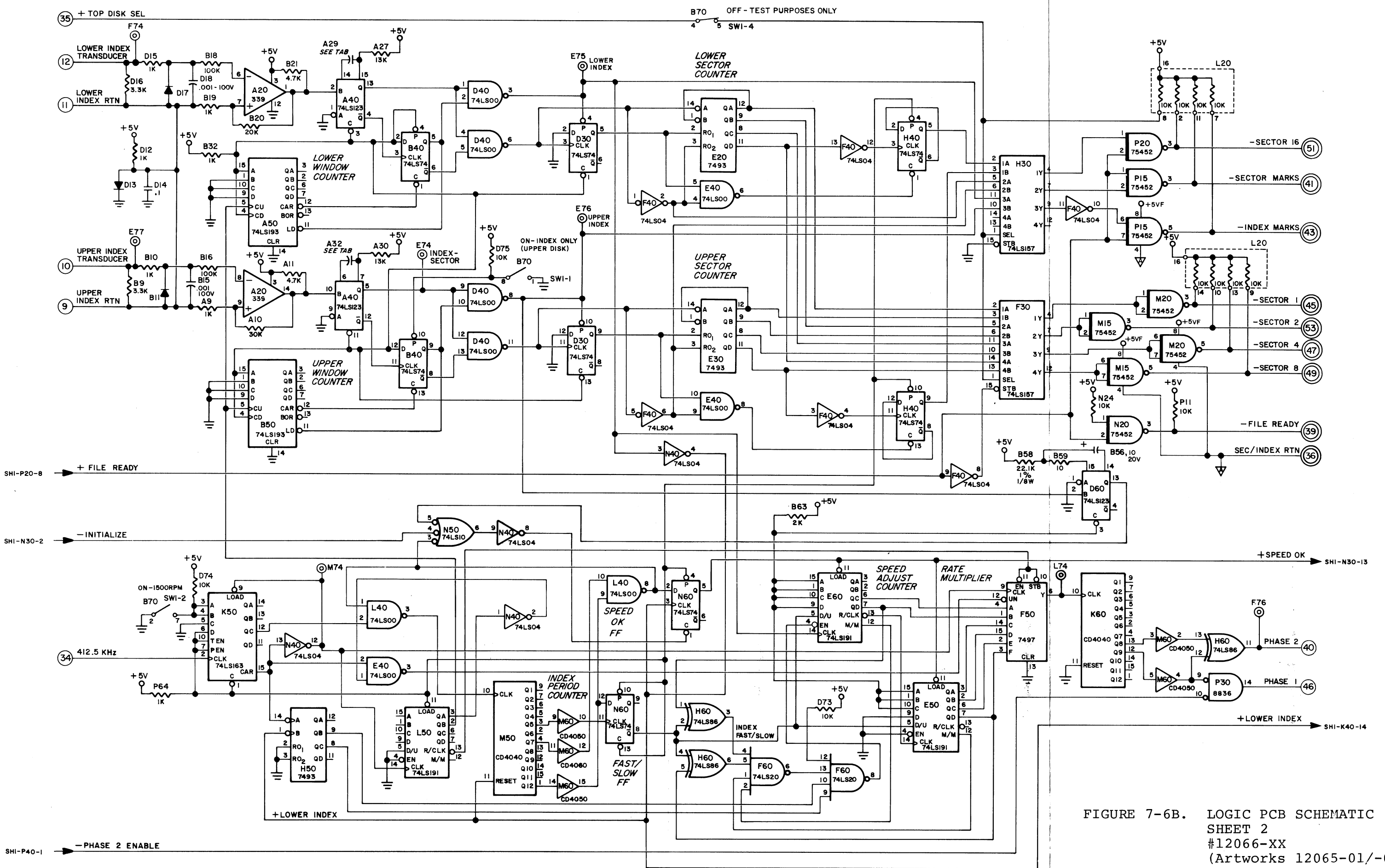
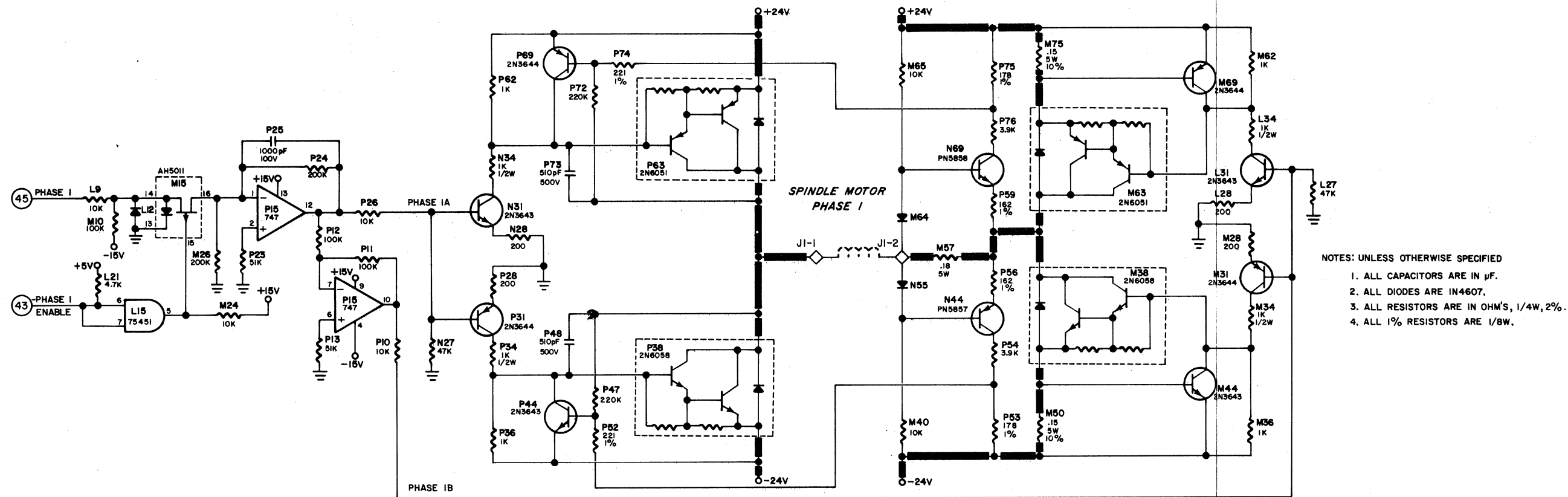


FIGURE 7-6B. LOGIC PCB SCHEMATIC SHEET 2 #12066-XX (Artworks 12065-01/-02)



- NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITORS ARE IN μF .
 2. ALL DIODES ARE IN4607.
 3. ALL RESISTORS ARE IN OHM'S, 1/4W, 2%.
 4. ALL 1% RESISTORS ARE 1/8W.

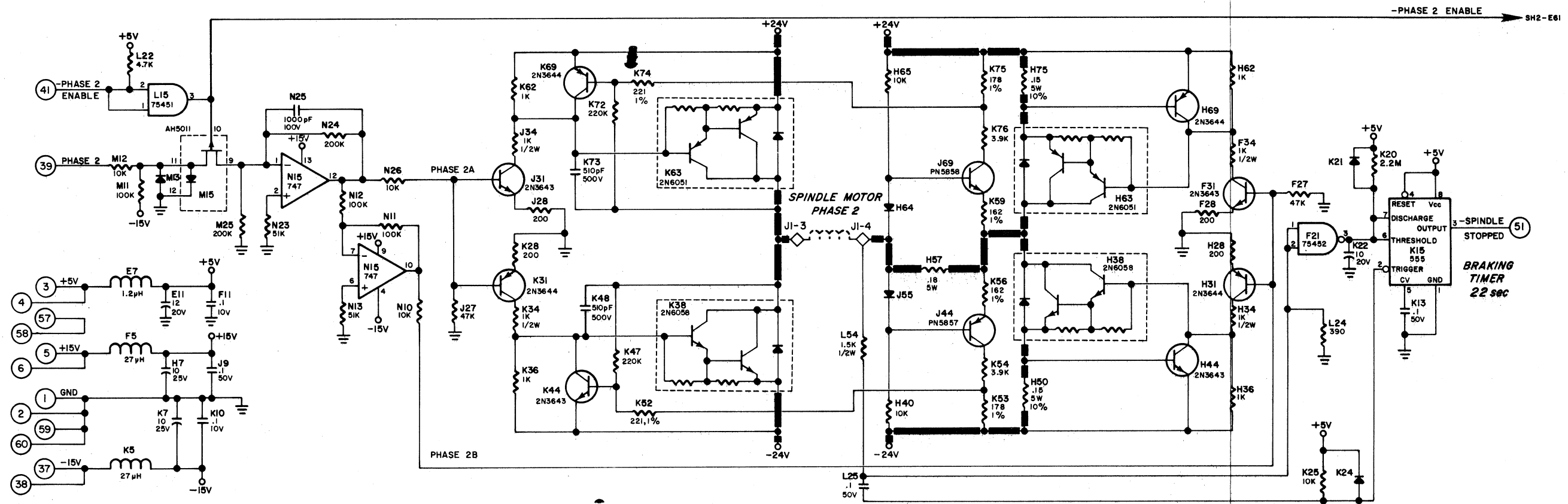


FIGURE 7-13. POWER DRIVER PCB SCHEMATIC - SHEET 1 #12062

REVISION HISTORY - POWER DRIVER PCB No. 12062-00

<u>Rev.</u>	<u>XECO</u>	
XD-D	055	Earliest version shipped.
XD-E	060	For spindle circuit noise reduction, diodes changed to resistors at locations N28, P28, L28, M28, J28, K28, F28, H28.
XD-F	074	Resistors D10/D20 in I OK amp change from 2.7M to 2M.
XD-G	123	Bill-of-Material change.
XD-H	185	Resistor K20 changed from 1.5M to 2.2M for longer braking period.

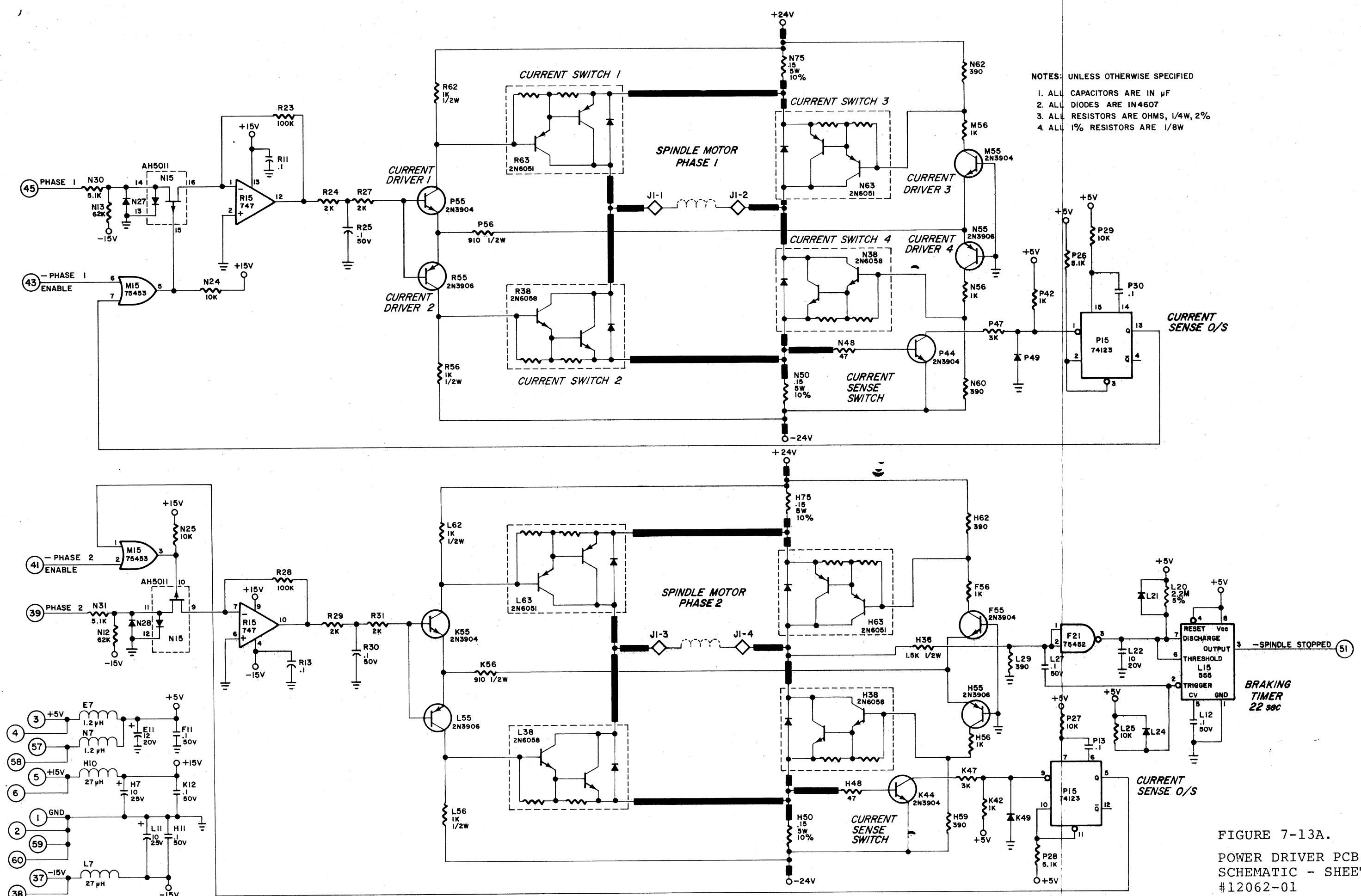
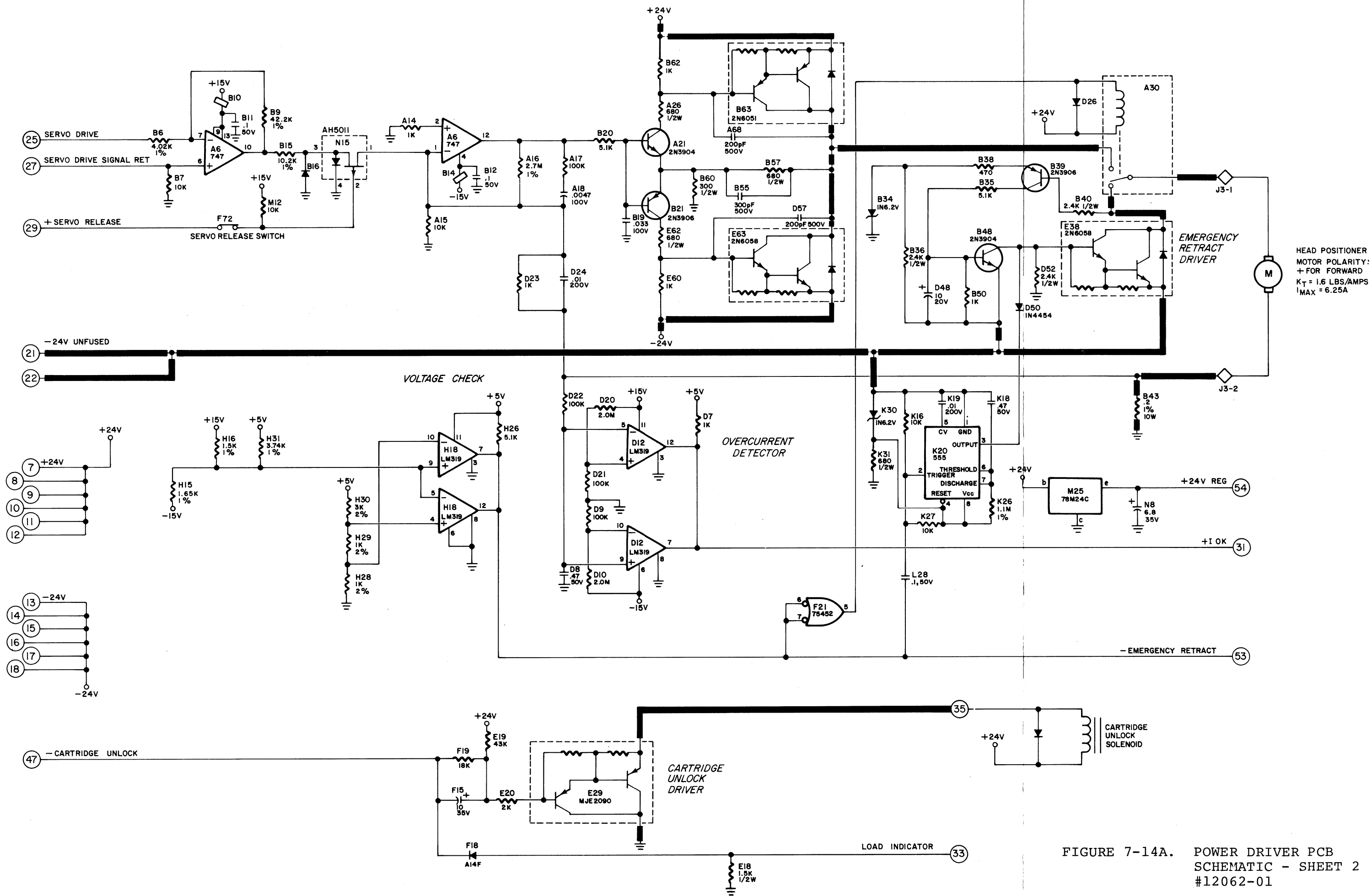


FIGURE 7-13A.
 POWER DRIVER PCB
 SCHEMATIC - SHEET 1
 #12062-01

REVISION HISTORY - POWER DRIVER PCB No. 12062-01

<u>Rev.</u>	<u>XECO</u>	
XD-A	084	XECO release of schematic and assembly.
XD-B	136	Document correction.
XD-C	186	1) Resistors P47 and K47 changed from 4.7K to 3K at inputs to Current Sense One-Shots. 2) Resistor L20 changed from 1.5M to 2.2M for longer braking period.

<u>Rev.</u>	<u>ECO</u>	
A	2096	ECO release of schematic and assembly.
B	2177	PCB artwork correction.
C	2223	Resistor L20 changed from 1.5M to 2.2M for longer braking period.



HEAD POSITIONER
MOTOR POLARITY:
+ FOR FORWARD
K_T = 1.6 LBS/AMPS
I_{MAX} = 6.25A

FIGURE 7-14A. POWER DRIVER PCB SCHEMATIC - SHEET 2 #12062-01

Diablo Systems Incorporated

24500 Industrial Boulevard
Hayward, California 94545
415 786-5000

Field Service Aid

No. 34

Xerox Company

August 11, 1978

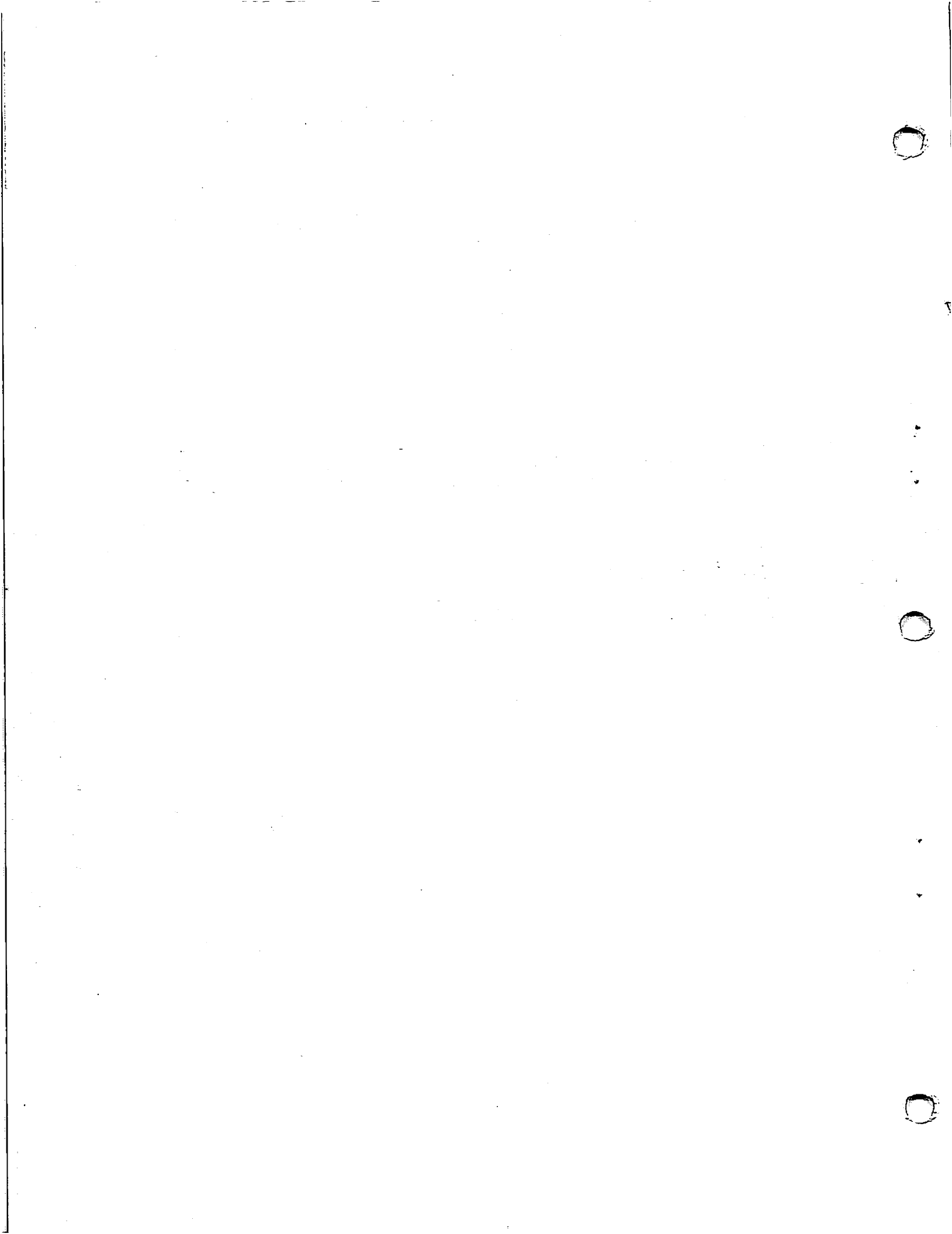
TO: Model 44B Disk Drive Customers
FROM: Diablo Customer Service
SUBJECT: Revision 'C' to the Maintenance Manual #81903-01

Attached is Revision 'C' to the Model 44B Disk Drive Maintenance Manual, Publication No. 81903-01. This revision will be included with units shipped during August, 1978.



Paul Miller, Manager
Customer Service Publications

kc



Diablo Systems Incorporated

24500 Industrial Boulevard
 Hayward, California 94545
 415 786-5000

A Xerox Company

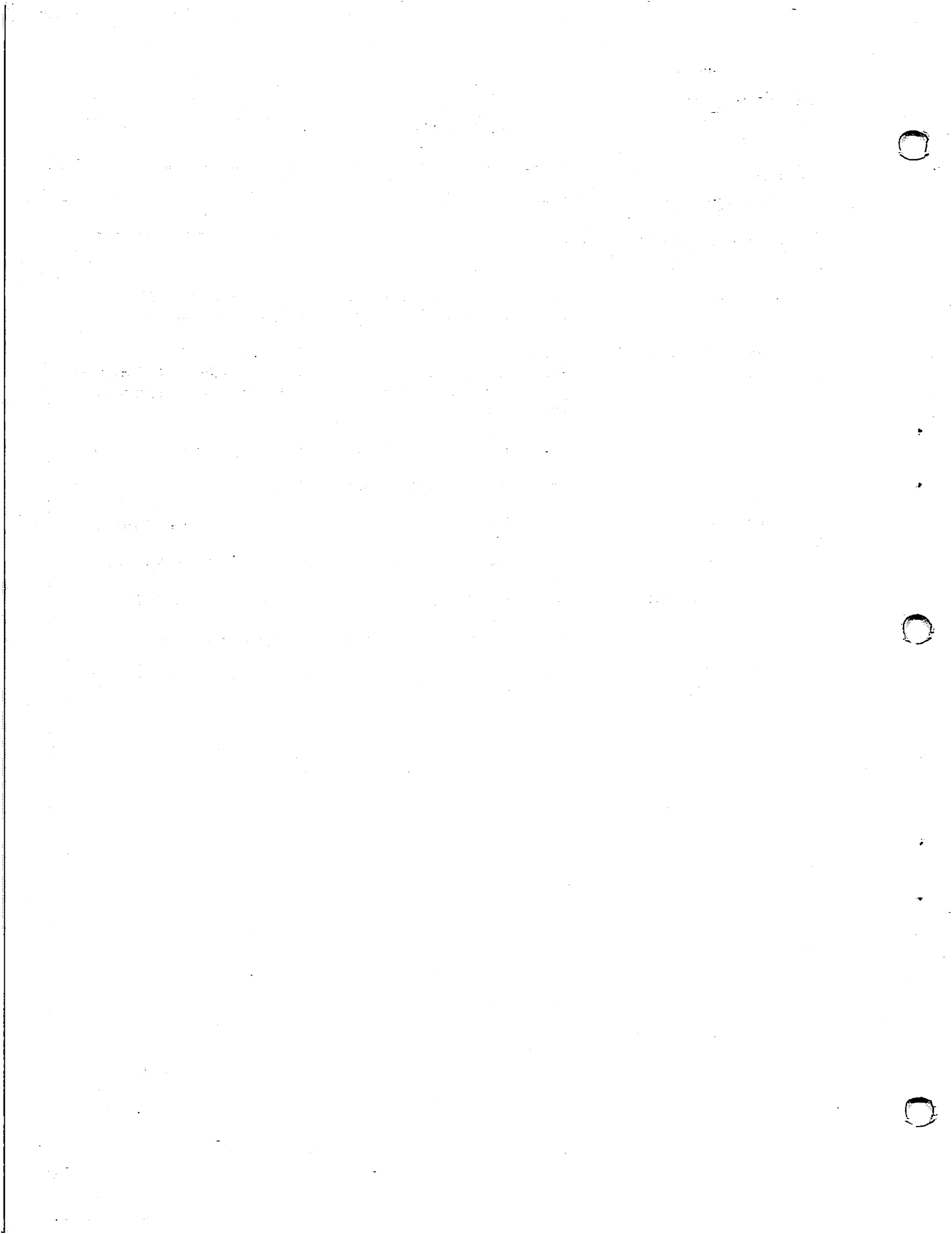
Addenda

Date	Page
July, 1978	1 of 1

Publication Being Revised
 Model 44B Disk Drive Maintenance Manual
 Publication No. 81903-01 Rev. C

Please enter the following revisions and/or corrections in your copy of this manual:

- Page 4-20 Discard old page 4-20 and insert new page 4-20.
 This corrects Flowchart No. 1 - Load to Run.
- Pages 4-25 thru 4-28 Discard old pages 4-25,-26,-27,-28.
 Insert new pages 4-25,-26,-26a,-26b,-26c,-27,-28.
 This adds text describing new Power Supply Assembly 19240-XX.
- Page 6-1 Discard old page 6-1, and insert new pages 6-1 thru 6-6.
 This updates Section 6.1 - Options.
- Figures 7-4C/7-5C Discard old Figure 7-4C/7-5C, and insert new Figures 7-4C/7-5C.
 This updates A/L PCB schematic 12152-XX to Rev. E.
- Figures 7-4E/7-5E Discard old Figures 7-4E/7-5E, and insert new Figures 7-4E/7-5E.
 This updates A/L PCB schematic 12129-XX to Rev. D.
- Figures 7-8A
 7-8B
 7-8D Input line in upper left corner should be +LOWER INDEX instead of +SELECTED INDEX.
- Figure 7-8C Upper half of Brush Cycle Latch (N50-8):
 Change input numbers as follows:
- | | |
|-------------------|----|
| Top input was: | 10 |
| Should be: | 11 |
| Middle input was: | 9 |
| Should be: | 10 |
| Bottom input was: | 11 |
| Should be: | 9 |
- Figure 7-8D IC N50-8 in Brush Cycle Latch should be 74LS10 instead of 74LS00.
- Figures 7-8E/7-9E Discard old Figures 7-8E/7-9E, and insert new Figures 7-8E/7-9E.
 This updates Logic PCB schematic 12141-XX to Rev. F'.
- Figures 7-12B
 7-13B
 7-14B
 7-15B Discard old Figures 7-12B thru 7-15B, and insert new Figures 7-12B thru 7-15B.
 This updates D/T PCB schematic 12121-XX to Rev. G.



will be passed out to the +READ DATA line. The data window then terminates prior to receipt of the next clock pulse.

4.2.7.7.2 VFO Data Separator Option

The optional VFO data separator can be used with either sector mark format or address mark format. The VFO separator provides the following features:

- ◆ Generates a clock signal that is synchronized with the read data.
- ◆ Removes most of the jitter caused by pulse crowding.
- ◆ Provides closer timing tolerances than the standard single-shot separator.

The VFO separator consists of a phase-locked loop and a data separator. The phase-locked loop provides a stable clock signal which is used to relock the data and clock signals from the disk.

When -READ CLOCK goes LO, a 2 μ s general reset pulse initializes the VFO separator. The VFO separator is then activated by the first data or clock pulse received from the disk. With continued receipt of data from the disk, the phase-locked loop will achieve frequency lock within 22 μ s. After frequency lock occurs, two Zeros Detector circuits look for a pattern of eight consecutive zeros passing through the Data Separator. Receipt of these zeros from anyplace in the format allows detection of which Data Separator channel is passing the clock pulses and which is passing the data pulses. The Output Selector is then enabled and conditioned to pass clock pulses to the READ CLOCK output and data pulses to the READ DATA output.

4.2.7.8 Fault Detection

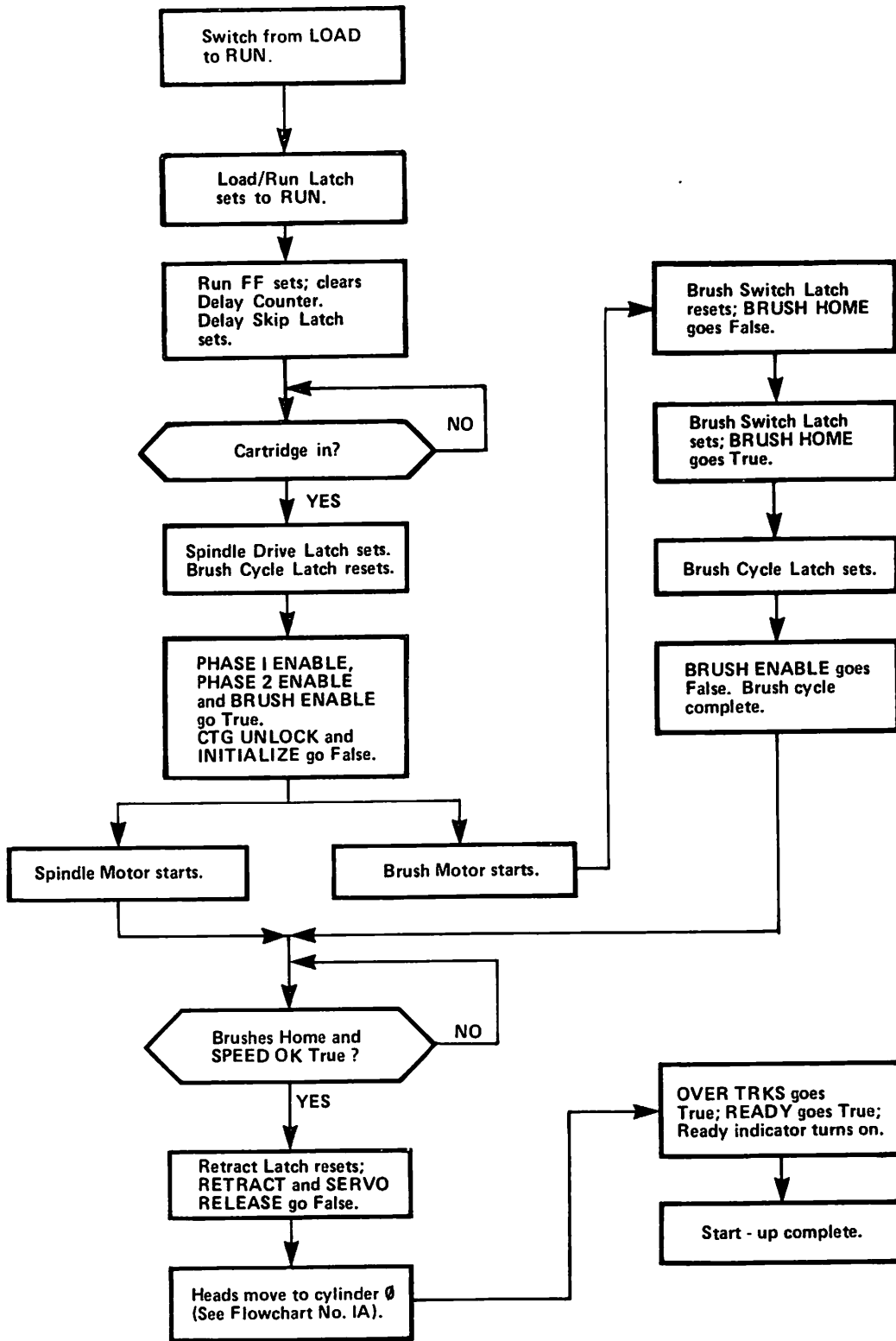
The fault detection circuitry is designed to detect the faults listed below. Having detected a fault, this circuitry puts a LO on the -WRITE CHECK interface line, turns on the WRITE CHECK indicator light, turns out the READY indicator light, and disables the read/write functions on the Data Transfer PCB by generating a Write Protect condition.

Fault Conditions:

- ◆ Write current without -WRITE GATE = LO.
- ◆ No AC write current with -WRITE GATE = LO.
- ◆ No DC write current with -WRITE GATE = LO.
- ◆ Erase current without +ERASE CMD = HI.
- ◆ No erase current with +ERASE CMD = HI.
- ◆ Multiple head selection.
- ◆ Open R/W head coil.

4.2.8 Function Flowcharts

The Flowcharts which follow serve as a general guideline to the major functions of the Model 44B Disk Drive. These Flowcharts also serve as an effective troubleshooting aid when used in conjunction with the circuit schematics contained in Section 7 of this manual.



FLOWCHART No. 1
LOAD TO RUN

4.3 CIRCUIT DESCRIPTIONS

Figure 7-1 shows the interconnection diagram for circuit boards and peripheral components of the Model 44B Disk Drive.

4.3.1 Power Supply Assembly (#19033-XX/#19220-XX)

(Text based on 19033-XX Rev. XD-P/19220-XX Rev. XD-B)

Power Supply Assemblies 19033-XX Rev. XD-P and 19220-XX Rev. XD-B are identical except for the power transformer. For Power Supply 19033-XX the AC input voltage tolerance is $\pm 10\%$, while that of the 19220-XX is $+10\%$, -15% .

4.3.1.1 General Characteristics

The internal power supply assembly of the Model 44B performs the following functions:

1. Produces the DC voltages:
 - +24 VDC/-24 VDC/-24 VDC UNFUSED
 - +15 VDC/-15 VDC
 - +5 VDC
2. Produces an "AC OK" signal to indicate the status of AC input power.
3. Provides on-off control and power for the brush motor.
4. Provides power for the fan motor.

The Model 44B power supply is adaptable to any one of four different AC input voltages: 100, 120, 220 or 240 VAC at 49 to 61 Hz. The disk drive is set for the appropriate input voltage by a small 4-position voltage selector printed circuit card. This card is located in the fuse compartment near the on-off switch at the rear of the machine. To adapt the drive to a different input voltage, the selector card is simply pulled out, turned to the desired position (as indicated on the card), and reinserted. (See subsection 5.7.1.12).

4.3.1.2 Theory of Operation

Refer to Figure 7-2.

1. +24 VDC/-24 VDC/-24 VDC UNFUSED

The circuit to develop these voltages consists of a standard bridge rectifier (BR1) with center-tapped transformer winding and capacitive filter. No regulation is required. The +24 VDC and -24 VDC are both fused at 15 A. In addition, a -24 VDC UNFUSED output is provided to drive the emergency head retract circuit.

2. +15 VDC/-15 VDC

These two voltages are derived from the +24 VDC and -24 VDC by an integrated voltage regulator, H24. The regulator senses the voltage across the sensing resistors, H32 and H33, and controls the series pass transistors, H10 and E10 accordingly.

3. +5 VDC

The +5 VDC supply includes a standard bridge rectifier (BR2) with capacitive filtering at its output.

Overvoltage Protection — Overvoltage protection is provided by a silicon controlled rectifier (SCR) at E63. When overvoltage occurs, the SCR fires, shorting the rectifier output and causing fuse A42 to open.

The overvoltage protection circuit consists of the SCR, capacitors E37 and E40, resistor E39, diode E41 and 5 volt zener diode E42. The resistor, diode and zener form a voltage divider network, with the positive end of the resistor connected to the SCR gate. As long as the "+5 V"

output remains below +6.5 volts, the voltage across the resistor will be less than .8 volt, since diode E41 and the 5 volt zener will absorb about 5.7 volts. Any further increase of the output above +6.5 volts appears across the 100 ohm resistor and is applied to the SCR gate. If the SCR gate voltage rises to +1.25 volts, the SCR fires and opens fuse A42. This occurs when the output has reached about 6.95 volts.

Capacitors E37 and E40 prevent firing of the SCR by transients reflected by the load.

Voltage Regulation — Regulation of the +5 VDC is accomplished by an integrated regulator (D30) which varies the voltage dropped across a series pass transistor (B62) to compensate for changes in the output voltage.

The integrated regulator is connected as a positive voltage regulator with foldback current limiting. The regulator compares the +5 VDC output voltage, applied to pins 3 and 4, with an internal reference voltage. If the +5 VDC drops, the regulator increases the drive to the base of transistor H60, which in turn increases drive to transistor B62. This reduces the voltage dropped across transistor B62, to compensate for the drop in the +5 VDC output voltage.

The amplitude of the +5 VDC output is adjustable by means of the 500 ohm potentiometer at D31. This pot varies the internal reference voltage of the integrated regulator.

Current Limiting — The foldback current limiting circuit consists of a .01 ohm current sensing resistor at D48, operational amplifier E30, the integrated regulator at D30, the series pass transistor B62, and associated circuitry.

The voltage across the current sensing resistor is applied to pins 2 and 3 of the operational amplifier, which has an amplification factor of about 10. The output at pin 1 is applied to a voltage divider consisting of resistors E24 and E25. The top of resistor E24 connects to the current limit input at pin 2 of the regulator. When the voltage between pins 2 and 3 of the regulator exceeds .65 volt, the regulator turns off the Darlington amplifier. This causes the series pass transistor to become a high impedance, reducing the current to approximately 2.5 A. This action occurs when the +5 VDC load current reaches about 7 A.

The four diodes at pin 4 of the operational amplifier set the negative V_c at -2.8 volts.

4. AC OK

The central element of the AC OK circuit is a type 555 V timer (D20) connected as a retriggerable one-shot. The values of resistor E16 (39K ohms) and capacitor D24 (1 mfd) are selected to produce a one-shot time interval equivalent to slightly more than one AC cycle.

During each negative half cycle of AC at transformer terminal 9, a negative pulse is coupled through capacitor D15 and resistor D21. Each of these negative pulses retriggers the one-shot at input D20-2 to renew the time interval, and also turns on transistor E13 to discharge capacitor D24. As a result, the +AC OK output of the one-shot at D20-3 remains HI.

Upon loss of AC power, the negative pulses no longer occur. As a result, capacitor D24 continues to charge. After a period of time equal to slightly more than one AC cycle, the potential at the positive end of capacitor D24 reaches the time-out threshold of the one-shot. At that point, the output of the one-shot (+ AC OK) goes LO.

Diode E18 limits the negative excursion of the retrigger pulses to .7 volt.

5. Brush Motor

The 24 volt brush motor is switched on and off by triac B15. When +BRUSH ENABLE is HI, transistor B24 turns on. This raises the gate potential of the triac and turns it on. With the triac conducting, the brush motor is effectively connected across terminals 6 and 7 of the transformer. (5V COM at the bottom end of the triac connects with 24V RTN on the Motherboard PCB.)

6. Fan Motor

The 24 volt fan motor connects directly across terminals 6 and 7 of the transformer.

4.3.1A Power Supply Assembly 19240-XX

(Text based on 19240-XX Rev B)

This power supply has an input voltage tolerance of +10%/-15%.

4.3.1.1A General Characteristics

As listed below, the 19240-XX internal power supply of the Model 44B performs the same functions as the 19033-XX and 19220-XX power supply assemblies, with one exception; the AC OK function was deemed unnecessary and the AC OK signal line connects directly to +5V.

Functions:

1. Produces the DC voltages:
 - +24VDC/-24VDC/-24VDC UNFUSED
 - +15VDC/-15VDC
 - +5VDC
2. Provides on-off control of 24VAC power to the brush motor.
3. Provides 24VAC power for the fan motor.

The power supply is adaptable to any one of four AC input voltages: 100, 120, 220 and 240 VAC at 49 to 61 Hz. The disk drive is matched to the available input AC voltage by a 4-position voltage selector printed circuit card. This card is located in the fuse compartment at the rear of the machine. To adapt the drive to a different input voltage, the selector card is pulled out, turned to the appropriate position and reinserted. (See subsection 5.7.1.12)

4.3.1.2A Theory of Operation

Refer to Figure 7-2A.

+24VDC/-24VDC/-24VDC UNFUSED

The circuit to develop these voltages consists of a standard bridge rectifier (BR1) with center-tapped transformer winding and capacitive filter. No regulation is required. The +24VDC and -24VDC are both fused at 10 A. In addition, a -24VDC UNFUSED output is provided to drive the emergency head retract circuit. Capacitor C1 across rectifier BR1 blocks any noise generated by the spindle drive circuits from reaching the AC power lines.

+15VDC/-15VDC

These two voltages are derived from +24VDC and -24VDC by two 3-terminal integrated voltage regulators E33 and A33. These regulators feature internal thermal overload protection and short circuit current limiting.

Operational amplifier D26-12 provides for tracking between the +15V and -15V outputs. Amplifier input D26-2 connects to 15V COM, and input D26-1 connects to a balanced voltage divider between +15V and -15V. The tracking amplifier output controls the reference potential on the COM terminal of the +15V regulator. When this terminal is at 0 volts, the regulator output is at 15 volts.

The reference potential for the COM terminal of the -15V regulator is taken from potentiometer E38. The potentiometer provides for initial adjustment of the $\pm 15\text{VDC}$ outputs. As the potentiometer is adjusted, the -15V regulator output potential changes. This change is sensed by input D26-1 of the tracking amplifier which adjusts the COM reference potential of the +15V regulator to produce an equal but opposite change on the +15V output line.

The three capacitors (D28, D32, D34) in the $\pm 15\text{V}$ power supply circuits prevent circuit oscillations.

+5VDC

The +5VDC supply uses a standard bridge rectifier (BR2) with capacitive filtering at its output.

Overvoltage Protection — is provided by a silicon controlled rectifier (SCR) at H33. When overvoltage occurs, the SCR fires, shorting the rectifier output and causing fuse H43 to open.

The overvoltage protection circuit consists of the SCR, transistor H32, resistors F34, F33, F31, capacitor F30 and the 5.6 volt zener diode F32. The base of transistor H32 is biased from the constant +5.6 volts at the top end of zener diode F32. If the voltage on the +5V line rises, transistor H32 begins conducting through resistor F34. If the voltage across resistor F34 reaches approximately 1.25 volts, SCR H33 fires and opens fuse H43. The firing point of the SCR is reached when the +5V line is in the range from 5.75 volts to 6.9 volts.

Capacitor F30 prevents firing the SCR by transients reflected by the load.

Voltage Regulation — of the +5VDC is performed by an integrated regulator (F25) which varies the voltage dropped across a series pass transistor (H17) to compensate for changes in the output voltage.

The integrated regulator is connected as a positive voltage regulator with foldback current limiting. The regulator compares the +5VDC output voltage, applied to pins 3 and 4, with an internal reference voltage. If the +5VDC begins to decrease, the regulator increases drive to the base of transistor H17. This reduces the voltage dropped across transistor H17 to offset the drop in the +5VDC output voltage.

The amplitude of the +5VDC output is adjustable by means of the 1K potentiometer at H24. This potentiometer varies the internal reference voltage of the integrated regulator.

Current Limiting — The foldback current limiting circuit consists of a .1 ohm current sensing resistor at H15, operational amplifier D26-10, the integrated regulator at F25 and the series pass transistor H17.

The voltage across the current sensing resistor is applied to pins 6 and 7 of the operational amplifier. The amplifier output at D26-10 is applied to a voltage divider consisting of resistors D15 and D17. The top end of resistor D15 connects to the current limit input at pin 2 of the regulator. As +5V output current increases, the voltage applied to the current limit input F25-2 of the regulator also increases. Foldback occurs when output current is somewhere in the range of approximately 3.45 A to 5.02 A. At this point, drive to the series pass transistor H17 decreases and output current is limited to the range of approximately 1.19 A to 2.1 A by the increased impedance of the series pass transistor.

Brush Motor

The 24VDC brush motor is switched on and off by triac A8 in the Brush Motor Return line under control of the BRUSH ENABLE signal. Figure 4-14A shows a composite schematic of the Brush

Motor and Fan Motor circuits.

When BRUSH ENABLE is LO, the triac is nonconductive, so the Brush Motor is "off". When BRUSH ENABLE goes HI, the triac conducts and the Brush Motor is "on".

Fan Motor

The fan motor effectively is connected directly across the 24VAC transformer winding.

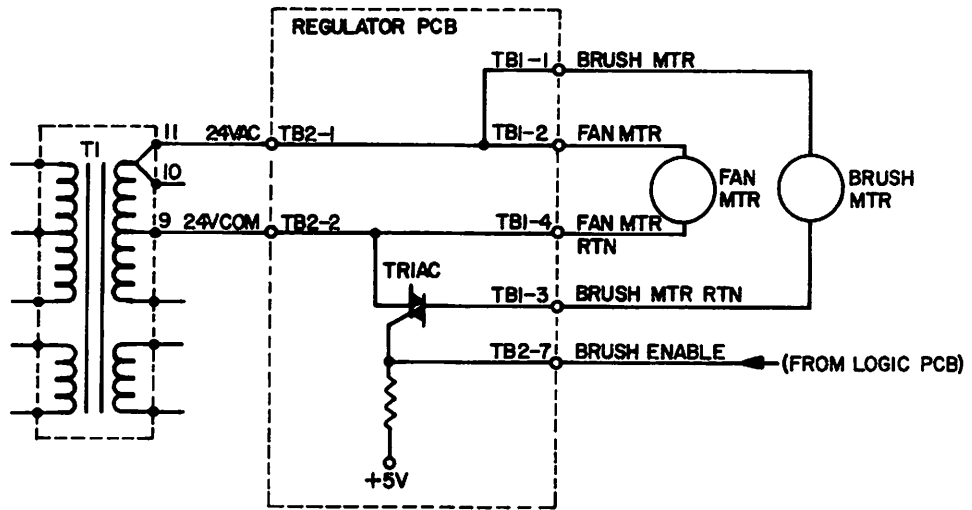
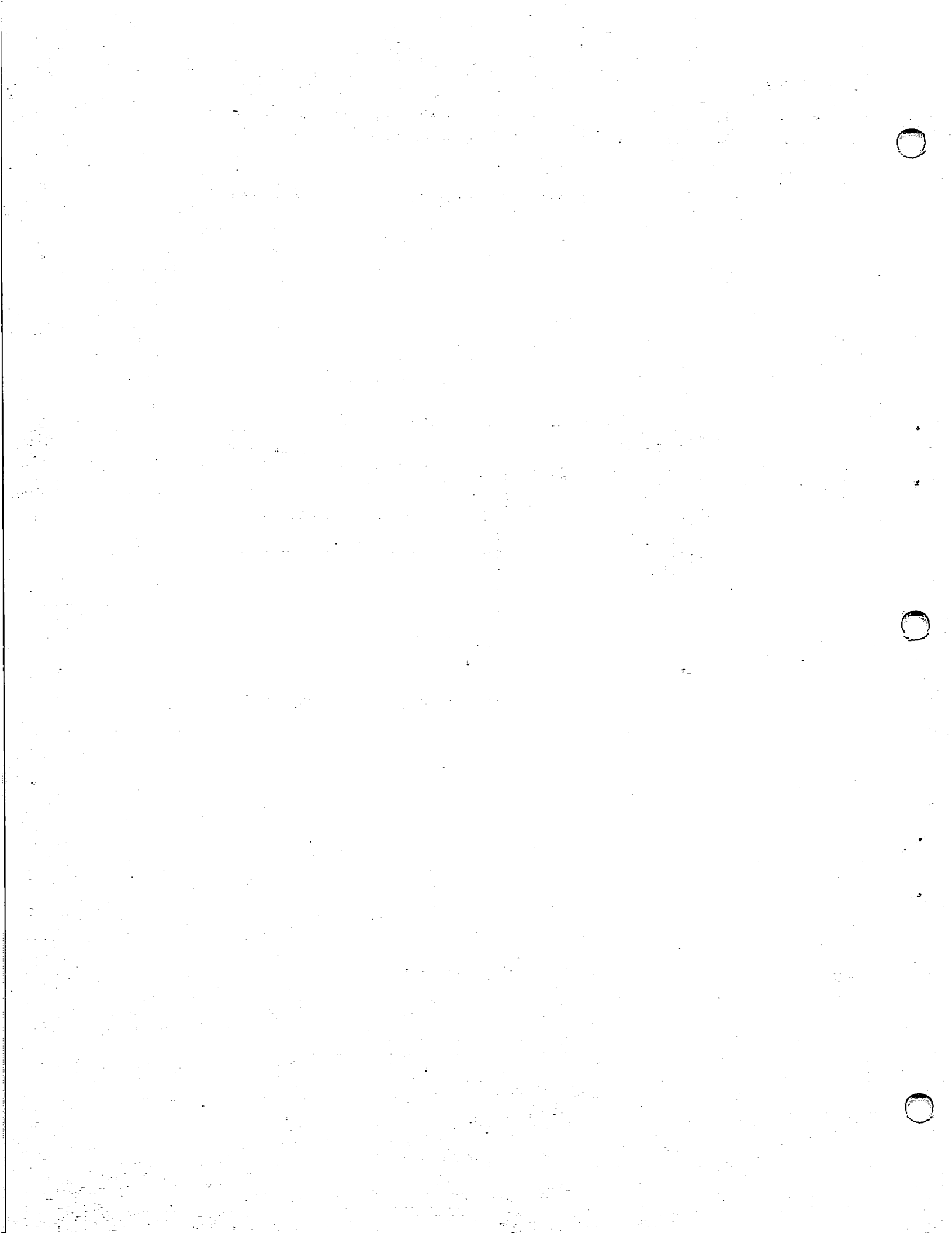


Figure 4-14A FAN AND BRUSH MOTOR CIRCUITS



4.3.2 Input/Output (I/O) PCB Assy No. 12025

(Text based on Assy 12025, Rev. A.)

Refer to Figure 7-3, I/O PCB Schematic.

The I/O PCB holds the two parallel-connected I/O connectors. The Read Clock and Read Data output drivers are located on the I/O PCB to avoid switching relatively high currents on the Data Transfer PCB. +5 V is supplied to the I/O connectors for use by the Terminator. Isolation diode D1 decouples the internal +5 V from the +5 V lines of other drives in a daisy-chain system.

4.3.3A Address Logic (A/L) PCB Assy 12101/12101-XX/12152-XX/12129

(Text based on Assy 12101-XX, Rev. F. Differences in Assy 12152-XX summarized in subsection 4.3.3B. Differences in Assy 12129 summarized in subsection 4.3.3C.)

The Address Logic PCB contains the circuits that perform the following functions:

1. Hold the present cylinder address in the Present Address Register (PAR).
2. Hold the new address from the controller in the New Address Register (NAR).
3. Detect invalid new addresses.
4. Specify direction the heads are to move during a seek operation.
5. Provide to the head positioner servo an analog current output signal proportional to the distance to go to the new address location.
6. Detect when head motion stops, and then issue the RSRW (Ready to **S**eek, **R**ead or **W**rite) signal or SEEK INCOMPLETE signal.
7. Decode the Unit Select and Attention lines.
8. Provide interface buffering for seek control and status lines.

4.3.3.1A New Address Register (NAR)

Refer to Figure 7-4B, Address Logic Schematic – Sheet 1.

The NAR consists of nine D-type flip-flops (N40, N50 and D50-5). The data inputs to the NAR are controlled by two data selectors (H40 and H50) and a set of input gates.

The NAR input gates are controlled by the +SELECTED signal in conjunction with -CAL (Calibrate). When +SELECTED and -CAL are both HI, the new cylinder address is gated through to the data selector inputs.

Data selector control is provided by switch SW-1 (M75). For 200 tpi operation, the "select" inputs of the data selectors are held HI by switch SW-1 being open. This conditions the data selectors to pass their "B" inputs to the NAR. Consequently, address bit 2 goes to NAR input N50-4 and bit 256 goes to N40-13. Bit 1 goes directly from input gate K20-14 to FF input D50-2.

For 100 tpi operation, the "select" inputs of the data selectors are held LO by switch SW-1 being closed. This conditions the data selectors to pass their "A" inputs to the NAR. Consequently, bit 1 goes to NAR

input N50-4 and bit 128 goes to input N40-13. FF D50-5 is held set by the LO at D50-4.

The new address is clocked into the NAR approximately 400 ns after receiving the leading edge of the STROBE pulse from the controller. See subsection 4.3.3.4A for STROBE utilization.

When a Restore command occurs, -CAL goes LO. This simultaneously disables the NAR input gates and raises the output of gate P30-3. As the gate output goes HI, the NAR clocks to zero.

The six highest bits of the new address are encoded to detect invalid addresses (addresses greater than 407 for 200 tpi, and greater than 203 for 100 tpi). The resultant signal, ->407 (203), is sent to the Strobe Logic, where it enables ADRS ACK (Address Acknowledge) if the address is valid, or LAI (Logical Address Interlock) if the address is invalid. When an invalid address is detected, the NAR clock pulse does not occur, consequently, the NAR retains the last valid address.

The RAMP signal is ORed with the bit 8 output of the NAR for head positioner velocity control during loading and unloading of the heads. The combination of the bit 8 provided by RAMP plus the bit 1 provided by -CAL produces a speed command of 9.

The HI RAMP signal also appears to the input of the Adder as a new address value of 8; consequently, during head loading the heads proceed out to cylinder 8. At cylinder 8 the Ramp FF becomes reset, and since the NAR is holding zeros, a seek to track 0 occurs immediately. See subsection 4.3.3.5A for RAMP signal control.

4.3.3.2A Present Address Register (PAR) and Count Control Logic

Refer to Figure 7-4B, Address Logic Schematic – Sheet 1.

The PAR is a 10-bit UP/DOWN counter implemented with cascaded synchronous UP/DOWN counters H60, F60 and D60. H60 and F60 hold the lower eight bits of the cylinder address. The ninth and tenth bits are held by D60. Although no valid address utilizes the tenth bit, this bit is summed with a fixed "one" bit in the Adder. This is done to eliminate the possibility of an extra count pulse (due to an overshoot past track 0) creating a maximum value servo error signal which would force the head positioner to retract at full velocity into the rear end stop.

The count pulses and DOWN/UP control signal are decoded from two signals entitled "C" and "D" supplied by the Servo PCB. C and D are derived from the recovered transducer signal which indicates head-to-track positional relationship. Signals C and D each make one complete cycle for every four tracks crossed by the R/W heads. The count pulses are supplied to the counter through gate E60-8; the DOWN/UP control signal is supplied through gate E60-3.

Refer to Figure 4-15. When the heads are moving forward, the C signal leads the D signal by 90°; when the heads are moving in reverse, the C signal lags the D signal by 90°. Each transition of C and D generates a count pulse which increments or decrements the PAR. NOTE: The PAR holds the present address in one's complement form. This allows a difference value to be obtained when the contents of the PAR and NAR are summed in the Adder.

When the head positioner is moving forward, the DOWN/UP control line is HI as each count pulse occurs, causing the PAR to be decremented by one count for each count pulse. Conversely, when the head positioner is moving in reverse, the DOWN/UP control line is LO when each count pulse occurs, causing the PAR to be incremented by one count for each count pulse.

The L (Load) input of the PAR is controlled by the -CAL signal. -CAL goes LO during a restore operation or during a retract condition. When this occurs, the lower nine bit positions of the PAR are loaded with ones through the parallel load inputs (A, B, C and D) of the Present Address Register. With -CAL holding

SECTION 6 APPENDICES

6.1 OPTIONS

A summary of options available for the Model 44B Disk Drive is given in Table 6-1. For those options involving extra cost, an asterisk (*) appears with the Option Number. A Request For Quotation is required before such special options can be provided. A brief description of each option is given below.

Fixed Disk Sectoring

- Option 44B-01 — Index Only
- 44B-08 — 8 Sector
- 44B-12 — 12 Sector
- 44B-14 — 14 Sector
- 44B-16 — 16 Sector
- 44B-20 — 20 Sector
- 44B-24 — 24 Sector
- 44B-32 — 32 Sector

- Requirements:
- 1) SW1 on Logic PCB set to ON for Option 44B-01.
SW1 on Logic PCB set to OFF for all other sectoring options.
 - 2) Each sectoring option also requires a spindle assembly with the appropriate number of sector slots.

Separated/Unseparated Data

Standard: Data and Clock signals retrieved from disk sent to interface on separate lines.

Option 408: Multiplexed Data and Clock signal (double frequency encoded) sent to interface on Read Data line.

Requirements: SW4 on D/T PCB set to ON.

Attention Polarity

Standard: Positive Attention signal (High inactive state)

Option 490: Negative Attention signal (Low inactive state)

- Requirements:
- 1) SW2 on A/L PCB set to ON.
 - 2) With I/O PCB Assy 12160-XX, close the attention line switch corresponding to the ID number of the drive, and open the other 3 attention line switches. With I/O PCB Assy 12025, modification for negative attention is unnecessary unless units are daisy chained. With daisy chain, proceed as follows:
 - a) Determine unit position in daisy chain (Unit ID number).
 - b) Leave the corresponding attention line intact and cut the remaining 3 attention line traces on the I/O PCB

Note: Thereafter, the unit must retain this position in the daisy chain to operate properly.

Track Density/Spindle Speed

Standard: 200tpi/2400rpm

Option 491: 100tpi/2400rpm

Option 492: 100tpi/1500rpm

Requirements: Option 491

- 1) R/W heads for 100tpi, 2400rpm.
- 2) Special A/L PCB assembly 12152-05, with SW1 set to ON.

Option 492

- 1) R/W Heads for 100tpi, 1500rpm.
- 2) Base plate assembly for 1500rpm.
- 3) Special D/T PCB assembly 12143-02.
- 4) SW2 on Logic PCB assembly set to ON.
- 5) Special A/L PCB assembly 12152-05, with SW1 set to ON.

Data Separator

Standard: Single-Shot Data/Clock Separator

Optional: VFO Data/Clock Separator for 200tpi, 2400rpm drives.

The VFO option permits the Model 44B to be used with System 3 type format, or other systems with missing clock pulse formats.

Option 493-01* — 100ns output pulse width

Option 493-02 — 200ns output pulse width

Requirements: Option 493-01*

Special D/T PCB assembly 12121-04 (without Write Protect); or
12121-05 (with Write Protect).

Option 493-02

Special D/T PCB assembly 12121-02 (without Write Protect); or
12121-03 (with Write Protect).

Write Protect

Standard: Both disks unprotected.

Option 494: Lower disk write protected.

Option 495: Upper disk write protected.

Requirements: Option 494

SW3 on D/T PCB assembly set to OFF.

Option 495

SW2 on D/T PCB assembly set to OFF.

Installation

Standard: Drive furnished with rack slides and hardware for rack mounting.

Option 496: Desk top version.

Requirements: Drive furnished with Desk Top Kit installed.

Front Panel Logo

Standard: Diablo logo on front panel.

Option 497: No logo on front panel.

Series 30 Compatibility

Standard: The standard Model 44B is not directly compatible with Diablo Series 30 disk drives.

Option 498: With this option, the Model 44B disk drive is Series 30 compatible.

Requirements: 1) -02 version of A/L PCB assembly.

2) -02 version of Logic PCB assembly.

3) I/O PCB assembly 12160-01.

Erase Gate Control

Standard: Erase and Write functions controlled separately by ERASE GATE and WRITE GATE signals.

Option 499: WRITE GATE controls the Write function and Erase function together.

Requirements: SW1 on D/T PCB set to OFF.

Busy Seeking

Standard: One of four Attention lines from drive is enabled by Unit ID switches on A/L PCB. The enabled line produces a LO output under the following conditions:

- 1) LO level during seek to new address, beginning with leading edge of -ADRS ACK and ending with leading edge of -RSRW. If a seek incomplete condition occurs, the Attention LO level continues until the seek incomplete is cleared.
- 2) LO pulse when a command is received to seek to present address.
- 3) LO pulse when an invalid address is received.

Option 500*: This option consists of the following:

- 1) The four Attention output interface lines ATTN 1 – ATTN 4 are reidentified as BUSY SEEKING 1 – BUSY SEEKING 4 and the enabled line transmits RSRW (Ready to Seek/Read/Write) status to the controller.
- 2) +SECTOR MARK replaces -SECTOR MARK at the output interface.
- 3) Index/Sector mark pulse width of $7 \pm 2 \mu\text{s}$.
- 4) 32 sector spindle assembly.
- 5) Brown and Beige colored front panel assembly.

Requirements: 1) Special A/L PCB assembly 12129-01. .
2) Special Logic PCB assembly 12127-01.
3) 32 sector spindle assembly.
4) Special front panel assembly 19004-04.

Front Panel

Standard: Drive equipped with front panel.

Option 502*: No front panel on drive.

LAI Signal

Standard: LAI is a TTL level which goes LO upon receipt of an invalid address and remains LO until a valid address is received.

Option 504: LAI is a $1 \mu\text{s}$ pulse which occurs when an invalid address is received.

Requirements: A/L PCB assembly 12152-03.

Front Panel Paint

Standard: Color combination Charcoal/Black/White

Option 506*: Color combination Brown/Creme

Option 511*: Gray Front Trim Panel

Power-On Indicator

This option is available only in units using the optional VFO Data Separator.

Standard: When either of the two Write Protect switches on the D/T PCB is set for protect, the red indicator on the front panel functions as Protect indicator. When neither of the two switches is set for protect, the indicator functions as Power-On indicator.

Option 507*: The red indicator on the front panel functions as Power-On indicator regardless of the

settings of the Write Protect switches on the D/T PCB.

Requirements: VFO D/T PCB 12121-02 (200ns data/clock output pulse); or,
VFO D/T PCB 12121-04 (100ns data/clock output pulse)

Interrupt Option

Standard: The RSRW (Ready to Seek/Read/Write), SEEK INC., and FILE READY status signals to the output interface are read by unit selection from the controller.

Option 508*: The above listed status lines are unrestricted by unit selection from the controller, so status change information appears immediately at the output interface.

This option also includes the features of Series 30 compatibility. (See option 498)

Requirements: 1) A/L PCB Assy 12152-04
2) Logic PCB Assy 12141-04

Busy Seeking Function and 7 μ s Index/Sector Pulse

Standard: Attention function and 40 μ s Index/Sector pulse width.

Option 509*: Busy Seeking function and 7 μ s Index/Sector pulse width. (See Option 500 for description of Busy Seeking function.) In addition to the normal Busy Seeking function, the 12129-02 A/L PCB Assy used in this option produces a 1 μ s pulse on the Busy Seeking line whenever a seek-to-same-address command is received.

Requirements: 1) Special A/L PCB Assy 12129-02.
2) Logic PCB Assy 12141-05.

Index/Sector Pulse

Standard: Index and Sector pulses have a pulse width of 40 μ s.

Option 510*: Index and Sector pulses have a pulse width of 5 μ s.

Requirements: Logic PCB Assy 12141-02.

**Table 6-1
44B OPTION SUMMARY**

FEATURE	STANDARD	OPTIONAL	OPTION No.
Fixed Disk Sectoring	-----	Index Only	44B-01
	-----	8 Sector	44B-08
	-----	12 Sector	44B-12
	-----	14 Sector	44B-14
	-----	16 Sector	44B-16
	-----	20 Sector	44B-20
	-----	24 Sector	44B-24
	-----	32 Sector	44B-32
Separated/Unseparated Data	Data & Clock separated	Data & Clock unseparated	408
Attention Polarity	Positive Attention	Negative Attention	490
Track Density/Spindle Speed	200tpi/2400rpm	100tpi/2400rpm	491
		100tpi/1500rpm	492
Data Separator	Single-Shot Data Separator	VFO Data Separator	
		200tpi, 2400rpm: 100ns pulse width	493-01*
		200ns pulse width	493-02
Write Protect	No Protect	Write Protect: Lower Disk	494
		Upper Disk	495
Installation	Rack Mounting	Desk Top Version	496
Front Panel Logo	With Diablo Logo	Without Logo	497
Series 30 Compatibility	-----	Series 30 Compatible	498
Erase Gate Control	Erase and Write functions controlled separately	Combined control of Erase and Write functions	499
Busy Seeking	Attention function	Busy Seeking function	500*
Front Panel	Includes Front Panel	Without Front Panel	502*
LAI Signal	TTL level	1 μ s pulse	504
Front Panel Paint	Color Charcoal/Black/White	Color Brown/Creme	506*
Power-On Indicator	Write Protect Indicator	Power-on Indicator	507*
Interrupt Option	RSRW and Seek Inc. status read by unit selection from controller.	RSRW and Seek Inc. status lines unrestricted by unit select from controller.	508*
Busy Seeking and 7 μ s Index/Sector Pulse	Attention function and 40 μ s Index/Sector pulse width.	Busy Seeking function and 7 μ s Index/Sector pulse width.	509*
Index/Sector Pulse	40 μ s pulse width	5 μ s pulse width	510*
Front Trim Panel	Color White	Color Gray	511*
Input Voltage	100 - 120 VAC	220 - 240 VAC	220-240VAC

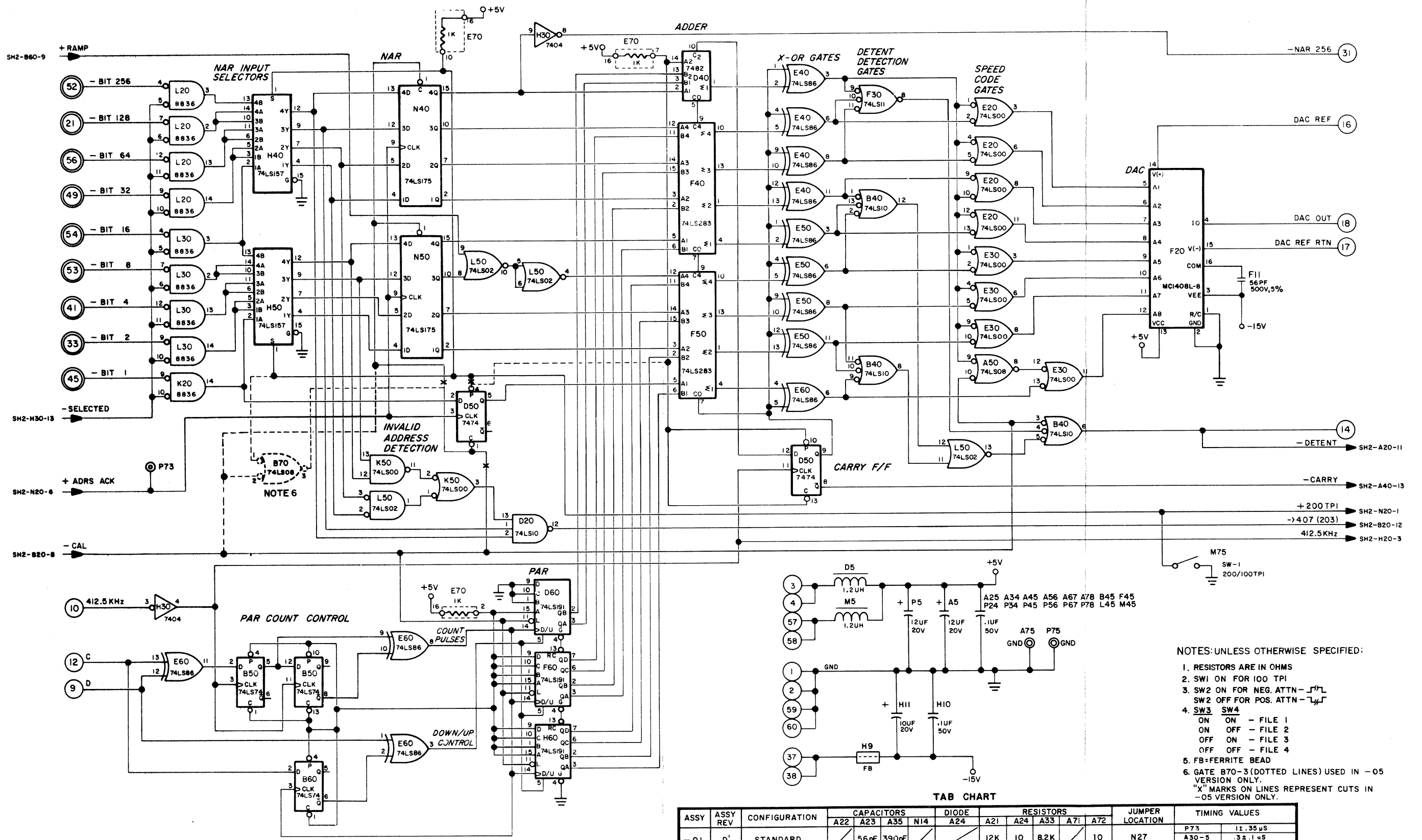
* Options marked with an asterisk (*) involve extra cost and require a Request For Quotation before they can be provided.

6.2 ACCESSORIES

Table 6-2 lists the accessories available for the Model 44B Disk Drive.

**Table 6-2
ACCESSORIES**

No.	ITEM
400	Type 5440 cartridge with index mark only
	Type 5400 cartridge:
402-08	8 Sector
-12	12 Sector
-14	14 Sector
-16	16 Sector
-20	20 Sector
-24	24 Sector
-32	32 Sector
436	I/O Terminator
	I/O Cable Assembly:
453-05	5 feet
453-07	7 feet
	(Other lengths available by special request)



- NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE IN OHMS
 2. SW1 ON FOR 100 TPI
 3. SW2 ON FOR NEG. ATTN - \overline{L}
SW2 OFF FOR POS. ATTN - \overline{L}
 4. SW3 SW4
ON ON - FILE 1
ON OFF - FILE 2
OFF ON - FILE 3
OFF OFF - FILE 4
 5. FB=FERRITE BEAD
 6. GATE B70-3 (DOTTED LINES) USED IN -05 VERSION ONLY.
"X" MARKS ON LINES REPRESENT CUTS IN -05 VERSION ONLY.

TAB CHART

ASSY	ASSY REV	CONFIGURATION	CAPACITORS				DIODE	RESISTORS				JUMPER LOCATION	TIMING VALUES	
			A22	A23	A35	N14	A24	A21	A24	A33	A71			A72
-01	D'	STANDARD	/	56pF	390pF	/	/	12K	10	8.2K	/	10	N27	P73 1 ± .35 μs A30-5 .3 ± .1 μs A70 TTL LEVEL
-02	D'	SERIES 30 COMPATIBLE	5600 pF	/	820pF	330pF	IN 4454	22K	/	20K	10	/	N 27	P73 5 ± 2 μs A30-5 35.5 ± 10 μs A70 5 ± 2 μs
-03	D'	PULSED LAI	/	56pF	390pF	/	/	12K	10	8.2K	10	/	N 27	P73 1 ± .35 μs A30-5 .3 ± .1 μs A70 1 ± .35 μs
-04	D'	INTERRUPT OPTION	5600 pF	/	820pF	330pF	IN 4454	22K	/	20K	10	/	N 24	P73 5 ± 2 μs A30-5 35.5 ± 10 μs A70 5 ± 2 μs
-05	E	100 TPI	/	56pF	390pF	/	/	12K	10	8.2K	/	10	N27	P73 1 ± .35 μs A30-5 .3 ± .1 μs A70 TTL LEVEL

Figure 7-4C. ADDRESS LOGIC PCB ASSY SHEET 1
#12152-XX Rev. E

ADDRESS LOGIC PCB ASSY. 12152-XX

REVISION HISTORY

Schematic Rev.	Assy. Rev. Levels					ECO	
	-01	-02	-03	-04	-05		
A	A	A	A			2389	ECO release of schematic and assembly.
B	B	B	B			2533	1. Circuit changes for FF's H20-5, H20-9 and Unit Select Decoder M40 to prevent false File Ready at AC turn-on. 2. Circuit change for Seek Inc. FF to prevent false seek incomplete indication after quick OFF-ON cycle of AC power. 3. Release of PCB etch 12151-01.
C	C	C	C			2657	In 12152-02 Assy., 330 pF capacitor (N14) added to -RSRW output interface line to slow the rise time of -RSRW.
D	D	D	D	D		2639	Releases -04 version of assembly 12152-XX for Interrupt option. Releases 12151-02 PCB etch.
D'	D'	D'	D'	D'		2884	Corrects documentation error.
E	D'	D'	D'	D'	E	2993	Releases -05 version of assembly 12152-XX for use in 100 TPI drives. This allows the same Track 0 adjustment procedure to be used for both 200 TPI drives and 100 TPI drives.

COMPONENT TYPES

Diode, 1N4454	A24
Resistor Pack, 1K	E70
Resistor Pack, 10K	P20
IC, 74LS00	A40, E20, E30, K50
IC, 74LS02	L50
IC, 7404	H30
IC, 74LS08	A50, B20, B70
IC, 74LS10	B40, D20
IC, 74LS11	F30
IC, 7474	D50
IC, 74LS74	B30, B50, B60, D30, H20
IC, 7482	D40
IC, 8836	K20, L20, L30, L40
IC, 74LS86	E40, E50, E60, M30
IC, 74123	A30
IC, 74LS151	M40
IC, 74LS155	M50
IC, 74LS157	H40, H50
IC, 74LS175	N40, N50
IC, 74LS191	D60, F60, H60
IC, 74LS283	F40, F50
IC, 75452	M15, M20, N15, N20, N30, P30
IC, MC1408L-8	F20
IC, CD4040	A20

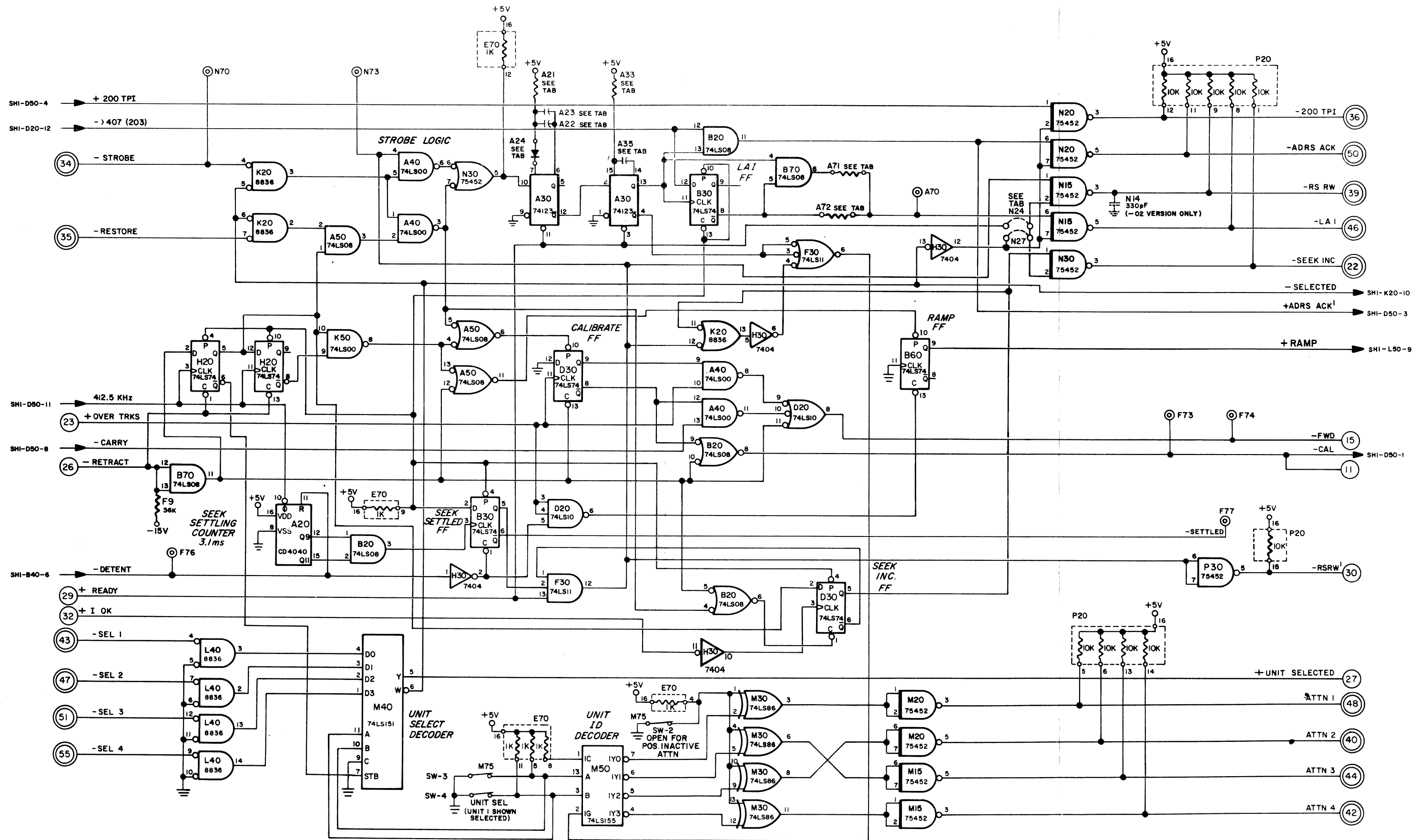
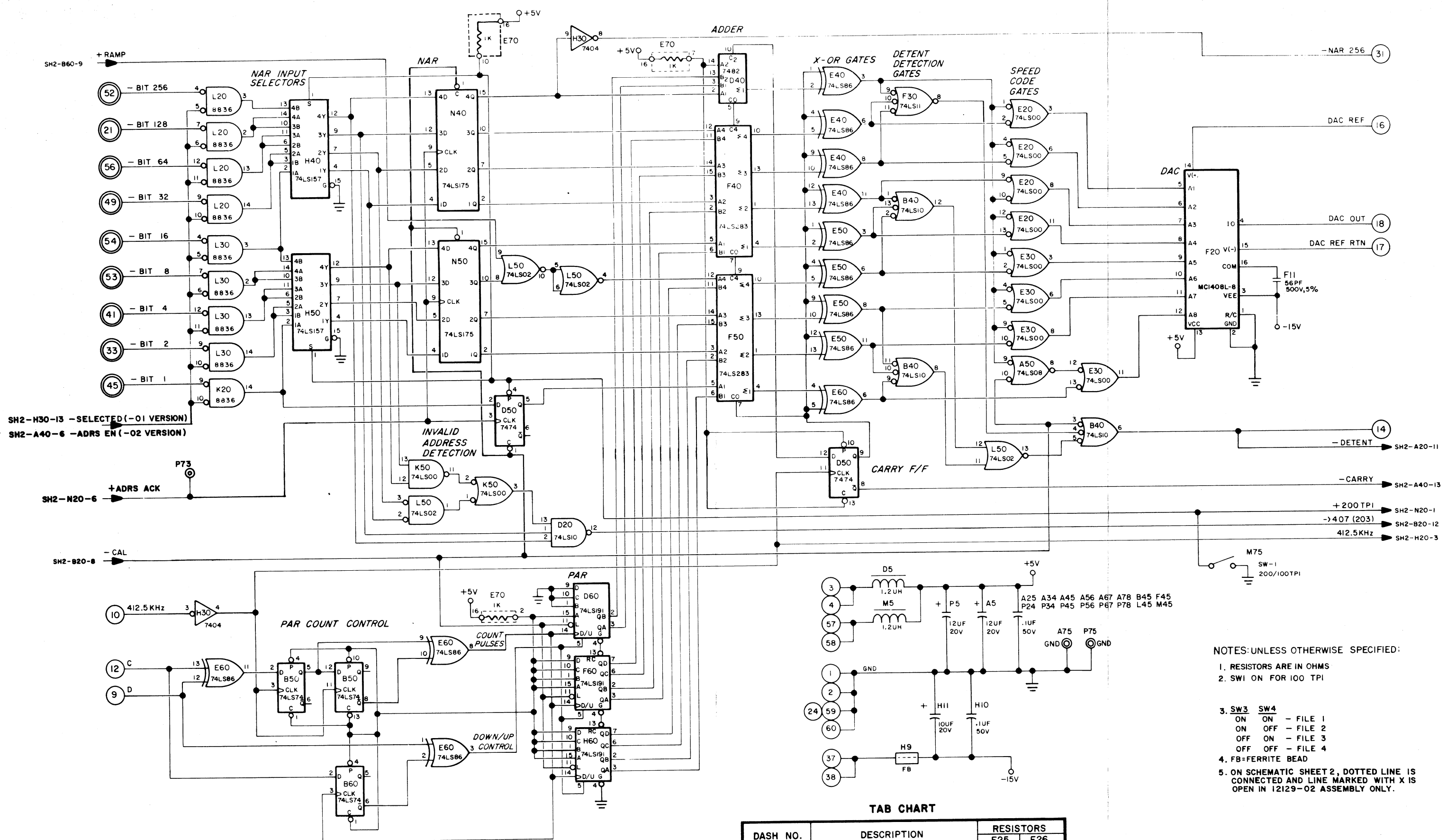
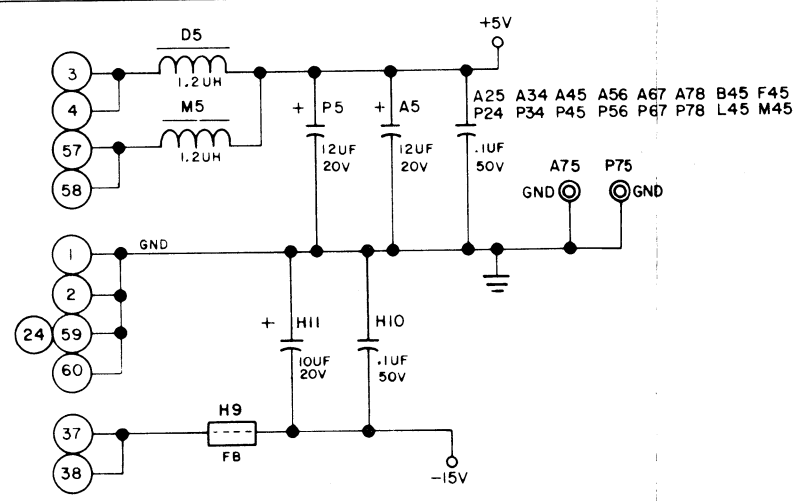


Figure 7-5C. ADDRESS LOGIC PCB ASSY SHEET 2 #12152-XX Rev. E



SH2-H30-13 --SELECTED (-01 VERSION)
 SH2-A40-6 --ADRS EN (-02 VERSION)



- NOTES: UNLESS OTHERWISE SPECIFIED:
1. RESISTORS ARE IN OHMS
 2. SW1 ON FOR 100 TPI
 3. SW3 SW4
 ON ON - FILE 1
 ON OFF - FILE 2
 OFF ON - FILE 3
 OFF OFF - FILE 4
 4. FB=FERRITE BEAD
 5. ON SCHEMATIC SHEET 2, DOTTED LINE IS CONNECTED AND LINE MARKED WITH X IS OPEN IN 12129-02 ASSEMBLY ONLY.

TAB CHART

DASH NO.	DESCRIPTION	RESISTORS	
		F25	F26
- 01	-BUSY SEEKING FOLLOWS RSRW	/	10 Ω
- 02	PULSED BUSY SEEKING	10 Ω	/

Figure 7-4E. ADDRESS LOGIC PCB ASSY
 SHEET 1
 OPTION SPECIAL
 #12129-01 Rev. D
 #12129-02 Rev. E

ADDRESS LOGIC PCB ASSY. 12129-XX

OPTION SPECIAL
(PCB Etch 12128-01)

For revision levels A and B, see Figures 7-4D/7-5D.

REVISION HISTORY

Assy. Rev.		ECO	
Levels			
<u>-01</u>	<u>-02</u>		
C	C	2785	Releases new PCB Etch 12128-01 to incorporate cuts and adds, and makes provision for -02 version of 12129-XX.
D	D	2994	Corrects documentation error.
	E	5029	Circuit changed in -02 version to enable address inputs only for duration of input Strobe pulse.

COMPONENT TYPES

Diode, 1N4454	A24
Resistor Pack, 1K	E70
Resistor Pack, 10K	P20
IC, 74LS00	A40, E20, E30, K50
IC, 74LS02	L50
IC, 7404	H30
IC, 74LS08	A50, B20, B70
IC, 74LS10	B40, D20
IC, 74LS11	F30
IC, 7474	D50
IC, 74LS74	B30, B50, B60, D30, H20
IC, 7482	D40
IC, 8836	K20, L20, L30, L40
IC, 74LS86	E40, E50, E60, M30
IC, 74123	A30
IC, 74LS151	M40
IC, 74LS155	M50
IC, 74LS157	H40, H50
IC, 74LS175	N40, N50
IC, 74LS191	D60, F60, H60
IC, 74LS283	F40, F50
IC, 75452	M15, M20, N15, N20, N30, P30
IC, MC1408L-8	F20
IC, CD4040	A20

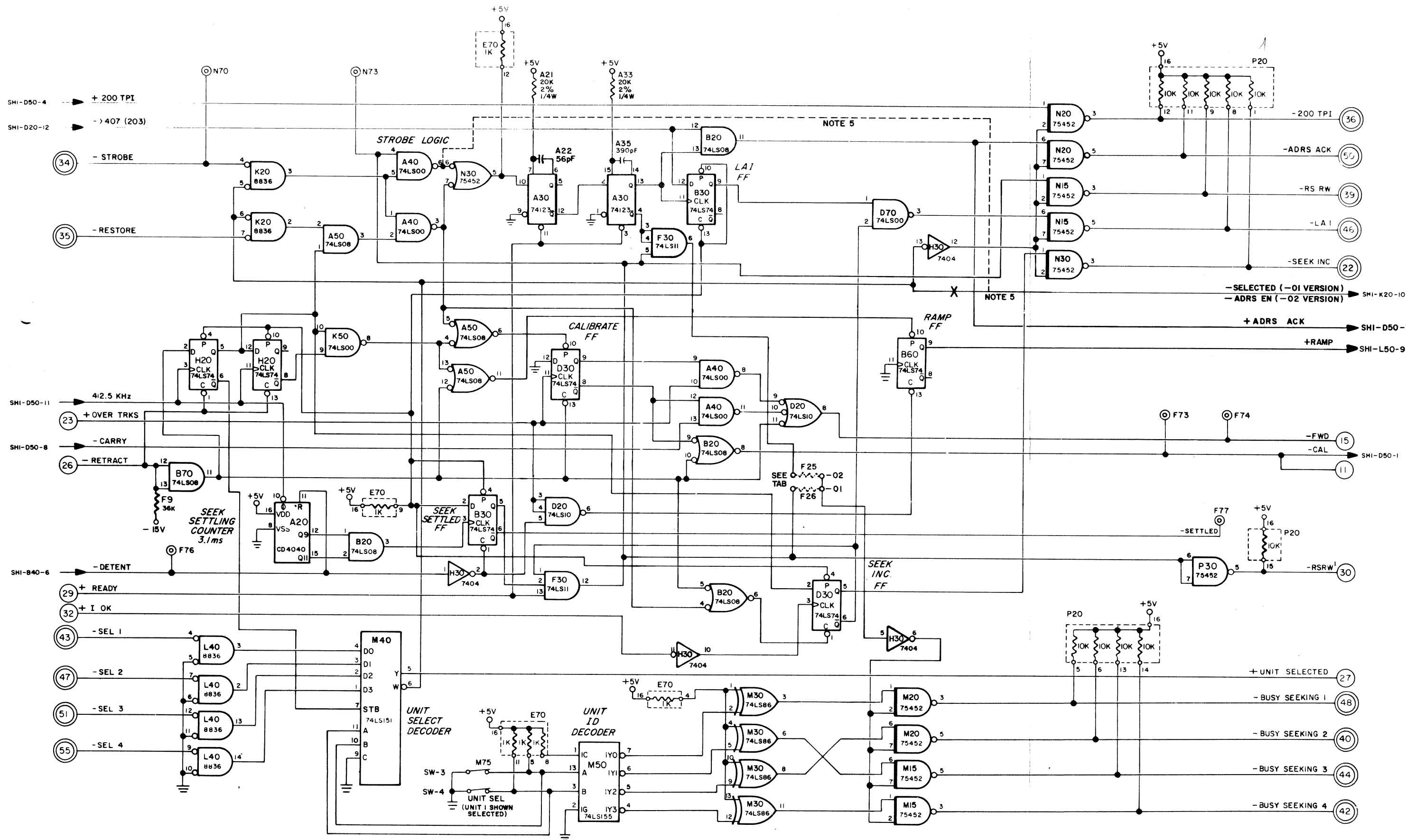


Figure 7-5E. ADDRESS LOGIC PCB ASSY SHEET 2
 OPTION SPECIAL
 #12129-01 Rev. D
 #12129-02 Rev. E

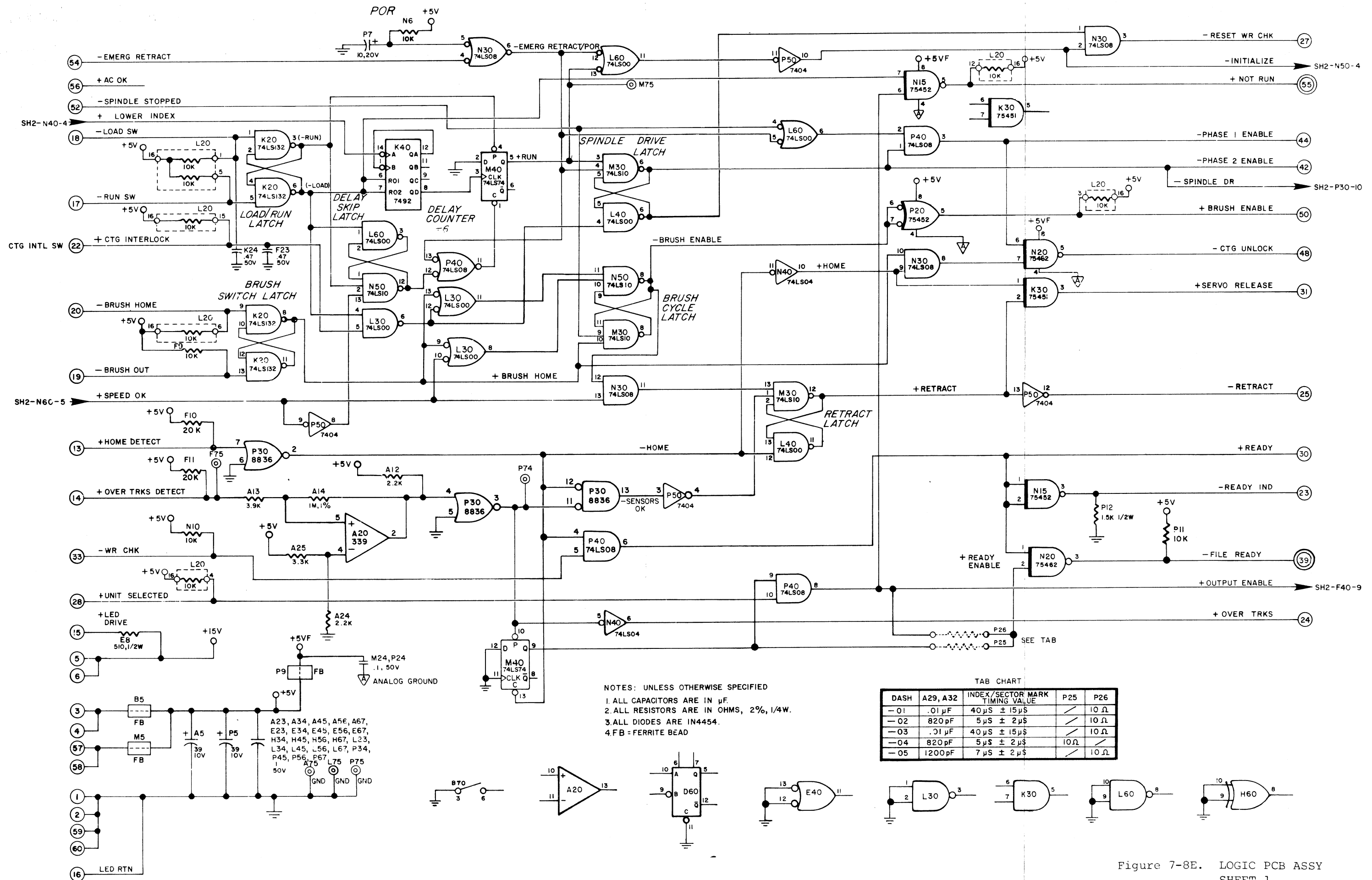


Figure 7-8E. LOGIC PCB ASSY SHEET 1 #12141-XX Rev. F'

LOGIC PCB ASSY. 12141-XX
(PCB etches 12140/12140-01)

For revision level A of 12141-XX, see Figures 7-8C/7-9C.

REVISION HISTORY

<u>Rev.</u>	<u>ECO</u>	
B	2614	Produces 12141-03 PCB Assy using modified 12140 PCB etch.
C	2630	Releases PCB etch 12140-01 for PCB Assy 12141-XX. Adds -04 version for Interrupt option.
D	2731	1) Following changes made in Upper and Lower Index Transducer Amplifiers to obtain increased output from index sensor: (Sheet 2) Resistors D16/B9 changed from 3.3K to 10K. Resistors B18/B16 changed from 100K to 1K. Capacitors D18/B15 changed from .001 mFd to .0033 mFd. 2) -05 version added for 7 microsecond index/sector timing and long cable lengths. Capacitor P13 added to Sector Marks output line for -05 version only. (Sheet 2)
E	2845	To extend its maximum supply voltage limit, IC N20 changed from type 75452 to 75462.
F	2929	Following cuts and adds made to eliminate erroneous initial seeks when loading heads and to correct erroneous early interface ready status in -04 version. 1) Trace cut between M40-9 and P40-4. 2) Trace cut between P40-6 and P40-9. 3) Jumper added from M40-9 to P40-9. 4) Jumper added from P30-12 to P40-4. 5) Trace cut between resistor P25 and P40-9. 6) Jumper added from M40-9 to free side of resistor P25.
F'	2933	Drafting errors corrected.

COMPONENT TYPES

Diode, 1N4454	B11, D13, D17
Resistor Pack, 10K	L20
IC, LM339	A20
IC, 8836	P30
IC, 74LS00	D40, E40, L30, L40, L60
IC, 7404	P50
IC, 74LS04	F40, N40
IC, 74LS08	N30, P40
IC, 74LS10	M30, N50
IC, 74LS20	F60
IC, 74LS74	B40, D30, H40, M40, N60
IC, 74LS86	H60
IC, 7492	K40
IC, 7493	E20, E30, H50
IC, 7497	F50
IC, 74LS123	A40, D60
IC, 74LS132	K20
IC, 74LS157	F30, H30
IC, 74LS163	K50
IC, 74LS191	E50, E60, L50
IC, 74LS193	A50, B50
IC, 75451	K30
IC, 75452	M15, M20, N15, P15, P20
IC, 75462	N20
IC, CD4040	K60, M50
IC, CD4050	M60

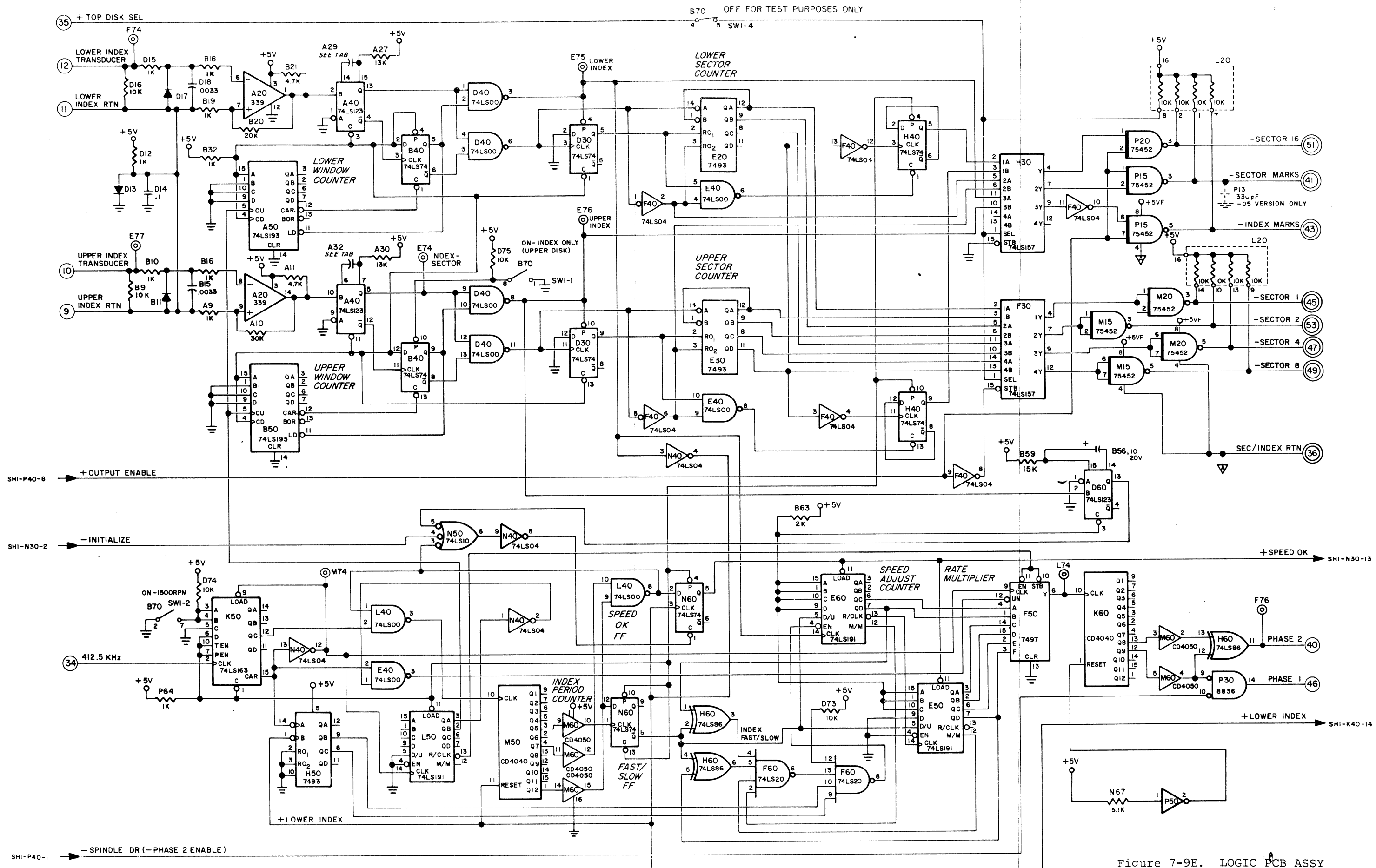
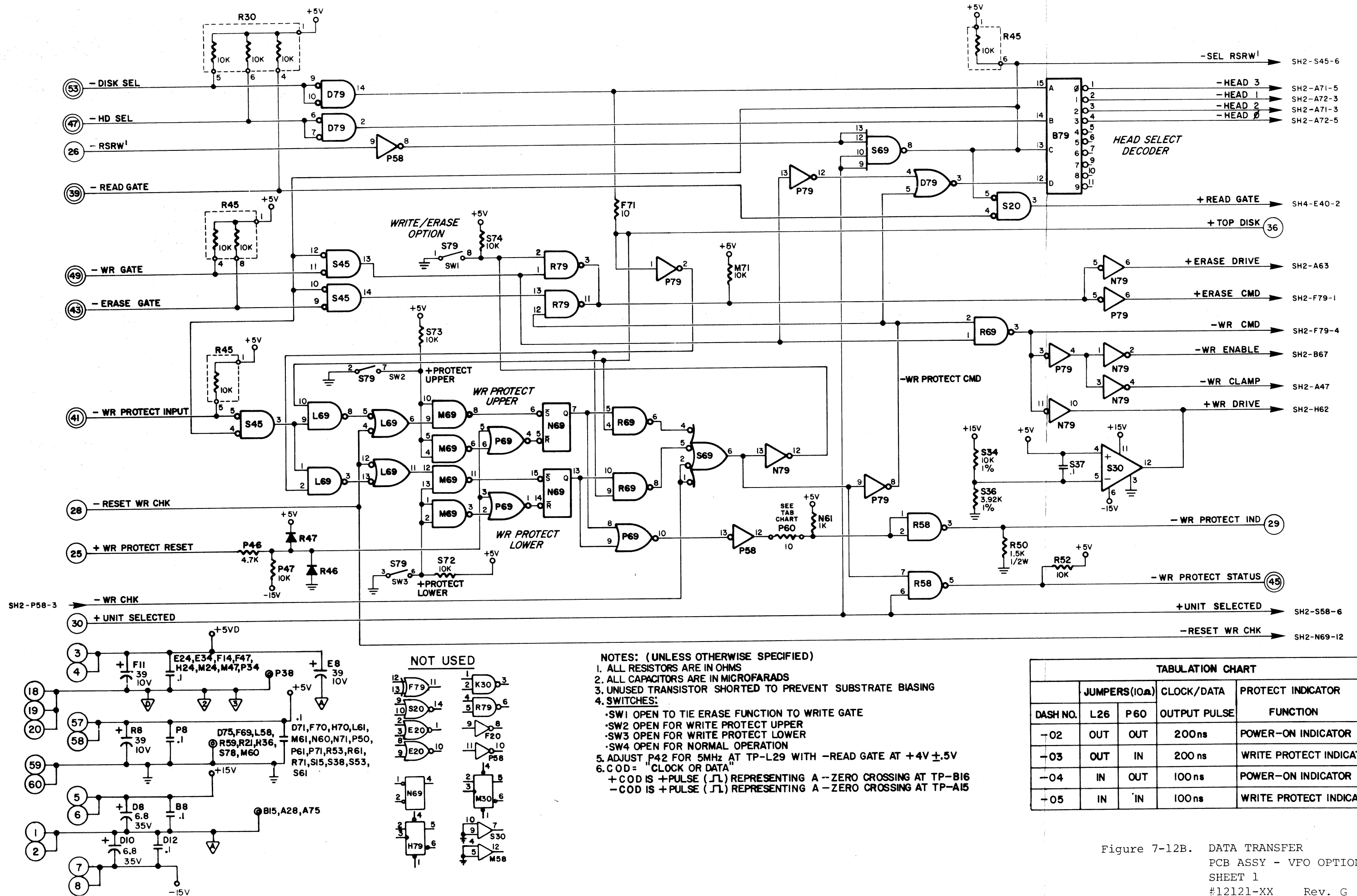


Figure 7-9E. LOGIC PCB ASSY
 SHEET 2
 #12141-XX Rev. F'



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL RESISTORS ARE IN OHMS
2. ALL CAPACITORS ARE IN MICROFARADS
3. UNUSED TRANSISTOR SHORTED TO PREVENT SUBSTRATE BIASING
4. SWITCHES:
 - SW1 OPEN TO TIE ERASE FUNCTION TO WRITE GATE
 - SW2 OPEN FOR WRITE PROTECT UPPER
 - SW3 OPEN FOR WRITE PROTECT LOWER
 - SW4 OPEN FOR NORMAL OPERATION
5. ADJUST P42 FOR 5MHz AT TP-L29 WITH -READ GATE AT +4V ±.5V
6. COD = "CLOCK OR DATA"
 - + COD IS +PULSE (JL) REPRESENTING A -ZERO CROSSING AT TP-B16
 - COD IS +PULSE (JL) REPRESENTING A -ZERO CROSSING AT TP-A15

TABULATION CHART				
DASH NO.	JUMPERS(10a)		CLOCK/DATA OUTPUT PULSE	PROTECT INDICATOR FUNCTION
	L26	P60		
-02	OUT	OUT	200ns	POWER-ON INDICATOR
-03	OUT	IN	200 ns	WRITE PROTECT INDICATOR
-04	IN	OUT	100 ns	POWER-ON INDICATOR
-05	IN	IN	100 ns	WRITE PROTECT INDICATOR

Figure 7-12B. DATA TRANSFER
PCB ASSY - VFO OPTION
SHEET 1
#12121-XX Rev. G

REVISION HISTORY

<u>Rev.</u>	<u>ECO</u>	
A	2539	Initial release of schematic and assembly.
B	2652	Schematic corrected to include capacitor N47 (sheet 4).
B'	2728	Bill of Material correction.
C	2757	Bill of Material correction.
D	2827	Bill of Material change.
E	2873	Following changes allow Model 500 tester to set write protect on lower disk without also causing write check condition. (Sheet 2) 1) Resistor L56 changes from 7.5K to 6.8K. 2) Capacitor S10 changes from .0022 mFd to .0033 mFd. 3) Resistor S11 changes from 75K to 47K.
F	2928	Resistor E47 changed from 3.9K to 3.3K to accomodate manufacturing board test. (Sheet 4)
G	2978	Following changes improve VFO lock-in characteristics to increase acceptance rate during production testing. (Sheet 4) 1) Capacitor K42 removed; was 390 pF. 2) Capacitor K41 changed from .033 mFd to .082 mFd. 3) Resistor K39 changed from 330 ohms to 82 ohms. 4) Capacitor N47 changed from 330 pF to 100 pF.

COMPONENT TYPES

Diode, Signal, IN4454	A20, A21, A51, A54, A57, A60, A74, B62, B63, B64, B65, B69, D26, D27, D47, D48, D50, D52, D53, D55, D56, D58, D59, D61, E52, E53, E54, E55, K53, K64, K66, R46, R47, S13, N48
Diode, Zener, IN5231, 5.1V, 2%	E60
Transistor, 2N3725	F53, F58, F62
Transistor, NPN, 2N3904	A69, B21, B22, B42, B43, D63, E64, F55, H55, K58, L36, L46
Transistor, PNP, 2N3906	A29, A30, A52, A55, A58, A61, A64, B25, B26, B44, B45, B48, B49, E68, H62, H65, K36, K46, K57
Resistor Network, 1K, 2K	A71, A72
Resistor Network, 10K	R30, R45
IC, LM319	M58, S30
Transistor Array, 3146	B19, B34
IC, 7400	E30, K30, M20
IC, 74LS00	L69, M69, R69, H20
IC, 7402	E20
IC, 74LS02	N30, P69
IC, 7404	F20
IC, 74LS04	P58, P79
IC, 7406	N79
IC, 74LS20	S69
IC, 74LS26	R79
IC, 7445	B79
IC, 7474	L20, M30, N20, P30
IC, 74LS74	F30, H30, H79
IC, 74LS86	F79
IC, 74S124	N45
IC, 74157	K20
IC, 74LS161	P20, R20
IC, 74LS221	E40
IC, 74LS279	N69
IC, 75452	R58, S58
IC, 8836	D79, S20, S45

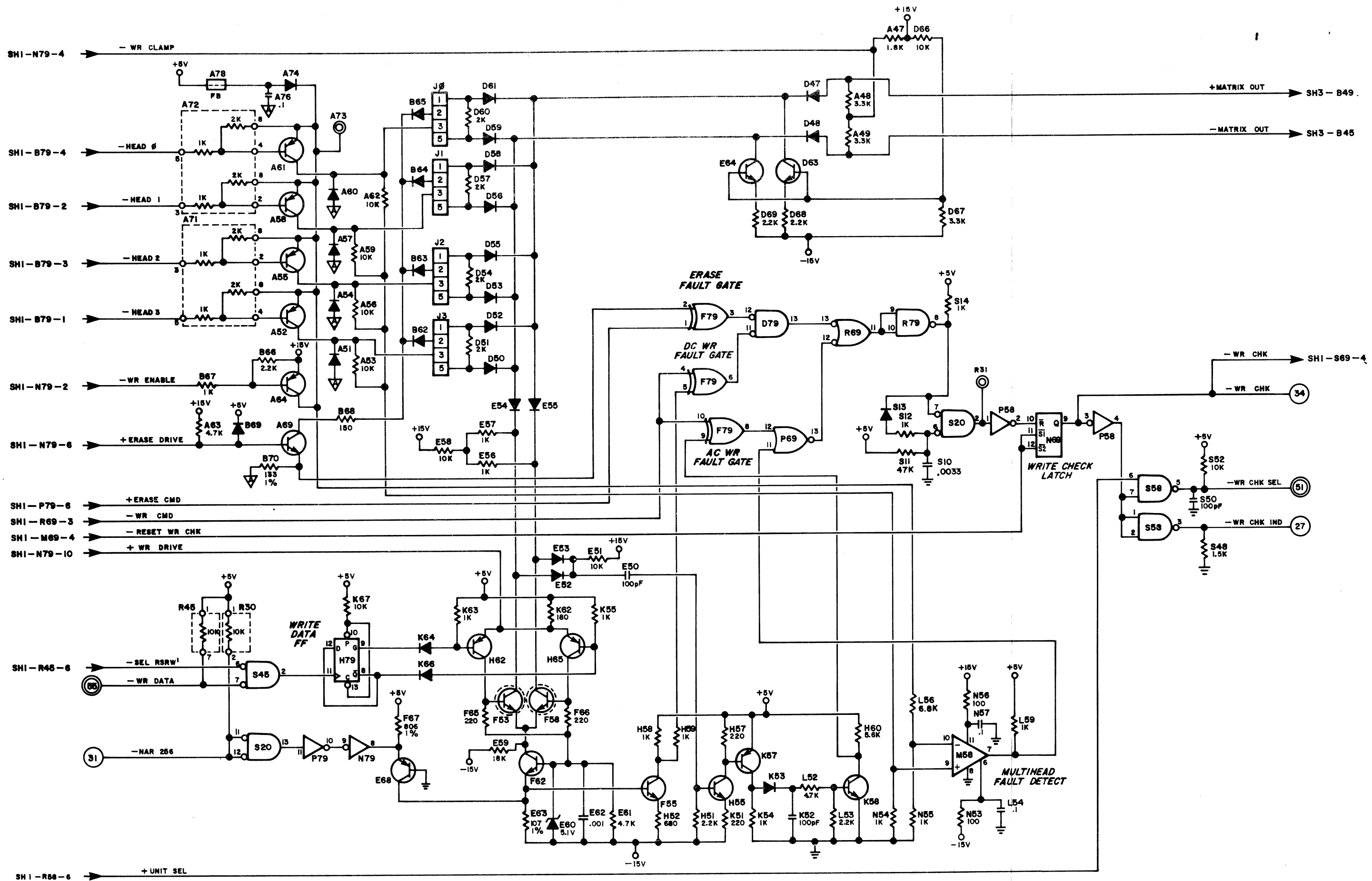


Figure 7-13B. DATA TRANSFER
PCB ASSY - VFO OPTION
SHEET 2
#12121-XX Rev. G

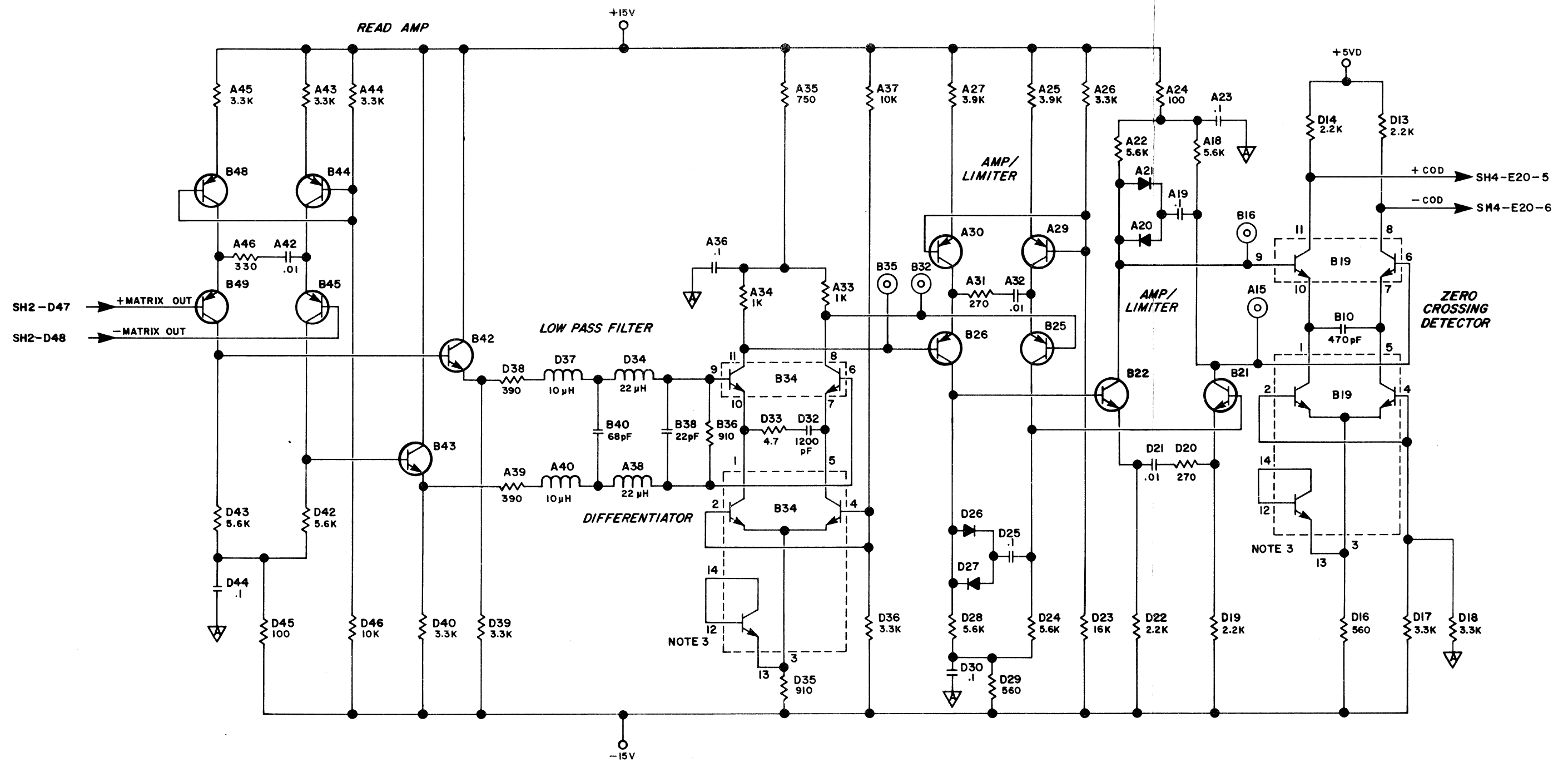


Figure 7-14B. DATA TRANSFER
PCB ASSY - VFO OPTION
SHEET 3
#12121-XX Rev. G

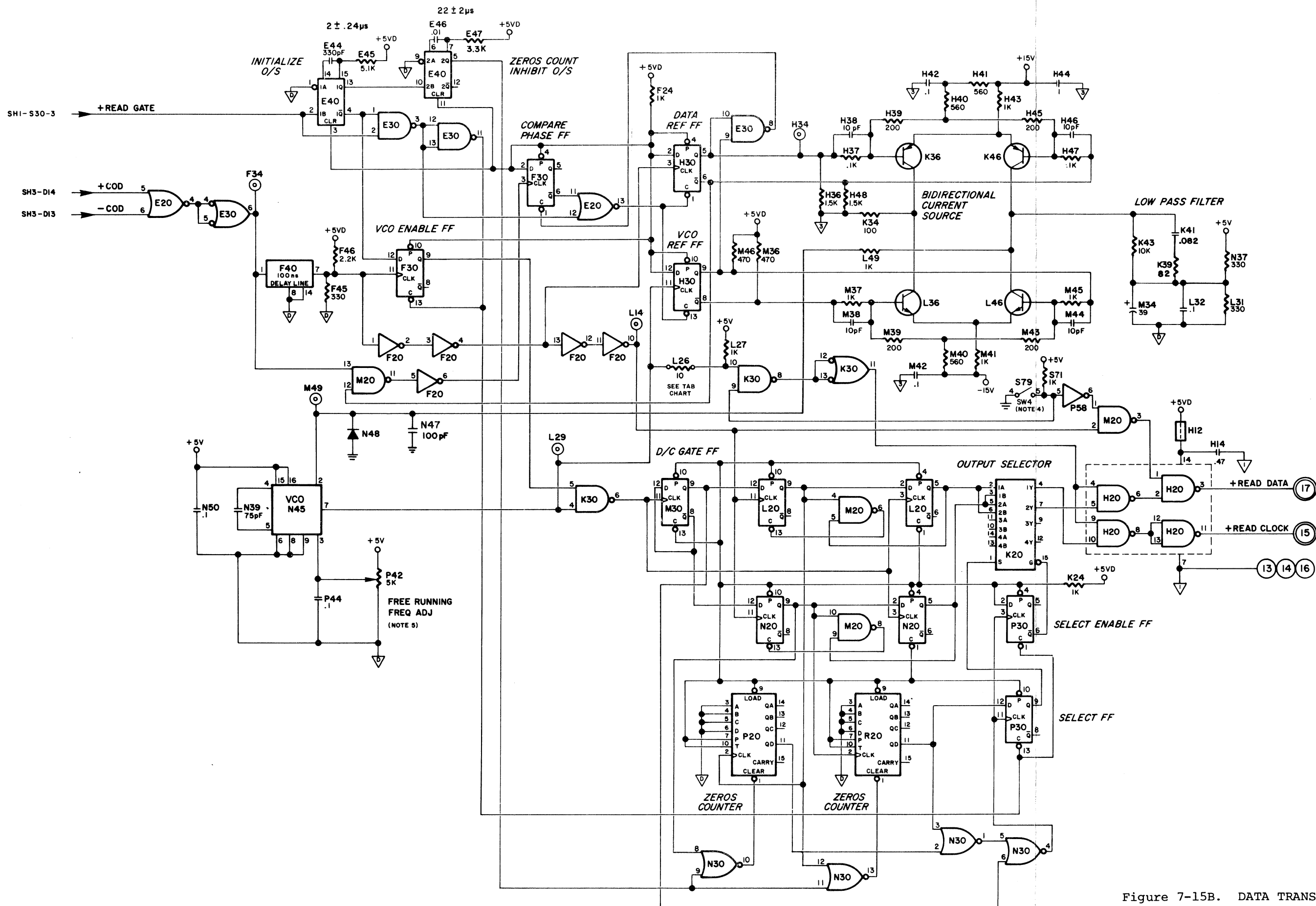


Figure 7-15B. DATA TRANSFER
PCB ASSY - VFO OPTION
SHEET 4
#12121-XX Rev. G