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NEC INFORMATION SYSTEMS, INC. WINCHESTER DISK DRIVE MAINTENANCE GUIDE

Model: D2257

Customer Engineering Reprint
Product Maintenance Manual

729-1503

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PREFACE

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the D2257 Winchester Disk Drive.

First Edition (May 1984)

This edition is the first reprint of NEC Information Systems, Inc. maintenance guide for the D2257 Winchester Disk Drive. The material in this document may only be used for the purpose stated in the Preface. Updates and/or changes to this document will be published as Publication Update Bulletins (PUB's) or subsequent editions.

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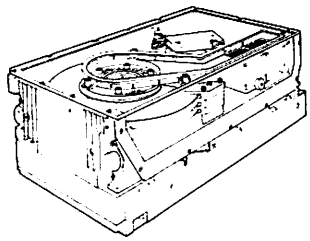


The D2257 and D2247E disk drives are the newest models in the NEC D2200 series. They are compact, highly reliable, low-cost disk drives fully compatible with earlier D2200 models. They offer up to 167.7 megabytes (MB) of unformatted data storage on 8-inch platters. Actual storage capacity depends upon the model and formatting method used.

1.1 D22x7 SYSTEM DESIGN

Both models use fixed-disk, Winchester-type technology, which provides the most advanced method of storing and retrieving large amounts of data. Each 22x7 disk drive contains a number of 8-inch platters (see Table 1-1) sealed within a protective, air-tight enclosure. This enclosure protects the recording platters from atmospheric dust and dirt to improve operational reliability. A spindle, a drive motor, a rotary actuator assembly, and movable read/ write heads are also contained within the enclosure.

Table 1-1 D22x7 Disk Drive Storage Capacity

MODEL	UNFORMATTED CAPACITY (MB)	NUMBER OF 8-INCH DISK PLATTERS	NUMBER OF MOVABLE R/W HEADS
D2257	167.7	5	8
D2247E	103.2	3	5

Both the D2257 and the D2247E are equipped with standard features which simplify installation and integration into an existing system. Installation in a rack or cabinet is easily accomplished with the mounting frame bracket that allows the drive to be installed in either a horizontal or vertical position.

System integration is simplified by signal line terminators and by Sector and Index signals in the B cable. Switch-selectable sector length and address mark detect functions configure the D22x7 drives for virtually any system.

NEC's large scale integrated circuits (LSIs) protect even the weakest signals from noise and insure high operational reliability. D22x7 drives require no scheduled maintenance and are adjustment-free. As a result, customer maintenance costs are low, while satisfaction is high.

Figure 1-1 shows the major components of the D22x7 series.

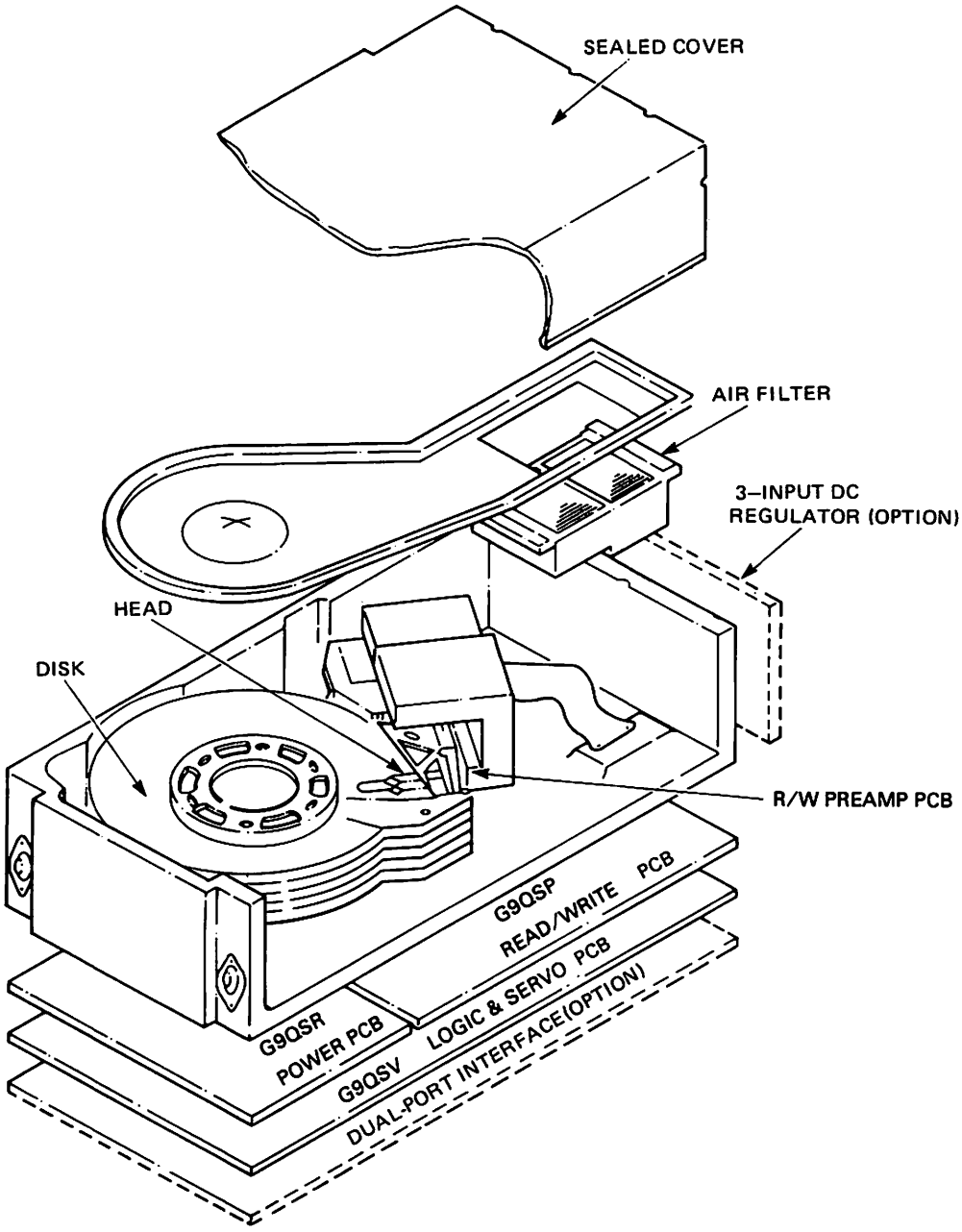


Figure 1-1 Major Components of the D22x7 Series Disk Drives

Figures 1-2 and 1-3 show the arrangement of recording platters and read/write heads within the D2257 and D2247E disk drives.

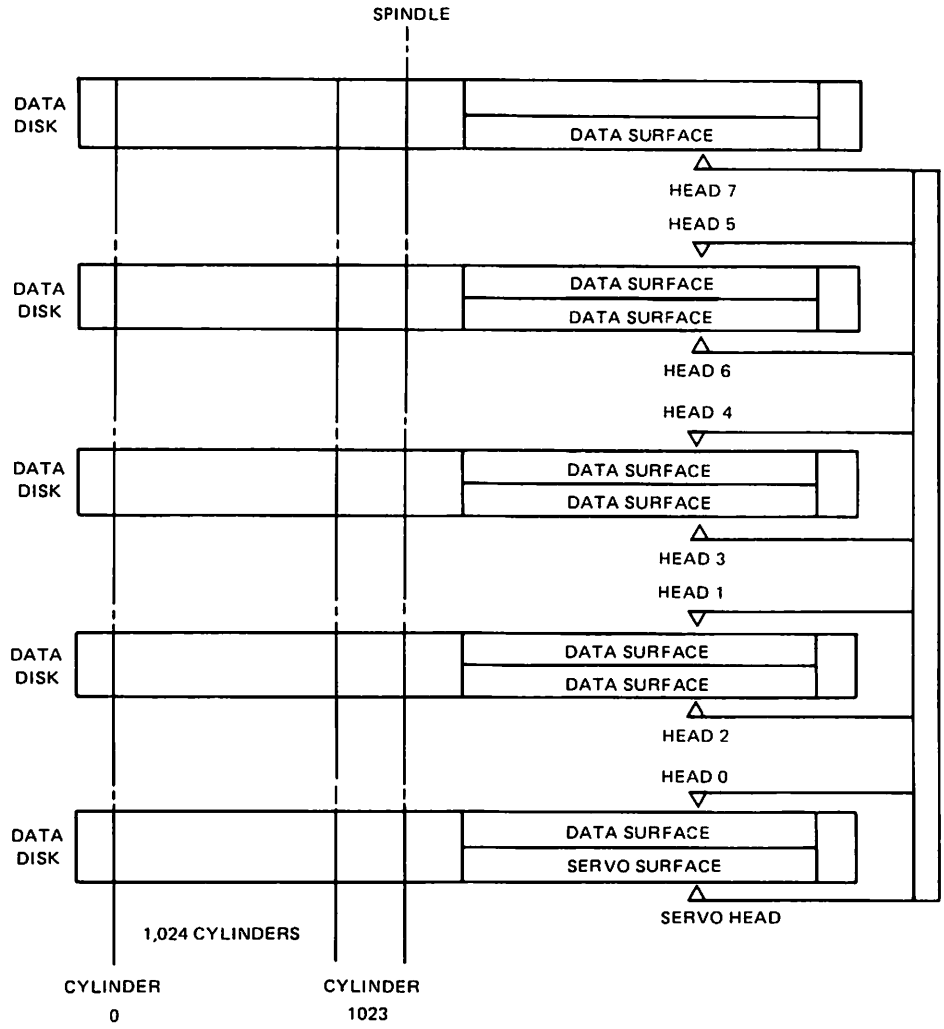


Figure 1-2 D2257 Disk Arrangement

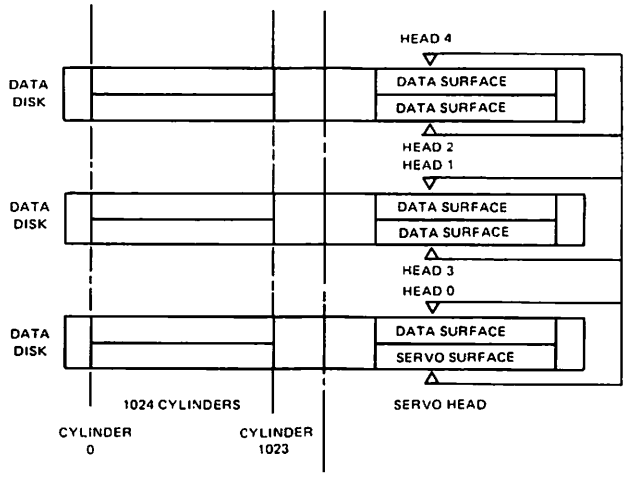


Figure 1-3 D2247E Disk Arrangement

The servo disk surface is shown in Figure 1-4.

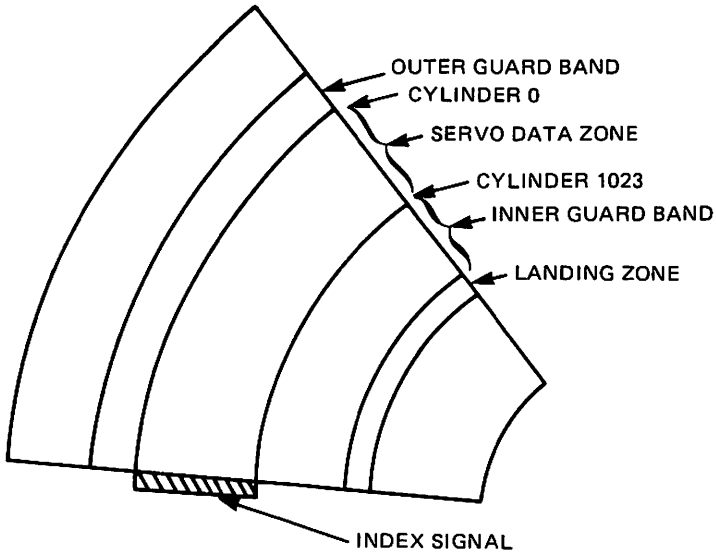


Figure 1-4 Servo Disk Surface

The Index signal is a six-bit pattern written along one radius of the servo surface. It identifies the beginning of a recording track. The index pattern repeats each time the radius intersects one of the recording tracks.

The servo data zone contains 1024 concentric recording tracks. Each recording track contains prerecorded positioning data, including clock and synchronization signals, that provides the necessary information to place and maintain the read/ write heads on track.

The inner and outer guard bands bracket the servo data zone. They contain six-bit patterns that distinguish them from the servo data zone. These patterns recur every 320 bytes. Table 1-2 lists the bit patterns used on the servo surface.

Table 1-2 Servo Surface Bit Patterns

SIGNAL	BIT PATTERN
Index	0 1 1 0 1 0
Inner Guard Band	0 1 1 0 0 1
Outer Guard Band	0 1 1 1 0 0

The landing zone is a silicon-coated surface where the read/write heads rest when the recording disks are not spinning. During read, write, and seek operations the heads "float" approximately 20 microinches above the surface of the disk, supported by a cushion of air.

1.2 DISK CIRCUITRY

A block diagram of a D22x7 disk drive is shown in Figure 1-5. The functional components consist of the interface, the read/write circuits, the servo control, and the motor control circuits.

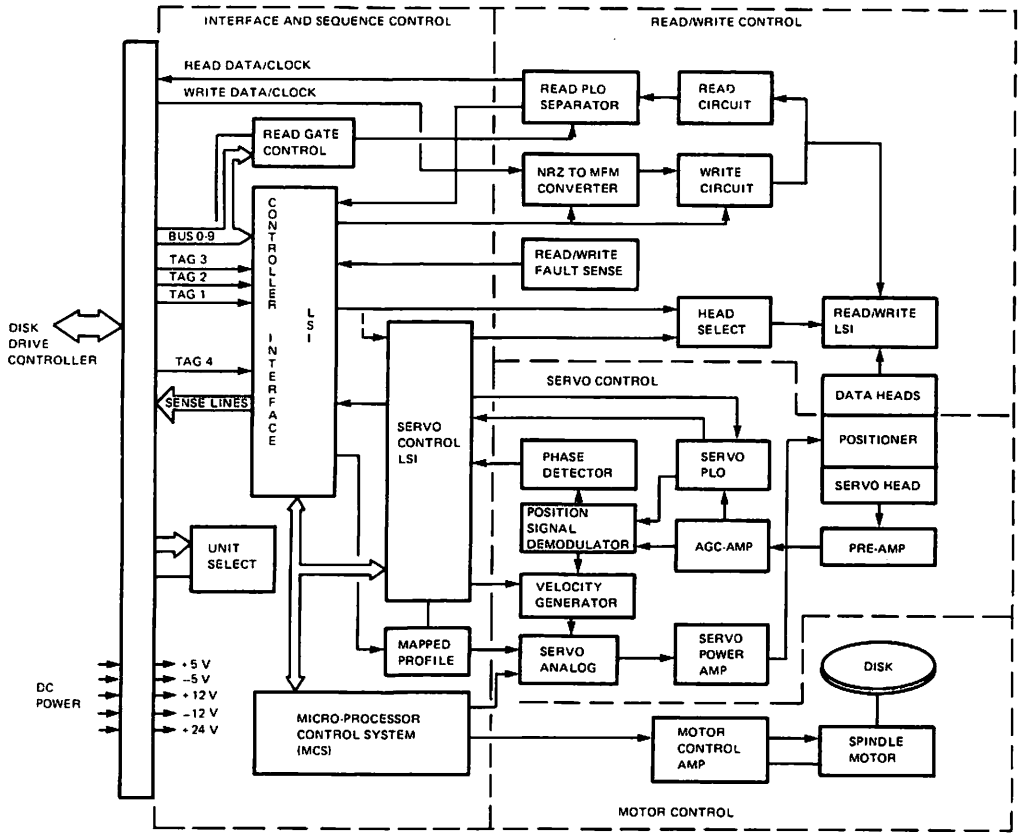


Figure 1-5 D22x7 Functional Block Diagram

The interface routes data, addresses, status information, and control signals between the disk drive and the controller.

The read/write circuits control the transfer of data from the disk (read operation), and to the disk (write operation). During a write operation, the circuits receive serial nonreturn-to-zero (NRZ) format data from the controller and convert the data to a modified frequency modulation (MFM) format. The MFM data is then written on the disk. During a read operation, the circuits read and amplify the data from the disk, convert it from MFM to NRZ format, and send the NRZ data serially to the controller.

The servo control reads the data prerecorded on the servo disk. The servo control uses this data to position and maintain the read/write heads on the correct cylinder.

The motor control circuits drive the spindle motor.

1.3 POWER REQUIREMENTS

D22x7 disk drives operate on externally supplied dc power. DC power requirements are listed in Table 1-3.

Table 1-3 DC Power Requirements

REQUIRED VOLTAGE	TOLERANCE	DAMAGE THRESHOLD	CURRENT	RIPPLE (PEAK TO PEAK)
+5.0 V	±0.25 V	±25%	4.0 A	100 mV
-5.0 V	±0.25 V	±25%	0.5 A	100 mV
+12.0 V	±0.60 V	±25%	0.6 A	100 mV
-12.0 V	±0.60 V	±25%	0.5 A	100 mV
+24.0 V	±2.40 V	±25%	2.7 A* 5.0 A**	240 mV

*2.7 A — average running current
**5.0 A — peak starting current (25 seconds maximum duration)

All power line voltages must be established within 500 milliseconds (ms) of power on. When power is turned on, voltages must be enabled in the following order: +5V, -5V, ±12V, +24V. When power is turned off, lines must be disabled in the reverse order: +24V, ±12V, -5V, +5V.

1.4 FEATURES

Shorter access times, high-speed data transfers, and mechanical reliability are required for efficient computer network operations. To meet these demands the NEC D22x7 disk drives offer the following features.

1.4.1 Enhanced Seek Time

Seek time is the time required to find requested data on the disk. Both D22x7 models have an average seek time of 20 milliseconds (ms), and a maximum seek time of 40 ms.

1.4.2 Rapid Data Transfer Rate

Both the D2257 and the D2247E offer a data transfer rate of approximately 1.2 MB per second.

1.4.3 Compact Mounting

The D22x7's compact size allows for either horizontal or vertical mounting in a limited space. The drive's lock mechanism is easily accessible even after the drive has been placed within a system cabinet.

D22x7 drives also feature an integrated cooling fan that reduces space and power requirements.

1.4.4 Simplified Maintenance

The air-tight, sealed disk/head assembly and the D22x7's simplified design produce a disk drive that requires no periodic maintenance. Servo circuits are maintenance-free and require no adjustment. Neither installation nor field service requires special tools. Motor electronics are placed outside the head/disk assembly and do not need "clean room" repair facilities.

An optional diagnostic panel is available for test and maintenance purposes (see Appendix C).

1.4.5 Design Reliability

D22x7 disk drives use lightweight, contact-type start/stop heads that eliminate damage to the heads and disk. A simplified rotary actuator, a directly coupled, brushless dc motor, and a closed-loop air circulation system are the system's major mechanical components. The control logic is microprocessor controlled and designed to minimize electronic components. This design strategy ensures high reliability and low cost.

1.4.6 Standard Interfaces

Both the D2257 and the D2247E use the same standard original equipment manufacturer interfaces for connection to a disk controller and to a power supply.

1.4.7 Safety

D22x7 models conform to Underwriter's Laboratories Safety Regulation UL478.

1.4.8 System Configuration Flexibility

One to sixteen D22x7 disk drives can be connected to a single controller in either a daisy-chain or radial system (see Figures 1-6 and 1-7).

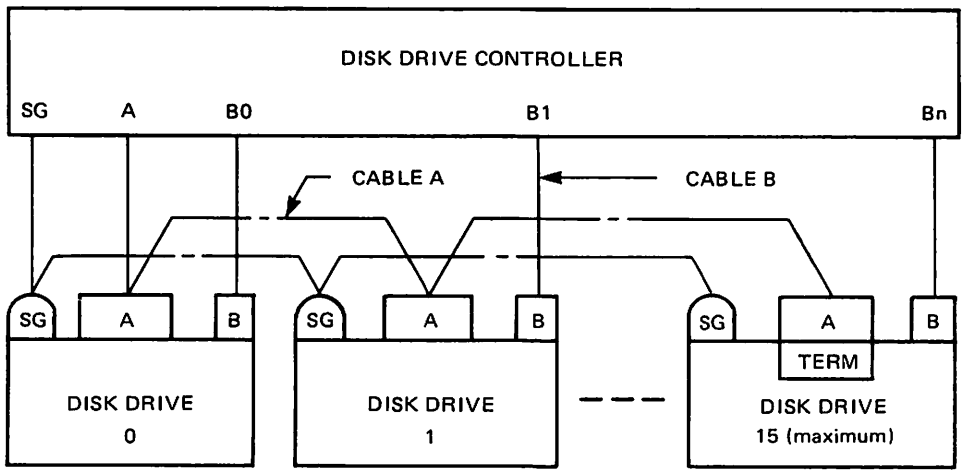


Figure 1-6 Daisy-Chain System Configuration

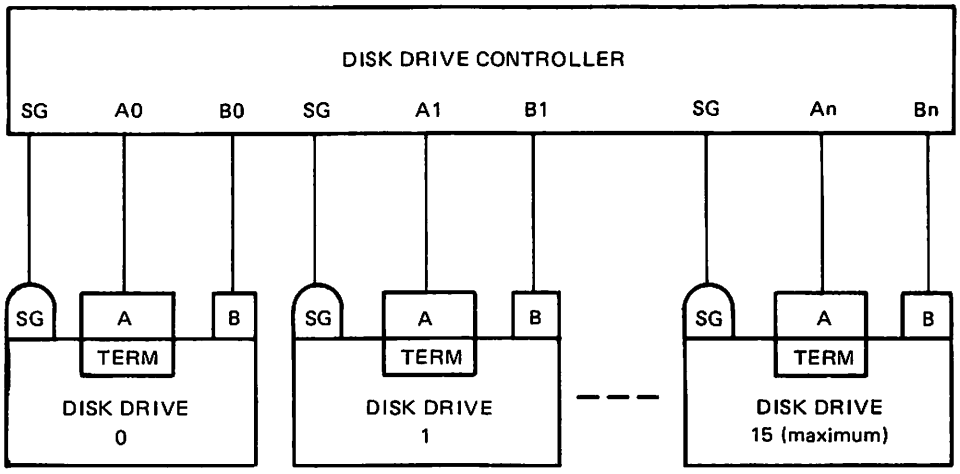


Figure 1-7 Radial System Configuration

1.5 RELATED DOCUMENT

For additional information on D22x7 disk drives, refer to the *D22x7 Series 8-Inch Winchester Disk Drive Product Description* (NEC document number 819-000080-7001).

1.6 SPECIFICATIONS

D22x7 specifications are listed in Appendix B.

1.7 OPTIONS

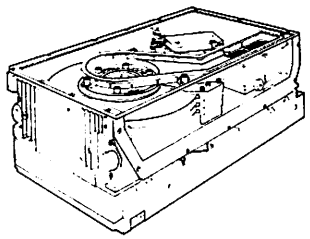
Table 1-4 lists available options for D22x7 disk drives.

Table 1-4 Available Options

OPTION	DESCRIPTION
3-Input DC Regulator Option	Supplies internal dc "power set" (+24V, +12V, +5V, -5V, -12V) by converting external dc input of +24V, +5V, and -12V.
Dual-Port Option	Enables a D22x7 drive to interface with two controllers.
DC Power Supply	Supplies internal dc "power set" (+24V, +12V, +5V, -5V, -12V) from ac input power. The unit provides power for two disk drives.
Diagnostic Panel	Maintenance tool for monitoring and testing disk drive operation.

Chapter 2

Installation Procedures



This chapter provides the recommended procedures for installing a D22x7 disk drive. When preparing the installation site, refer to the environmental specifications listed in Appendix B.

2.1 UNPACKING/REPACKING

Before unpacking the disk drive, examine the shipping carton for damage. If damage has occurred, notify the carrier immediately. Do not open the carton until the carrier's representative is present.

If there is no damage to the shipping carton, use these procedures to unpack the disk drive. Failure to follow these procedures can void the product warranty.

1. Open the top of the shipping carton.
2. Remove the top packing cushion (see Figure 2-1).
3. Carefully remove the disk drive from the shipping carton.
4. Remove the plastic shipping bag from the disk drive.
5. Save all packing material for reshipping.
6. Check all items against the bill of material to insure that no items are missing.
7. Check all items for shipping damage.

To repack the disk drive, reverse these procedures.

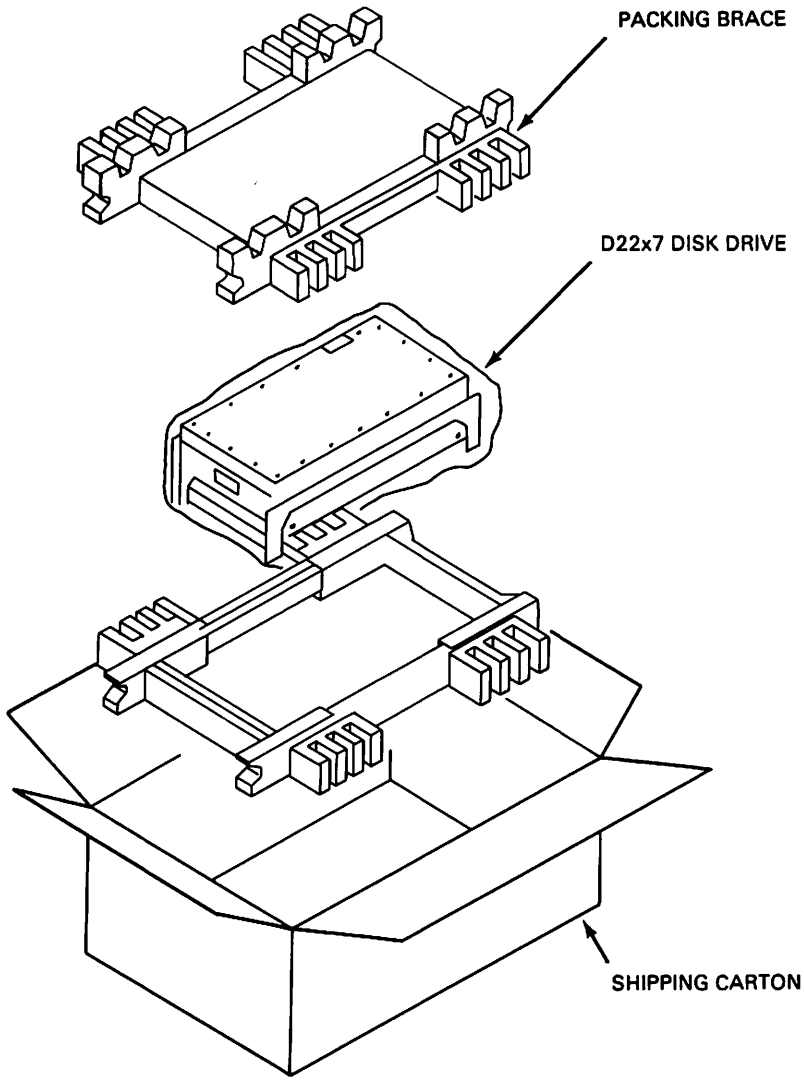


Figure 2-1 D22x7 Packaging

2.2 TERMINATING RESISTORS

Each D22x7 disk drive is shipped with four 56 Ω terminating resistors installed on the G9QSV logic and servo printed circuit board (PCB) as shown in Figure 2-2.

If the D22x7 drive is connected to the controller in a radial configuration, leave these four resistors in place. If a daisy-chain configuration is used, remove these resistors from all except the last drive in the chain (see Figure 2-3).

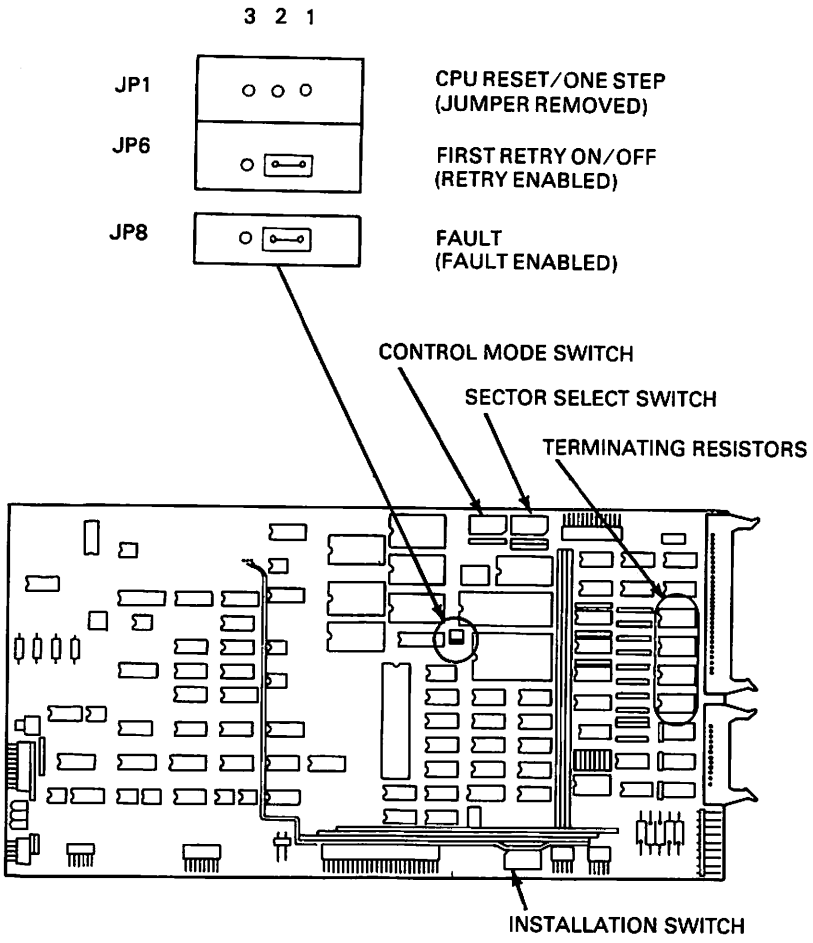


Figure 2-2 G9QSV Logic and Servo PCB

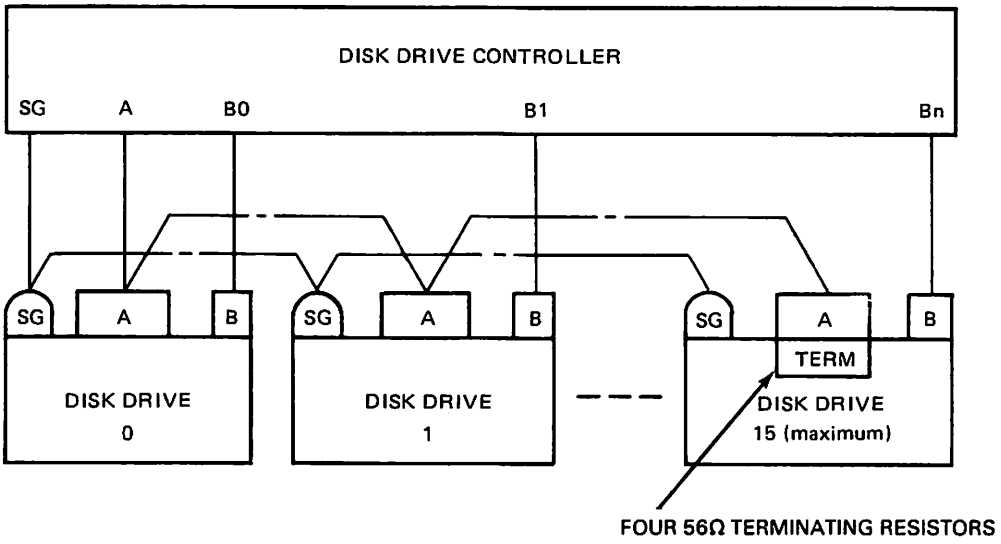


Figure 2-3 Daisy-Chain Terminating Resistors

2.3 JUMPER REQUIREMENTS

Three jumper settings must be verified before power is applied to the disk drive. The location of these three jumpers (JP1, JP6, and JP8) on the G9QSV PCB is shown in Figure 2-2. Insure that settings match those shown in Figure 2-2.

CAUTION

Do not alter these jumper settings. They are intended for factory adjustments only.

2.4 SWITCH SETTINGS

Three eight-segment, dual-inline-packaged (DIP) switch assemblies on the G9QSV logic and servo PCB configure the D22x7 to communicate with the controller and set the sector count. DIP switch assembly locations are shown in Figure 2-4.

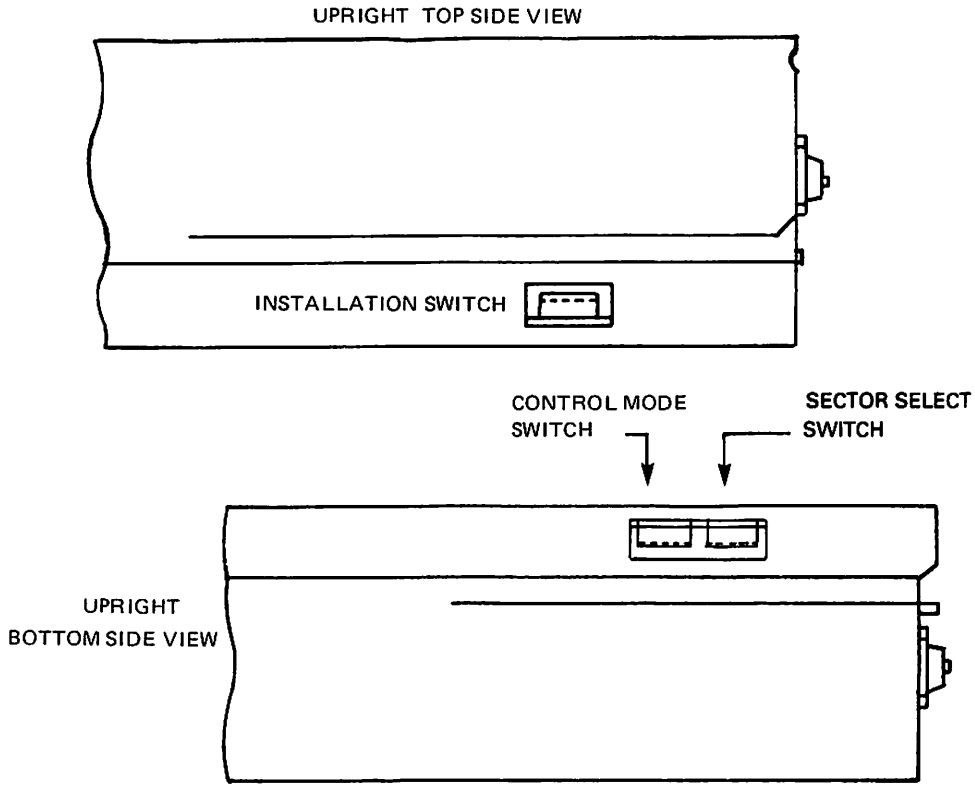


Figure 2-4 DIP Switch Locations on D22x7 Drives

2.4.1 Installation Switch Assembly

The installation switch assembly, shown in Figure 2-5, sets the device address and controls the power-on sequence.

Segments 1, 2, 3, and 4 assign the device address, a hexadecimal number from 0 to F.

Segment 5 determines which of the Unit Select bit lines are used to transmit the device address. For device addresses 0 to 3, set segment 5 to the 0 position; for addresses 4 to F, set segment 5 to the 1 position.

Segment 7 enables a 30-second delay in the start-up time of the spindle motor. This segment can be used in dual-drive configurations to insure that both drives do not overload the power supply by simultaneously activating their power-up sequence.

Segment 8 places the D22x7 in local or remote mode at power-on. Segment 6 of the installation switch assembly is not used.

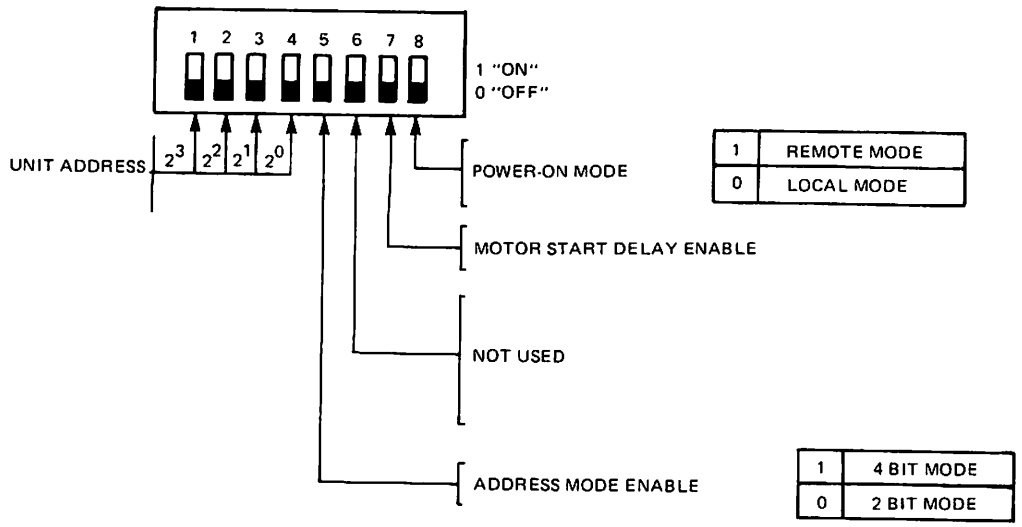


Figure 2-5 Installation DIP Switch

2.4.2 Control Mode Switch Assembly

The control mode switch assembly (shown in Figure 2-6) configures the D22x7 to communicate with the disk controller and enables certain optional drive features.

Segments 1, 2, and 3 are set according to the D22x7 model used.

Segment 4 enables the Address Mark function.

Segment 5 enables the Read Sector function. When segments 5 and 7 of the control mode switch assembly are set to 1, Tag 4 can be used in conjunction with bus bits 8 and 9 to request the current sector address. The D22x7 issues the address across the sense lines.

Segment 6 enables the Format Write Release Option used with some controllers.

Segment 7 enables the Tag 4 line.

Segment 8 enables the controller interface.

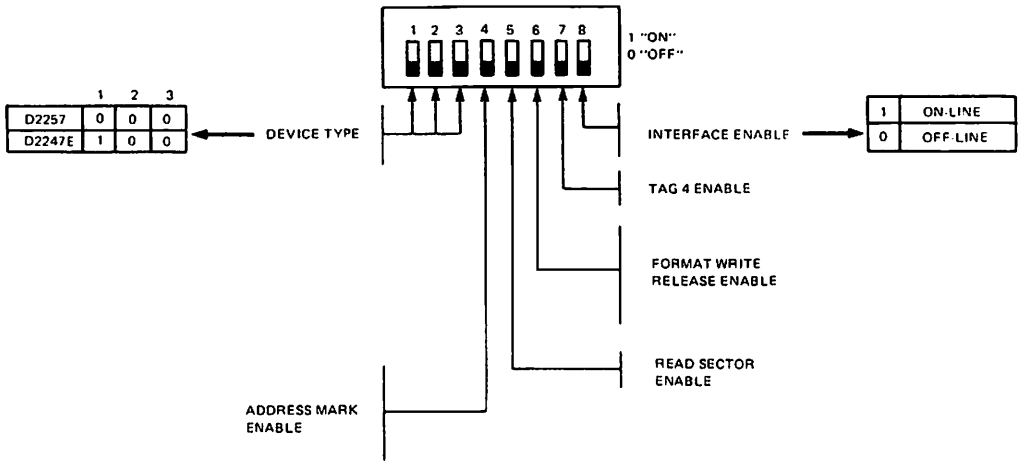


Figure 2-6 Control Mode DIP Switch

2.4.3 Sector Select Switch Assembly

The Sector Select switch sets the number of sectors per track. Any number of sectors from 1 to 128 can be chosen.

Segment 1 of this assembly determines the disposition of odd or remainder bytes. These are extra bytes that must be allocated when the available bytes per track are not evenly divisible by the number of sectors per track. With segment 1 in the 0 position, odd bytes are grouped together in an extra sector at the end of the track. With this segment in the 1 position, the last sector is reduced to account for odd bytes.

Figure 2-7 shows the allocation of 33 sectors using each of these disposition methods.

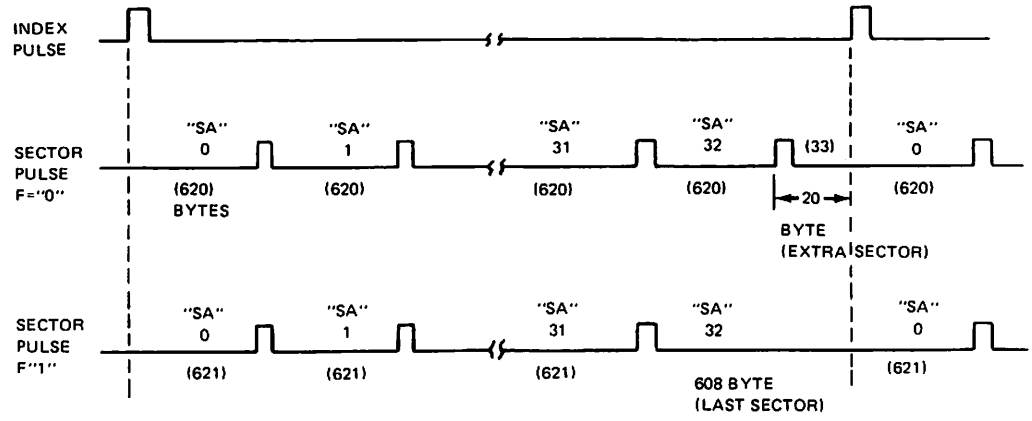
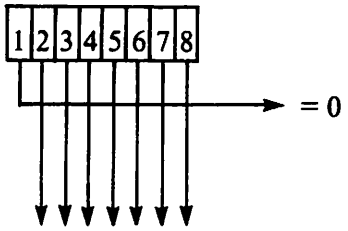


Figure 2-7 Sector Allocation

Tables 2-1 and 2-2 list Sector Select switch settings and the resulting sector allocations for D22x7 drives.

Table 2-1 Sector Selection List (Disposition Switch = 0)

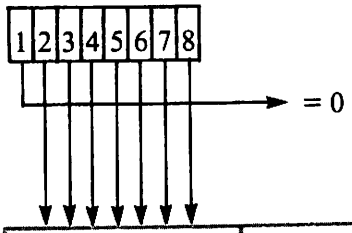
SECTOR SWITCH SETTING



		TRACK = 20,480 BYTES	
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	EXTRA SECTOR BYTES
0 0 0 0 0 0 1	1	20480	0
0 0 0 0 0 1 0	2	10240	0
0 0 0 0 0 1 1	3	6826	2
0 0 0 0 1 0 0	4	5120	0
0 0 0 0 1 0 1	5	4096	0
0 0 0 0 1 1 0	6	3413	2
0 0 0 0 1 1 1	7	2925	5
0 0 0 1 0 0 0	8	2560	0
0 0 0 1 0 0 1	9	2275	5
0 0 0 1 0 1 0	10	2048	0
0 0 0 1 0 1 1	11	1861	9
0 0 0 1 1 0 0	12	1706	8
0 0 0 1 1 0 1	13	1575	5
0 0 0 1 1 1 0	14	1462	12
0 0 0 1 1 1 1	15	1365	5
0 0 1 0 0 0 0	16	1280	0
0 0 1 0 0 0 1	17	1204	12
0 0 1 0 0 1 0	18	1137	14
0 0 1 0 0 1 1	19	1077	17
0 0 1 0 1 0 0	20	1024	0
0 0 1 0 1 0 1	21	975	5
0 0 1 0 1 1 0	22	930	20
0 0 1 0 1 1 1	23	890	10
0 0 1 1 0 0 0	24	853	8
0 0 1 1 0 0 1	25	819	5
0 0 1 1 0 1 0	26	787	18
0 0 1 1 0 1 1	27	758	14
0 0 1 1 1 0 0	28	731	12
0 0 1 1 1 0 1	29	706	6
0 0 1 1 1 1 0	30	682	20

Table 2-1 Sector Selection List (Disposition Switch = 0) (cont'd)

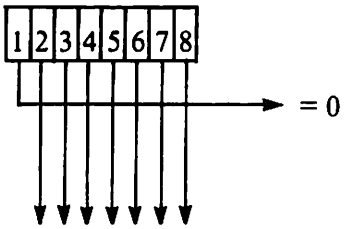
SECTOR SWITCH SETTING



		TRACK = 20,480 BYTES	
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	EXTRA SECTOR BYTES
0 0 1 1 1 1 1	31	660	20
0 1 0 0 0 0 0	32	640	0
0 1 0 0 0 0 1	33	620	20
0 1 0 0 0 1 0	34	602	12
0 1 0 0 0 1 1	35	585	5
0 1 0 0 1 0 0	36	568	32
0 1 0 0 1 0 1	37	553	19
0 1 0 0 1 1 0	38	538	36
0 1 0 0 1 1 1	39	525	5
0 1 0 1 0 0 0	40	512	0
0 1 0 1 0 0 1	41	499	21
0 1 0 1 0 1 0	42	487	26
0 1 0 1 0 1 1	43	476	12
0 1 0 1 1 0 0	44	465	20
0 1 0 1 1 0 1	45	455	5
0 1 0 1 1 1 0	46	445	10
0 1 0 1 1 1 1	47	435	35
0 1 1 0 0 0 0	48	426	32
0 1 1 0 0 0 1	49	417	47
0 1 1 0 0 1 0	50	409	30
0 1 1 0 0 1 1	51	401	29
0 1 1 0 1 0 0	52	393	44
0 1 1 0 1 0 1	53	386	22
0 1 1 0 1 1 0	54	379	14
0 1 1 0 1 1 1	55	372	20
0 1 1 1 0 0 0	56	365	40
0 1 1 1 0 0 1	57	359	17
0 1 1 1 0 1 0	58	353	6
0 1 1 1 0 1 1	59	347	7
0 1 1 1 1 0 0	60	341	20

Table 2-1 Sector Selection List (Disposition Switch = 0) (cont'd)

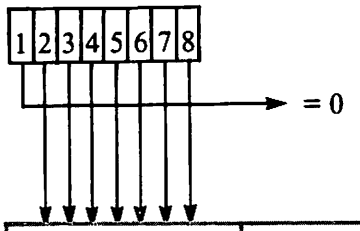
SECTOR SWITCH SETTING



	TRACK = 20,480 BYTES		
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	EXTRA SECTOR BYTES
0 1 1 1 1 0 1	61	335	45
0 1 1 1 1 1 0	62	330	20
0 1 1 1 1 1 1	63	325	5
1 0 0 0 0 0 0	64	320	0
1 0 0 0 0 0 1	65	315	5
1 0 0 0 0 1 0	66	310	20
1 0 0 0 0 1 1	67	305	45
1 0 0 0 1 0 0	68	301	12
1 0 0 0 1 0 1	69	296	56
1 0 0 0 1 1 0	70	292	40
1 0 0 0 1 1 1	71	288	32
1 0 0 1 0 0 0	72	284	32
1 0 0 1 0 0 1	73	280	40
1 0 0 1 0 1 0	74	276	56
1 0 0 1 0 1 1	75	273	5
1 0 0 1 1 0 0	76	269	36
1 0 0 1 1 0 1	77	265	75
1 0 0 1 1 1 0	78	262	44
1 0 0 1 1 1 1	79	259	19
1 0 1 0 0 0 0	80	256	0
1 0 1 0 0 0 1	81	252	68
1 0 1 0 0 1 0	82	249	62
1 0 1 0 0 1 1	83	246	62
1 0 1 0 1 0 0	84	243	68
1 0 1 0 1 0 1	85	240	80
1 0 1 0 1 1 0	86	238	12
1 0 1 0 1 1 1	87	235	35
1 0 1 1 0 0 0	88	232	64
1 0 1 1 0 0 1	89	230	10
1 0 1 1 0 1 0	90	227	50

Table 2-1 Sector Selection List (Disposition Switch = 0) (cont'd)

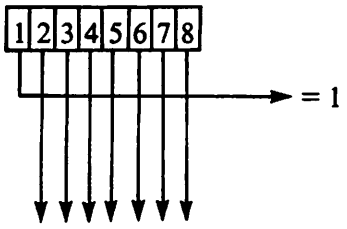
SECTOR SWITCH SETTING



		TRACK = 20,480 BYTES	
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	EXTRA SECTOR BYTES
1 0 1 1 0 1 1	91	225	5
1 0 1 1 1 0 0	92	222	56
1 0 1 1 1 0 1	93	220	20
1 0 1 1 1 1 0	94	217	82
1 0 1 1 1 1 1	95	215	55
1 1 0 0 0 0 0	96	213	32
1 1 0 0 0 0 1	97	211	13
1 1 0 0 0 1 0	98	208	96
1 1 0 0 0 1 1	99	206	86
1 1 0 0 1 0 0	100	204	80
1 1 0 0 1 0 1	101	202	78
1 1 0 0 1 1 0	102	200	80
1 1 0 0 1 1 1	103	198	86
1 1 0 1 0 0 0	104	196	96
1 1 0 1 0 0 1	105	195	5
1 1 0 1 0 1 0	106	193	22
1 1 0 1 0 1 1	107	191	43
1 1 0 1 1 0 0	108	189	68
1 1 0 1 1 0 1	109	187	97
1 1 0 1 1 1 0	110	186	20
1 1 0 1 1 1 1	111	184	56
1 1 1 0 0 0 0	112	182	96
1 1 1 0 0 0 1	113	181	27
1 1 1 0 0 1 0	114	179	74
1 1 1 0 0 1 1	115	179	10
1 1 1 0 1 0 0	116	176	64
1 1 1 0 1 0 1	117	175	5
1 1 1 0 1 1 0	118	173	66
1 1 1 0 1 1 1	119	172	12
1 1 1 1 0 0 0	120	170	80
1 1 1 1 0 0 1	121	169	31
1 1 1 1 0 1 0	122	167	106
1 1 1 1 0 1 1	123	166	62
1 1 1 1 1 0 0	124	165	20
1 1 1 1 1 0 1	125	163	105
1 1 1 1 1 1 0	126	162	68
1 1 1 1 1 1 1	127	161	33
0 0 0 0 0 0 0	128	160	0

Table 2-2 Sector Selection List (Disposition Switch = 1)

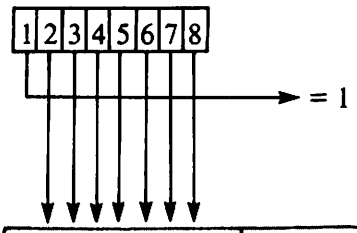
SECTOR SWITCH SETTING



		TRACK = 20,480 BYTES	
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	LAST SECTOR SHORTER
0 0 0 0 0 0 1	1	20480	0
0 0 0 0 0 1 0	2	10240	0
0 0 0 0 0 1 1	3	6827	-1
0 0 0 0 1 0 0	4	5120	0
0 0 0 0 1 0 1	5	4096	0
0 0 0 0 1 1 0	6	3414	-4
0 0 0 0 1 1 1	7	2926	-2
0 0 0 1 0 0 0	8	2560	0
0 0 0 1 0 0 1	9	2276	-4
0 0 0 1 0 1 0	10	2048	0
0 0 0 1 0 1 1	11	1862	-2
0 0 0 1 1 0 0	12	1707	-4
0 0 0 1 1 0 1	13	1576	-8
0 0 0 1 1 1 0	14	1463	-2
0 0 0 1 1 1 1	15	1366	-10
0 0 1 0 0 0 0	16	1280	0
0 0 1 0 0 0 1	17	1205	-5
0 0 1 0 0 1 0	18	1138	-4
0 0 1 0 0 1 1	19	1078	-2
0 0 1 0 1 0 0	20	1024	0
0 0 1 0 1 0 1	21	976	-16
0 0 1 0 1 1 0	22	931	-2
0 0 1 0 1 1 1	23	891	-13
0 0 1 1 0 0 0	24	854	-16
0 0 1 1 0 0 1	25	820	-20
0 0 1 1 0 1 0	26	788	-8
0 0 1 1 0 1 1	27	759	-13
0 0 1 1 1 0 0	28	732	-16
0 0 1 1 1 0 1	29	707	-23
0 0 1 1 1 1 0	30	683	-10

Table 2-2 Sector Selection List (Disposition Switch = 1) (cont'd)

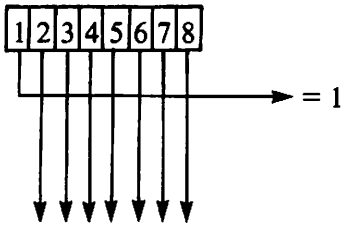
SECTOR SWITCH SETTING



$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	TRACK = 20,480 BYTES: BYTES PER SECTOR	TRACK = 20,480 BYTES: LAST SECTOR SHORTER
0 0 1 1 1 1 1	31	661	-11
0 1 0 0 0 0 0	32	640	0
0 1 0 0 0 0 1	33	621	-13
0 1 0 0 0 1 0	34	603	-22
0 1 0 0 0 1 1	35	586	-30
0 1 0 0 1 0 0	36	569	-4
0 1 0 0 1 0 1	37	554	-18
0 1 0 0 1 1 0	38	539	-2
0 1 0 0 1 1 1	39	526	-34
0 1 0 1 0 0 0	40	512	0
0 1 0 1 0 0 1	41	500	-20
0 1 0 1 0 1 0	42	488	-16
0 1 0 1 0 1 1	43	477	-31
0 1 0 1 1 0 0	44	466	-24
0 1 0 1 1 0 1	45	456	-40
0 1 0 1 1 1 0	46	446	-36
0 1 0 1 1 1 1	47	436	-12
0 1 1 0 0 0 0	48	427	-16
0 1 1 0 0 0 1	49	418	-2
0 1 1 0 0 1 0	50	410	-20
0 1 1 0 0 1 1	51	402	-16
0 1 1 0 1 0 0	52	394	-8
0 1 1 0 1 0 1	53	387	-31
0 1 1 0 1 1 0	54	380	-40
0 1 1 0 1 1 1	55	373	-35
0 1 1 1 0 0 0	56	366	-16
0 1 1 1 0 0 1	57	360	-40
0 1 1 1 0 1 0	58	354	-52
0 1 1 1 0 1 1	59	348	-52
0 1 1 1 1 0 0	60	342	-40

Table 2-2 Sector Selection List (Disposition Switch = 1) (cont'd)

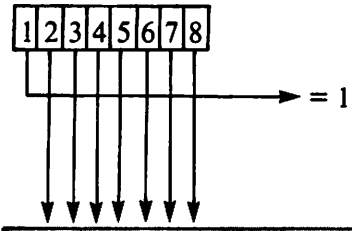
SECTOR SWITCH SETTING



	TRACK = 20,480 BYTES		
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	LAST SECTOR SHORTER
0 1 1 1 1 0 1	61	336	-16
0 1 1 1 1 1 0	62	331	-42
0 1 1 1 1 1 1	63	326	-58
1 0 0 0 0 0 0	64	320	0
1 0 0 0 0 0 1	65	316	-60
1 0 0 0 0 1 0	66	311	-46
1 0 0 0 0 1 1	67	306	-22
1 0 0 0 1 0 0	68	302	-56
1 0 0 0 1 0 1	69	297	-13
1 0 0 0 1 1 0	70	293	-30
1 0 0 0 1 1 1	71	289	-39
1 0 0 1 0 0 0	72	285	-40
1 0 0 1 0 0 1	73	281	-33
1 0 0 1 0 1 0	74	277	-18
1 0 0 1 0 1 1	75	274	-70
1 0 0 1 1 0 0	76	270	-40
1 0 0 1 1 0 1	77	266	-2
1 0 0 1 1 1 0	78	263	-34
1 0 0 1 1 1 1	79	260	-60
1 0 1 0 0 0 0	80	256	0
1 0 1 0 0 0 1	81	253	-13
1 0 1 0 0 1 0	82	250	-20
1 0 1 0 0 1 1	83	247	-21
1 0 1 0 1 0 0	84	244	-16
1 0 1 0 1 0 1	85	241	-5
1 0 1 0 1 1 0	86	239	-74
1 0 1 0 1 1 1	87	236	-52
1 0 1 1 0 0 0	88	233	-24
1 0 1 1 0 0 1	89	231	-79
1 0 1 1 0 1 0	90	228	-40

Table 2-2 Sector Selection List (Disposition Switch = 1) (cont'd)

SECTOR SWITCH SETTING



		TRACK = 20,480 BYTES	
$2^6 2^5 2^4 2^3 2^2 2^1 2^0$	SECTORS PER TRACK	BYTES PER SECTOR	LAST SECTOR SHORTER
1 0 1 1 0 1 1	91	226	-86
1 0 1 1 1 0 0	92	223	-36
1 0 1 1 1 0 1	93	221	-73
1 0 1 1 1 1 0	94	218	-12
1 0 1 1 1 1 1	95	216	-40
1 1 0 0 0 0 0	96	214	-64
1 1 0 0 0 0 1	97	212	-84
1 1 0 0 0 1 0	98	209	-2
1 1 0 0 0 1 1	99	207	-13
1 1 0 0 1 0 0	100	205	-20
1 1 0 0 1 0 1	101	203	-23
1 1 0 0 1 1 0	102	201	-22
1 1 0 0 1 1 1	103	199	-17
1 1 0 1 0 0 0	104	197	-8
1 1 0 1 0 0 1	105	196	-100
1 1 0 1 0 1 0	106	194	-84
1 1 0 1 0 1 1	107	192	-64
1 1 0 1 1 0 0	108	190	-40
1 1 0 1 1 0 1	109	188	-12
1 1 0 1 1 1 0	110	187	-90
1 1 0 1 1 1 1	111	185	-55
1 1 1 0 0 0 0	112	183	-16
1 1 1 0 0 0 1	113	182	-86
1 1 1 0 0 1 0	114	180	-40
1 1 1 0 0 1 1	115	179	-105
1 1 1 0 1 0 0	116	177	-52
1 1 1 0 1 0 1	117	176	-112
1 1 1 0 1 1 0	118	174	-52
1 1 1 0 1 1 1	119	173	-107
1 1 1 1 0 0 0	120	171	-40
1 1 1 1 0 0 1	121	170	-90
1 1 1 1 0 1 0	122	168	-16
1 1 1 1 0 1 1	123	167	-61
1 1 1 1 1 0 0	124	166	-104
1 1 1 1 1 0 1	125	164	-20
1 1 1 1 1 1 0	126	163	-58
1 1 1 1 1 1 1	127	162	-94
0 0 0 0 0 0 0	128	160	0

2.5 CABINET/RACK INSTALLATION

The mounting bracket (see Figure 2-8) shipped with the D22x7 secures the disk drive when it is installed in a cabinet or rack.

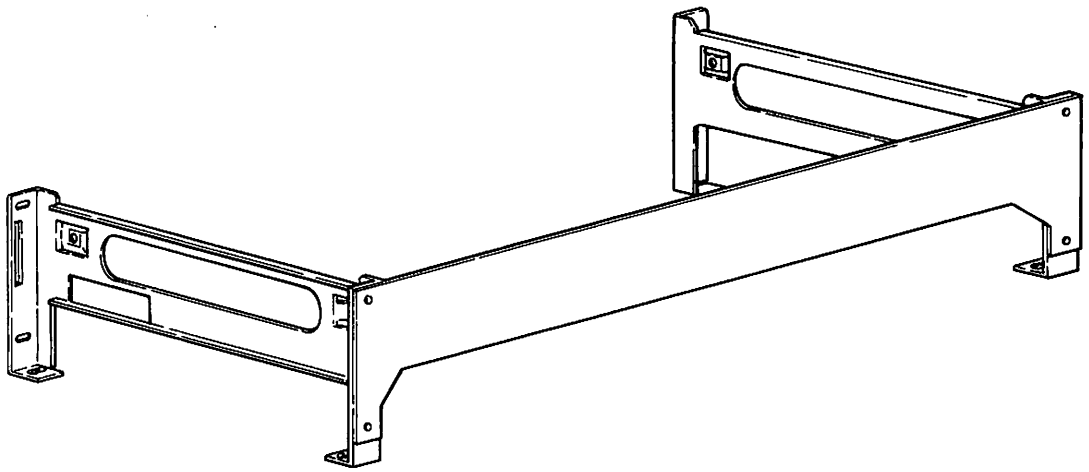


Figure 2-8 Mounting Bracket

The drive can be installed in either a horizontal or vertical position as shown in Figure 2-9. Figure 2-9 also shows the required ventilation for each mounting position. An air flow of 1.1 cubic yards per minute (1.1 yd^3/min) is required on a 0.4-inch surface.

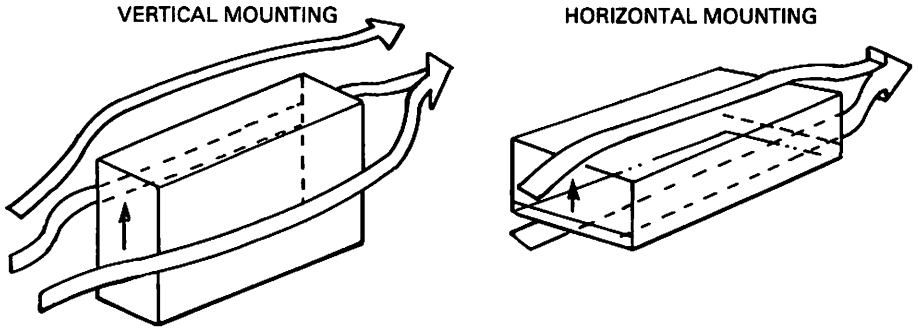


Figure 2-9 Vertical and Horizontal Installation

When installing the disk drive, first verify that the mounting holes in the rack or cabinet align with the holes in the mounting bracket. Refer to Appendix B for information on unit dimensions.

2.6 CABLE CONNECTIONS

This section describes the different connectors for the interface signal cables (cables A and B), for the system ground cable, and for the power cable.

2.6.1 Interface Cables

Interface cables A and B are connected to the G9QSV PCB as shown in Figure 2-10.

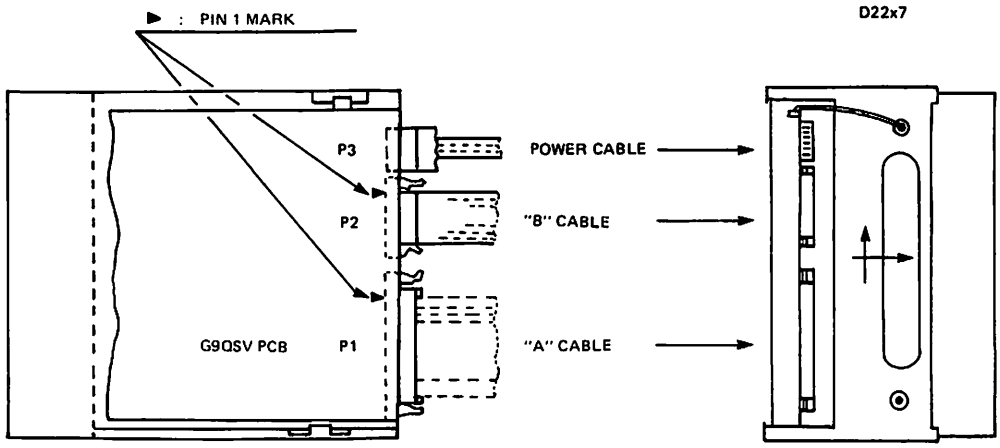


Figure 2-10 Interface Cable Connections

Cable B should not exceed 49.2 ft (15 m) in length. Cable A should not exceed 98.4 ft (30 m) in length. In a daisy chain configuration, the total length of cable A (from the first to the last drive) should not exceed 98.4 ft (see Figure 2-11).

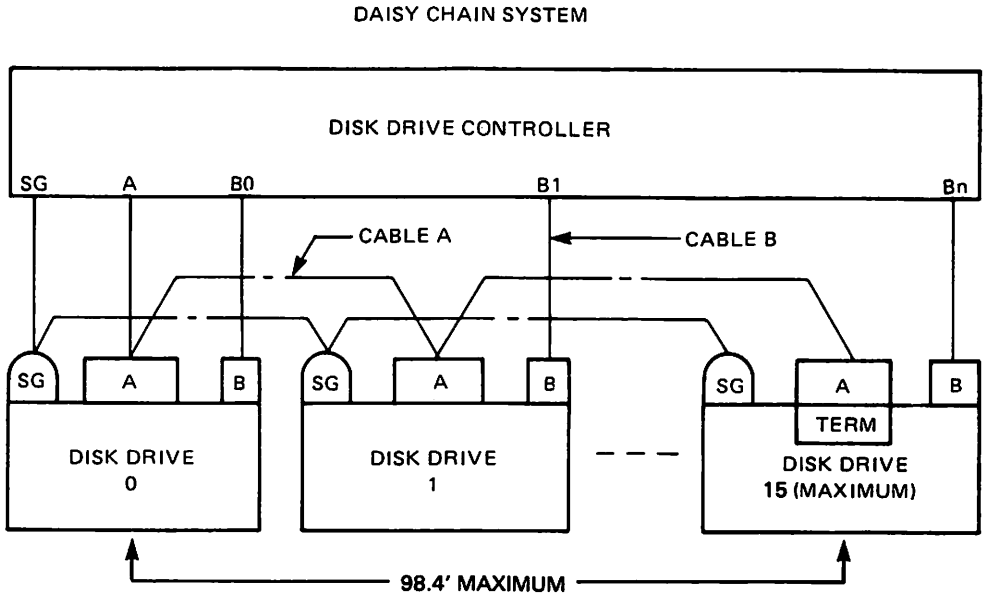


Figure 2-11 Daisy-Chain Cabling

2.6.2 System Ground Cable

Connect a system ground cable to the Signal Ground terminal at the rear of the disk drive (see Figure 2-12).

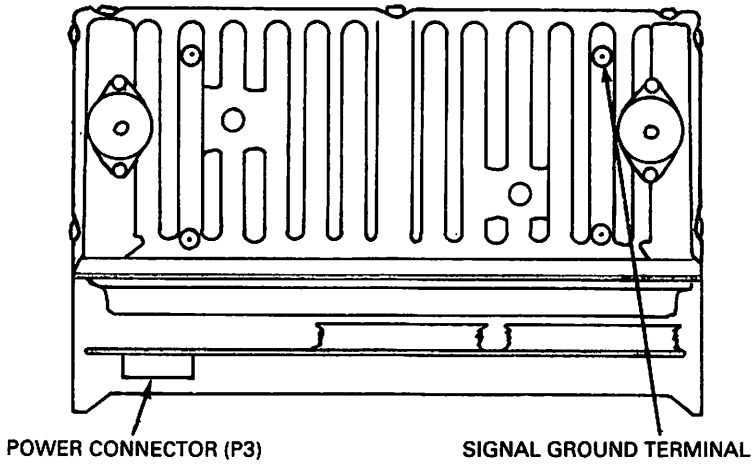


Figure 2-12 Signal Ground and Power Connections

2.6.3 Power Cable

Connect the power cable to connector P3 at the rear of the disk drive (see Figure 2-12).

2.7 LOCK CONTROL ASSEMBLY

When the disk drive is shipped, the spindle and actuator positioner are secured with a lock device to prevent movement. This device must be released prior to operating the drive. To unlock the spindle and actuator, slide the lock control lever (see Figure 2-13) to the FREE position.

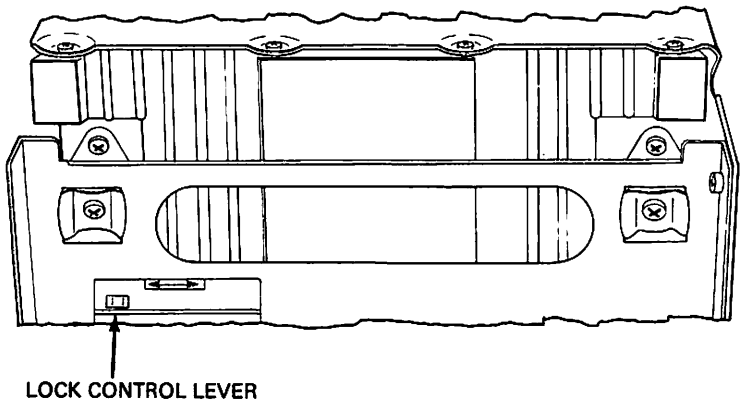
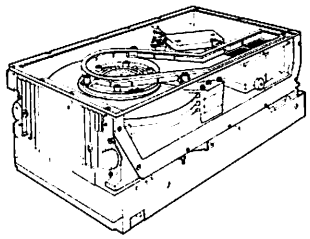


Figure 2-13 Lock Control Assembly

Chapter 3



Preventive Maintenance and Troubleshooting

This chapter outlines maintenance and troubleshooting procedures for the D22x7 disk drive. It describes preventive maintenance, test operations and test points, and associated waveforms. Refer to Appendix C for information on how to use the optional diagnostic panel.

3.1 GENERAL MAINTENANCE RULES

Always observe the following general rules when replacing parts or servicing the disk drive.

- Turn off the disk drive and disconnect all ac power to the drive power supply before performing any maintenance procedure on the drive.
- Never remove or install any PCB, or disconnect any connector, plug, or wire while power is on.
- When removing any connector, grasp it firmly by its sides and pull it out. Do not remove any connector by pulling on the wire bundle.
- Do not remove any parts that are not specified in the replacement procedures.
- Package PCBs in an electrostatic-free envelope when they are transported.

3.2 MAINTENANCE TOOLS

Standard maintenance procedures require the following common hand tools.

- No. 1 Phillips screwdriver
- No. 2 Phillips screwdriver
- Small straight-tip screwdriver

The following instruments are also required.

- High impedance voltmeter
- Oscilloscope (Tektronics 465 or equivalent)

A rotor handler (NEC part number 134-233280) and a diagnostic panel (NEC part number 134-200267) are recommended.

3.3 PREVENTIVE MAINTENANCE

Preventive maintenance is limited to periodic dusting of the surface of the drive. No lubrication or further cleaning is required or recommended. D22x7 disk drives contain no parts that require scheduled adjustment or replacement.

NOTE

The air filter in the sealed head/disk assembly cannot be replaced or cleaned.

As part of a periodic preventive maintenance routine, run system-specific (software) diagnostic programs or use the diagnostic panel to run offline test procedures (see Appendix C).

3.4 TROUBLESHOOTING

If a fault occurs, attempt to isolate the fault to the host, to the host controller, to the disk drive, or to another connecting component. For faults isolated to the disk drive, use the troubleshooting procedures outlined in the following flowcharts. These procedures localize the fault to a specific drive component.

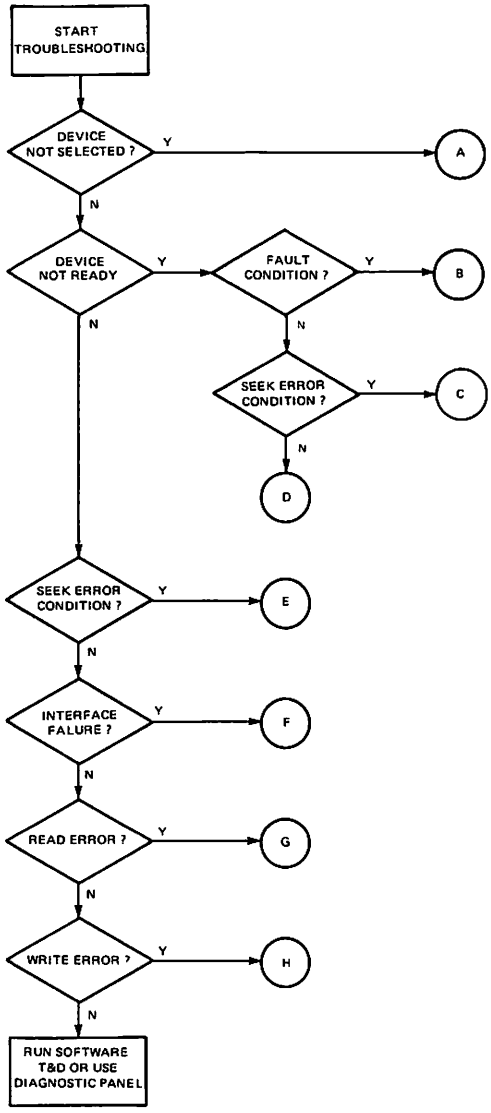


Figure 3-1 Troubleshooting Flowcharts

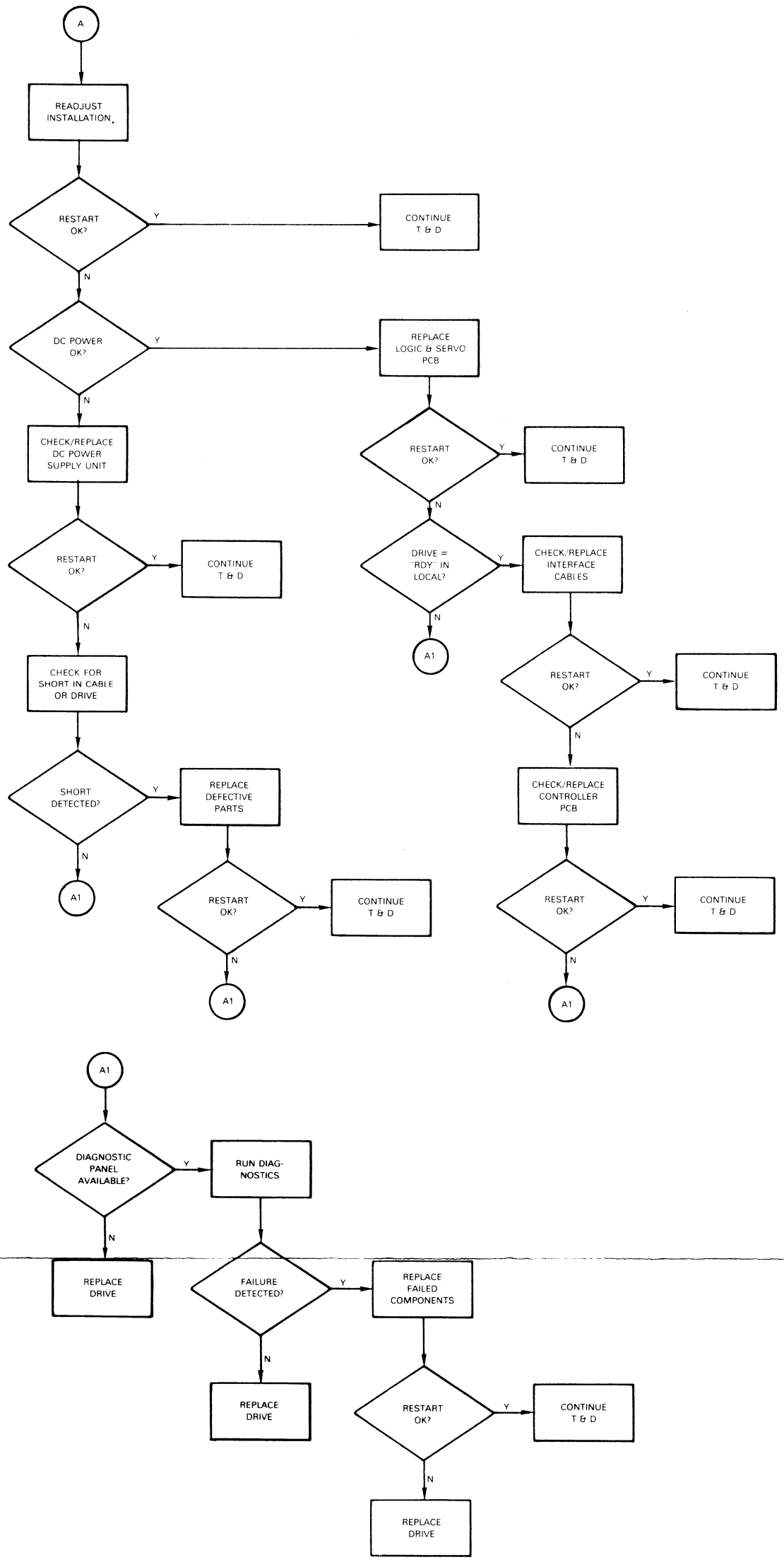


Figure 3-1 Troubleshooting Flowcharts (cont'd)

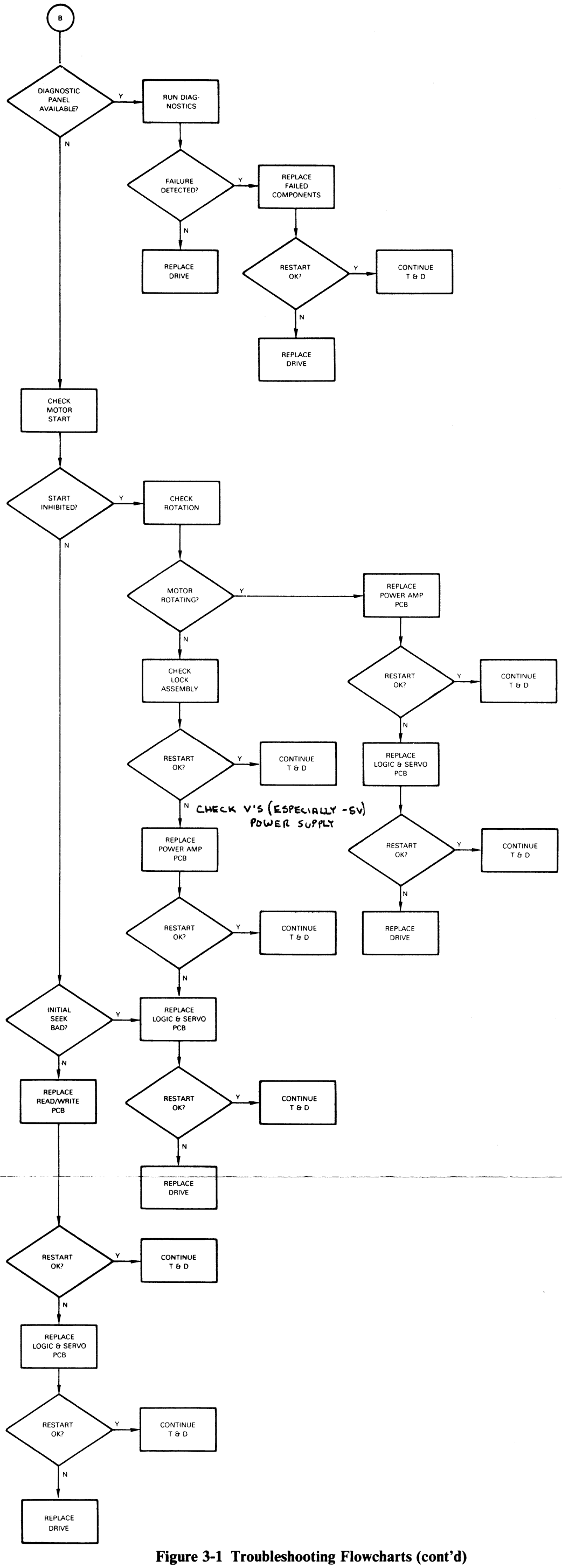


Figure 3-1 Troubleshooting Flowcharts (cont'd)

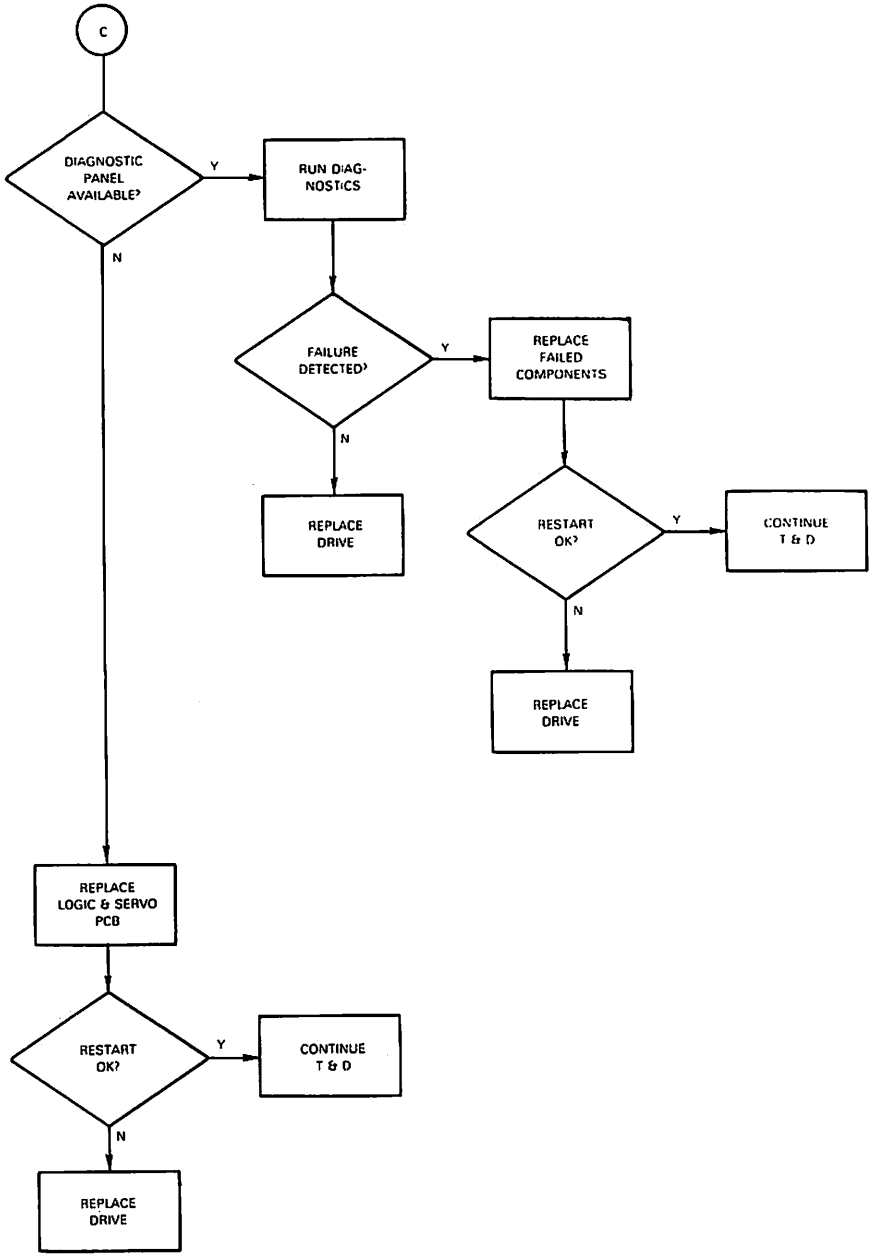


Figure 3-1 Troubleshooting Flowcharts (cont'd)

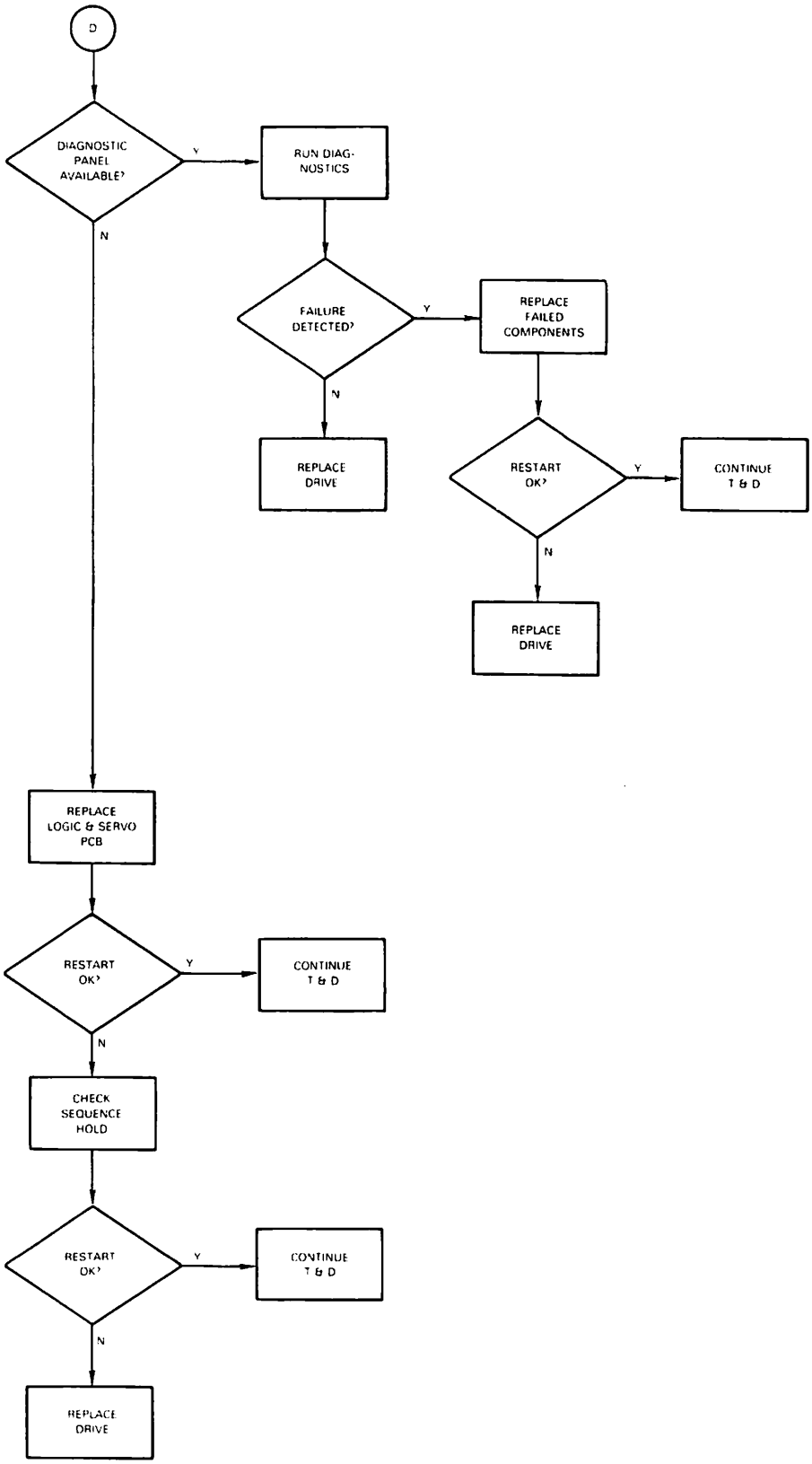


Figure 3-1 Troubleshooting Flowcharts (cont'd)

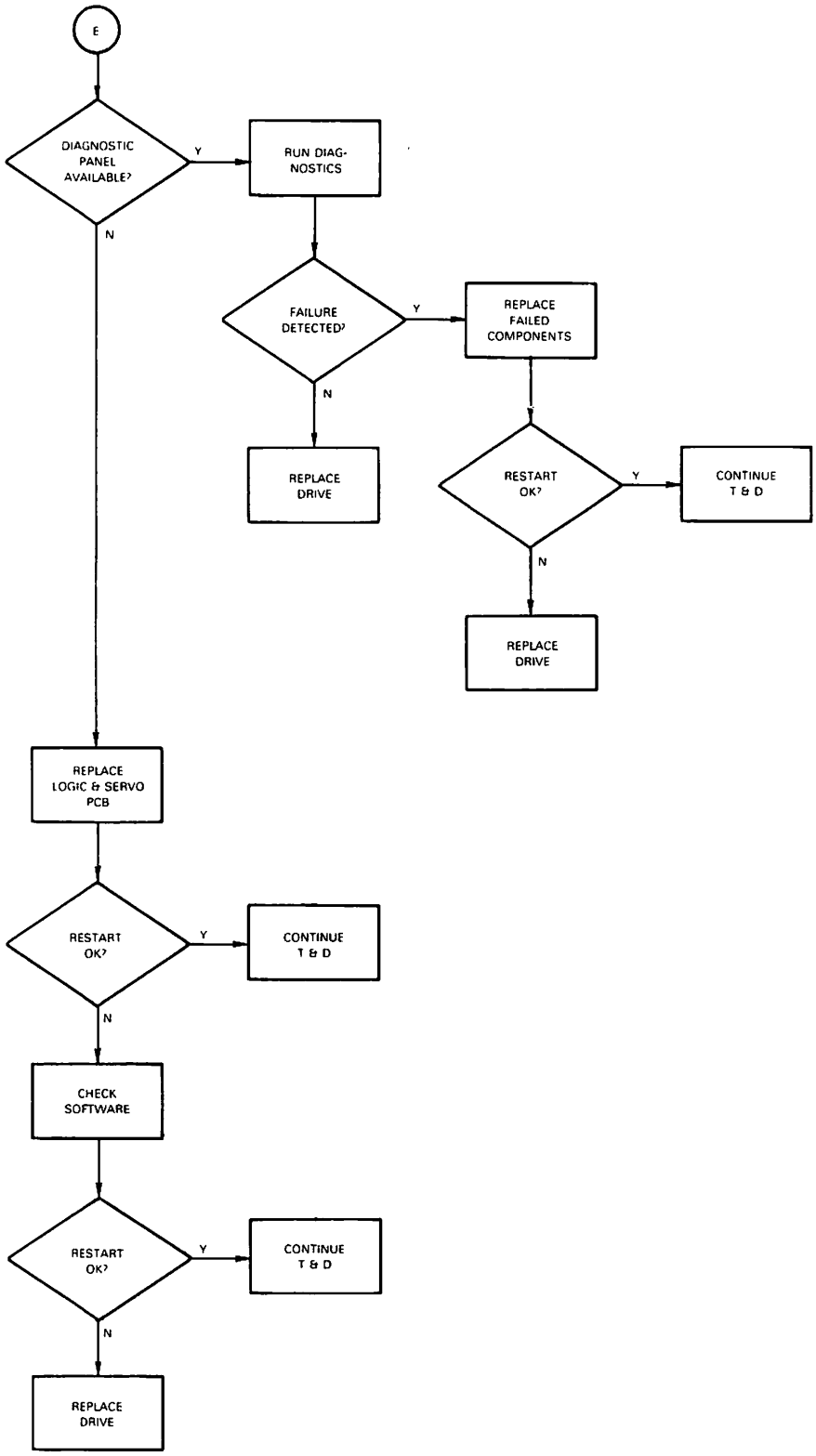


Figure 3-1 Troubleshooting Flowcharts (cont'd)

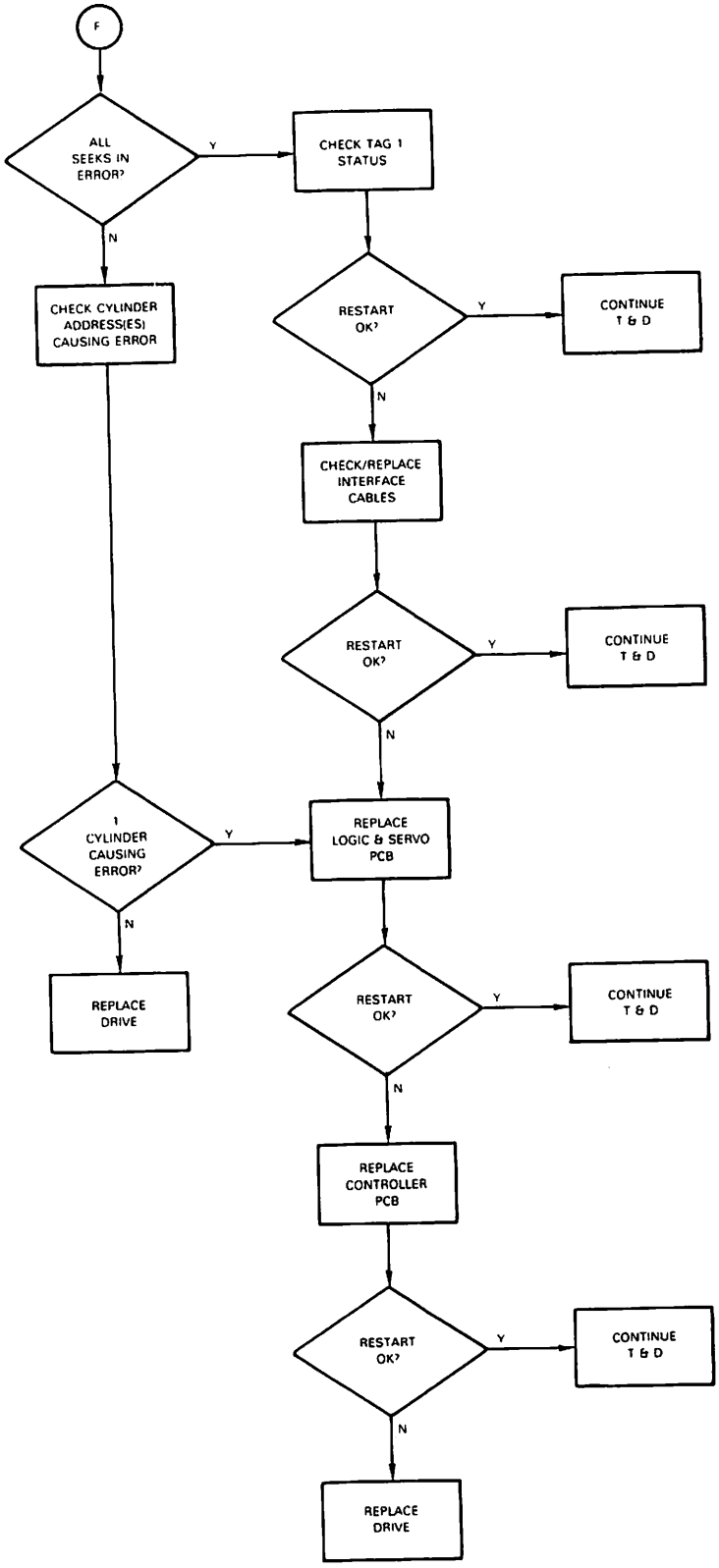


Figure 3-1 Troubleshooting Flowcharts (cont'd)

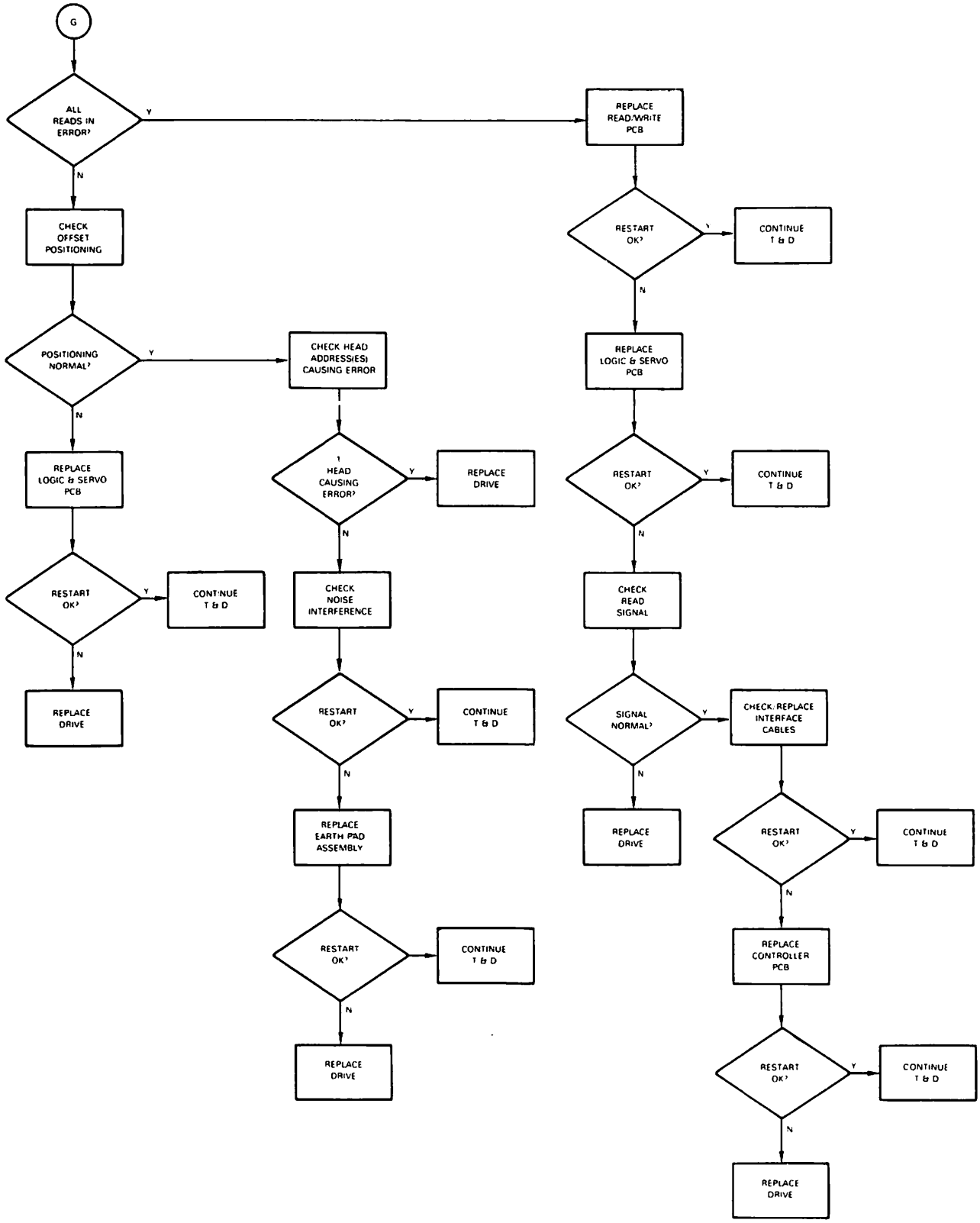


Figure 3-1 Troubleshooting Flowcharts (cont'd)

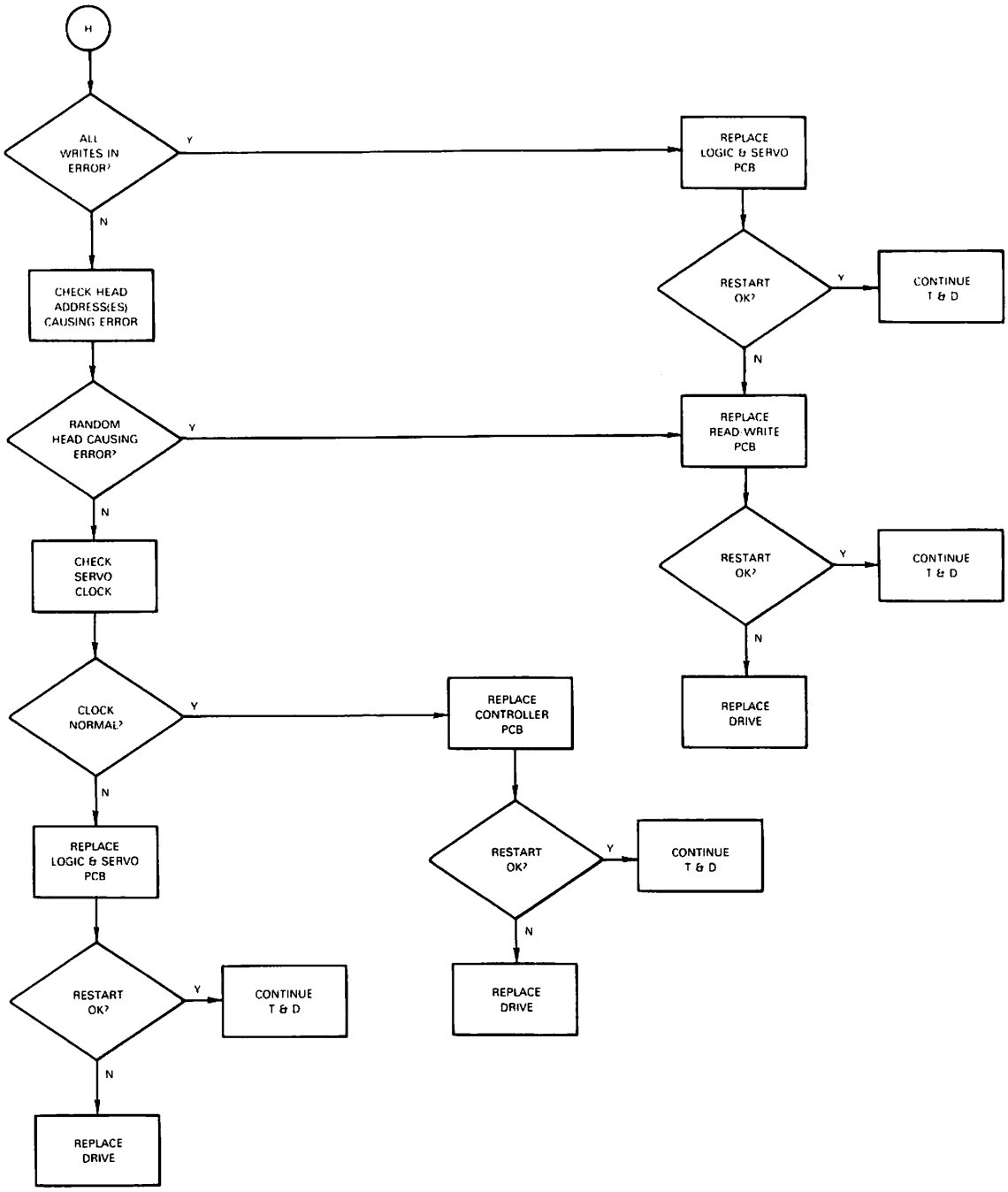


Figure 3-1 Troubleshooting Flowcharts (cont'd)

3.5 SERVO SYSTEM SIGNALS

Test point locations on the G9QSV logic and servo PCB are shown in Figure 3-2. Figures 3-3 and 3-4 show how to access these test points from the exterior of the D22x7 drive. Table 3-1 lists the signal output and signal level from each test point.

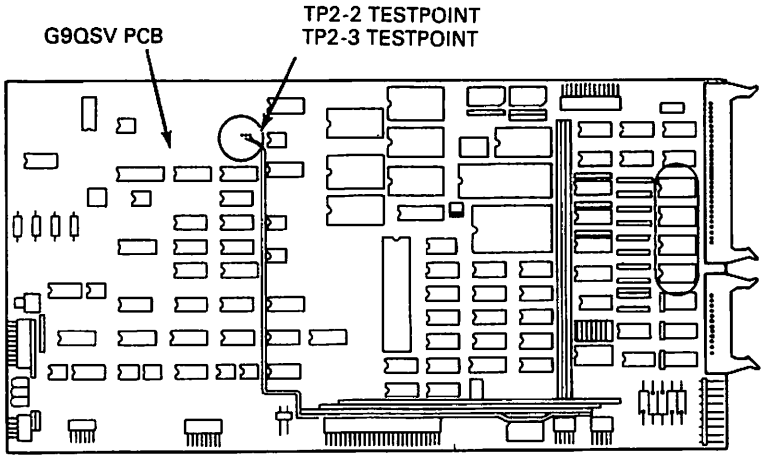


Figure 3-2 G9QSV Test Point Locations

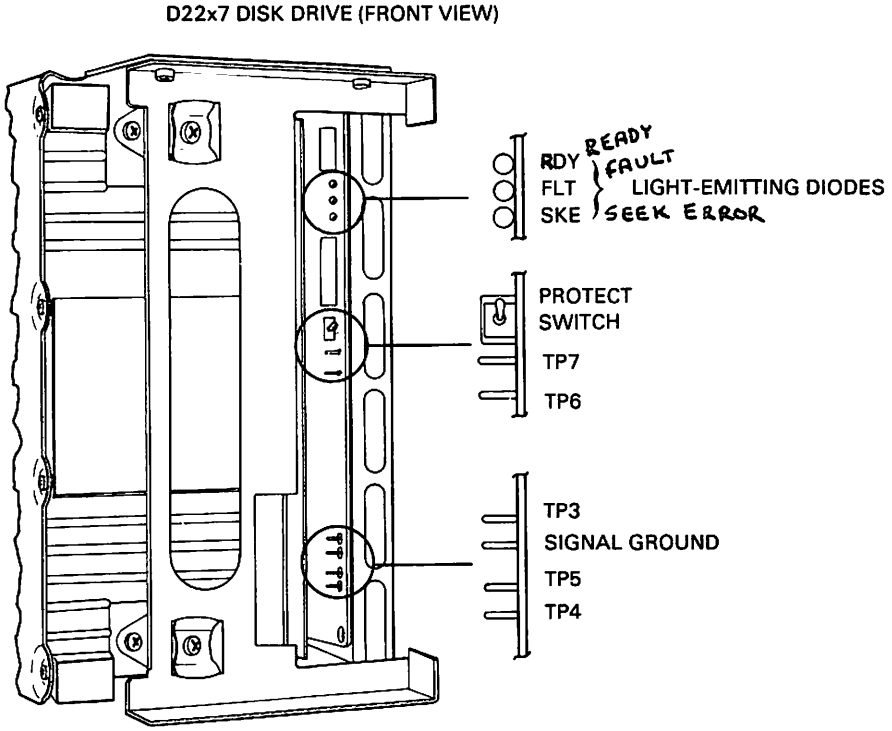


Figure 3-3 Test Points — Front View

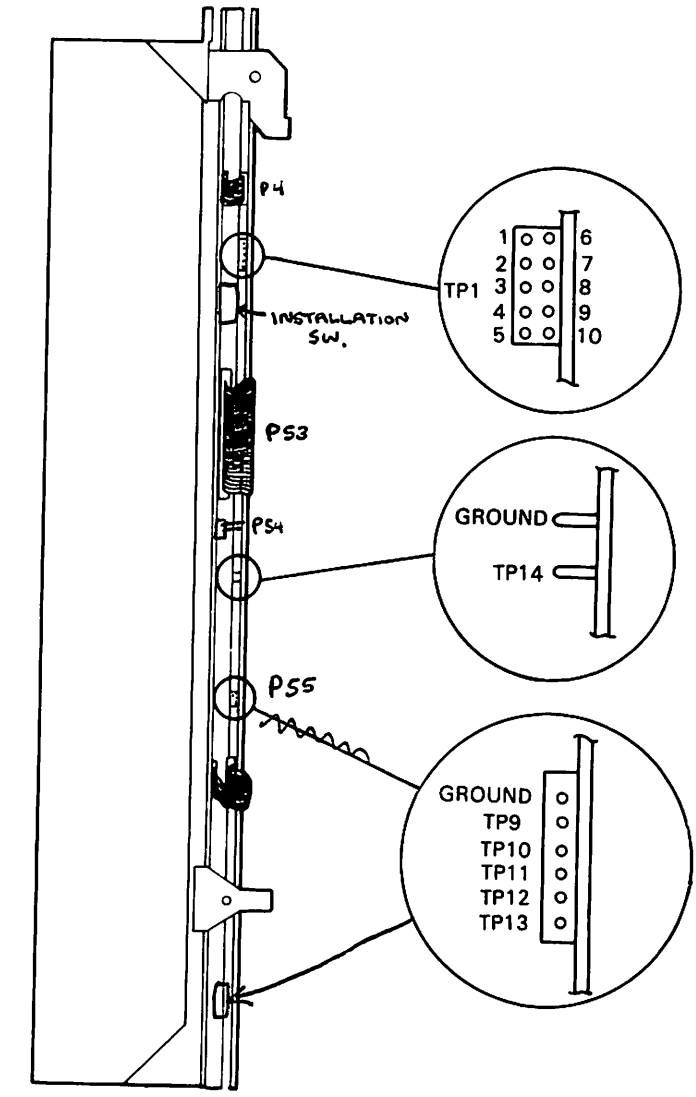


Figure 3-4 Test Points — Side View

Table 3-1 Test Point Signal Outputs

TEST POINT	SIGNAL	LEVEL
TP-2	Tripulse input (positive polarity)	20–90 mVpp
TP2-3	Tripulse input (negative polarity)	20–90 mVpp
TP3	Automatic gain control (AGC) standard voltage	1.4 V (approx)
TP4	AGC control voltage	6.0 V (approx)
TP5	Dipulse output (AGC output)	6.0 Vpp (approx)
TP6	Q position signal	0 to ±6.0 V
TP7	N position signal	0 to ±6.0 V
TP8	Servo window signal (NW1)	TTL levels
TP9	Speed set signal	0 to +8.0 V
TP10	Speed signal	0 to ±8.0 V
TP11	Rectified speed signal	0 to -8.0 V
TP12	Noise injunction terminal	0 to 2.0 Vpp
TP13	Selected position signal	0 to ±6.0 V
TP14	Servo current (0.5 V corresponds to 1.0A)	0 to 1.5 Vpp

Normal servo system signals match the specifications and waveforms listed in Table 3-2.

Table 3-2 G9QSV Servo Signals

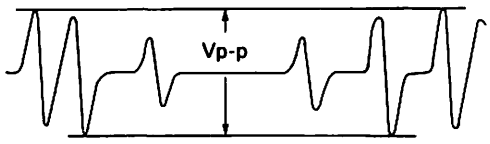
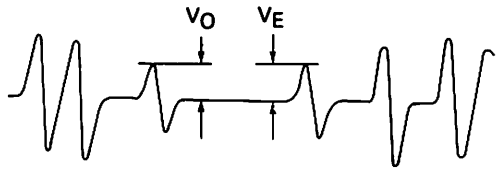
FUNCTION	TEST POINT	COMMENTS
Tripulse input amplitude	TP2-2, TP2-3	 40mVpp≦Vpp≦180mVpp at Cylinder 000 and Cylinder 1023
AGC output amplitude	TP5	 V_O, V_E = About 1.6 $V_{O\text{-}p}$
AGC standard voltage	TP3	DC about 1.4V

Table 3-2 G9QSV Servo Signals (cont'd)

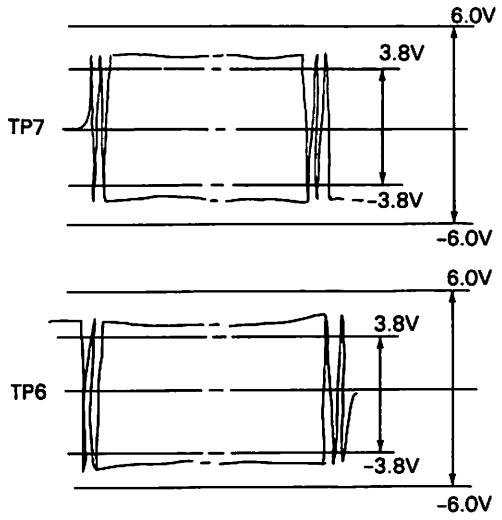
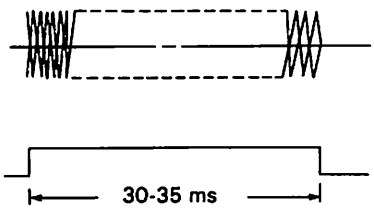
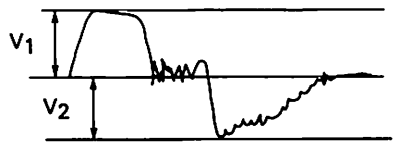
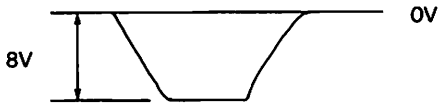
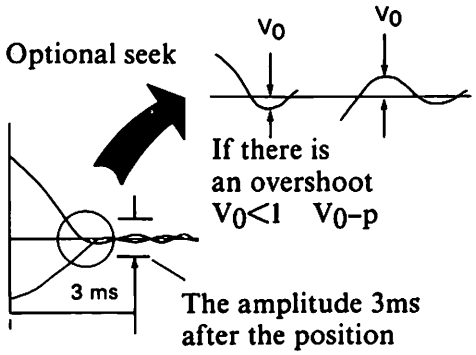
FUNCTION	TEST POINT	COMMENTS
Position signal amplitude	TP6, TP7 TP1-4 of G9QSV is the trigger.	000 ⇄ 1023 Cylinder Repeat Seek 
Seek time	TP1-3 TP1-5	000 ⇄ 1023 Cylinder Repeat Seek  *The settling time is not included.

Table 3-2 G9QSV Servo Signals (cont'd)

FUNCTION	TEST POINT	COMMENTS
Current waveform	TP14 The trigger is TP1-4 and TP1-3 of G9QSV.	000 ⇄ 1023 Cylinder Repeat Seek  V_1 + 0.8 – 1.2 V $V_2 < 1.3$ V (The polarity changes according to the seek direction.)
Speed profile follows	TP10, TP11 The trigger is TP1-4 and TP1-3 of G9QSV.	000 ⇄ 1023 Cylinder Repeat Seek  The speed set signal (TP10) is inverted and made to overlap the speed signal (TP11).
Position transient response	TP13 The trigger is TP1-5 of G9QSV.	Optional seek  If there is an overshoot $V_0 < 1$ V_{0-p} The amplitude 3ms after the position mode is set shall be less then $0.5V_{0p}$.

3.6 SEEK OPERATIONS TESTING

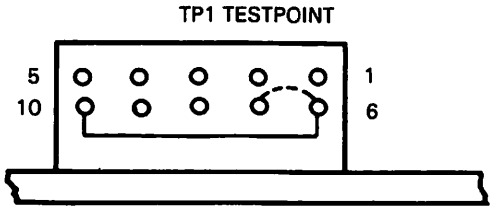
A repeat seek or a one-cylinder seek operation can be initiated by connecting strapping wire to TP1.

3.6.1 Repeat Seek Operation

A repeat seek operation seeks from the low cylinder (cylinder 000) to the high cylinder (cylinder 1023), and then from the high cylinder back to the low cylinder. To perform a repeat seek operation, connect wires to TP1 as shown in Figure 3-5.

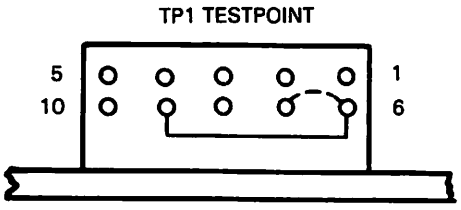
3.6.2 One-Cylinder Seek Operation

A one-cylinder seek operation seeks from cylinder 000, to cylinder 001, to cylinder 002, and continues to the high cylinder. From the high cylinder, the unit seeks to cylinder 1022, to cylinder 1021, and continues back to the low cylinder. To perform a one-cylinder seek operation, connect wires to TP1 as shown in Figure 3-6.



IF PINS 6 AND 7 ARE CONNECTED, THE SEEK INTERVAL TIME IS 100 MILLISECONDS.

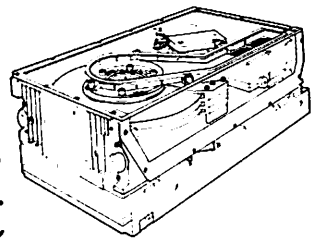
Figure 3-5 Repeat Seek Using TP1



IF PINS 6 AND 7 ARE CONNECTED, THE SEEK INTERVAL TIME IS 1.5 SECONDS.

Figure 3-6 One-Cylinder Seek Using TP1

Chapter 4



Removal and Replacement Procedures

This chapter provides procedures for removing and replacing D22x7 components and assemblies. Field-replaceable items are listed in Table 4-1.

Table 4-1 D22x7 Field Replaceable Components

COMPONENT/ASSEMBLY	NEC PART NUMBER
G9QSV Logic and Servo PCB	134-832956
G9QSR Power Amplifier PCB	134-832952
G9QSP Read/Write PCB	134-832950
Earth Pad Assembly	134-232861
Motor Stator Assembly	806-942281-003

4.1 G9QSV (LOGIC AND SERVO) PCB REMOVAL

Follow these steps to remove the G9QSV logic and servo PCB.

1. Turn off the D22x7.
2. Disconnect the dc power supply.
3. Loosen the two screws that secure the board cover to the drive unit (see Figure 4-1).

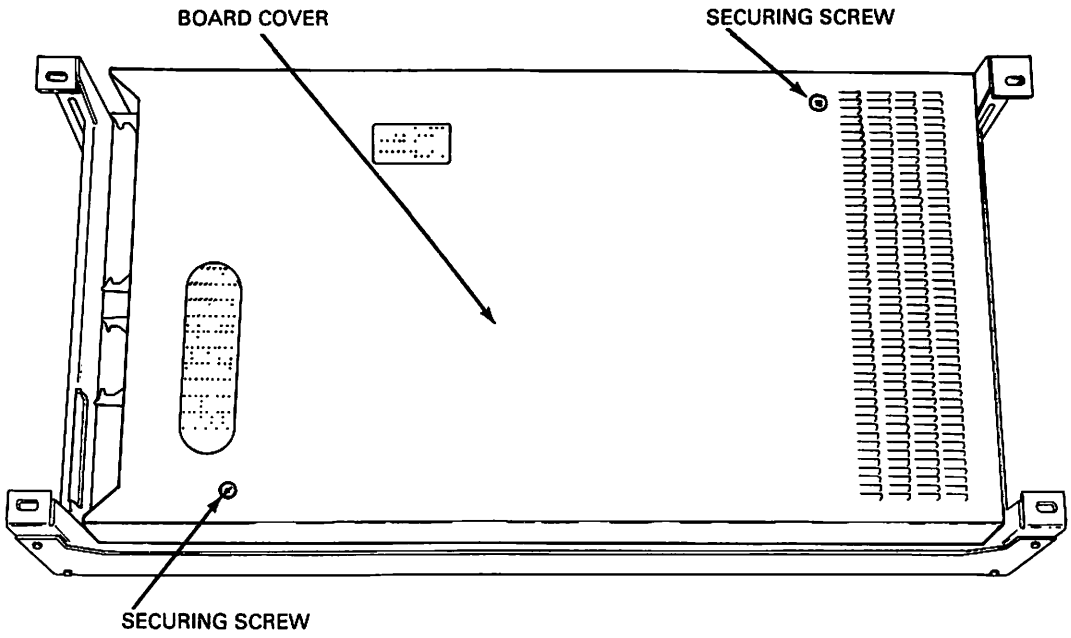


Figure 4-1 D22x7 Board Cover

4. Lift the board cover straight up to remove it.
5. Disconnect cable connectors J55, J54, J53, and J41 (see Figure 4-2).

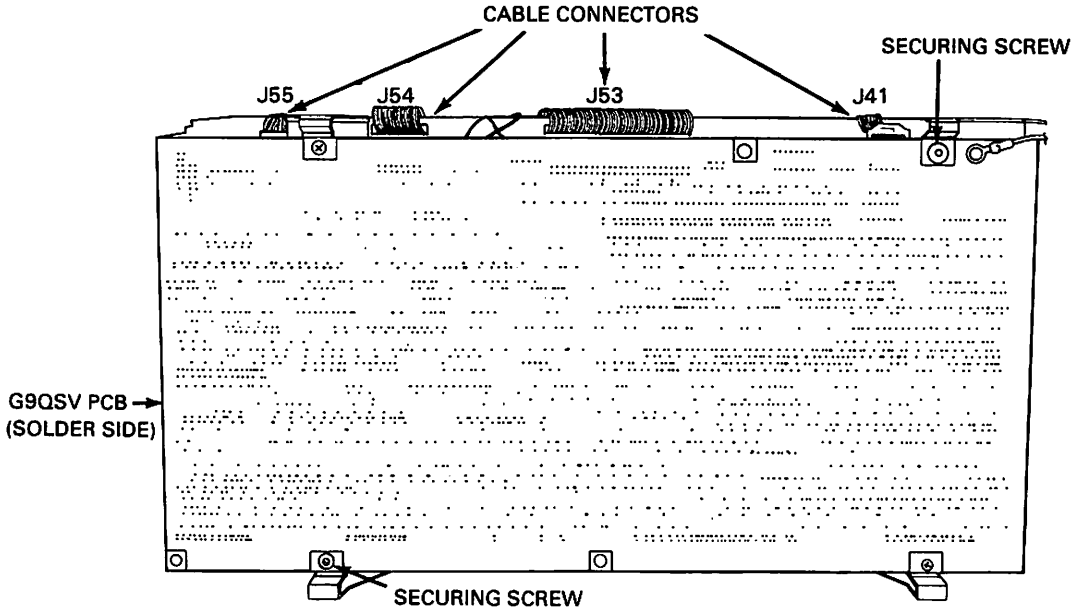


Figure 4-2 G9QSV Cable Connectors

6. Remove the two screws that fasten the G9QSV to the drive unit (see Figure 4-2).
7. Lift the G9QSV PCB straight up to remove it.

When installing a new G9QSV PCB, be sure that the DIP switch, jumper, and terminating resistor configurations on the replacement board match those on the old board.

4.2 G9QSP (READ/WRITE) PCB REMOVAL

Follow these steps to remove the G9QSP read/write PCB.

1. Turn off the D22x7.
2. Disconnect the dc power supply.
3. Remove the G9QSV PCB (see Section 4.1).
4. Remove the four screws that secure the larger air separator (air separator A) to the drive unit (see Figure 4-3).

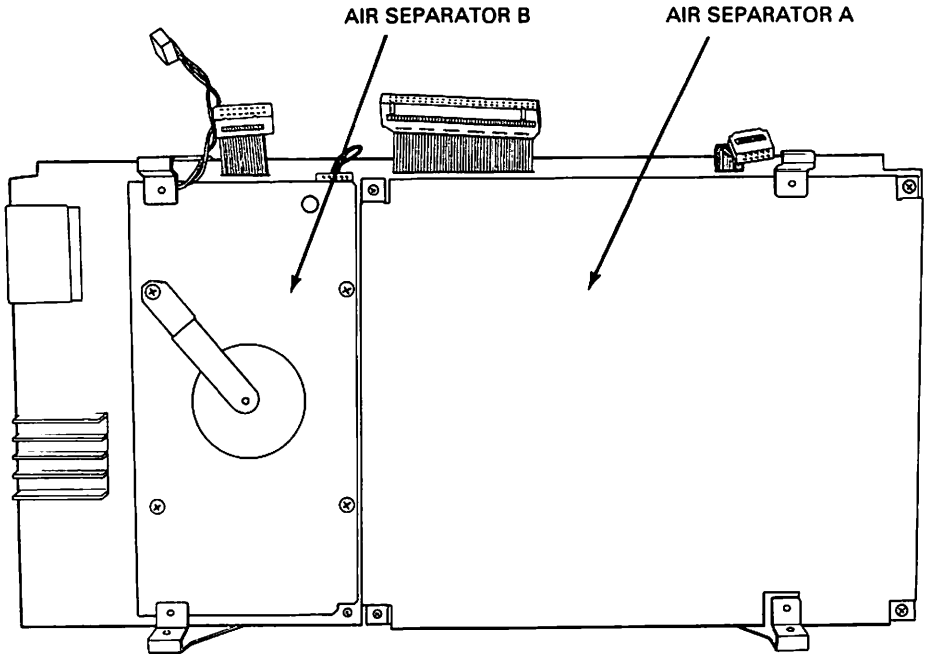


Figure 4-3 D22x7 Air Separators

5. Lift air separator A straight up to remove it.
6. Disconnect cable connectors J31 and J32 (see Figure 4-4).
7. Lift the G9QSP PCB slightly and slide it away from the earth pad assembly to remove it (see Figure 4-4).

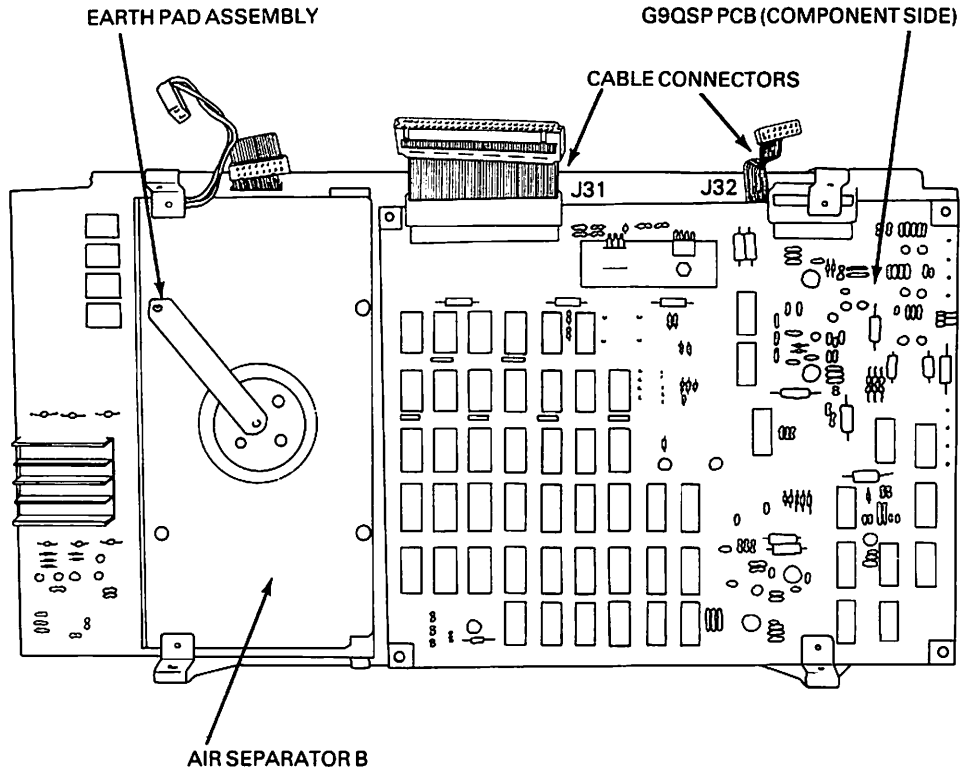


Figure 4-4 G9QSP Cable Connectors

4.3 EARTH PAD ASSEMBLY REMOVAL

Follow these steps to remove the earth pad assembly.

1. Turn off the D22x7.
2. Disconnect the dc power supply.
3. Remove the G9QSV PCB (see Section 4.1).
4. Remove the screw that attaches the earth pad assembly to the smaller air separator (air separator B — see Figure 4-4).
5. Lift the earth pad assembly straight up to remove it.

4.4 G9QSR (POWER AMPLIFIER) PCB REMOVAL

Follow these steps to remove the G9QSR power amplifier PCB.

1. Turn off the D22x7.
2. Disconnect the dc power supply.
3. Remove the G9QSV PCB (see Section 4.1).
4. Remove the earth pad assembly (see Section 4.3).
5. Remove the three screws that secure air separator B to the drive unit (see Figure 4-4).
6. Lift air separator B and slide it to the side to remove it.
7. Disconnect cable connectors J22, J23, J24, and J44 (see Figure 4-5).

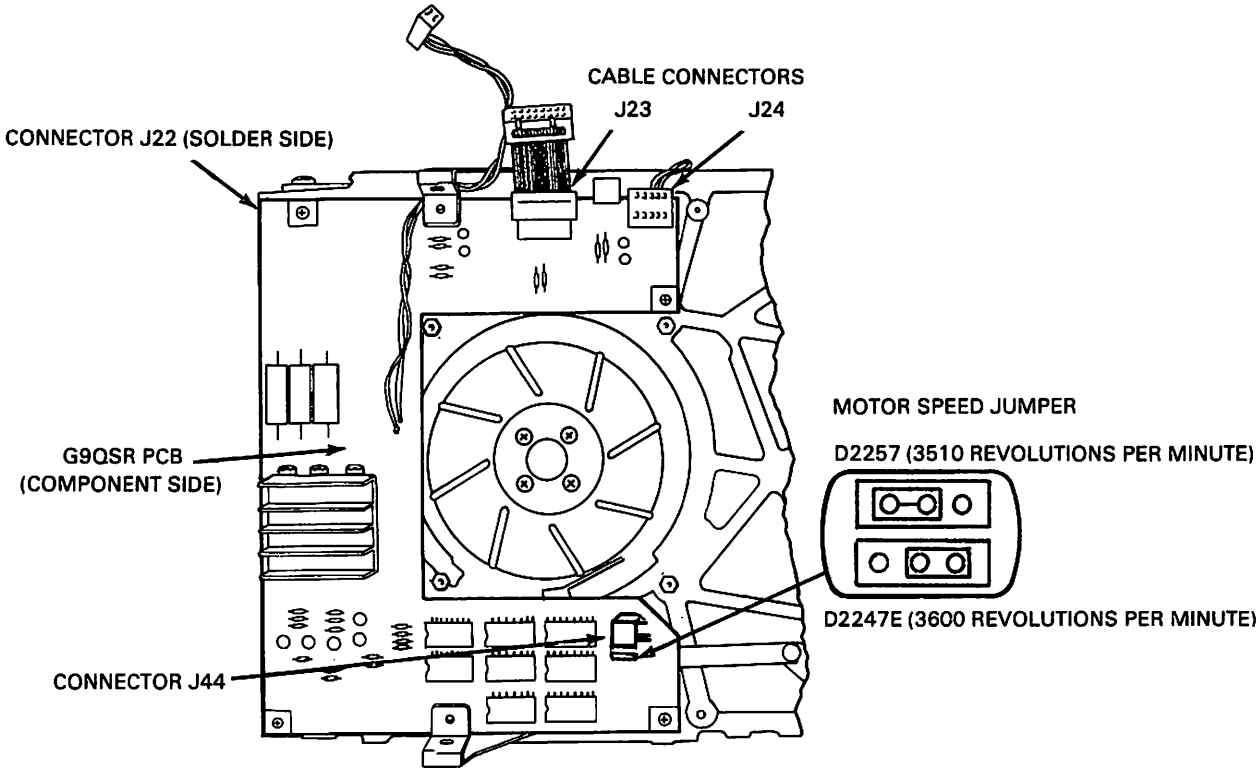


Figure 4-5 G9QSR Cable Connectors

8. Remove the three screws that attach the G9QSR PCB to the drive unit (see Figure 4-5).
9. Lift the G9QSR PCB slightly and slide it to the side to remove it.

When installing a new G9QSR PCB, be sure that the motor speed jumper (see Figure 4-5) is correctly set. Figure 4-5 shows the correct settings for D2247E and D2257 disk drives.

4.5 MOTOR STATOR ASSEMBLY REMOVAL

Follow these steps to remove the motor stator assembly.

1. Turn off the D22x7.
2. Disconnect the dc power supply.
3. Remove the G9QSV PCB (see Section 4.1).
4. Remove the earth pad assembly (see Section 4.3).
5. Remove the G9QSR PCB (see Section 4.4).
6. Loosen the four screws that secure the fan (see Figure 4-6) and remove the fan by lifting it straight up.

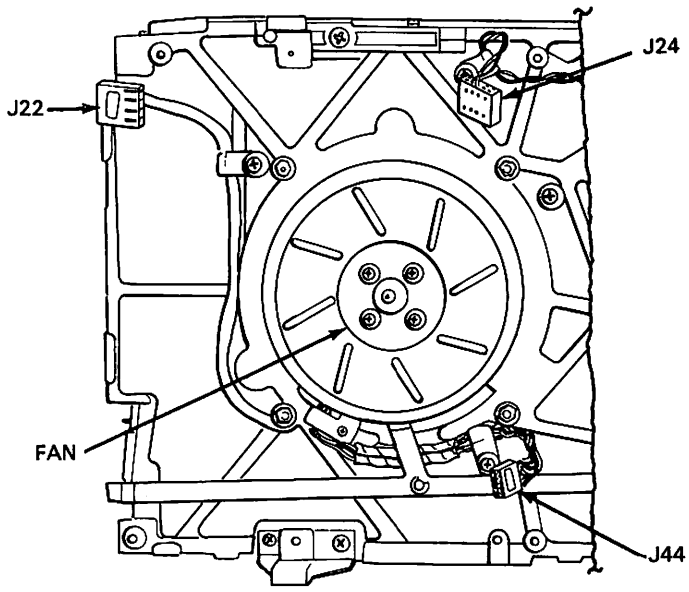


Figure 4-6 D22x7 Fan

7. Remove the rotor using the special rotor handling tool (see Figure 4-7).
8. Loosen the three screws that secure the claw stopper (see Figure 4-7) and remove the claw stopper.
9. Loosen the three screws that secure the motor shield and remove it.
10. Slide the motor stator assembly carefully along the spindle to remove it.

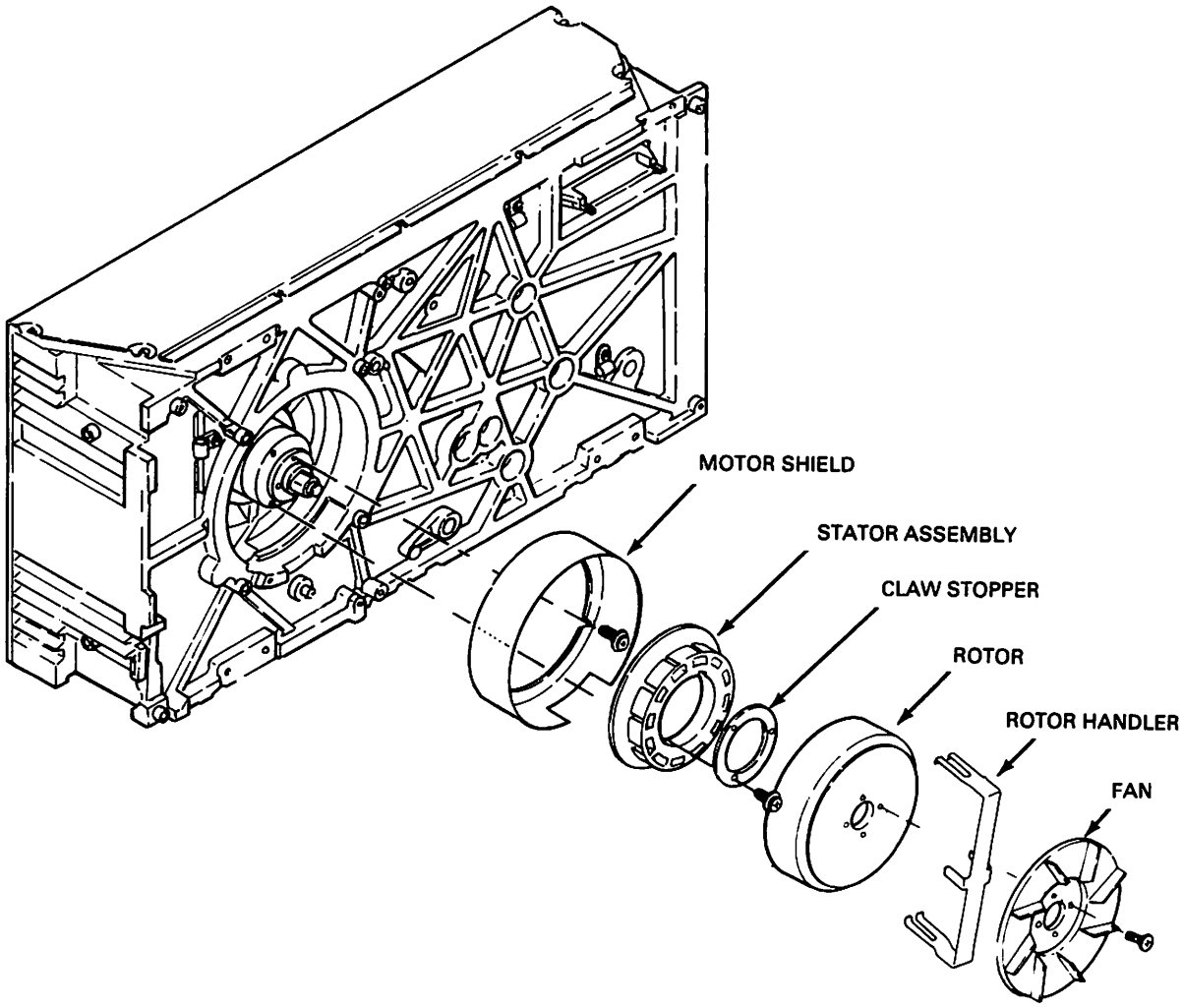


Figure 4-7 D22x7 Stator Assembly

Chapter 5

Illustrated Parts Breakdown

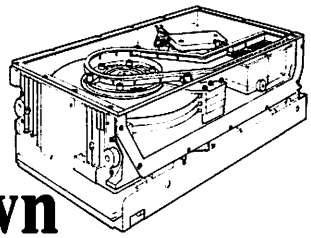


Figure 5-1 shows the D22x7 standard assembly. Figure 5-2 shows the sealed head/disk enclosure along with its external parts. Items are described in the accompanying tables.

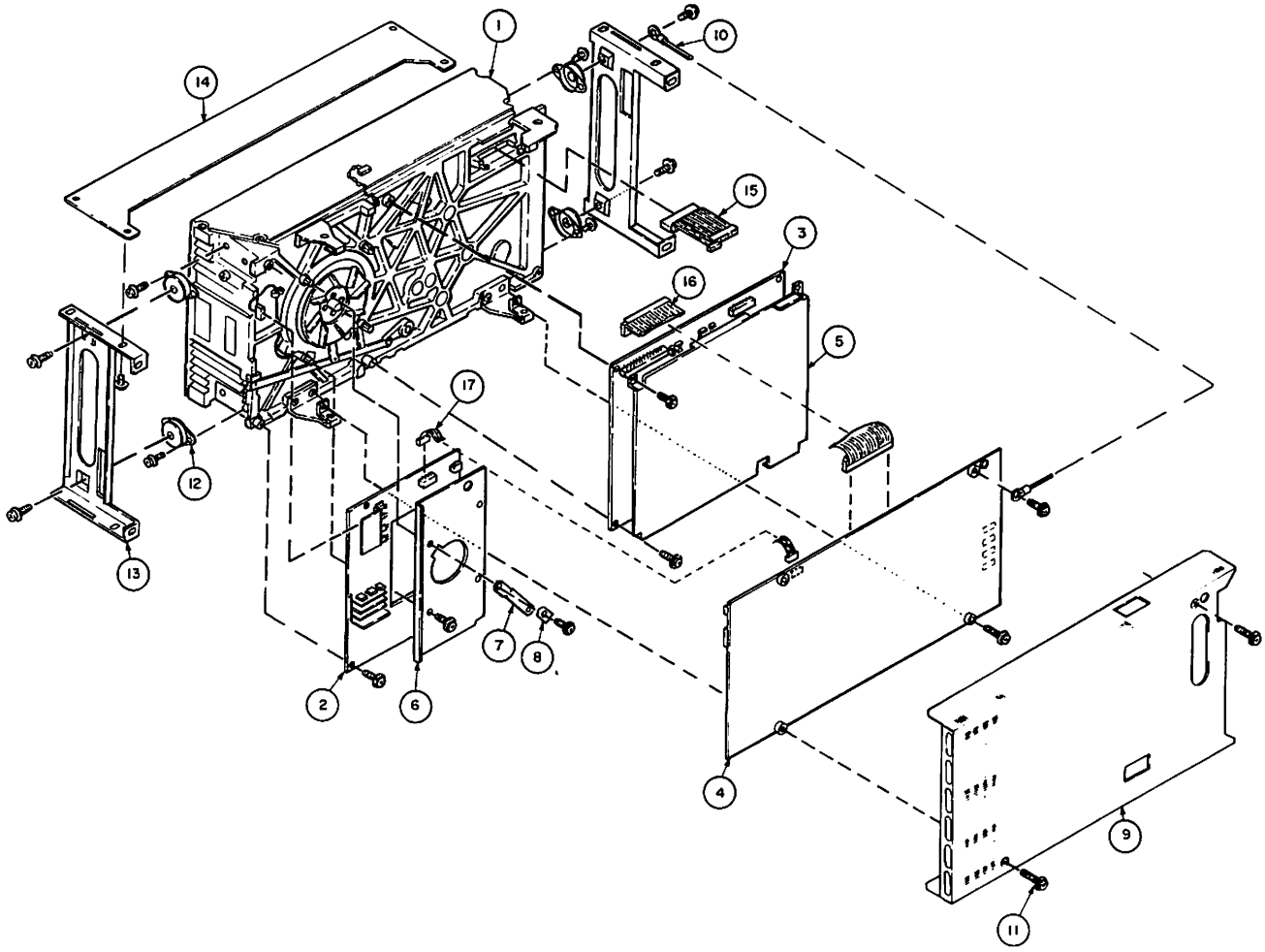


Figure 5-1 D22x7 Standard Assembly

Table 5-1 D22x7 Standard Assembly

ITEM	DESCRIPTION	PART NUMBER	QUANTITY	
			D2247E	D2257
1	047 Head/Disk Enclosure	134-200339-402	1	
1	057 Head/Disk Enclosure	134-200339-502		1
2	G9QSR PCB	134-832952	1	1
3	G9QSP PCB	134-832950	1	1
4	G9QSV PCB	134-832956	1	1
5	Air Separator (A)	134-247626	1	1
6	Air Separator (B)	134-248945	1	1
7	Earth Pad Assembly	134-232861	1	1
8	Spring Clamp	134-247779	1	1
9	Board Cover	134-249448	1	1
10	Grounding Cable	134-232933-0	1	1
11	Screw	805-300003-008	2	2
12	Cushion (Rubber)	806-937115	4	4
13	Bracket Frame	134-249453	2	2
14	Bracket Plate	134-247929	1	1
15	Head/Disk Enclosure Cable Assembly	134-232842	1	1
16	G9QSP PCB Cable Assembly	134-233527	1	1
17	G9QSR PCB Cable Assembly	134-233528	1	1

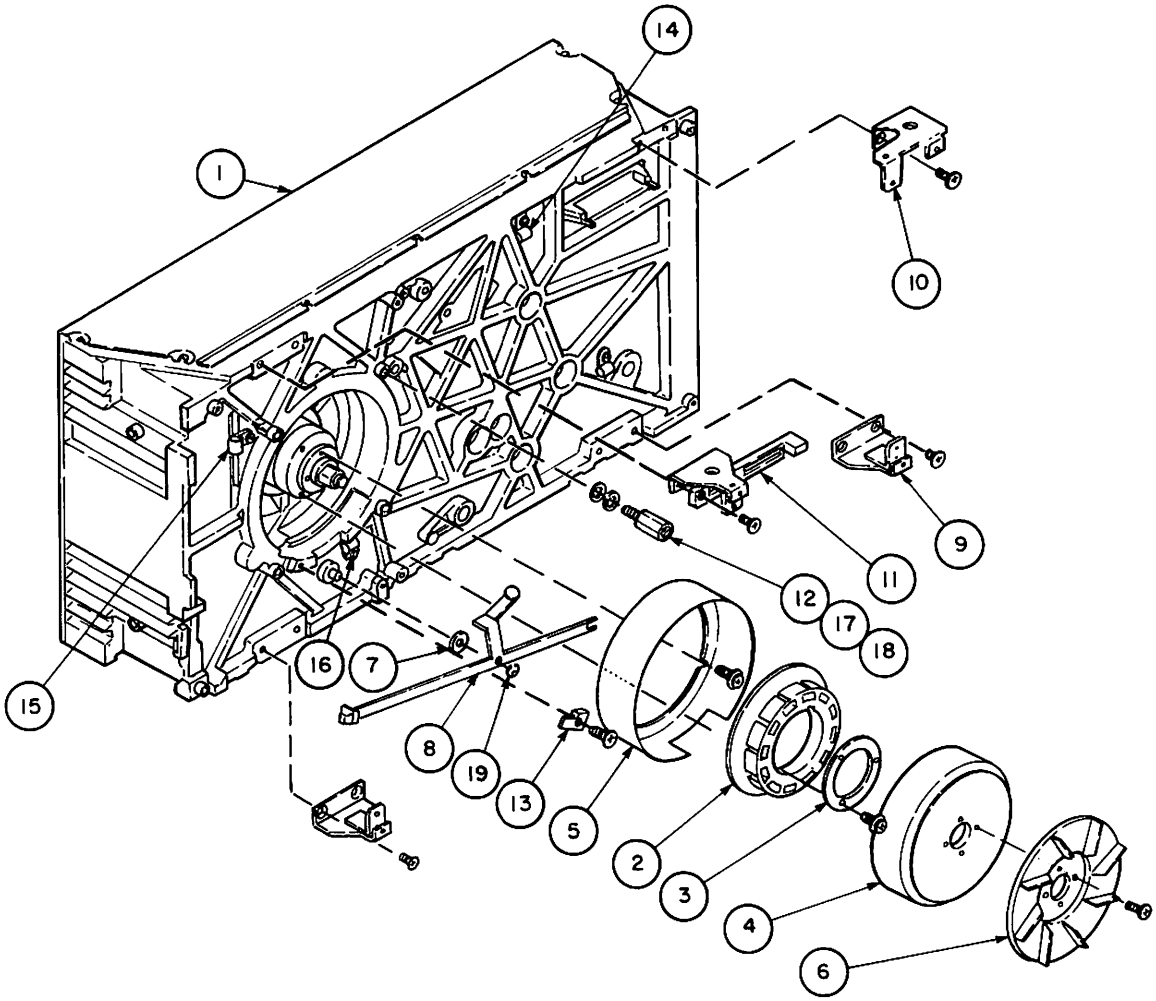


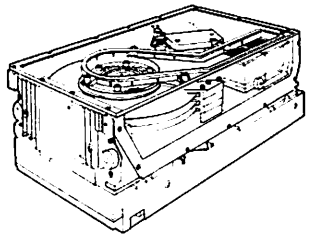
Figure 5-2 D22x7 Head/Disk Enclosure (External Parts)

Table 5-2 Head/Disk Enclosure External Parts

ITEM	DESCRIPTION	PART NUMBER	QUANTITY	
			D2247E	D2257
1	047 Head/Disk Enclosure	134-200339-402	1	
1	057 Head/Disk Enclosure	134-200339-502		1
2	Stator Assembly	806-942281-003	1	1
3	Claw Stopper	134-247662	1	1
4	Rotor	806-942281-002	1	1
5	Motor Shield	134-247782	1	1
6	Fan	134-247663	1	1
7	Pivot Spacer	134-247674	1	1
8	Stopper Link Assembly	134-233039	1	1
9	PCB Support A	134-233510	3	3
10	PCB Support B	134-249452	1	1
11	PCB Guide	134-248516	1	1
12	Stud	134-247621	4	4
13	Cable Clamp	134-248222	1	1
14	Nylon Clip HK-2N	803-070031-002	3	3
15	Nylon Clip HK-3N	803-070031-003	1	1
16	Nylon Clip HK-4N	803-070031-004	1	1
17	Washer	805-604204	4	4
18	Washer	806-931079-004	4	4
19	E-Ring	803-010001-030	1	1

Appendix A

Schematic Diagrams



This Appendix includes the logic diagrams and schematics for each PCB in the D22x7 disk drive. It also includes drawings illustrating the interface and cable connections between PCBs and the signal pin assignments for each connector.

A.1 SIGNAL TRACING SCHEME

The signal tracing scheme provides the ability to easily trace a signal from source to destination within the D22x7 logic. Each individual drawing contains, in its lower right-hand corner, a page number, an identifier, and a drawing number as shown in Figure A-1.

Figure A-1 also shows the horizontal/vertical coordinates that are used to locate and identify a signal upon a specific page.

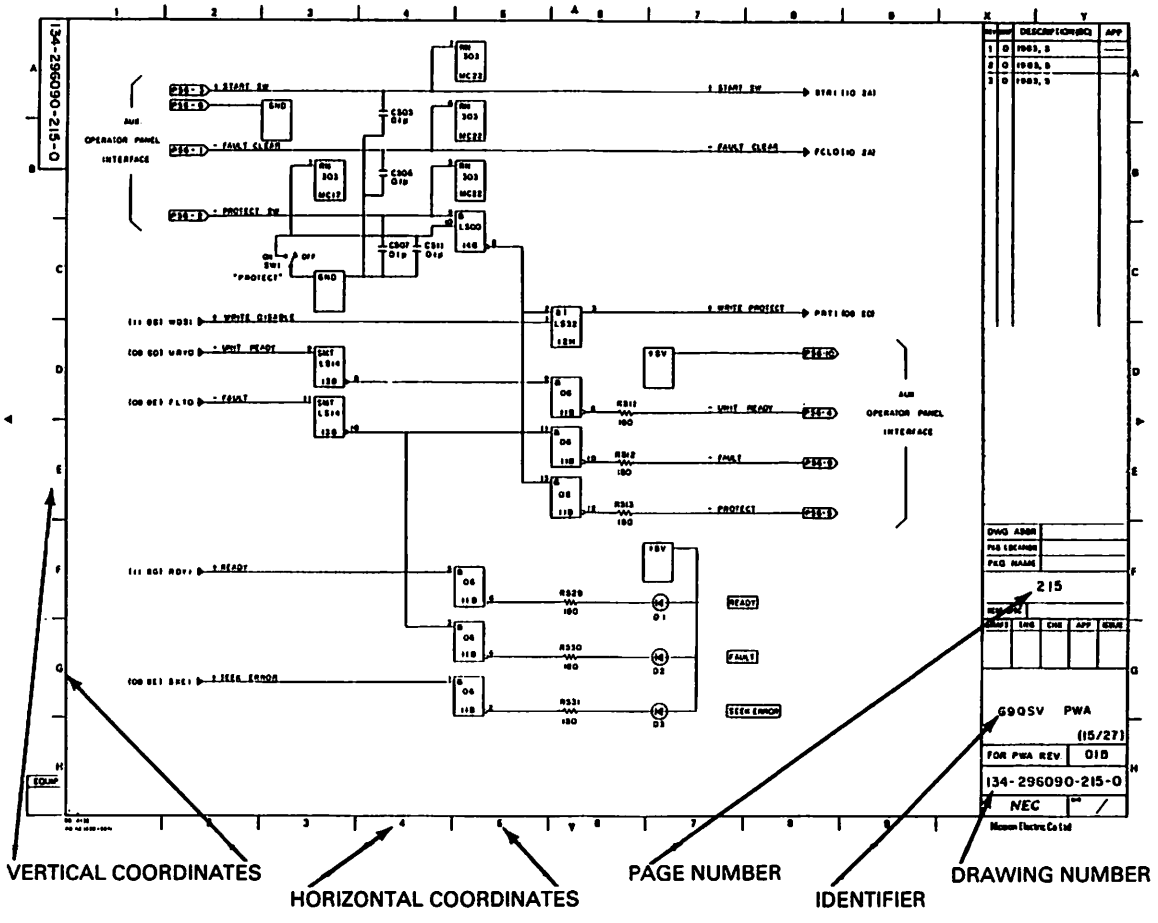


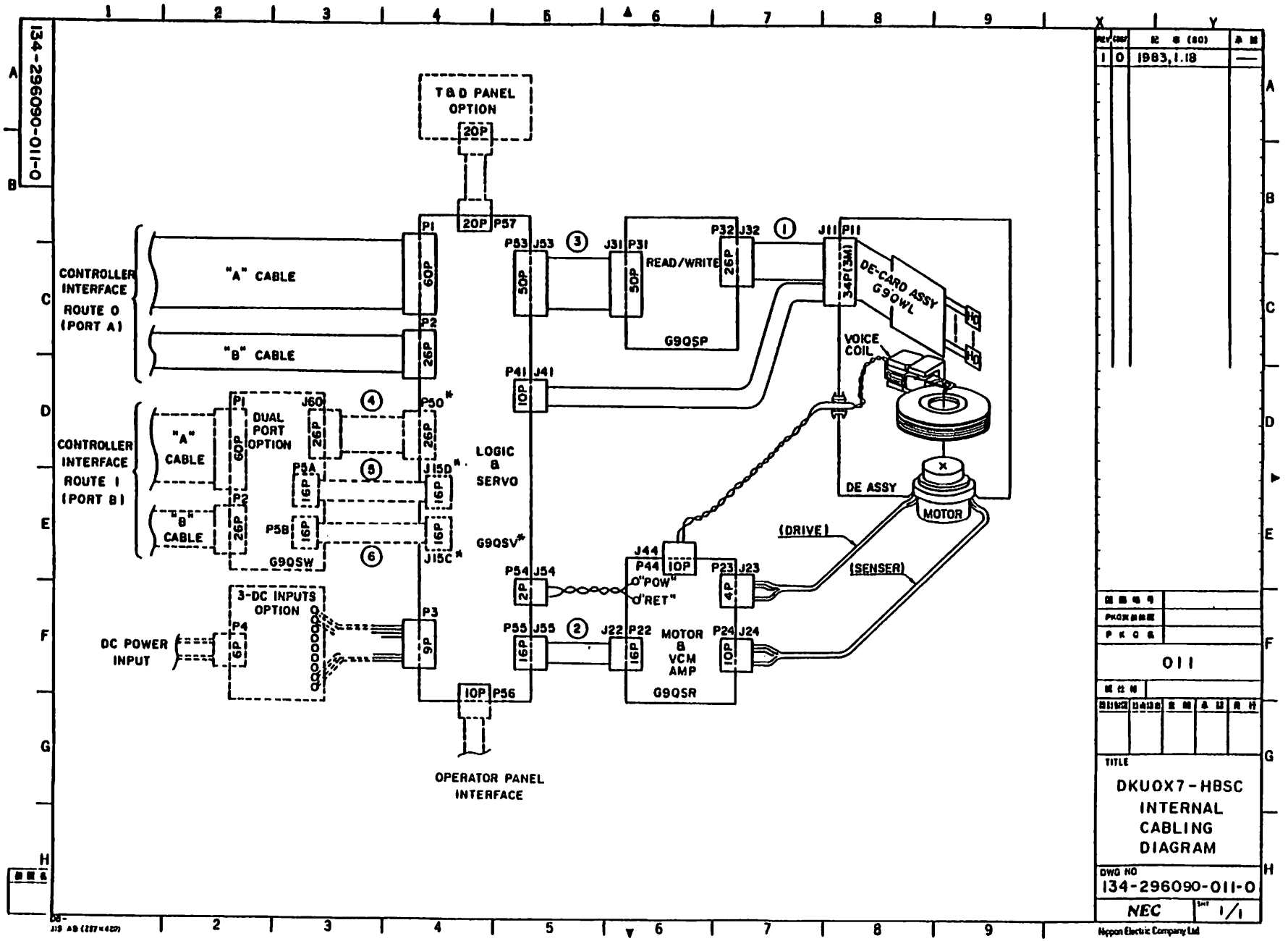
Figure A-1 Schematic Format

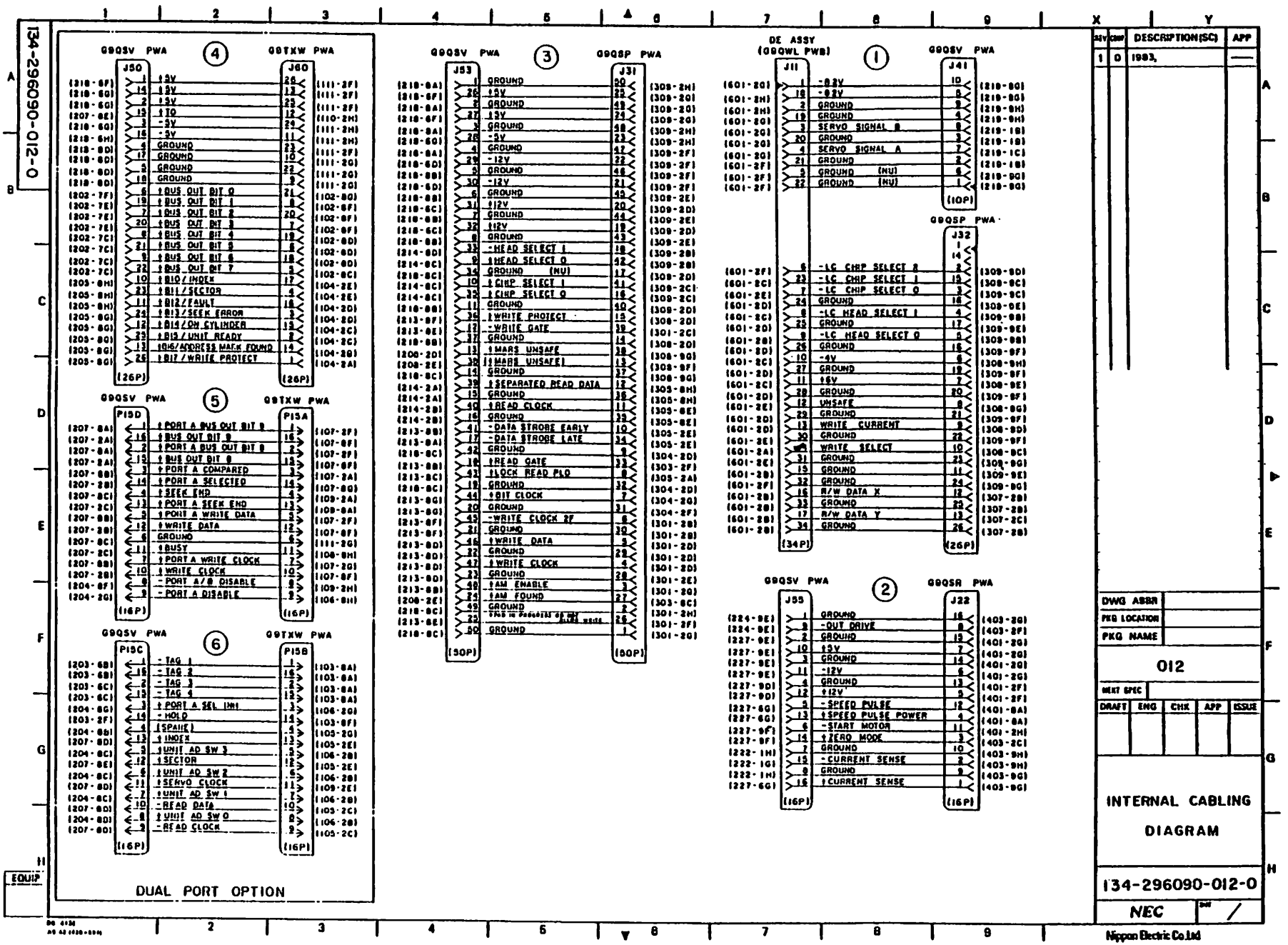
A.2 DRAWINGS

Table A-1 lists the drawings contained in this Appendix along with their drawing numbers.

Table A-1 Schematic Drawings

DIAGRAM	DRAWING NUMBER
I/O Connectors	134-296090-021
Interface and Power Connectors	134-296090-022
Head/Disk Assembly Internal Cabling Diagram	134-296090-011
Internal Cabling Diagram	134-296090-012
Route 0 (Port A) Interface	134-296090-051
Route 1 (Port B) Interface	134-296090-052
G9TXW PCB Schematic	134-296090-101/111
G9QSV PCB Schematic	134-296090-201/227
G9QSP PCB Schematic	134-296090-301/309
G9QSR PCB Schematic	134-296090-401/403
Head/Disk Assembly and Motor Circuit Diagram	134-296090-501
G9QWL PCB Schematic	134-296090-601


134-296090-011-0
T&D PANEL OPTION
20P
20P P57
P1
60P
P2
26P
CONTROLLER INTERFACE ROUTE 0 (PORT A)
"A" CABLE
"B" CABLE
CONTROLLER INTERFACE ROUTE 1 (PORT B)
"A" CABLE
"B" CABLE
DUAL PORT OPTION
G90SW
P50*
J15D*
J15C*
G90SV*
LOGIC & SERVO
P53 J53
50P
J31 P31
READ/WRITE
G90SP
P32 J32
26P
J11 P11
34P(3M)
DE-CARD ASSY G90WL
VOICE COIL
DE ASSY
MOTOR
P41 J41
10P
(DRIVE)
(SENSER)
J44
P44 10P
"POW"
"RET"
P23 J23
4P
P54 J54
2P
P55 J55
16P
J22 P22
MOTOR & VCM AMP
G90SR
P24 J24
10P
3-DC INPUTS OPTION
P4
6P
DC POWER INPUT
P3
9P
10P P56
OPERATOR PANEL INTERFACE
REV 1 0
1983.1.18
011
TITLE
DKUOX7-HBSC INTERNAL CABLING DIAGRAM
DWG NO
134-296090-011-0
NEC
SHT 1/1
Nippon Electric Company Ltd


134-296090-012-0
G9QSV PWA
G9TXW PWA
J50
J60
(26P)
(26P)
G9QSV PWA
G9TXW PWA
P15D
P15A
(16P)
(16P)
G9QSV PWA
G9TXW PWA
P15C
P15B
(16P)
(16P)
DUAL PORT OPTION
G9QSV PWA
G9QSP PWA
J53
J31
(50P)
(50P)
DE ASSY (G9QWL PWB)
G9QSV PWA
J11
J41
(34P)
(10P)
G9QSP PWA
J32
(26P)
G9QSV PWA
G9QSR PWA
J55
J22
(16P)
(16P)
EQUIP
REV
CHG
DESCRIPTION(SC)
APP
1
0
1983,
DWG ASSR
PKG LOCATION
PKG NAME
012
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
INTERNAL CABLING DIAGRAM
134-296090-012-0
NEC
Nippon Electric Co.ltd

134-296090-051-0

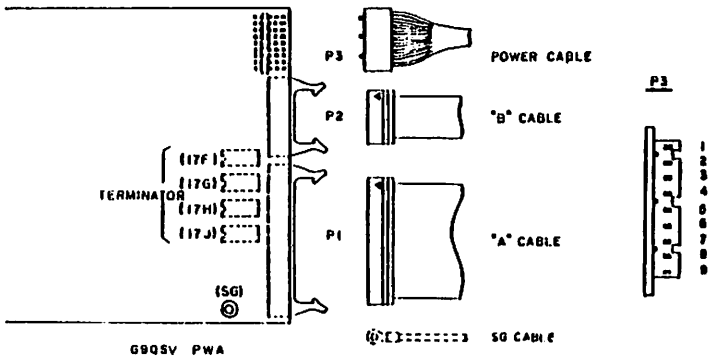
"A" CABLE INTERFACE

PIN NO.	FUNCTION	NAME	JUMP LOCATION
1	YSOTG1Z	TAG 1	203-2A
51	YSOTG1Y		203-2A
2	YSOTG2Z	TAG 2	203-2B
52	YSOTG2Y		203-2B
3	YSOTG3Z	TAG 3	203-2C
53	YSOTG3Y		203-2C
4	YSOBT0Z	BUS OUT BIT 0	202-2H
54	YSOBT0Y		202-2H
5	YSOBT1Z	BUS OUT BIT 1	202-2H
55	YSOBT1Y		202-2G
6	YSOBT2Z	BUS OUT BIT 2	202-2G
56	YSOBT2Y		202-2G
7	YSOBT3Z	BUS OUT BIT 3	202-2F
57	YSOBT3Y		202-2F
8	YSOBT4Z	BUS OUT BIT 4	202-2F
58	YSOBT4Y		202-2E
9	YSOBT5Z	BUS OUT BIT 5	202-2E
59	YSOBT5Y		202-2E
10	YSOBT6Z	BUS OUT BIT 6	202-2D
60	YSOBT6Y		202-2D
11	YSOBT7Z	BUS OUT BIT 7	202-2D
61	YSOBT7Y		202-2C
12	YSOBT8Z	BUS OUT BIT 8	202-2C
62	YSOBT8Y		202-2C
13	YSOBT9Z	BUS OUT BIT 9	202-2C
63	YSOBT9Y		202-2B
14	YSOOCDZ	OPEN CABLE DETECT	202-2G
64	YSOOCDY		202-2G
15	YSOBI2Z	BUS IN BIT 2 (FAULT)	205-8E
65	YSOBI2Y		205-8E

PIN NO.	FUNCTION	NAME	JUMP LOCATION
16	YSOBI3Z	BUS IN BIT 3 (SEEK ERROR)	205-8D
66	YSOBI3Y		205-8D
17	YSOBI4Z	BUS IN BIT 4 (ON CYLINDER)	205-8D
67	YSOBI4Y		205-8C
18	YSOBI0Z	BUS IN BIT 0 (INDEX)	205-8F
68	YSOBI0Y		205-8F
19	YSOBI5Z	BUS IN BIT 5 (UNIT READY)	205-8C
69	YSOBI5Y		205-8C
20	YSOBI6Z	BUS IN BIT 6 (ADDRESS MARK FOUND)	205-8B
70	YSOBI6Y		205-8B
21	YSOBSYZ	BUSY	206-8B
71	YSOBSYY		206-8A
22	YSOUSTZ	UNIT SELECT TAG	201-2F
72	YSOUSTY		201-2E
23	YSOUS0Z	UNIT SELECT 2^0	201-2E
73	YSOUS0Y		201-2D
24	YSOUS1Z	UNIT SELECT 2^1	201-2D
74	YSOUS1Y		201-2C
25	YSOBI1Z	BUS IN BIT 1 (SECTOR)	205-8F
75	YSOBI1Y		205-8E
26	YSOUS2Z	UNIT SELECT 2^2	201-2C
76	YSOUS2Y		201-2B
27	YSOUS3Z	UNIT SELECT 2^3	201-2B
77	YSOUS3Y		201-2A
28	YSOBI7Z	BUS IN BIT 7 (WRITE PROTECT)	205-8B
78	YSOBI7Y		205-8A
29	(YKSPCKO)	(POWER SEQUENCE PICK)	203-2F
69	YKSHLDO	POWER SEQUENCE HOLD	203-2F
30	YSOTG4Z	TAG 4	203-2D
60	YSOTG4Y		203-2D

"B" CABLE INTERFACE

PIN NO.	FUNCTION	NAME	JUMP LOCATION
1	XOOO	GROUND	206-8G
14	YSOSCKY	SERVO CLOCK	206-8B
2	YSOSCKZ		206-8B
15	XOOO	GROUND	206-8G
3	YSORDTZ	READ DATA	206-8C
16	YSORDTY		206-8C
4	XOOO	GROUND	206-8G
17	YSORCKY	READ CLOCK	206-8D
5	YSORCKZ		206-8C
18	XOOO	GROUND	206-8G
6	YSOWCKZ	WRITE CLOCK	202-2B
19	YSOWCKY		202-2A
7	XOOO	GROUND	206-8G
20	YSOWDTY	WRITE DATA	202-2A
8	YSOWDTZ		202-2A
21	XOOO	GROUND	206-8G
9	YSOUSDY	UNIT SELECTED	206-8D
22	YSOUSDZ		206-8D
10	YSOSKDZ	SEEK END	206-8E
23	YSOSKDY		206-8E
11	XOOO	GROUND	206-8G
24	YSOINXY	INDEX	206-8E
12	YSOINXZ		206-8F
25	XOOO	GROUND	206-8H
13	YSOSECZ	SECTOR	206-8F
26	YSOSECY		206-8F



POWER INTERFACE

PIN NO.	VOLTAGE	JUMP LOCATION
1	GND	218-2A
2	+ 5V	218-2A
3	+ 5V	218-2A
4	- 5V	218-2B
5	-12V	218-2D
6	GND	218-2C
7	+12V	218-2C
8	+24V	218-2E
9	+24V RETURN	218-2E

REV	CHNG	DESCRIPTION(SC)	APP
1	0	1983. 1.18	—

DWG ABBR	
PKG LOCATION	
PKG NAME	
051	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE

ROUTE 0 (PORT A)

INTERFACE

134-296090-051-0

NEC SHT 1/1

Nippon Electric Co.,Ltd

EQUIP

134-296090-052-0

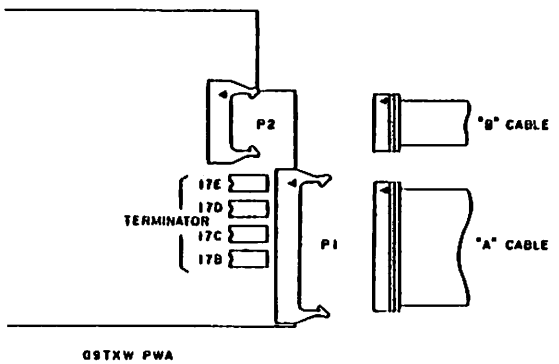
"A" CABLE INTERFACE

PIN NO.	FUNCTION	NAME	JUMP LOCATION
1	YSITG1Z	TAG 1	103-2A
31	YSITG1Y		103-2A
2	YSITG2Z	TAG 2	103-2B
32	YSITG2Y		103-2B
3	YSITG3Z	TAG 3	103-2C
33	YSITG3Y		103-2C
4	YSIBT0Z	BUS OUT BIT 0	102-2H
34	YSIBT0Y		102-2H
5	YSIBT1Z	BUS OUT BIT 1	102-2H
35	YSIBT1Y		102-2G
6	YSIBT2Z	BUS OUT BIT 2	102-2G
36	YSIBT2Y		102-2G
7	YSIBT3Z	BUS OUT BIT 3	102-2F
37	YSIBT3Y		102-2F
8	YSIBT4Z	BUS OUT BIT 4	102-2F
38	YSIBT4Y		102-2E
9	YSIBT5Z	BUS OUT BIT 5	102-2E
39	YSIBT5Y		102-2E
10	YSIBT6Z	BUS OUT BIT 6	102-2D
40	YSIBT6Y		102-2D
11	YSIBT7Z	BUS OUT BIT 7	102-2D
41	YSIBT7Y		102-2C
12	YSIBT8Z	BUS OUT BIT 8	102-2C
42	YSIBT8Y		102-2C
13	YSIBT9Z	BUS OUT BIT 9	102-2C
43	YSIBT9Y		102-2B
14	YSIOCDZ	OPEN CABLE DETECT	101-2G
44	YSIOCDY		101-2G
15	YSIBI2Z	BUS IN BIT 2 (FAULT)	104-8E
45	YSIBI2Y		104-8E

PIN NO.	FUNCTION	NAME	JUMP LOCATION
16	YSIDI3Z	BUS IN BIT 3 (SEEK ERROR)	104-8D
46	YSIBI3Y		104-8D
17	YSIBI4Z	BUS IN BIT 4 (ON CYLINDER)	104-8D
47	YSIBI4Y		104-8C
18	YSIBI0Z	BUS IN BIT 0 (INDEX)	104-8F
48	YSIBI0Y		104-8F
19	YSIBI5Z	BUS IN BIT 5 (UNIT READY)	104-8C
49	YSIBI5Y		104-8C
20	YSIBI6Z	BUS IN BIT 6 (ADDRESS MARK FOUND)	104-8B
50	YSIBI6Y		104-8B
21	YSIBSYZ	BUSY	105-8B
51	YSIBSYY		105-8A
22	YSIUSTZ	UNIT SELECT TAG	101-2F
52	YSIUSTY		101-2E
23	YSIUS0Z	UNIT SELECT 2^0	101-2E
53	YSIUS0Y		101-2D
24	YSIUS1Z	UNIT SELECT 2^1	101-2D
54	YSIUS1Y		101-2C
25	YSIBI1Z	BUS IN BIT 1 (SECTOR)	104-8F
55	YSIBI1Y		104-8E
26	YSIUS2Z	UNIT SELECT 2^2	101-2C
56	YSIUS2Y		101-2B
27	YSIUS3Z	UNIT SELECT 2^3	101-2B
57	YSIUS3Y		101-2A
28	YSIBI7Z	BUS IN BIT 7 (WRITE PROTECT)	104-8B
58	YSIBI7Y		104-8A
29	(YKSPCK0)	(POWER SEQUENCE PICK)	103-2F
59	YKSHLD0	POWER SEQUENCE HOLD	103-2F
30	YSITG4Z	TAG 4	103-2D
60	YSITG4Y		103-2D

"B" CABLE INTERFACE

PIN NO.	FUNCTION	NAME	JUMP LOCATION
1	XOOO	GROUND	105-8G
14	YSISCKY	SERVO CLOCK	105-8B
2	YSISCKZ		105-8B
15	XOOO	GROUND	105-8G
3	YSIRDTZ	READ DATA	105-8C
16	YSIRDTY		105-8C
4	XOOO	GROUND	105-8G
17	YSIRCKY	READ CLOCK	105-8D
5	YSIRCKZ		105-8C
18	XOOO	GROUND	105-8G
6	YSIWCKZ	WRITE CLOCK	102-2B
19	YSIWCKY		102-2A
7	XOOO	GROUND	105-8G
20	YSIWDTY	WRITE DATA	102-2A
8	YSIWDTZ		102-2A
21	XOOO	GROUND	105-8G
9	YSIUSDY	UNIT SELECTED	105-8D
22	YSIUSDZ		105-8D
10	YSISKDZ	SEEK END	105-8E
23	YSISKDY		105-8E
11	XOOO	GROUND	105-8G
24	YSIINXY	INDEX	105-8E
12	YSIINXZ		105-8F
25	XOOO	GROUND	105-8H
13	YSISECZ	SECTOR	105-8F
26	YSISECY		105-8F



REV	CORP	DESCRIPTION(ISC)	APP
1	0	1983,	—

DWG ABBR
PKG LOCATION
PKG NAME
052
NEXT SPEC

DRAFT	ENG	CHK	APP	ISSUE

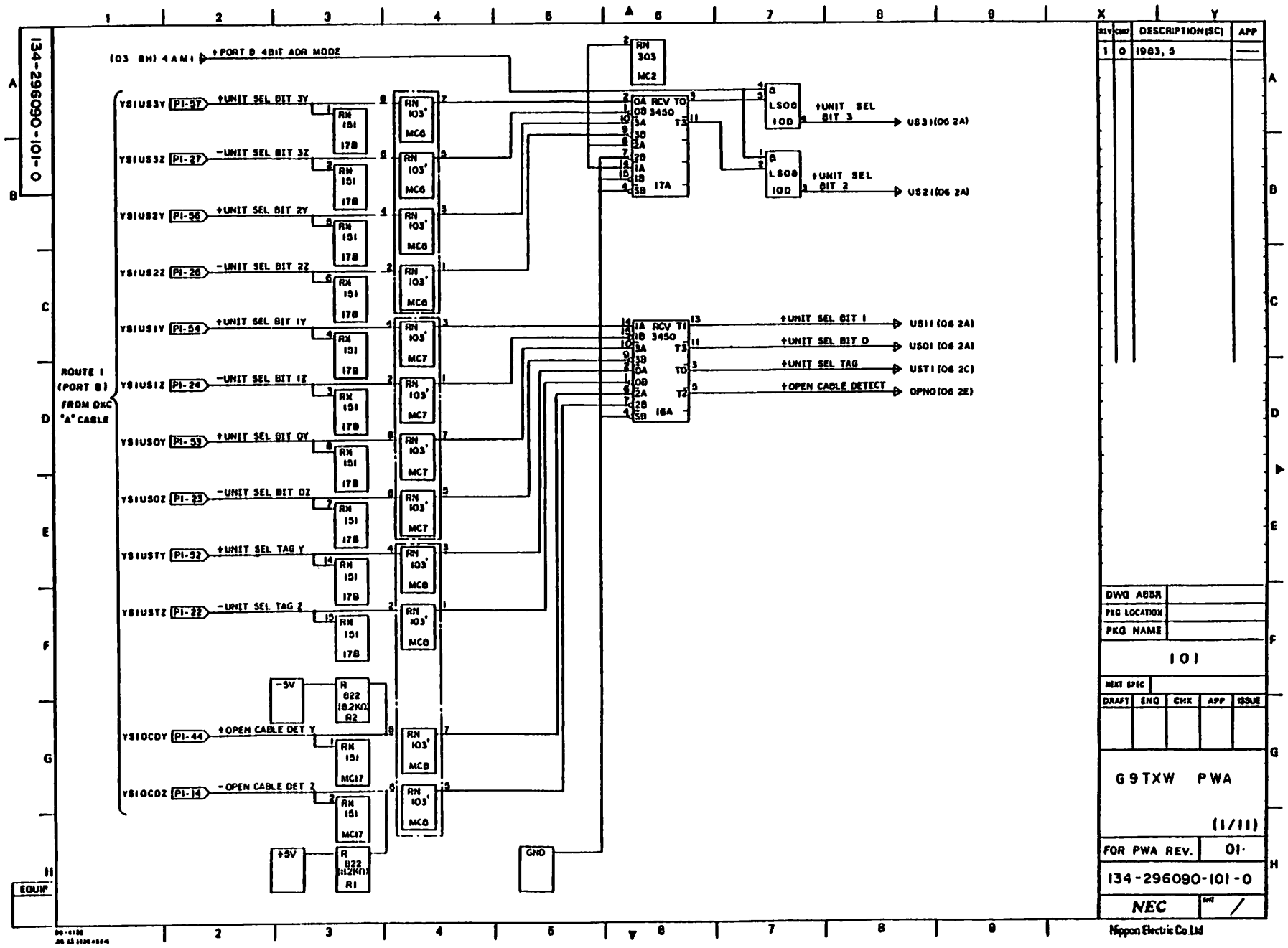
ROUTE 1 (PORT B)
INTERFACE

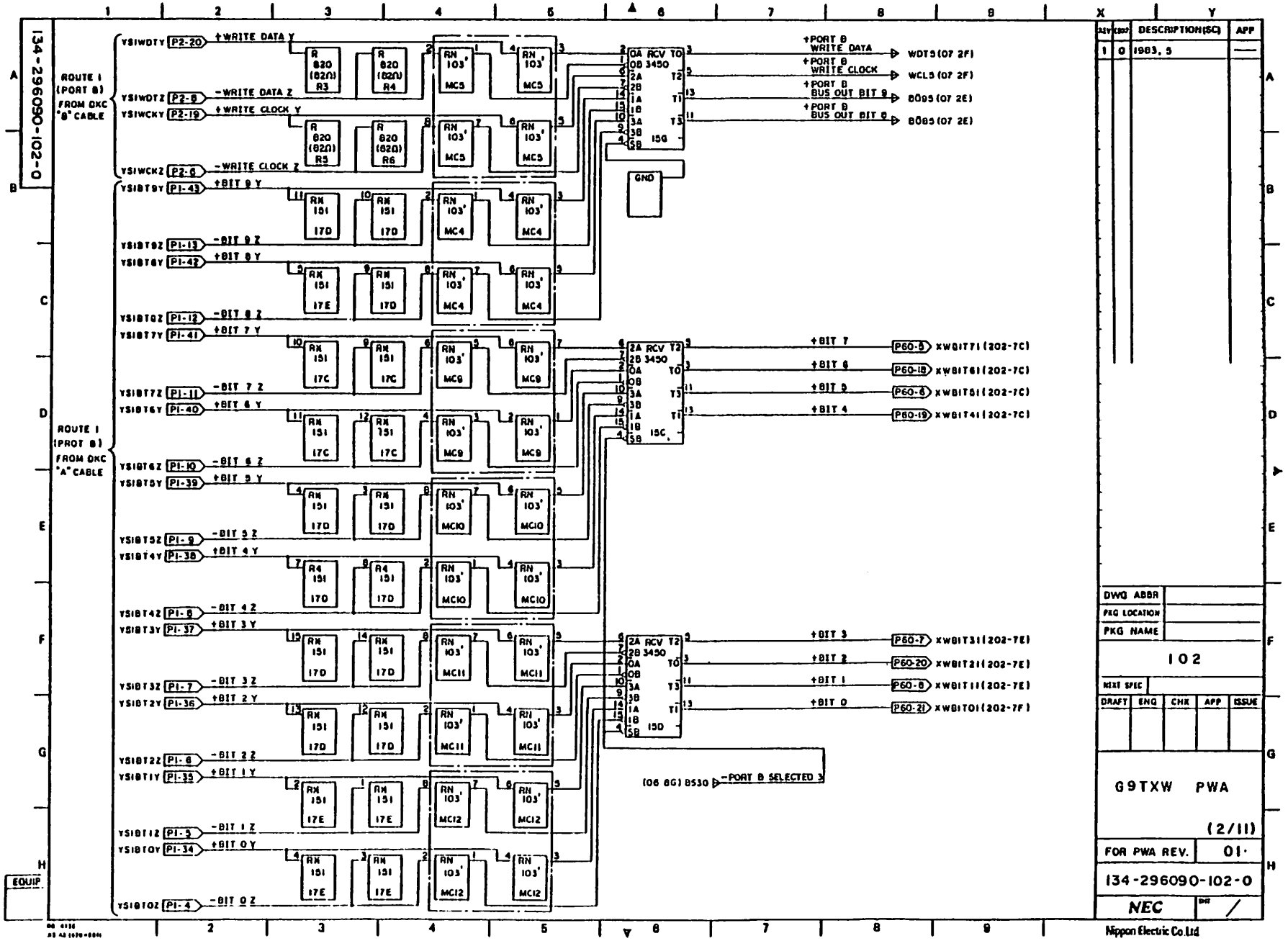
134-296090-052-0

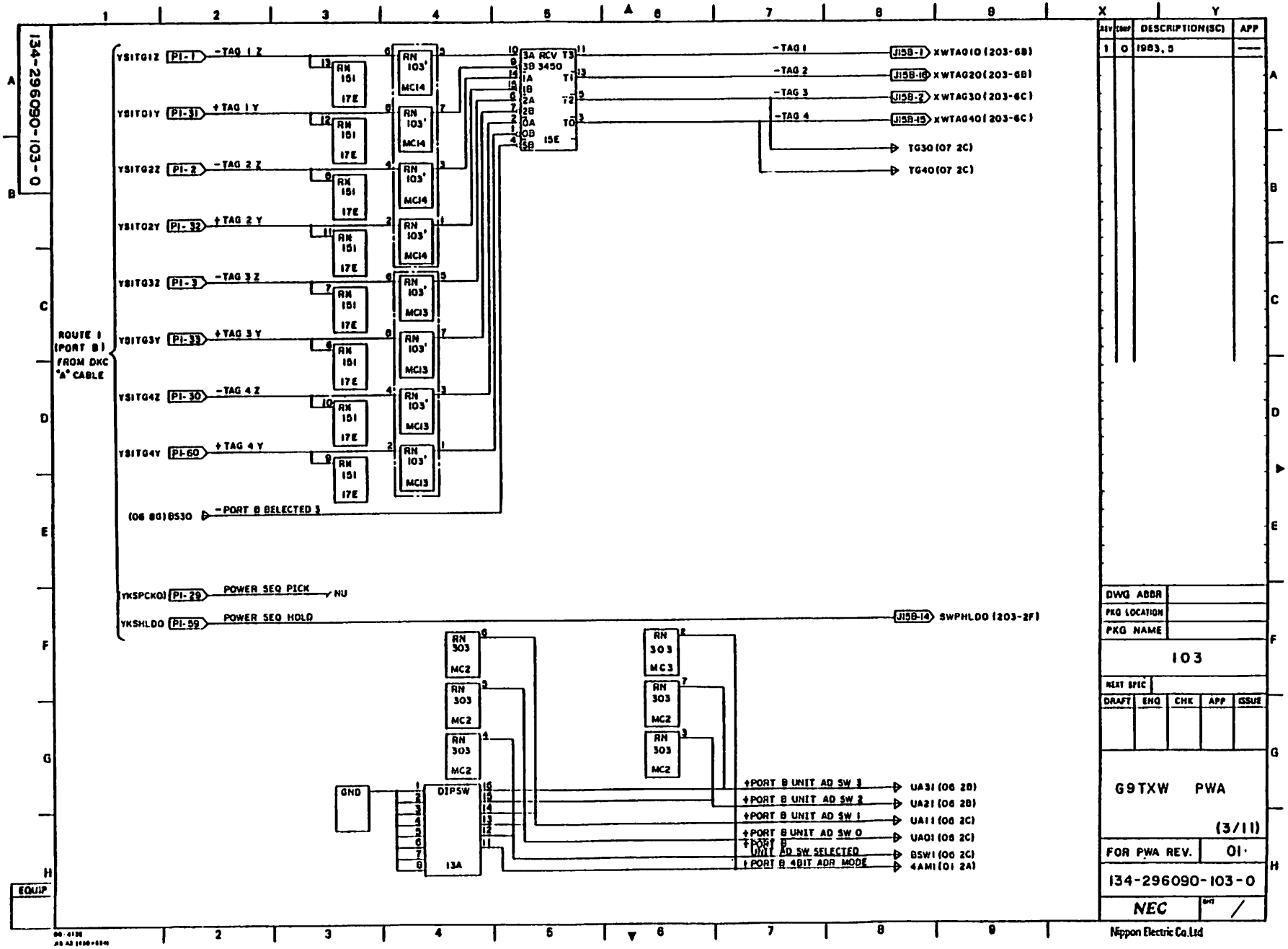
NEC SHT 1/1

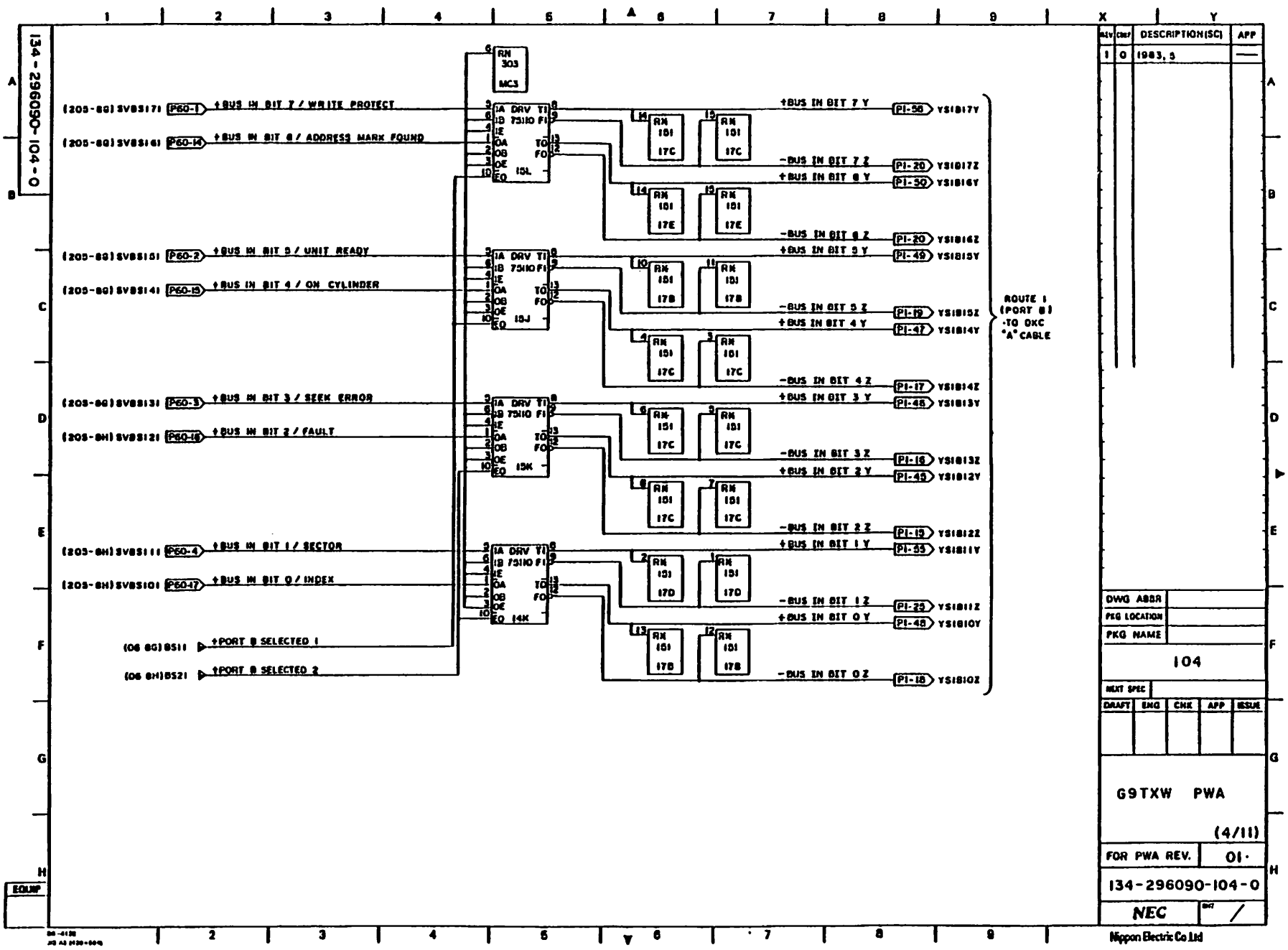
Nippon Electric Co.Ltd.

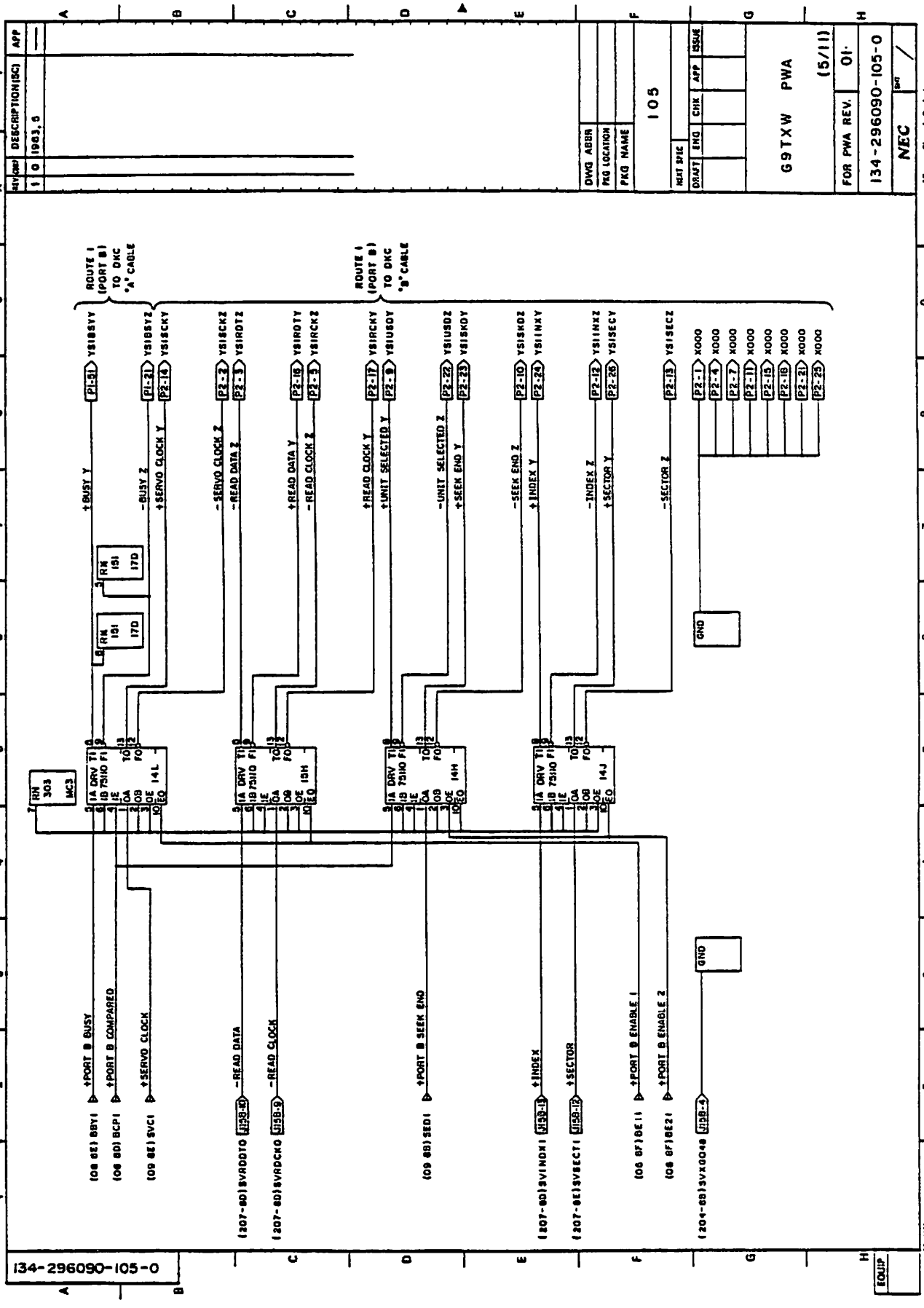
EQUIP

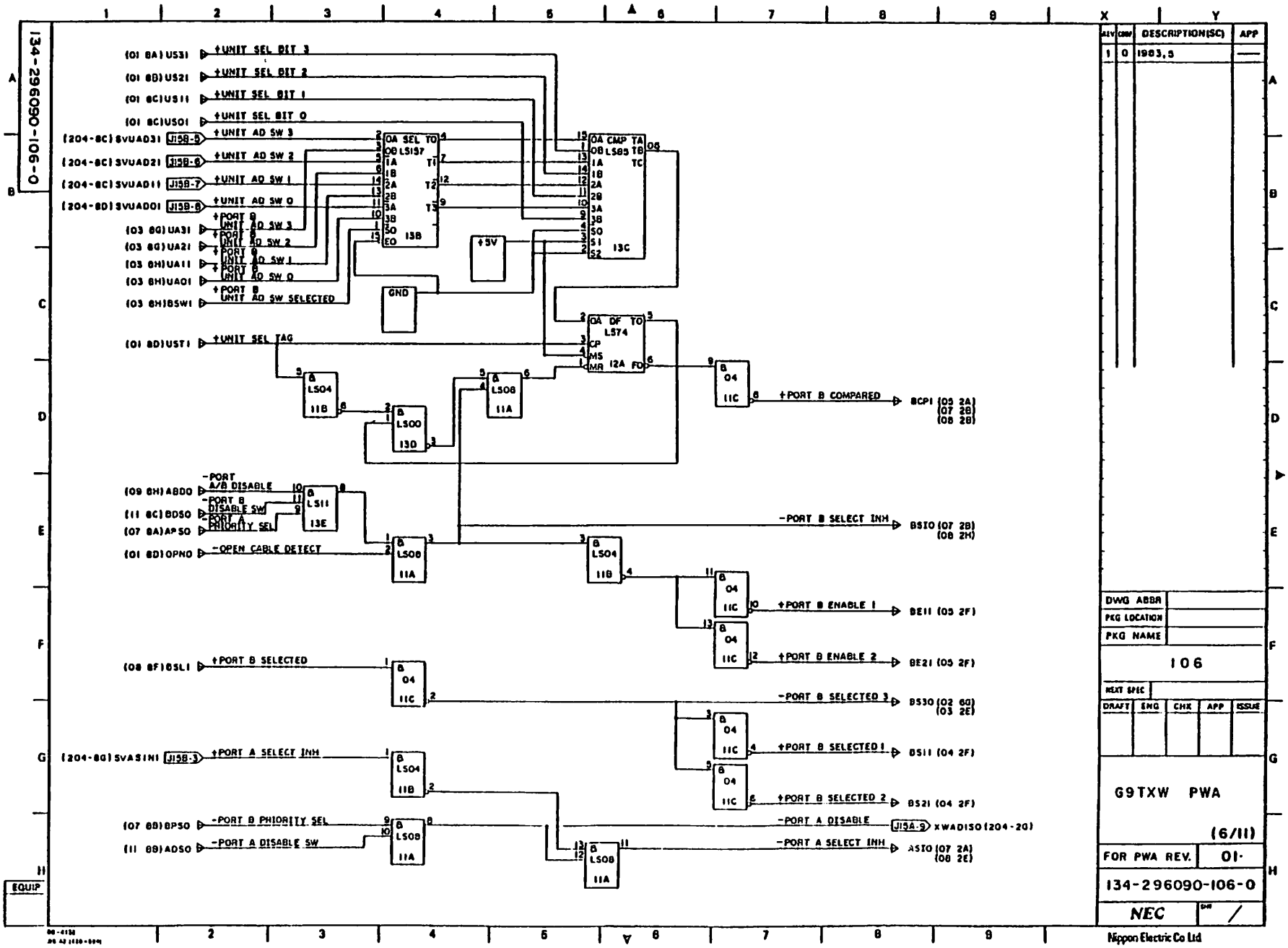

134-296090-101-0
(03 8H) 4AM1
↑PORT B 4BIT ADR MODE
YSIUS3Y PI-57 ↑UNIT SEL BIT 3Y
YSIUS3Z PI-27 -UNIT SEL BIT 3Z
YSIUS2Y PI-56 ↑UNIT SEL BIT 2Y
YSIUS2Z PI-26 -UNIT SEL BIT 2Z
YSIUS1Y PI-54 ↑UNIT SEL BIT 1Y
YSIUS1Z PI-24 -UNIT SEL BIT 1Z
YSIUS0Y PI-53 ↑UNIT SEL BIT 0Y
YSIUS0Z PI-23 -UNIT SEL BIT 0Z
YSIUSTY PI-52 ↑UNIT SEL TAG Y
YSIUSTZ PI-22 -UNIT SEL TAG Z
YSIOCDY PI-44 ↑OPEN CABLE DET Y
YSIOCDZ PI-14 -OPEN CABLE DET Z
ROUTE 1 (PORT B) FROM DXC "A" CABLE
RN 151 17B
RN 151 MC17
RN 103' MC6
RN 103' MC7
RN 103' MC8
RN 303 MC2
-5V
+5V
R 822 (8.2KΩ) R2
R 822 (1.2KΩ) R1
GND
17A RCV TO 3450 T3
16A RCV T1 3450 T3 T0 T2
LS08 10D
↑UNIT SEL BIT 3
↑UNIT SEL BIT 2
↑UNIT SEL BIT 1
↑UNIT SEL BIT 0
↑UNIT SEL TAG
↑OPEN CABLE DETECT
US31(06 2A)
US21(06 2A)
US11(06 2A)
US01(06 2A)
UST1(06 2C)
OPNO(06 2E)
EQUIP
DESCRIPTION(SC)
1 0 1983. 5
APP
DWG ABBR
PKG LOCATION
PKG NAME
101
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9TXW PWA
(1/11)
FOR PWA REV. 01
134-296090-101-0
NEC
Nippon Electric Co.Ltd

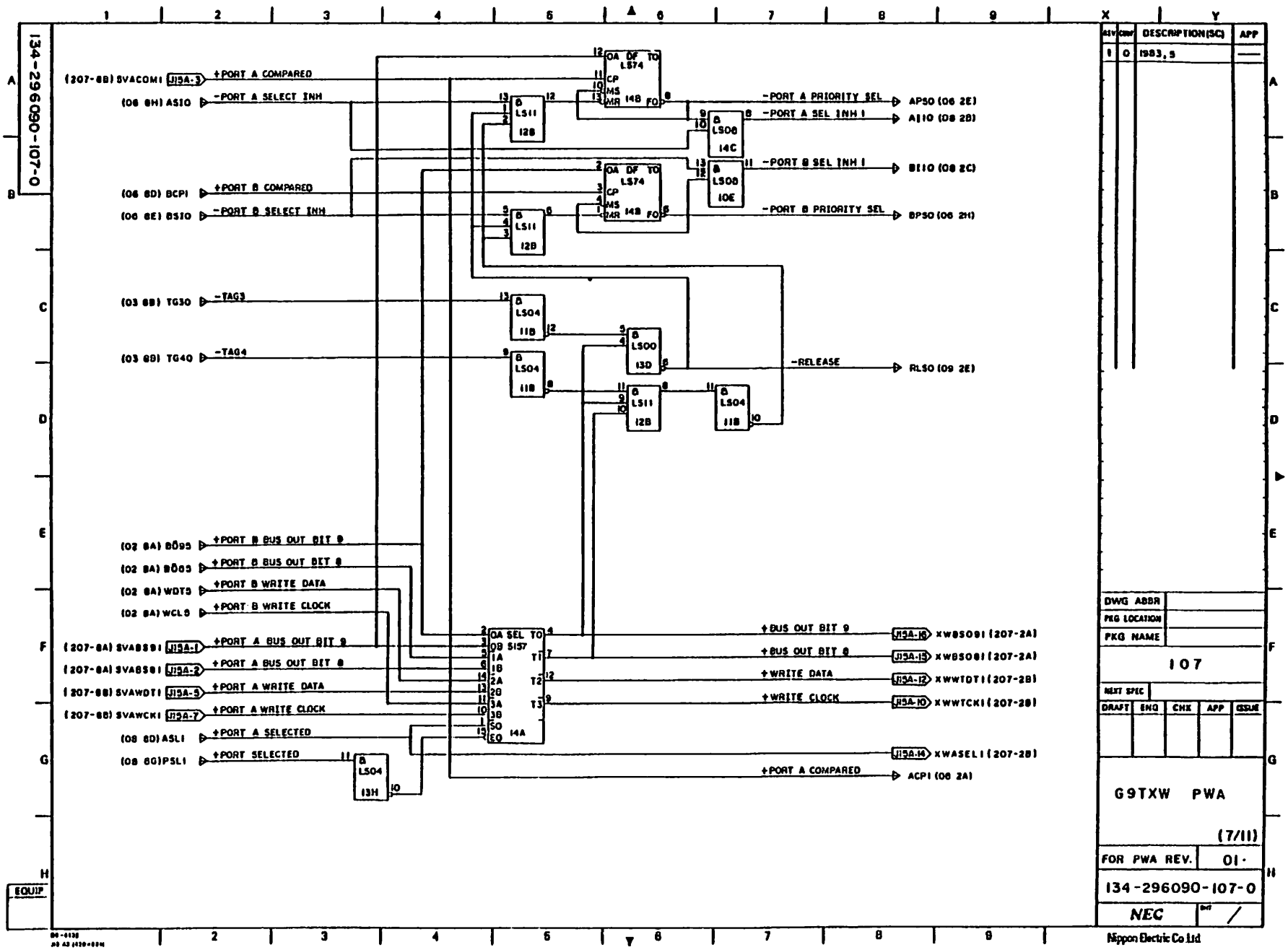

134-296090-102-0
ROUTE 1 (PORT B) FROM OKC "B" CABLE
ROUTE 1 (PROT B) FROM OKC "A" CABLE
EQUIP
YSIWDTY P2-20 +WRITE DATA Y
YSIWDTZ P2-9 -WRITE DATA Z
YSIWCKY P2-19 +WRITE CLOCK Y
YSIWCKZ P2-6 -WRITE CLOCK Z
YSIBT9Y P1-43 +BIT 9 Y
YSIBT9Z P1-13 -BIT 9 Z
YSIBT8Y P1-42 +BIT 8 Y
YSIBT8Z P1-12 -BIT 8 Z
YSIBT7Y P1-41 +BIT 7 Y
YSIBT7Z P1-11 -BIT 7 Z
YSIBT6Y P1-40 +BIT 6 Y
YSIBT6Z P1-10 -BIT 6 Z
YSIBT5Y P1-39 +BIT 5 Y
YSIBT5Z P1-9 -BIT 5 Z
YSIBT4Y P1-38 +BIT 4 Y
YSIBT4Z P1-8 -BIT 4 Z
YSIBT3Y P1-37 +BIT 3 Y
YSIBT3Z P1-7 -BIT 3 Z
YSIBT2Y P1-36 +BIT 2 Y
YSIBT2Z P1-6 -BIT 2 Z
YSIBT1Y P1-35 +BIT 1 Y
YSIBT1Z P1-5 -BIT 1 Z
YSIBT0Y P1-34 +BIT 0 Y
YSIBT0Z P1-4 -BIT 0 Z
R 820 (82Ω) R3
R 820 (82Ω) R4
R 820 (82Ω) R5
R 820 (82Ω) R6
RN 103' MC5
RN 103' MC4
RN 103' MC9
RN 103' MC10
RN 103' MC11
RN 103' MC12
RN 151 17D
RN 151 17E
RN 151 17C
R4 151 17D
0A RCV T0
0B 3450
2A T2
2B
1A T1
1B
3A T3
3B 15G
5B
GND
2A RCV T2
2B 3450
0A T0
0B
3A T3
3B
1A T1
1B 15C
5B
2A RCV T2
2B 3450
0A T0
0B
3A T3
3B
1A T1
1B 15D
5B
+PORT B WRITE DATA
+PORT B WRITE CLOCK
+PORT B BUS OUT BIT 9
+PORT B BUS OUT BIT 8
WDT5 (07 2F)
WCL5 (07 2F)
B09 5 (07 2E)
B08 5 (07 2E)
+BIT 7
+BIT 6
+BIT 5
+BIT 4
P60-5 XWBIT7 (202-7C)
P60-18 XWBIT6 (202-7C)
P60-6 XWBIT5 (202-7C)
P60-19 XWBIT4 (202-7C)
+BIT 3
+BIT 2
+BIT 1
+BIT 0
P60-7 XWBIT3 (202-7E)
P60-20 XWBIT2 (202-7E)
P60-8 XWBIT1 (202-7E)
P60-21 XWBIT0 (202-7F)
(06 8G) BS30 -PORT B SELECTED
REV
DESCRIPTION(SC)
APP
1 0 1983. 5
DWG ABBR
PKG LOCATION
PKG NAME
102
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9TXW PWA
(2/11)
FOR PWA REV. 01·
134-296090-102-0
NEC
Nippon Electric Co.Ltd

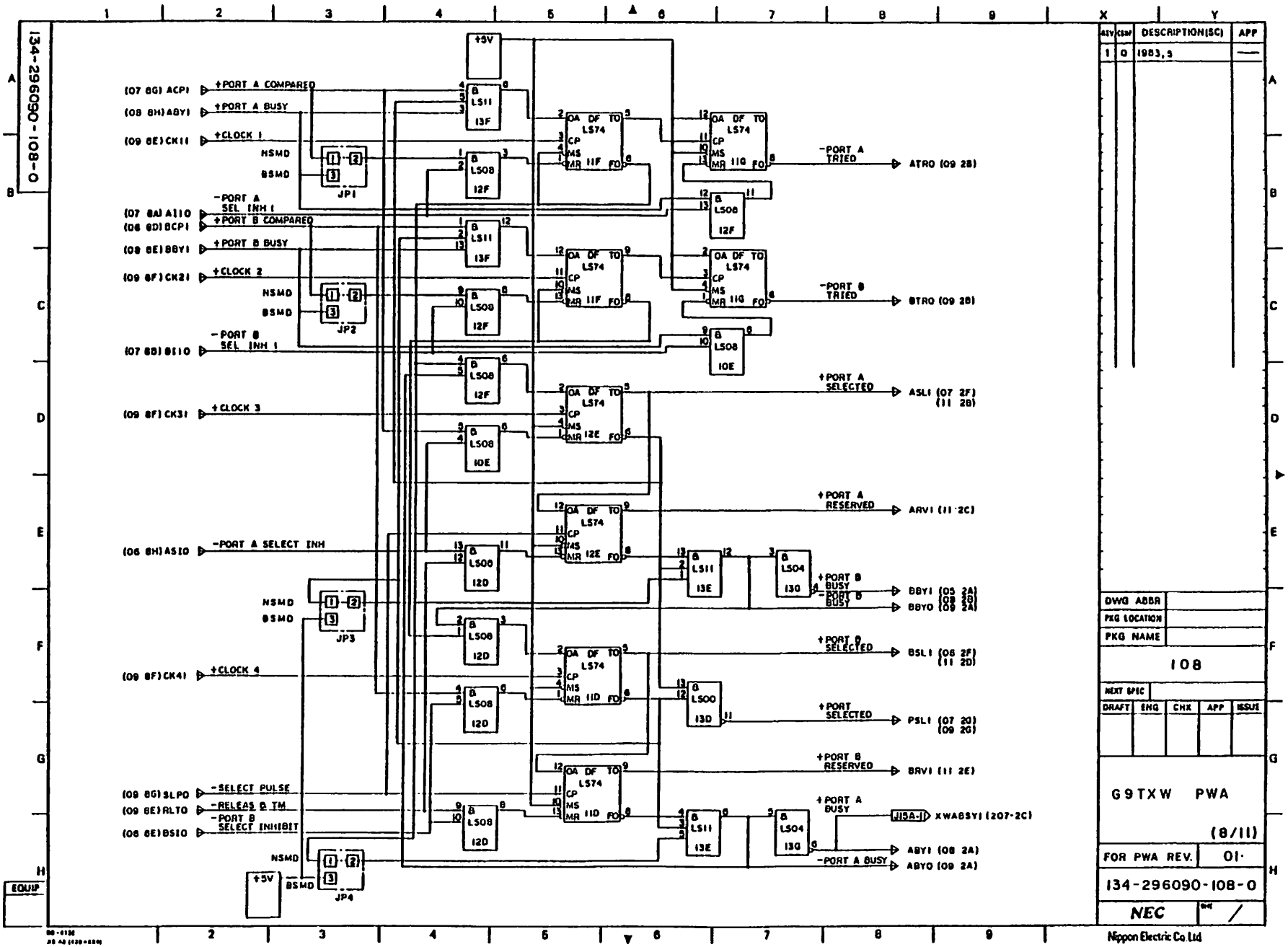

134-296090-103-0
ROUTE 1 (PORT B) FROM DKC "A" CABLE
YSITG1Z PI-1 -TAG 1 Z
YSITG1Y PI-31 +TAG 1 Y
YSITG2Z PI-2 -TAG 2 Z
YSITG2Y PI-32 +TAG 2 Y
YSITG3Z PI-3 -TAG 3 Z
YSITG3Y PI-33 +TAG 3 Y
YSITG4Z PI-30 -TAG 4 Z
YSITG4Y PI-60 +TAG 4 Y
RN 151 17E
RN 103' MC14
RN 103' MC13
3A RCV T3
3B 3450
1A T1
1B
2A T2
2B
0A T0
0B
5B 15E
-TAG 1
-TAG 2
-TAG 3
-TAG 4
J15B-1 XWTAG10 (203-6B)
J15B-10 XWTAG20 (203-6B)
J15B-2 XWTAG30 (203-6C)
J15B-15 XWTAG40 (203-6C)
TG30 (07 2C)
TG40 (07 2C)
(06 8G) BS30 -PORT B SELECTED 3
YKSPCK01 PI-29 POWER SEQ PICK NU
YKSHLD0 PI-59 POWER SEQ HOLD
J15B-14 SWPHLD0 (203-2F)
RN 303 MC2
RN 303 MC3
GND
DIPSW
13A
+PORT B UNIT AD SW 3
+PORT B UNIT AD SW 2
+PORT B UNIT AD SW 1
+PORT B UNIT AD SW 0
+PORT B UNIT AD SW SELECTED
+PORT B 4BIT ADR MODE
UA31 (06 2B)
UA21 (06 2B)
UA11 (06 2C)
UA01 (06 2C)
BSW1 (06 2C)
4AM1 (01 2A)
EQUIP
REV
CHNG
DESCRIPTION(SC)
APP
1
0
1983. 5
DWG ABBR
PKG LOCATION
PKG NAME
103
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9TXW PWA
(3/11)
FOR PWA REV.
01
134-296090-103-0
NEC
Nippon Electric Co.Ltd

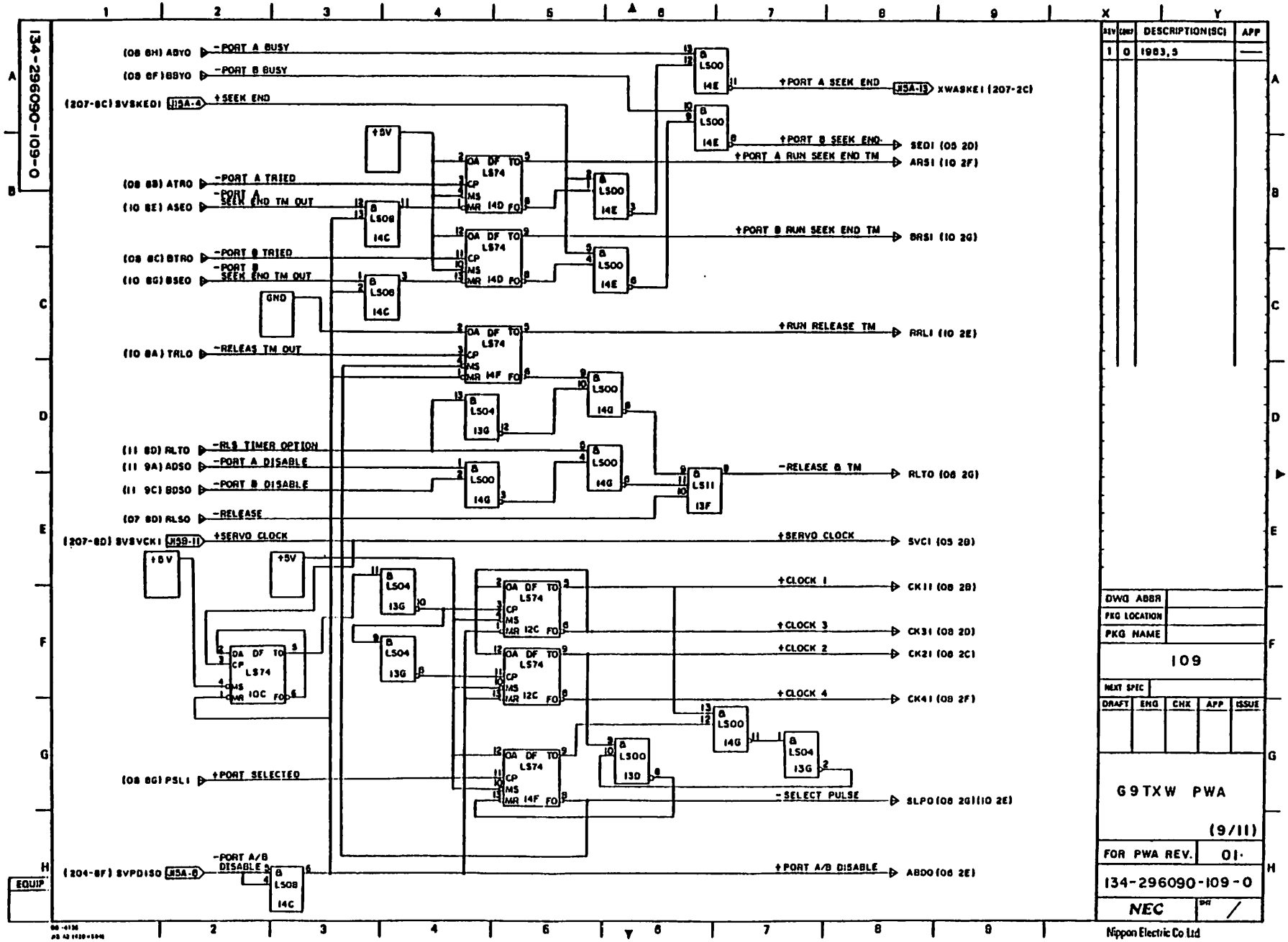

134-296090-104-0
(205-8G) SVBS17I P60-1 †BUS IN BIT 7 / WRITE PROTECT
(205-8G) SVBS16I P60-14 †BUS IN BIT 6 / ADDRESS MARK FOUND
(205-8G) SVBS15I P60-2 †BUS IN BIT 5 / UNIT READY
(205-8G) SVBS14I P60-15 †BUS IN BIT 4 / ON CYLINDER
(205-8G) SVBS13I P60-3 †BUS IN BIT 3 / SEEK ERROR
(205-8H) SVBS12I P60-16 †BUS IN BIT 2 / FAULT
(205-8H) SVBS11I P60-4 †BUS IN BIT 1 / SECTOR
(205-8H) SVBS10I P60-17 †BUS IN BIT 0 / INDEX
(06 8G) BS11 †PORT B SELECTED 1
(06 8H) BS21 †PORT B SELECTED 2
RN 303 MC3
15L
15J
15K
14K
RN 151 17C
RN 151 17E
RN 151 17B
RN 151 17D
†BUS IN BIT 7 Y
-BUS IN BIT 7 Z
†BUS IN BIT 6 Y
-BUS IN BIT 6 Z
†BUS IN BIT 5 Y
-BUS IN BIT 5 Z
†BUS IN BIT 4 Y
-BUS IN BIT 4 Z
†BUS IN BIT 3 Y
-BUS IN BIT 3 Z
†BUS IN BIT 2 Y
-BUS IN BIT 2 Z
†BUS IN BIT 1 Y
-BUS IN BIT 1 Z
†BUS IN BIT 0 Y
-BUS IN BIT 0 Z
P1-56 Y5IBI7Y
P1-20 Y5IBI7Z
P1-50 Y5IBI6Y
P1-20 Y5IBI6Z
P1-49 Y5IBI5Y
P1-19 Y5IBI5Z
P1-47 Y5IBI4Y
P1-17 Y5IBI4Z
P1-48 Y5IBI3Y
P1-16 Y5IBI3Z
P1-45 Y5IBI2Y
P1-15 Y5IBI2Z
P1-55 Y5IBI1Y
P1-25 Y5IBI1Z
P1-46 Y5IBI0Y
P1-18 Y5IBI0Z
ROUTE 1 (PORT B) -TO OXC "A" CABLE
REV 1 CHG 0 DESCRIPTION(SC) 1983.5 APP —
DWG ABBR
PKG LOCATION
PKG NAME
104
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9TXW PWA
(4/11)
FOR PWA REV. 01·
134-296090-104-0
NEC
Nippon Electric Co Ltd
EQUIP

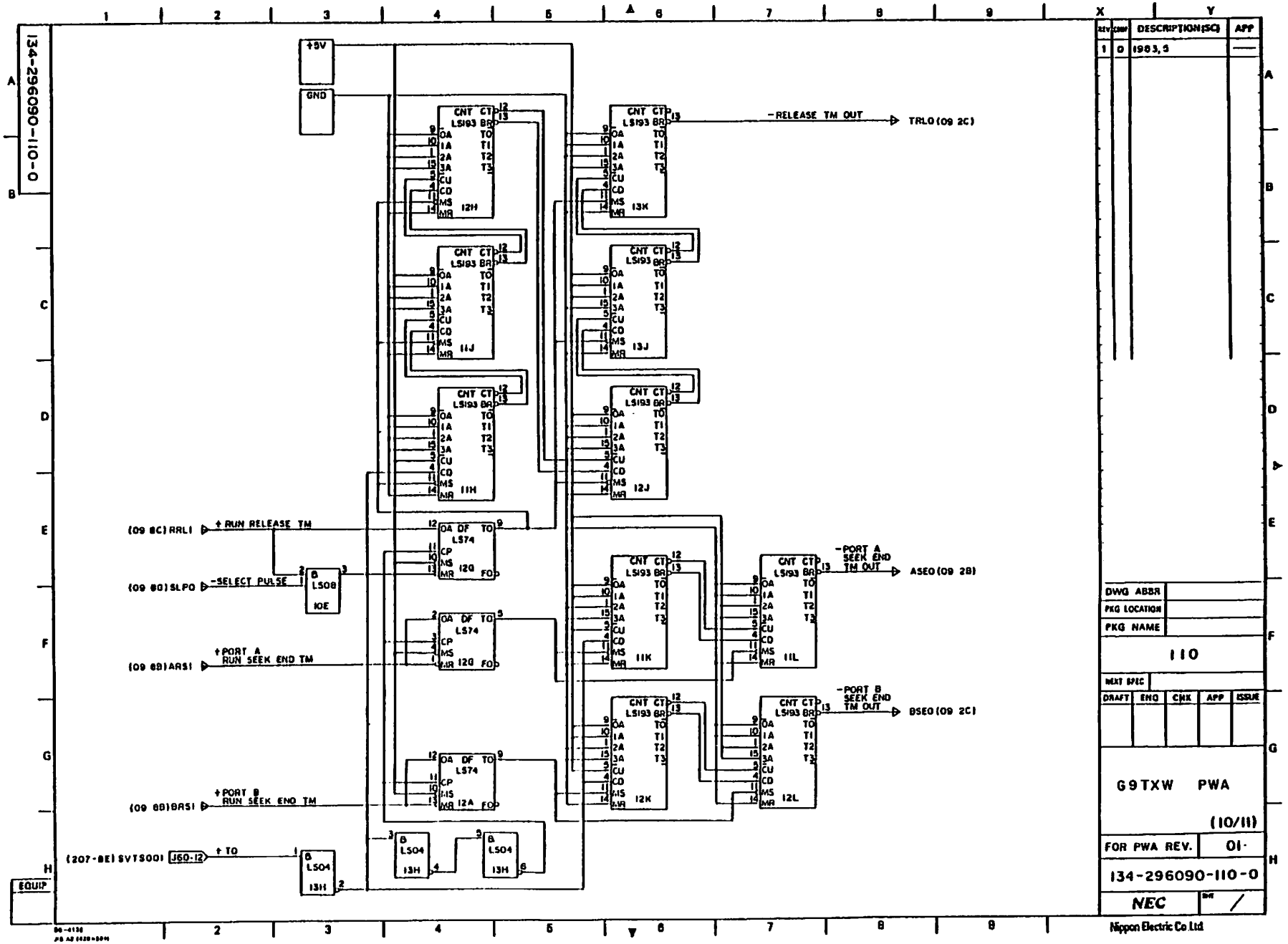

134-296090-105-0
G9TXW PWA
(5/11)
FOR PWA REV. 01
134-296090-105-0
NEC
Nippon Electric Co.Ltd
105
ROUTE 1 (PORT B) TO DKC "A" CABLE
ROUTE 1 (PORT B) TO DKC "B" CABLE
+PORT B BUSY
+PORT B COMPARED
+SERVO CLOCK
-READ DATA
-READ CLOCK
+PORT B SEEK END
+INDEX
+SECTOR
+PORT B ENABLE 1
+PORT B ENABLE 2
GND
+BUSY Y
-BUSY Z
+SERVO CLOCK Y
-SERVO CLOCK Z
-READ DATA Z
+READ DATA Y
-READ CLOCK Z
+READ CLOCK Y
+UNIT SELECTED Y
-UNIT SELECTED Z
+SEEK END Y
-SEEK END Z
+INDEX Y
-INDEX Z
+SECTOR Y
-SECTOR Z
XOOO

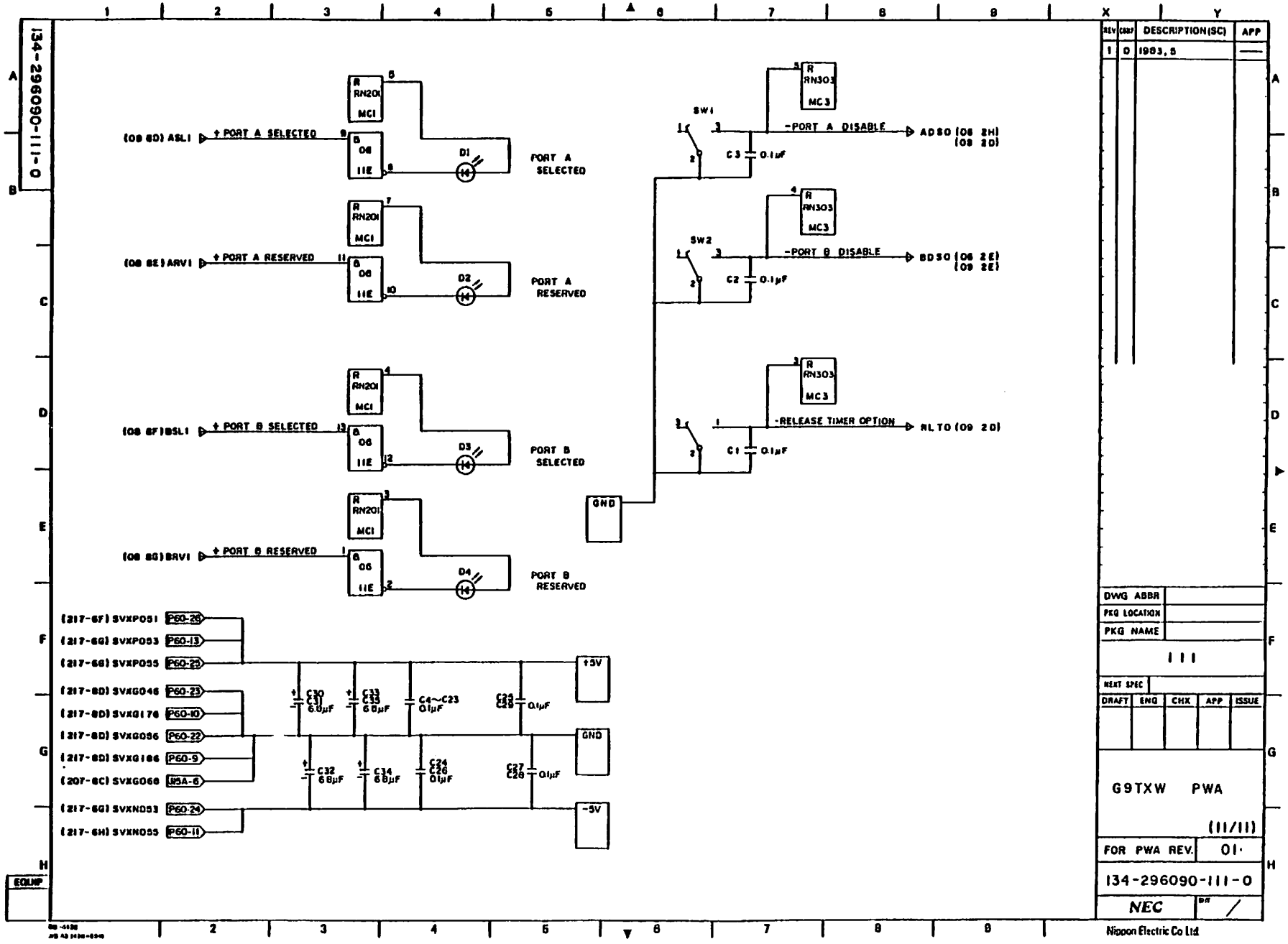

134-296090-106-0
(01 8A) US3I
(01 8B) US2I
(01 8C) US1I
(01 8C) US0I
+UNIT SEL BIT 3
+UNIT SEL BIT 2
+UNIT SEL BIT 1
+UNIT SEL BIT 0
(204-8C) SVUAD3I J158-5
(204-8C) SVUAD2I J158-6
(204-8C) SVUAD1I J158-7
(204-8D) SVUAD0I J158-8
+UNIT AD SW 3
+UNIT AD SW 2
+UNIT AD SW 1
+UNIT AD SW 0
(03 8G) UA3I
(03 8G) UA2I
(03 8H) UA1I
(03 8H) UA0I
(03 8H) BSWI
+PORT B UNIT AD SW 3
+PORT B UNIT AD SW 2
+PORT B UNIT AD SW 1
+PORT B UNIT AD SW 0
+PORT B UNIT AD SW SELECTED
LS157
13B
13C
LS85
LS74
12A
+5V
GND
(01 8D) UST1
+UNIT SEL TAG
LS04
LS00
LS08
LS11
LS32
11B
13D
11A
13E
11C
+PORT B COMPARED
BCP1 (05 2A) (07 2B) (08 2B)
(09 8H) ABDO
(11 8C) BDSO
(07 8A) APSO
(01 8D) OPNO
-PORT A/B DISABLE
-PORT B DISABLE SW
-PORT A PRIORITY SEL
-OPEN CABLE DETECT
-PORT B SELECT INH
BSI0 (07 2B) (08 2H)
+PORT B ENABLE 1
BE1I (05 2F)
+PORT B ENABLE 2
BE2I (05 2F)
(08 8F) BSLI
+PORT B SELECTED
-PORT B SELECTED 3
BS3O (02 6D) (03 2E)
+PORT B SELECTED 1
BS1I (04 2F)
+PORT B SELECTED 2
BS2I (04 2F)
(204-8G) SVASINI J158-3
+PORT A SELECT INH
(07 8B) BPSO
(11 8B) ADSO
-PORT B PRIORITY SEL
-PORT A DISABLE SW
-PORT A DISABLE
J15A-9 XWADISO (204-2D)
-PORT A SELECT INH
ASI0 (07 2A) (08 2E)
EQUIP
REV
DESCRIPTION(SC)
APP
1
0
1983.5
DWG ABBR
PKG LOCATION
PKG NAME
106
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9TXW PWA
(6/11)
FOR PWA REV.
01·
134-296090-106-0
NEC
Nippon Electric Co Ltd

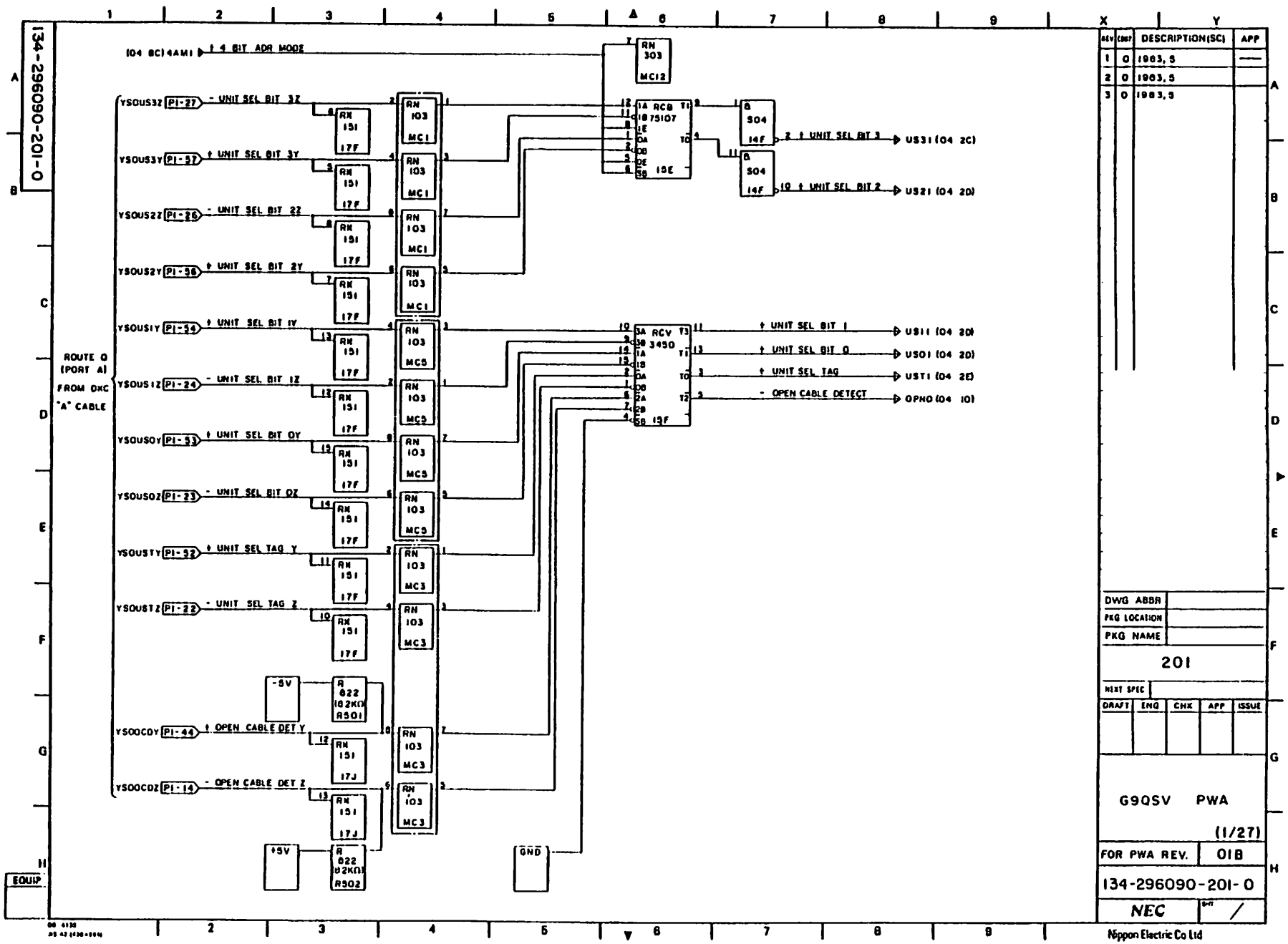

134-296090-107-0
(207-6B) SVACOM1 J15A-3 +PORT A COMPARED
(06 6H) AS10 -PORT A SELECT INH
(06 6D) BCP1 +PORT B COMPARED
(06 6E) BS10 -PORT B SELECT INH
(03 6B) TG30 -TAG3
(03 6B) TG40 -TAG4
(02 8A) BD95 +PORT B BUS OUT BIT 9
(02 8A) BD03 +PORT B BUS OUT BIT 8
(02 8A) WDT3 +PORT B WRITE DATA
(02 8A) WCL3 +PORT B WRITE CLOCK
(207-8A) SVAB91 J15A-1 +PORT A BUS OUT BIT 9
(207-8A) SVAB81 J15A-2 +PORT A BUS OUT BIT 8
(207-8B) SVAWDT1 J15A-5 +PORT A WRITE DATA
(207-8B) SVAWCK1 J15A-7 +PORT A WRITE CLOCK
(08 6D) AS11 +PORT A SELECTED
(08 6G) PS11 +PORT SELECTED
-PORT A PRIORITY SEL APS0 (06 2E)
-PORT A SEL INH 1 A110 (08 2B)
-PORT B SEL INH 1 B110 (08 2C)
-PORT B PRIORITY SEL BPS0 (06 2H)
-RELEASE RLS0 (09 2E)
+BUS OUT BIT 9 J15A-16 XWBS091 (207-2A)
+BUS OUT BIT 8 J15A-15 XWBS081 (207-2A)
+WRITE DATA J15A-12 XWWTDT1 (207-2B)
+WRITE CLOCK J15A-10 XWWTCK1 (207-2B)
J15A-14 XWASEL1 (207-2B)
+PORT A COMPARED ACP1 (06 2A)
DESCRIPTION(SC)
1983, 5
DWG ABBR
PKG NAME
107
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9TXW PWA
(7/11)
FOR PWA REV. 01
134-296090-107-0
NEC
Nippon Electric Co Ltd
EQUIP

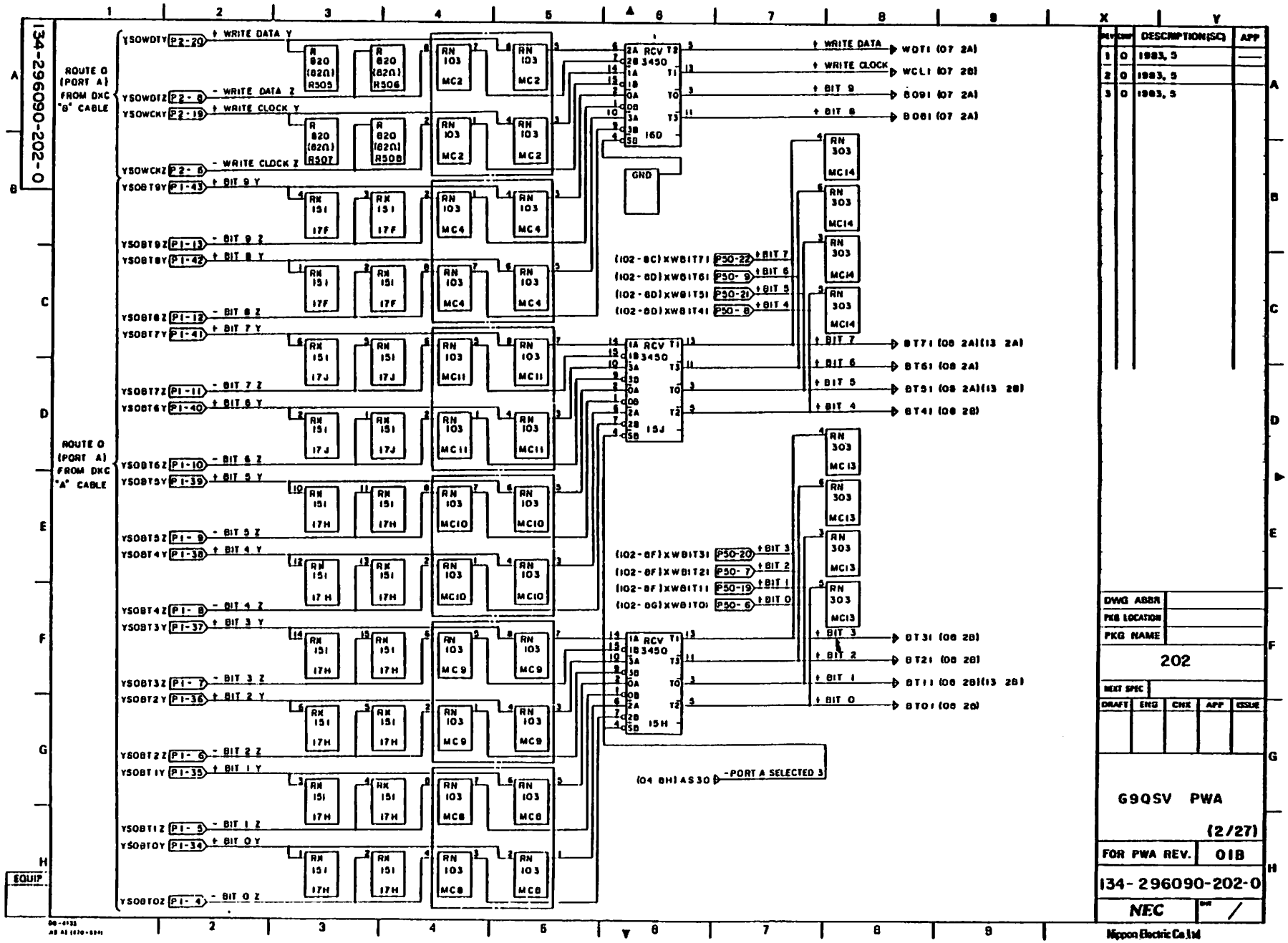

134-296090-108-0
+5V
(07 8G) ACP1
+PORT A COMPARED
(08 8H) ABY1
+PORT A BUSY
(09 8E) CK11
+CLOCK 1
NSMD
BSMD
JP1
-PORT A SEL INH 1
(07 8A) A110
(06 8D) BCP1
+PORT B COMPARED
(08 8E) BBY1
+PORT B BUSY
(09 8F) CK21
+CLOCK 2
JP2
-PORT B SEL INH 1
(07 8B) B110
(09 8F) CK31
+CLOCK 3
(06 8H) ASI0
-PORT A SELECT INH
JP3
(09 8F) CK41
+CLOCK 4
(09 8G) SLP0
-SELECT PULSE
(09 8E) RLT0
-RELEASE TIM
(06 8E) BSI0
-PORT B SELECT INHIBIT
JP4
LS11 13F
LS08 12F
LS74 11F
LS08 10E
LS74 12E
LS08 12D
LS74 11D
LS11 13E
LS04 13G
LS00 13D
-PORT A TRIED
ATR0 (09 2B)
-PORT B TRIED
BTR0 (09 2B)
+PORT A SELECTED
ASL1 (07 2F) (11 2B)
+PORT A RESERVED
ARV1 (11 2C)
+PORT B BUSY
-PORT B BUSY
BBY1 (05 2A) (08 2D) (09 2A)
BBY0 (09 2A)
+PORT B SELECTED
BSL1 (06 2F) (11 2D)
+PORT SELECTED
PSL1 (07 2D) (09 2C)
+PORT B RESERVED
BRV1 (11 2E)
+PORT A BUSY
J15A-J1
XWABSY1 (207-2C)
ABY1 (08 2A)
-PORT A BUSY
ABY0 (09 2A)
EQUIP
REV
DESCRIPTION(SC)
APP
1 0 1983.3
DWG ABBR
PKG LOCATION
PKG NAME
108
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9TXW PWA
(8/11)
FOR PWA REV. 01
134-296090-108-0
NEC
Nippon Electric Co.Ltd

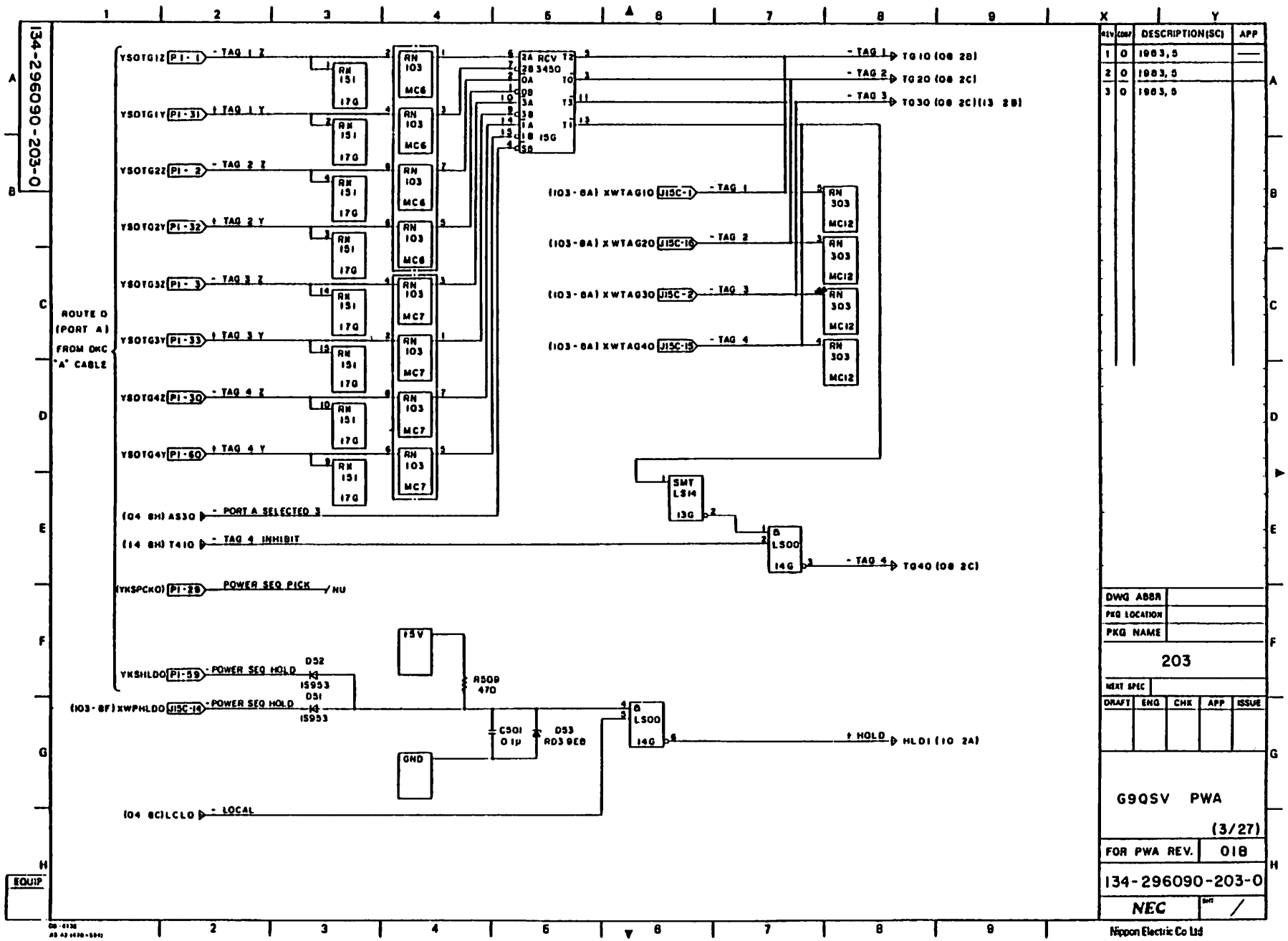

134-296090-109-0
(08 8H) ABYO -PORT A BUSY
(08 8F) BBYO -PORT B BUSY
(207-8C) SVSKED1 J15A-4 +SEEK END
(08 8B) ATRO -PORT A TRIED
(10 8E) ASEO -PORT A SEEK END TM OUT
(08 8C) BTRO -PORT B TRIED
(10 8G) BSEO -PORT B SEEK END TM OUT
(10 8A) TRLO -RELEAS TM OUT
(11 8D) RLTO -RLS TIMER OPTION
(11 9A) ADSO -PORT A DISABLE
(11 9C) BDSO -PORT B DISABLE
(07 8D) RLSO -RELEASE
(207-8D) SVSVCK1 J59-11 +SERVO CLOCK
(08 8G) PSL1 +PORT SELECTED
(204-8F) SVPDIS0 J15A-6 -PORT A/B DISABLE
+PORT A SEEK END J15A-13 XWASKE1 (207-2C)
+PORT B SEEK END SED1 (05 2D)
+PORT A RUN SEEK END TM ARS1 (10 2F)
+PORT B RUN SEEK END TM BRS1 (10 2G)
+RUN RELEASE TM RRL1 (10 2E)
-RELEASE B TM RLT0 (08 2G)
+SERVO CLOCK SVC1 (05 2B)
+CLOCK 1 CK11 (08 2B)
+CLOCK 3 CK31 (08 2D)
+CLOCK 2 CK21 (08 2C)
+CLOCK 4 CK41 (08 2F)
-SELECT PULSE SLP0 (08 2G)(10 2E)
+PORT A/B DISABLE ABD0 (06 2E)
+5V
GND
LS74
LS00
LS04
LS08
LS11
14C
14D
14E
14F
14G
13G
13F
13O
12C
10C
DESCRIPTION(SC)
1983.5
DWG ABBR
PKG LOCATION
PKG NAME
109
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9TXW PWA
(9/11)
FOR PWA REV. 01
134-296090-109-0
NEC
Nippon Electric Co Ltd
EQUIP

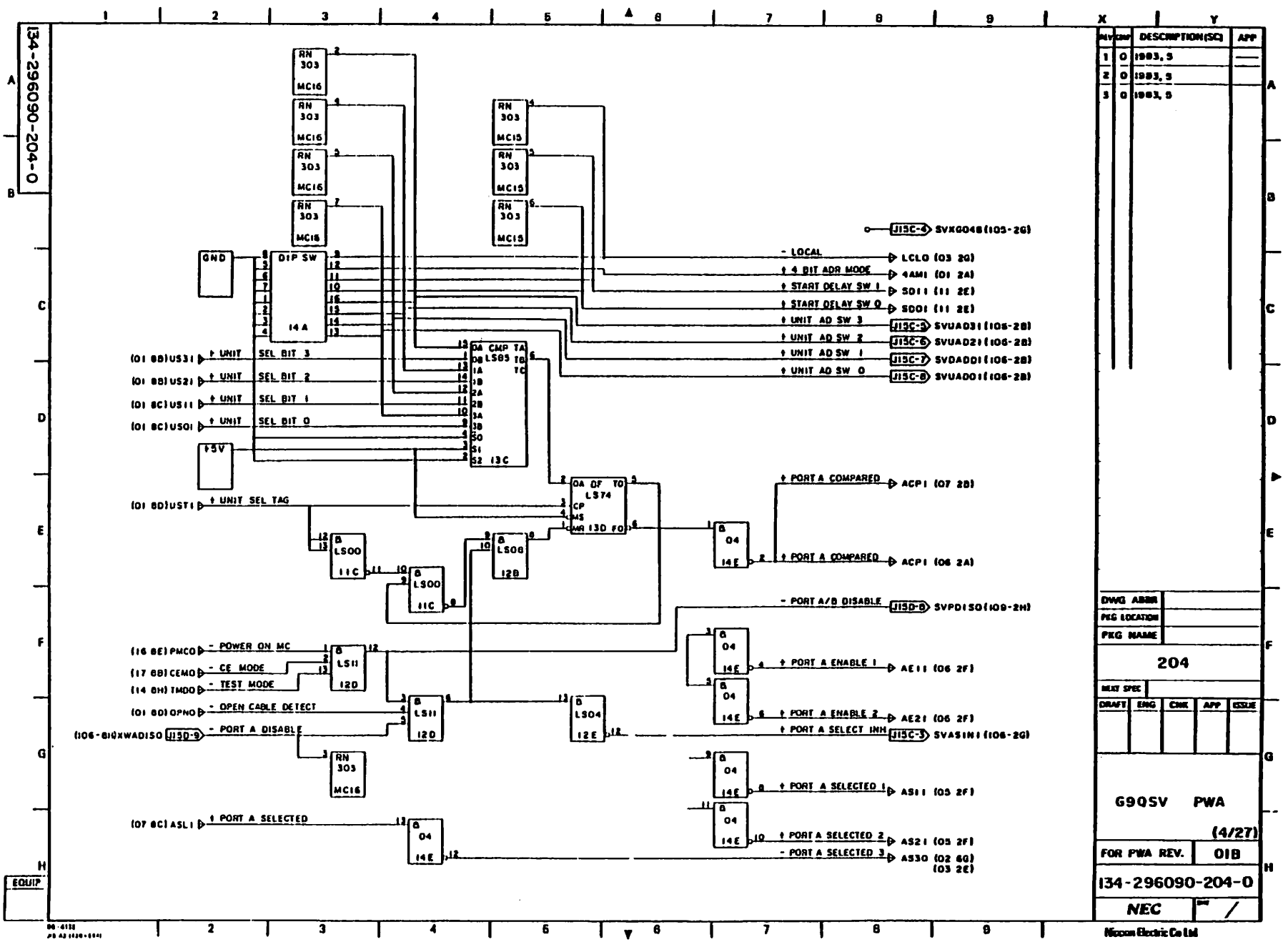

134-296090-110-0
+5V
GND
CNT CT LS193 BR
12H
11J
11H
13K
13J
12J
11K
11L
12K
12L
-RELEASE TM OUT
TRLO (09 2C)
(09 8C) RRLI
+RUN RELEASE TM
(09 8D) SLPO
-SELECT PULSE
LS08 10E
OA DF TO LS74 CP MS MR 12G FO
(09 8B) ARSI
+PORT A RUN SEEK END TM
(09 8B) BRSI
+PORT B RUN SEEK END TM
12A
-PORT A SEEK END TM OUT
ASEO (09 2B)
-PORT B SEEK END TM OUT
BSEO (09 2C)
(207-8E) SVTS001
J60-12
+TO
LS04 13H
LS04 11H
EQUIP
DESCRIPTION(SC)
1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
110
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9TXW PWA
(10/11)
FOR PWA REV.
01
134-296090-110-0
NEC
Nippon Electric Co.Ltd

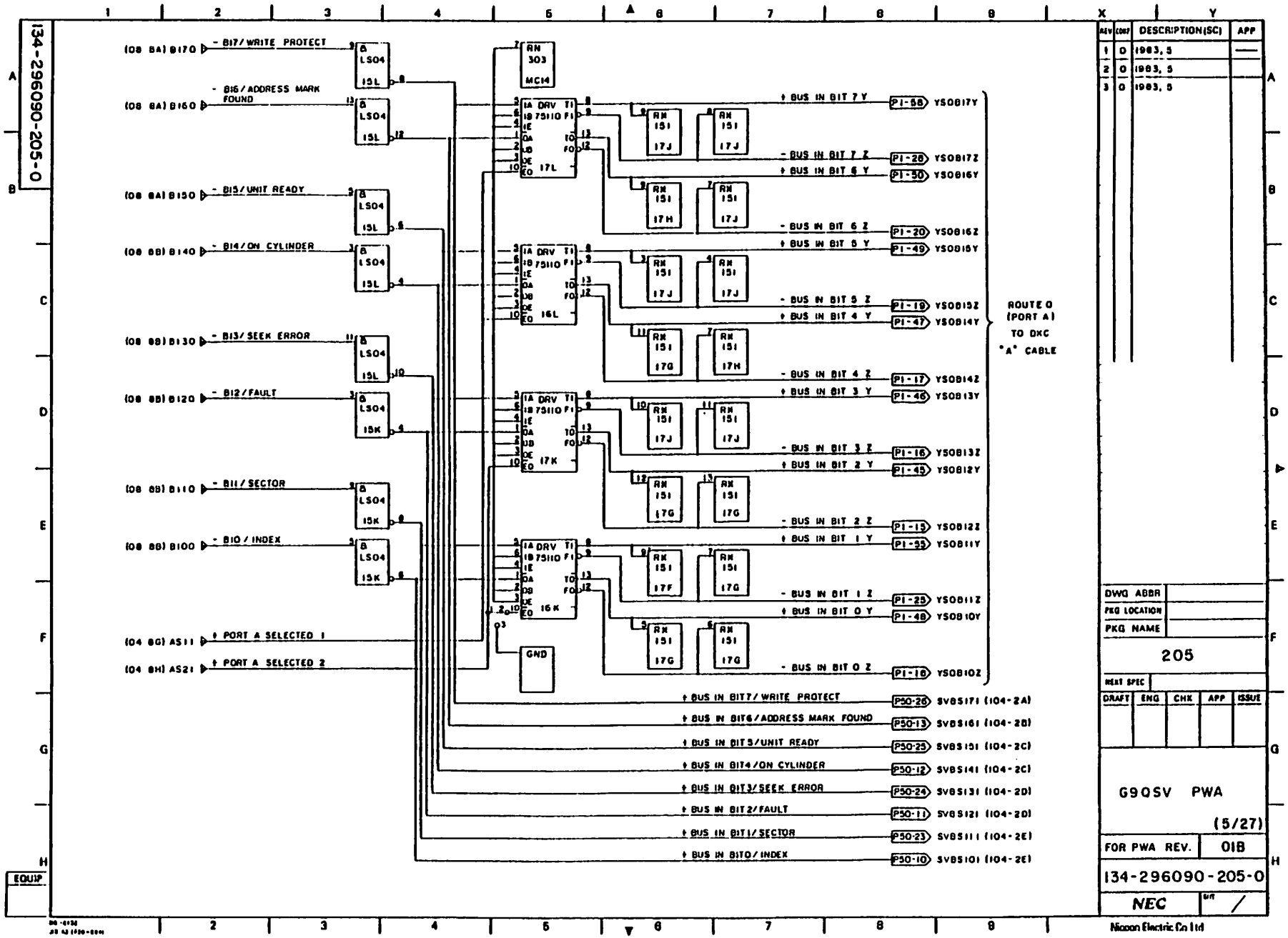

134-296090-111-0
(08 8D) ASL1
† PORT A SELECTED
PORT A SELECTED
(08 8E) ARV1
† PORT A RESERVED
PORT A RESERVED
(08 8F) BSL1
† PORT B SELECTED
PORT B SELECTED
(08 8G) BRV1
† PORT B RESERVED
PORT B RESERVED
SW1
SW2
-PORT A DISABLE
ADSO (06 2H) (08 2D)
-PORT B DISABLE
BDSO (06 2E) (09 2E)
-RELEASE TIMER OPTION
NLTO (09 2D)
GND
(217-6F) SVXP051
(217-6G) SVXP053
(217-6G) SVXP055
(217-8D) SVXG046
(217-8D) SVXG176
(217-8D) SVXG056
(217-8D) SVXG186
(207-8C) SVXG068
(217-6G) SVXN053
(217-6H) SVXN055
+5V
-5V
EQUIP
DESCRIPTION(SC)
1983, 8
DWG ABBR
PKG LOCATION
PKG NAME
111
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9TXW PWA
(11/11)
FOR PWA REV. 01
134-296090-111-0
NEC
Nippon Electric Co Ltd

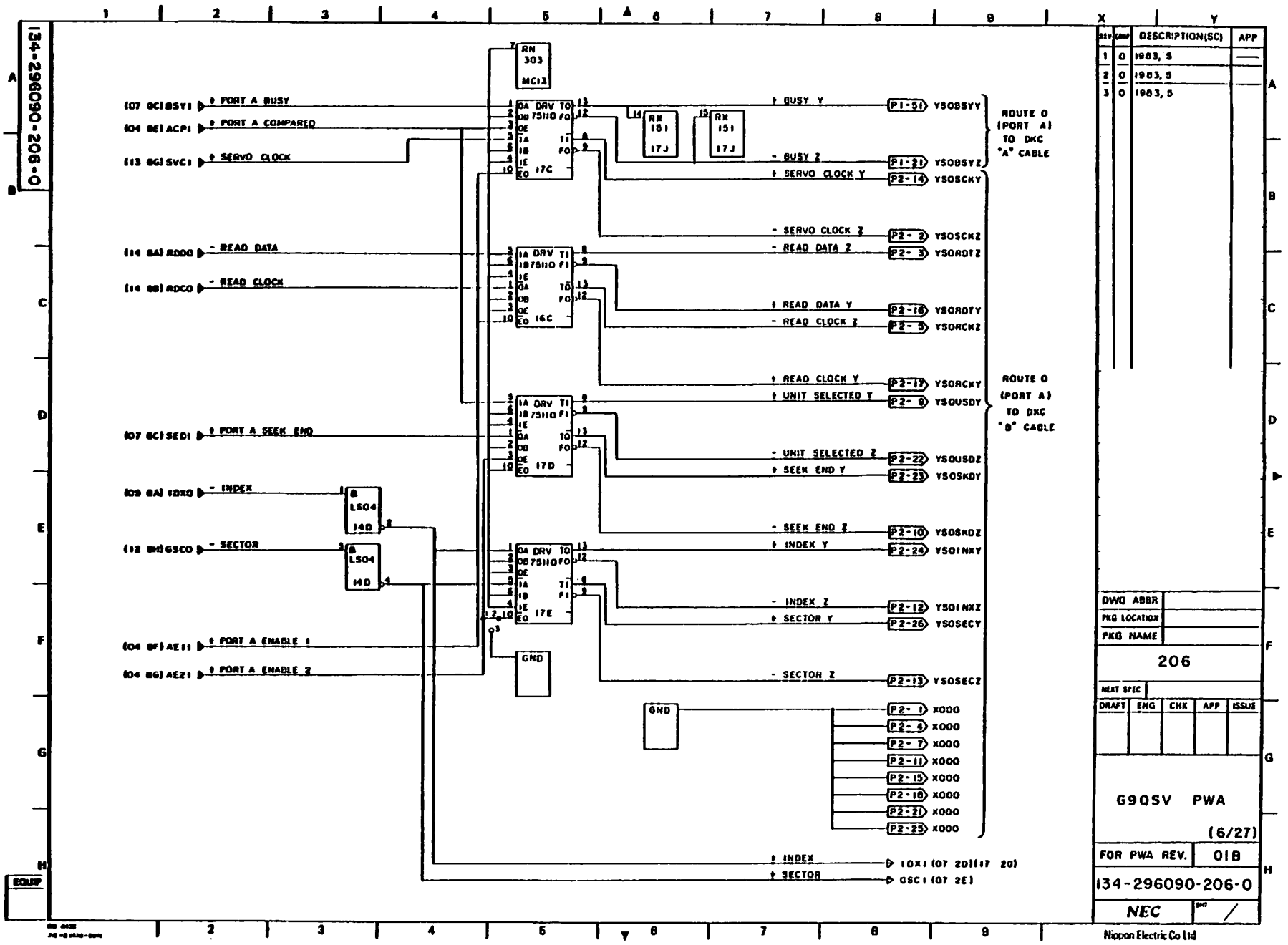

134-296090-201-0
104 BC) 4AM1 † 4 BIT ADR MODE
YSOUS3Z PI-27 - UNIT SEL BIT 3Z
YSOUS3Y PI-57 † UNIT SEL BIT 3Y
YSOUS2Z PI-26 - UNIT SEL BIT 2Z
YSOUS2Y PI-56 † UNIT SEL BIT 2Y
YSOUS1Y PI-54 † UNIT SEL BIT 1Y
YSOUS1Z PI-24 - UNIT SEL BIT 1Z
YSOUSOY PI-53 † UNIT SEL BIT OY
YSOUSOZ PI-23 - UNIT SEL BIT OZ
YSOUSTY PI-52 † UNIT SEL TAG Y
YSOUSTZ PI-22 - UNIT SEL TAG Z
YSOOCOY PI-44 † OPEN CABLE DET Y
YSOOCOZ PI-14 - OPEN CABLE DET Z
ROUTE 0 (PORT A) FROM DXC "A" CABLE
EQUIP
RN 303 MC12
RCB T1 75107 15E
RCV T3 3450 15F
S04 14F
-5V
+5V
GND
† UNIT SEL BIT 3 US31 (04 2C)
† UNIT SEL BIT 2 US21 (04 2D)
† UNIT SEL BIT 1 US11 (04 2D)
† UNIT SEL BIT 0 US01 (04 2D)
† UNIT SEL TAG UST1 (04 2E)
- OPEN CABLE DETECT OPNO (04 1D)
REV | DESCRIPTION(SC) | APP
1 | 0 | 1983, 5
2 | 0 | 1983, 5
3 | 0 | 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
201
NEXT SPEC
DRAFT | ENG | CHK | APP | ISSUE
G9QSV PWA
(1/27)
FOR PWA REV. 01B
134-296090-201-0
NEC
Nippon Electric Co Ltd

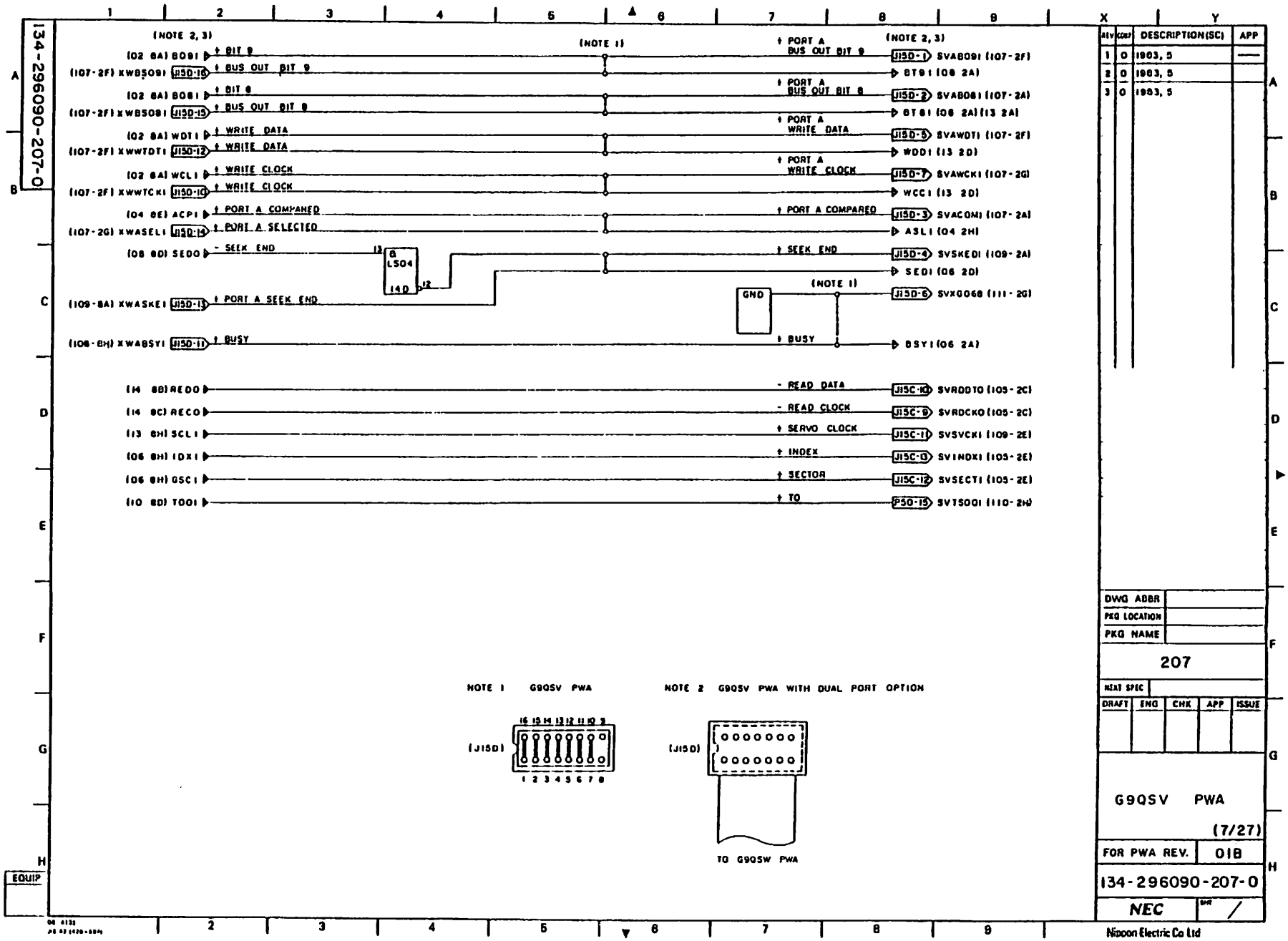

134-296090-202-0
ROUTE 0 (PORT A) FROM DXC "B" CABLE
ROUTE 0 (PORT A) FROM DXC "A" CABLE
EQUIP
YSOWDTY P2-20 + WRITE DATA Y
YSOWDTZ P2-9 - WRITE DATA Z
YSOWCKY P2-19 + WRITE CLOCK Y
YSOWCKZ P2-8 - WRITE CLOCK Z
YSOBT9Y P1-43 + BIT 9 Y
YSOBT9Z P1-13 - BIT 9 Z
YSOBT8Y P1-42 + BIT 8 Y
YSOBT8Z P1-12 - BIT 8 Z
YSOBT7Y P1-41 + BIT 7 Y
YSOBT7Z P1-11 - BIT 7 Z
YSOBT6Y P1-40 + BIT 6 Y
YSOBT6Z P1-10 - BIT 6 Z
YSOBT5Y P1-39 + BIT 5 Y
YSOBT5Z P1-9 - BIT 5 Z
YSOBT4Y P1-38 + BIT 4 Y
YSOBT4Z P1-8 - BIT 4 Z
YSOBT3Y P1-37 + BIT 3 Y
YSOBT3Z P1-7 - BIT 3 Z
YSOBT2Y P1-36 + BIT 2 Y
YSOBT2Z P1-6 - BIT 2 Z
YSOBT1Y P1-35 + BIT 1 Y
YSOBT1Z P1-5 - BIT 1 Z
YSOBT0Y P1-34 + BIT 0 Y
YSOBT0Z P1-4 - BIT 0 Z
R 820 (82Ω) R505
R 820 (82Ω) R506
R 820 (82Ω) R507
R 820 (82Ω) R508
RN 103 MC2
RN 103 MC4
RN 103 MC11
RN 103 MC10
RN 103 MC9
RN 103 MC8
RX 151 17F
RX 151 17J
RX 151 17H
2A RCV T8 2B 3450 1A 1B 0A 0B 3A 3B 5B T1 T0 T5 16D
GND
1A RCV T1 1B 3450 3A 3B 0A 0B 2A 2B 5B T3 T0 T2 15J
1A RCV T1 1B 3450 3A 3B 0A 0B 2A 2B 5B T3 T0 T2 15H
RN 303 MC14
RN 303 MC13
(I02-8C) XWBIT7I P50-22 + BIT 7
(I02-8D) XWBIT6I P50-9 + BIT 6
(I02-8D) XWBIT5I P50-21 + BIT 5
(I02-8D) XWBIT4I P50-8 + BIT 4
(I02-8F) XWBIT3I P50-20 + BIT 3
(I02-8F) XWBIT2I P50-7 + BIT 2
(I02-8F) XWBIT1I P50-19 + BIT 1
(I02-8G) XWBIT0I P50-6 + BIT 0
(I04-8H) AS30 -PORT A SELECTED 3
+ WRITE DATA
+ WRITE CLOCK
+ BIT 9
+ BIT 8
WDTI (07 2A)
WCLI (07 2B)
B09I (07 2A)
B08I (07 2A)
+ BIT 7
+ BIT 6
+ BIT 5
+ BIT 4
BT7I (08 2A)(13 2A)
BT6I (08 2A)
BT5I (08 2A)(13 2B)
BT4I (08 2B)
+ BIT 3
+ BIT 2
+ BIT 1
+ BIT 0
BT3I (08 2B)
BT2I (08 2B)
BT1I (08 2B)(13 2B)
BT0I (08 2B)
REV
DESCRIPTION(SC)
APP
1 0 1983. 5
2 0 1983. 9
3 0 1983. 5
DWG ASSR
PKG LOCATION
PKG NAME
202
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSV PWA
(2/27)
FOR PWA REV.
01B
134-296090-202-0
NEC
Nippon Electric Co.ltd

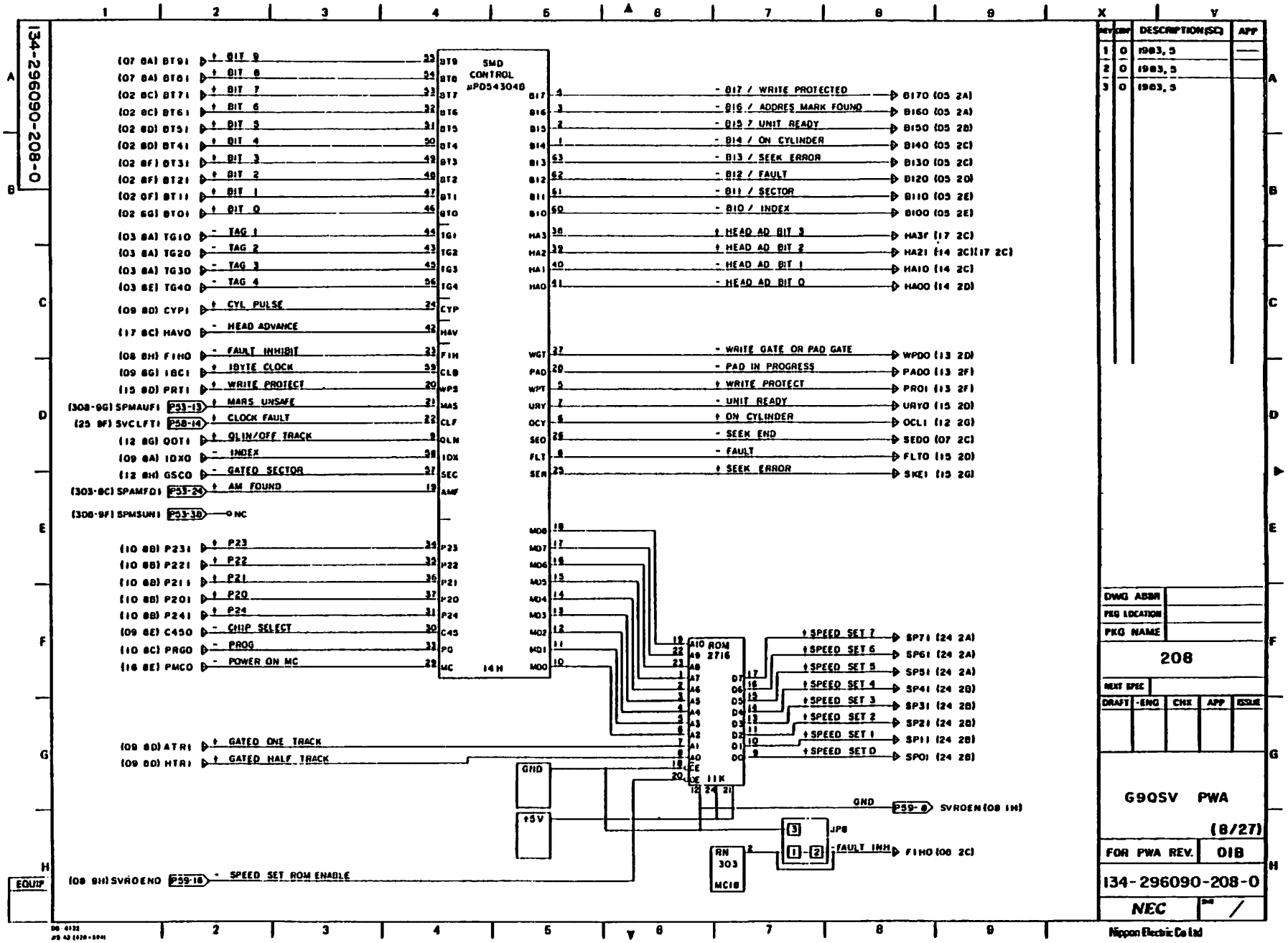

134-296090-203-0
ROUTE 0 (PORT A) FROM DKC "A" CABLE
YSOTG1Z PI-1 - TAG 1 Z
YSOTG1Y PI-31 + TAG 1 Y
YSOTG2Z PI-2 - TAG 2 Z
YSOTG2Y PI-32 + TAG 2 Y
YSOTG3Z PI-3 - TAG 3 Z
YSOTG3Y PI-33 + TAG 3 Y
YSOTG4Z PI-30 - TAG 4 Z
YSOTG4Y PI-60 + TAG 4 Y
RN 151 17G
RN 103 MC6
RN 103 MC7
2A RCV T2
2B 3450
0A T0
0B T3
3A T1
3B 15G
1A
1B
5B
- TAG 1 TG10 (08 2B)
- TAG 2 TG20 (08 2C)
- TAG 3 TG30 (08 2C)(13 2B)
(103-8A) XWTAG10 J15C-1 - TAG 1
(103-8A) XWTAG20 J15C-16 - TAG 2
(103-8A) XWTAG30 J15C-2 - TAG 3
(103-8A) XWTAG40 J15C-15 - TAG 4
RN 303 MC12
(04 8H) AS30 - PORT A SELECTED 3
(14 8H) T410 - TAG 4 INHIBIT
SMT LS14 13G
LS00 14G
- TAG 4 TG40 (08 2C)
YKSPCK0 PI-28 POWER SEQ PICK / NU
YKSHLD0 PI-59 - POWER SEQ HOLD
(103-8F) XWPHLD0 J15C-14 - POWER SEQ HOLD
D52 1S953
D51 1S953
15V
R509 470
C501 0.1μ
D53 RD3.9EB
GND
+ HOLD HLD1 (10 2A)
(04 8C) LCLO - LOCAL
EQUIP
REV COMP DESCRIPTION(SC) APP
1 0 1983.5
2 0 1983.5
3 0 1983.5
DWG ABBR
PKG LOCATION
PKG NAME
203
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9QSV PWA
(3/27)
FOR PWA REV. 018
134-296090-203-0
NEC
SHT /
Nippon Electric Co Ltd


134-296090-204-0
RN 303 MC16
RN 303 MC15
GND
DIP SW 14A
5V
LS85 13C
LS74 13D
LS00 11C
LS08 12B
LS11 12D
LS04 12E
04 14E
- LOCAL
↑ 4 BIT ADR MODE
↑ START DELAY SW 1
↑ START DELAY SW 0
↑ UNIT AD SW 3
↑ UNIT AD SW 2
↑ UNIT AD SW 1
↑ UNIT AD SW 0
↑ UNIT SEL BIT 3
↑ UNIT SEL BIT 2
↑ UNIT SEL BIT 1
↑ UNIT SEL BIT 0
↑ UNIT SEL TAG
- POWER ON MC
- CE MODE
- TEST MODE
- OPEN CABLE DETECT
- PORT A DISABLE
↑ PORT A SELECTED
↑ PORT A COMPARED
↑ PORT A COMPARED
- PORT A/B DISABLE
↑ PORT A ENABLE 1
↑ PORT A ENABLE 2
↑ PORT A SELECT INH
↑ PORT A SELECTED 1
↑ PORT A SELECTED 2
- PORT A SELECTED 3
J15C-4 SVXG04B (105-2G)
J15C-5 SVUA03 (106-2B)
J15C-6 SVUA02 (106-2B)
J15C-7 SVDA00 (106-2B)
J15C-8 SVUA00 (106-2B)
J15D-9 SVXWADI50 (106-8H)
J15D-8 SVPDI50 (109-2H)
J15C-5 SVASIN1 (106-2G)
LCLO (03 2G)
4AMI (01 2A)
SDI1 (11 2E)
SDI0 (11 2E)
ACPI (07 2B)
ACPI (06 2A)
AE11 (06 2F)
AE21 (06 2F)
AS11 (05 2F)
AS21 (05 2F)
AS30 (02 6G) (03 2E)
(01 8B) US31
(01 8B) US21
(01 8C) US11
(01 8C) US01
(01 8D) UST1
(16 8E) PMCO
(17 8B) CEMO
(14 8H) TMDO
(01 8D) OPNO
(07 8C) ASL1
EQUIP
DESCRIPTION(SC)
1 0 1983. 5
2 0 1983. 5
3 0 1983. 5
DWG ABBR
PKG LOCATION
PKG NAME
204
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G90SV PWA
(4/27)
FOR PWA REV. 01B
134-296090-204-0
NEC
Nippon Electric Co Ltd


134-296090-205-0
(08 8A) B17 0 - B17/WRITE PROTECT
(08 8A) B16 0 - B16/ADDRESS MARK FOUND
(08 8A) B15 0 - B15/UNIT READY
(08 8B) B14 0 - B14/ON CYLINDER
(08 8B) B13 0 - B13/SEEK ERROR
(08 8B) B12 0 - B12/FAULT
(08 8B) B11 0 - B11/SECTOR
(08 8B) B10 0 - B10/INDEX
(04 8G) AS1 1 + PORT A SELECTED 1
(04 8H) AS2 1 + PORT A SELECTED 2
LS04 15L
LS04 15K
RN 303 MC14
1A DRV TI 75110 F1
17L
16L
17K
16K
GND
RN 151 17J
RN 151 17H
RN 151 17G
RN 151 17F
+ BUS IN BIT 7 Y P1-58 YSOB17Y
- BUS IN BIT 7 Z P1-28 YSOB17Z
+ BUS IN BIT 6 Y P1-50 YSOB16Y
- BUS IN BIT 6 Z P1-20 YSOB16Z
+ BUS IN BIT 5 Y P1-49 YSOB15Y
- BUS IN BIT 5 Z P1-19 YSOB15Z
+ BUS IN BIT 4 Y P1-47 YSOB14Y
- BUS IN BIT 4 Z P1-17 YSOB14Z
+ BUS IN BIT 3 Y P1-46 YSOB13Y
- BUS IN BIT 3 Z P1-16 YSOB13Z
+ BUS IN BIT 2 Y P1-45 YSOB12Y
- BUS IN BIT 2 Z P1-15 YSOB12Z
+ BUS IN BIT 1 Y P1-93 YSOB11Y
- BUS IN BIT 1 Z P1-25 YSOB11Z
+ BUS IN BIT 0 Y P1-48 YSOB10Y
- BUS IN BIT 0 Z P1-18 YSOB10Z
ROUTE 0 (PORT A) TO DXC "A" CABLE
+ BUS IN BIT7/ WRITE PROTECT P50-26 SVBS17I (104-2A)
+ BUS IN BIT6/ADDRESS MARK FOUND P50-13 SVBS16I (104-2B)
+ BUS IN BIT5/UNIT READY P50-25 SVBS15I (104-2C)
+ BUS IN BIT4/ON CYLINDER P50-12 SVBS14I (104-2C)
+ BUS IN BIT3/SEEK ERROR P50-24 SVBS13I (104-2D)
+ BUS IN BIT2/FAULT P50-11 SVBS12I (104-2D)
+ BUS IN BIT1/SECTOR P50-23 SVBS11I (104-2E)
+ BUS IN BIT0/INDEX P50-10 SVBS10I (104-2E)
EQUIP
REV | CONT | DESCRIPTION(SC) | APP
1 | 0 | 1983. 5 | —
2 | 0 | 1983. 5 |
3 | 0 | 1983. 5 |
DWG ABBR
PKG LOCATION
PKG NAME
205
NEXT SPEC
DRAFT | ENG | CHK | APP | ISSUE
G90SV PWA
(5/27)
FOR PWA REV. 01B
134-296090-205-0
NEC
Nippon Electric Co Ltd


134-296090-206-0
RN 303 MC13
(07 6C) BSY1 ↑ PORT A BUSY
(04 6E) ACP1 ↑ PORT A COMPARED
(13 6G) SVC1 ↑ SERVO CLOCK
(14 6A) RDD0 - READ DATA
(14 6B) RDC0 - READ CLOCK
(07 6C) SED1 ↑ PORT A SEEK END
(09 6A) IDX0 - INDEX
(12 6H) GSC0 - SECTOR
(04 6F) AE11 ↑ PORT A ENABLE 1
(04 6G) AE21 ↑ PORT A ENABLE 2
17C
16C
17D
17E
LS04 14D
GND
↑ BUSY Y
- BUSY Z
↑ SERVO CLOCK Y
- SERVO CLOCK Z
- READ DATA Z
↑ READ DATA Y
- READ CLOCK Z
↑ READ CLOCK Y
↑ UNIT SELECTED Y
- UNIT SELECTED Z
↑ SEEK END Y
- SEEK END Z
↑ INDEX Y
- INDEX Z
↑ SECTOR Y
- SECTOR Z
P1-51 YSOBSYY
P1-21 YSOBSYZ
P2-14 YSOSCKY
P2- 2 YSOSCKZ
P2- 3 YSORDTZ
P2-16 YSORDTY
P2- 5 YSORCKZ
P2-17 YSORCKY
P2- 9 YSOUSDY
P2-22 YSOUSDZ
P2-23 YSOSKDY
P2-10 YSOSKDZ
P2-24 YSOINXY
P2-12 YSOINXZ
P2-26 YSOSECY
P2-13 YSOSECZ
P2- 1 XOOO
P2- 4 XOOO
P2- 7 XOOO
P2-11 XOOO
P2-15 XOOO
P2-18 XOOO
P2-21 XOOO
P2-25 XOOO
ROUTE 0 (PORT A) TO DKC "A" CABLE
ROUTE 0 (PORT A) TO DKC "B" CABLE
↑ INDEX ▷ IDX1 (07 2D)(17 2D)
↑ SECTOR ▷ GSC1 (07 2E)
DESCRIPTION(SC)
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
206
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9QSV PWA
(6/27)
FOR PWA REV. 01B
134-296090-206-0
NEC
Nippon Electric Co Ltd


134-296090-207-0
(NOTE 2, 3)
(NOTE 1)
(NOTE 2, 3)
(02 8A) BOB1 ↑ BIT 8
(107-2F) XWBSOB1 J150-16 ↑ BUS OUT BIT 8
↑ PORT A BUS OUT BIT 8
J15D-1 SVABOB1 (107-2F)
BTB1 (08 2A)
(02 8A) BOB1 ↑ BIT 8
(107-2F) XWBSOB1 J150-15 ↑ BUS OUT BIT 8
↑ PORT A BUS OUT BIT 8
J15D-2 SVABOB1 (107-2A)
BTB1 (08 2A) (13 2A)
(02 8A) WDT1 ↑ WRITE DATA
(107-2F) XWWTDT1 J150-12 ↑ WRITE DATA
↑ PORT A WRITE DATA
J15D-5 SVAWDT1 (107-2F)
WDD1 (13 2D)
(02 8A) WCL1 ↑ WRITE CLOCK
(107-2F) XWWTCK1 J150-10 ↑ WRITE CLOCK
↑ PORT A WRITE CLOCK
J15D-7 SVAWCK1 (107-2G)
WCC1 (13 2D)
(04 8E) ACP1 ↑ PORT A COMPARED
(107-2G) XWASEL1 J150-14 ↑ PORT A SELECTED
↑ PORT A COMPARED
J15D-3 SVACOM1 (107-2A)
ASL1 (04 2H)
(08 8D) SEDO - SEEK END
LS04
↑ SEEK END
J15D-4 SVSKED1 (109-2A)
SED1 (06 2D)
(NOTE 1)
GND
(109-8A) XWASKE1 J150-13 ↑ PORT A SEEK END
J15D-6 SVXGOG8 (111-2G)
(108-8H) XWABSY1 J150-11 ↑ BUSY
↑ BUSY
BSY1 (06 2A)
(14 8B) REDO - READ DATA
J15C-10 SVRDDT0 (105-2C)
(14 8C) RECO - READ CLOCK
J15C-9 SVRDCK0 (105-2C)
(13 8H) SCL1 ↑ SERVO CLOCK
J15C-11 SVSVCK1 (109-2E)
(06 8H) IDX1 ↑ INDEX
J15C-13 SVINDX1 (105-2E)
(06 8H) GSC1 ↑ SECTOR
J15C-12 SVSECT1 (105-2E)
(10 8D) TOO1 ↑ TO
P50-15 SVTSOO1 (110-2H)
NOTE 1 G90SV PWA
(J15D)
NOTE 2 G90SV PWA WITH DUAL PORT OPTION
(J15D)
TO G90SW PWA
REV
COMP
DESCRIPTION(SC)
APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
207
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G90SV PWA
(7/27)
FOR PWA REV. 018
134-296090-207-0
NEC
EQUIP
Nippon Electric Co Ltd


134-296090-208-0
SMD CONTROL μPD543048
14 H
A10 ROM 2716
11K
(07 8A) BT9I
(07 8A) BT8I
(02 8C) BT7I
(02 8C) BT6I
(02 8D) BT5I
(02 8D) BT4I
(02 8F) BT3I
(02 8F) BT2I
(02 0F) BT1I
(02 6G) BT0I
BIT 9
BIT 8
BIT 7
BIT 6
BIT 5
BIT 4
BIT 3
BIT 2
BIT 1
BIT 0
(03 8A) TG1O
(03 8A) TG2O
(03 8A) TG3O
(03 8E) TG4O
TAG 1
TAG 2
TAG 3
TAG 4
(09 8D) CYPI
CYL PULSE
(17 8C) HAVO
HEAD ADVANCE
(08 8H) FIHO
FAULT INHIBIT
(09 8G) IBCI
IBYTE CLOCK
(15 8D) PRTI
WRITE PROTECT
(308-9G) SPMAUFI P53-13
MARS UNSAFE
(25 9F) SVCLFTI P58-14
CLOCK FAULT
(12 8G) QOTI
QLIN/OFF TRACK
(09 8A) IDXO
INDEX
(12 8H) GSCO
GATED SECTOR
(303-8C) SPAMFOI P53-24
AM FOUND
(308-9F) SPMSUNI P53-38
NC
(10 8B) P23I
(10 8B) P22I
(10 8B) P21I
(10 8B) P20I
(10 8B) P24I
P23
P22
P21
P20
P24
(09 8E) C45O
CHIP SELECT
(10 8C) PRGO
PROG
(16 8E) PMCO
POWER ON MC
(08 8D) ATRI
GATED ONE TRACK
(09 8D) HTRI
GATED HALF TRACK
(08 9H) SVROENO P59-18
SPEED SET ROM ENABLE
GND
+5V
RN 303 MC18
JP8
FAULT INH
FIHO (08 2C)
SVROEN (08 1H)
- BI7 / WRITE PROTECTED
- BI6 / ADDRES MARK FOUND
- BI5 / UNIT READY
- BI4 / ON CYLINDER
- BI3 / SEEK ERROR
- BI2 / FAULT
- BI1 / SECTOR
- BI0 / INDEX
+ HEAD AD BIT 3
+ HEAD AD BIT 2
- HEAD AD BIT 1
- HEAD AD BIT 0
- WRITE GATE OR PAD GATE
- PAD IN PROGRESS
+ WRITE PROTECT
- UNIT READY
+ ON CYLINDER
- SEEK END
- FAULT
+ SEEK ERROR
+ SPEED SET 7
+ SPEED SET 6
+ SPEED SET 5
+ SPEED SET 4
+ SPEED SET 3
+ SPEED SET 2
+ SPEED SET 1
+ SPEED SET 0
SP7I (24 2A)
SP6I (24 2A)
SP5I (24 2A)
SP4I (24 2B)
SP3I (24 2B)
SP2I (24 2B)
SP1I (24 2B)
SP0I (24 2B)
BI7O (05 2A)
BI6O (05 2A)
BI5O (05 2B)
BI4O (05 2C)
BI3O (05 2C)
BI2O (05 2D)
BI1O (05 2E)
BI0O (05 2E)
HA3I (17 2C)
HA2I (14 2C)(17 2C)
HA1I (14 2C)
HA0I (14 2D)
WPDO (13 2D)
PADO (13 2F)
PROI (13 2F)
URYO (15 2D)
OCLI (12 2G)
SEDO (07 2C)
FLTO (15 2D)
SKEI (15 2G)
DESCRIPTION(SC)
1983, 5
APP
DWG ASSN
PKG LOCATION
PKG NAME
208
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G90SV PWA
(8/27)
FOR PWA REV. 01B
134-296090-208-0
NEC
Nippon Electric Co Ltd
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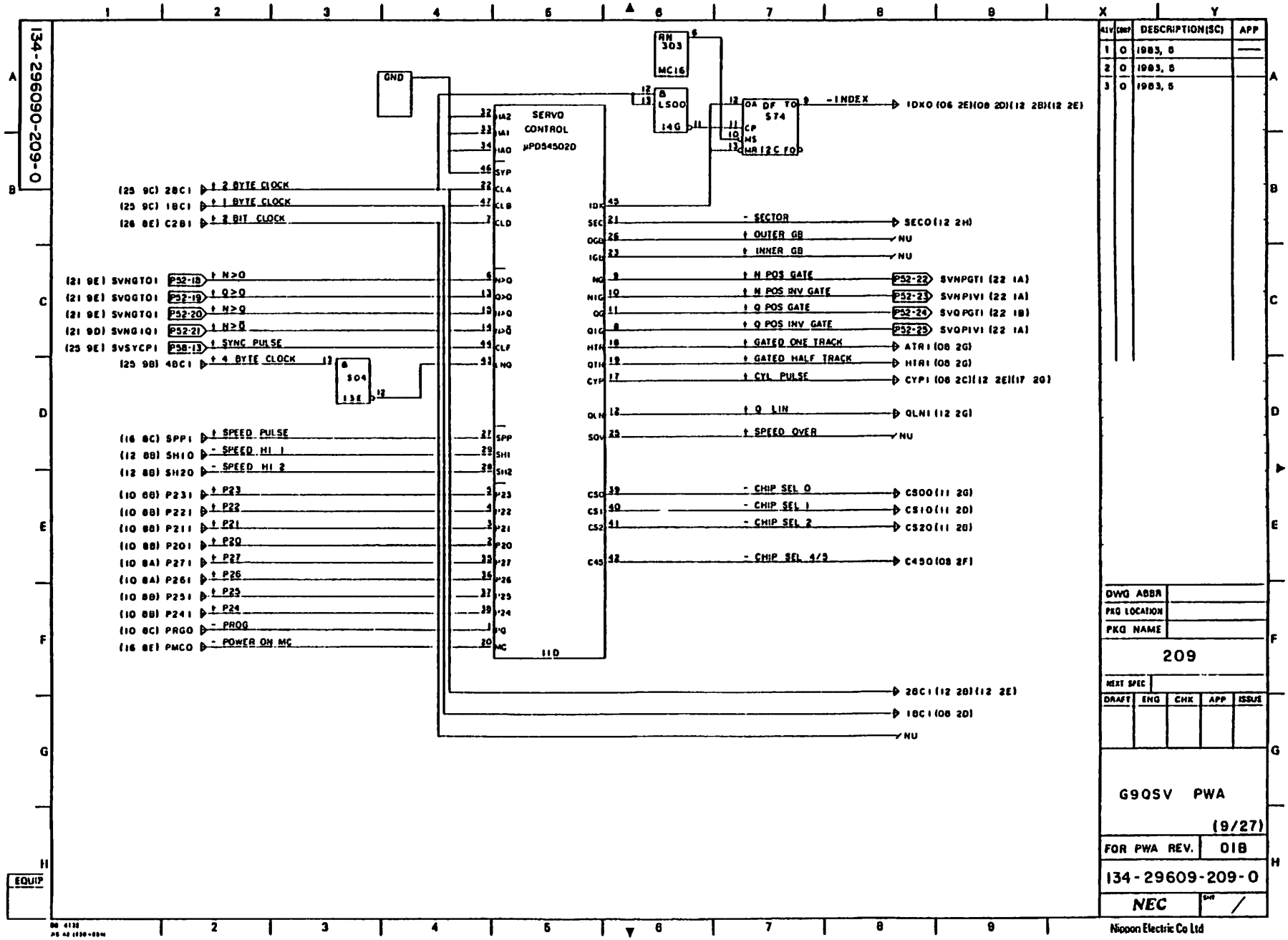
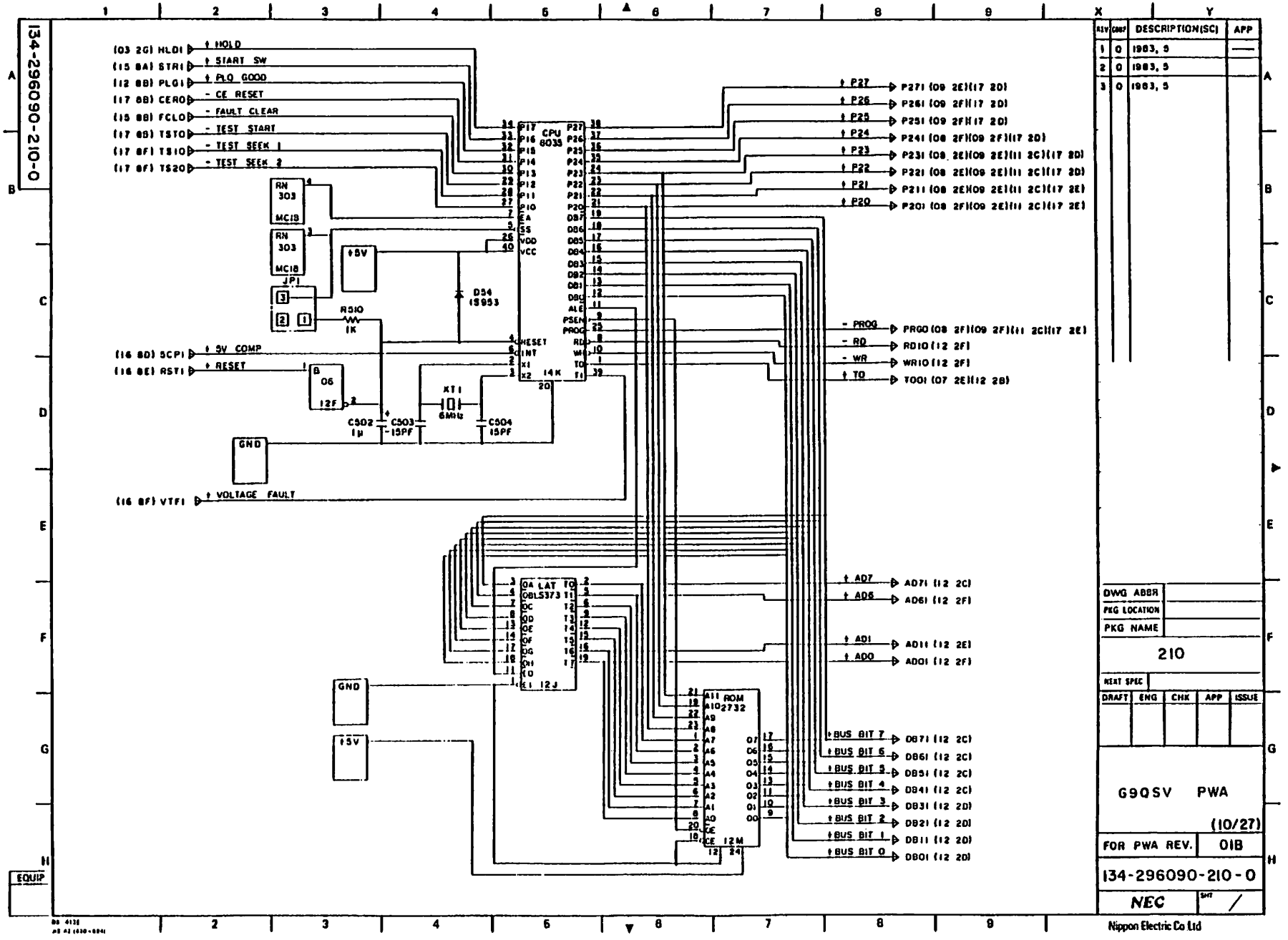
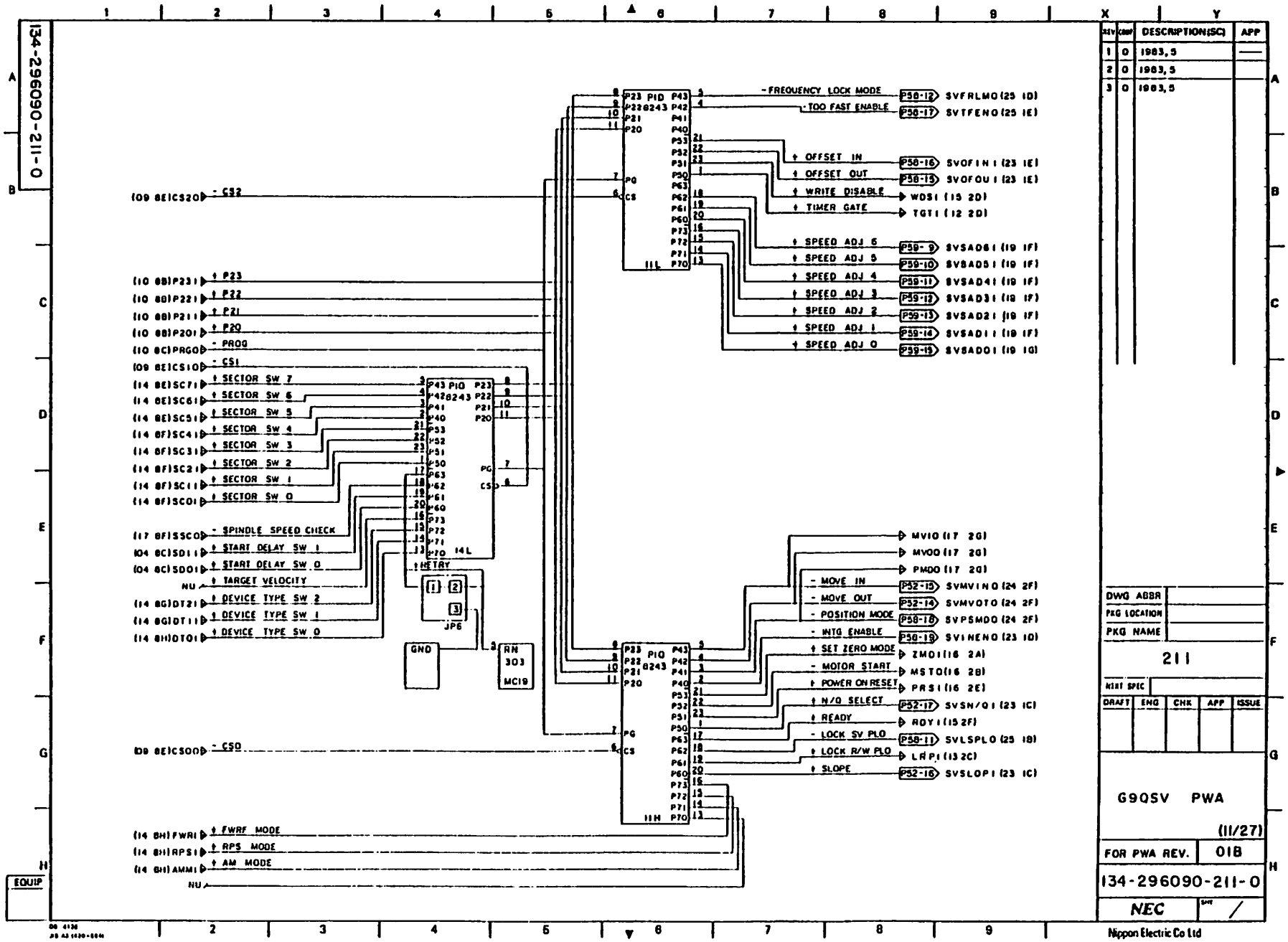
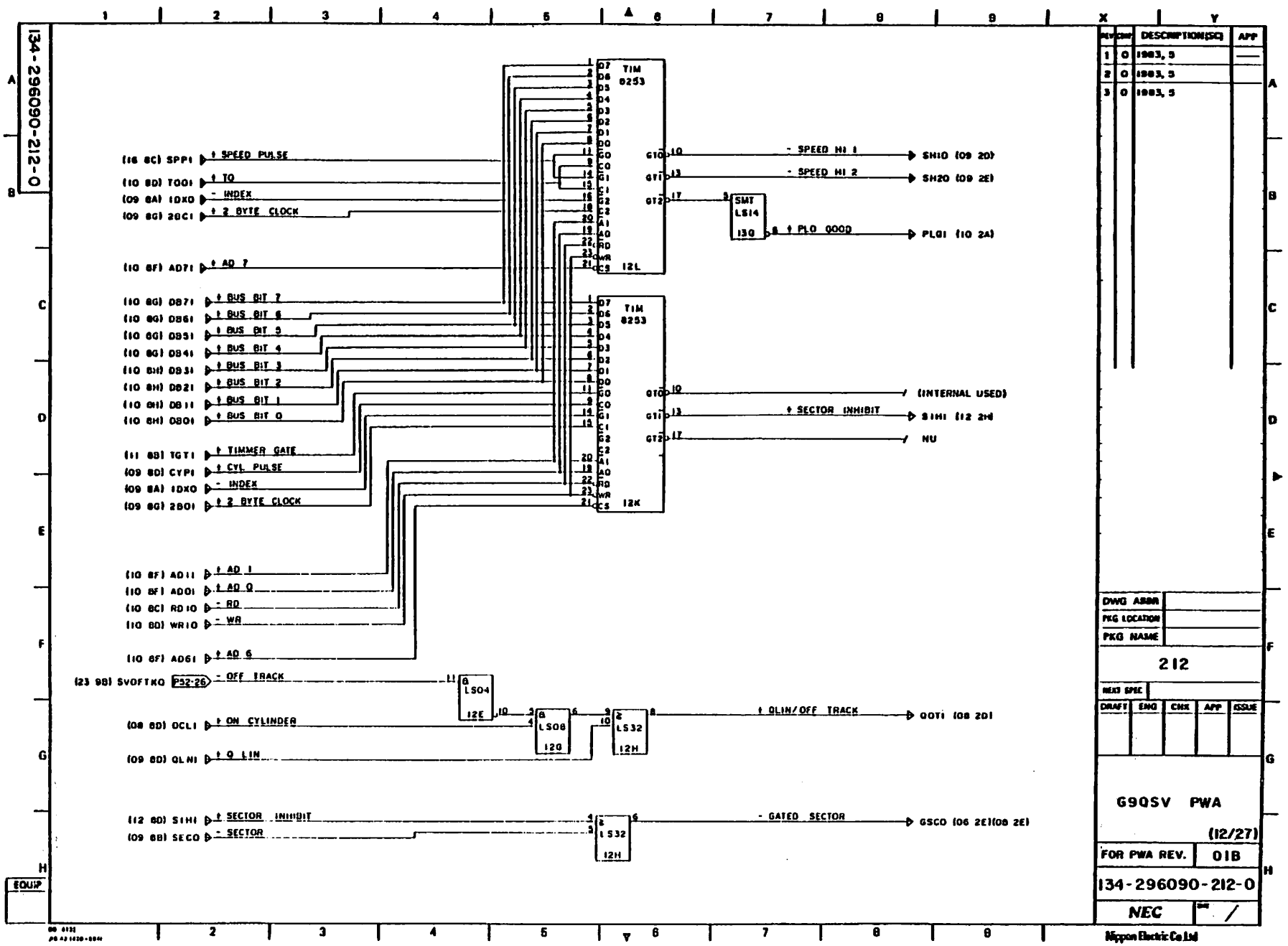
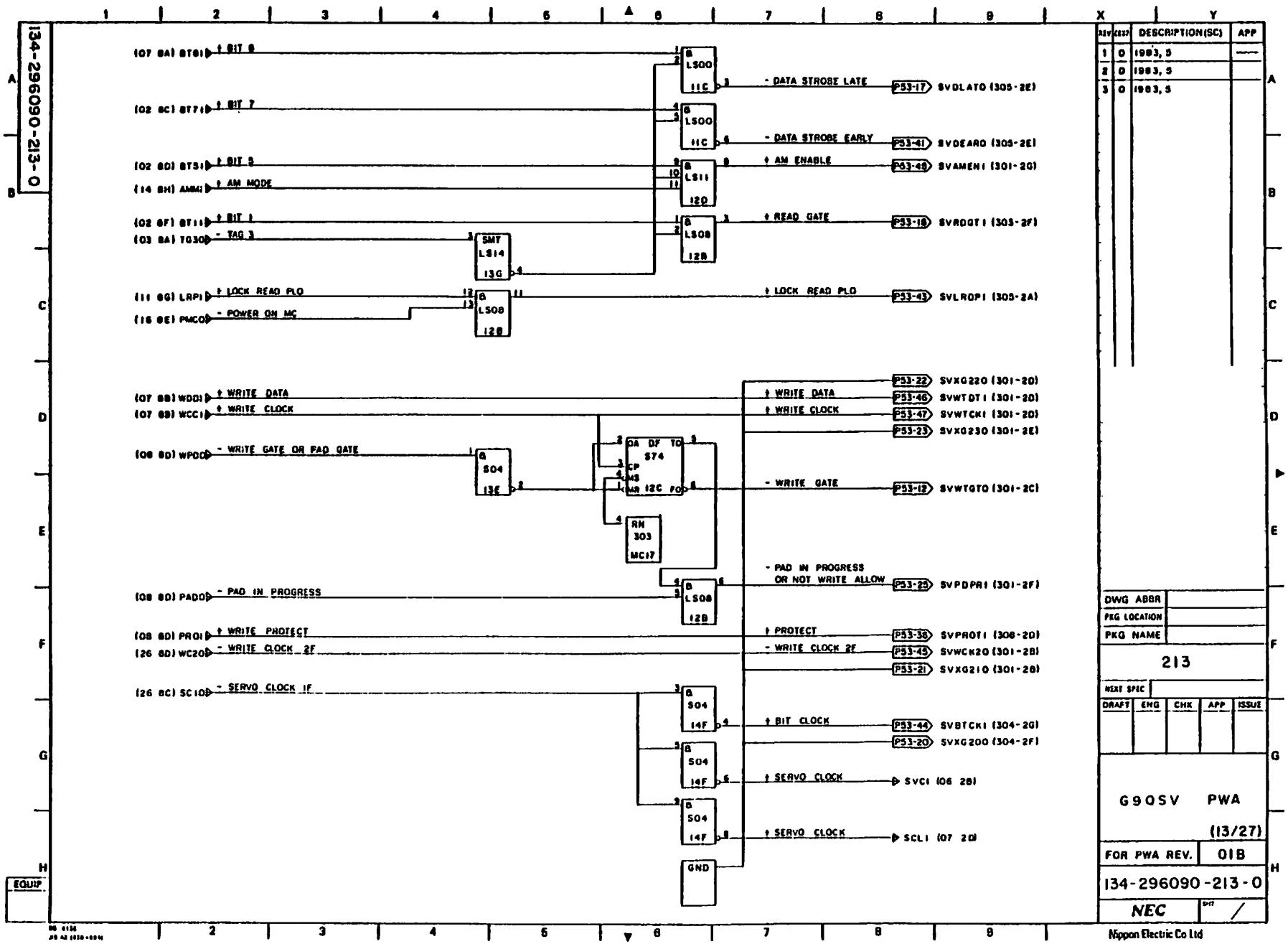

134-296090-209-0
GND
SERVO CONTROL μPD545020
AH 303 MC16
LS00 14G
S74
-INDEX
IDX0 (06 2E)(08 2D)(12 2B)(12 2E)
(25 9C) 28C1 ↑ 2 BYTE CLOCK
(25 9C) 18C1 ↑ 1 BYTE CLOCK
(26 8E) C2B1 ↑ 2 BIT CLOCK
(25 9C) 28C1 (12 2B)(12 2E)
(25 9C) 18C1 (08 2D)
NU
(21 9E) SVNGT01 P52-18 ↑ N>0
(21 9E) SVQGT01 P52-19 ↑ Q>0
(21 9E) SVNGTQ1 P52-20 ↑ N>Q
(21 9D) SVNG1Q1 P52-21 ↑ N>Q̄
(25 9E) SVSYCP1 P58-13 ↑ SYNC PULSE
(25 9B) 4BC1 ↑ 4 BYTE CLOCK
S04 13E
- SECTOR
SEC0 (12 2H)
↑ OUTER GB
↑ INNER GB
↑ N POS GATE
P52-22 SVNPGT1 (22 1A)
↑ N POS INV GATE
P52-23 SVNPIV1 (22 1A)
↑ Q POS GATE
P52-24 SVQPGT1 (22 1B)
↑ Q POS INV GATE
P52-25 SVQPIV1 (22 1A)
↑ GATED ONE TRACK
ATR1 (08 2G)
↑ GATED HALF TRACK
HTR1 (08 2G)
↑ CYL PULSE
CYP1 (08 2C)(12 2E)(17 2G)
↑ Q LIN
QLN1 (12 2G)
↑ SPEED OVER
NU
(16 8C) SPP1 ↑ SPEED PULSE
(12 8B) SH10 - SPEED HI 1
(12 8B) SH20 - SPEED HI 2
(10 6B) P231 ↑ P23
(10 8B) P221 ↑ P22
(10 8B) P211 ↑ P21
(10 8B) P201 ↑ P20
(10 8A) P271 ↑ P27
(10 8A) P261 ↑ P26
(10 8B) P251 ↑ P25
(10 8B) P241 ↑ P24
(10 8C) PRG0 - PROG
(16 8E) PMC0 - POWER ON MC
- CHIP SEL 0
CS00 (11 2G)
- CHIP SEL 1
CS10 (11 2D)
- CHIP SEL 2
CS20 (11 2B)
- CHIP SEL 4/5
C450 (08 2F)
28C1 (12 2B)(12 2E)
18C1 (08 2D)
NU
EQUIP
ALV CHNG DESCRIPTION(SC) APP
1 0 1983, 8
2 0 1983, 8
3 0 1983, 8
DWG ABBR
PKG LOCATION
PKG NAME
209
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G90SV PWA
(9/27)
FOR PWA REV. 018
134-29609-209-0
NEC
Nippon Electric Co Ltd


134-296090-210-0
(03 2G) HLDI
(15 8A) STRI
(12 8B) PLGI
(17 8B) CERO
(15 8B) FCLO
(17 8B) TSTO
(17 8F) TS1O
(17 8F) TS2O
↑ HOLD
↑ START SW
↑ PLO GOOD
- CE RESET
- FAULT CLEAR
- TEST START
- TEST SEEK 1
- TEST SEEK 2
CPU 8039
RN 303 MC1B
+5V
D34 1S953
R510 1K
JP1
(16 8D) SCPI
(16 8E) RSTI
↑ 5V COMP
↑ RESET
XT1 6MHz
C502 1μ
C503 15PF
C504 15PF
GND
(16 8F) VTFI
↑ VOLTAGE FAULT
LATCH 74LS373
ROM 2732
+5V
↑ P27
↑ P26
↑ P25
↑ P24
↑ P23
↑ P22
↑ P21
↑ P20
P27I (09 2E)(17 2D)
P26I (09 2F)(17 2D)
P25I (09 2F)(17 2D)
P24I (08 2F)(09 2F)(17 2D)
P23I (08 2E)(09 2E)(11 2C)(17 2D)
P22I (08 2E)(09 2E)(11 2C)(17 2D)
P21I (08 2E)(09 2E)(11 2C)(17 2E)
P20I (08 2F)(09 2E)(11 2C)(17 2E)
- PROG
- RD
- WR
↑ TO
PRGO (08 2F)(09 2F)(11 2C)(17 2E)
RDIO (12 2F)
WRIO (12 2F)
TOOI (07 2E)(12 2B)
↑ AD7
↑ AD6
↑ AD1
↑ AD0
AD7I (12 2C)
AD6I (12 2F)
AD1I (12 2E)
AD0I (12 2F)
↑ BUS BIT 7
↑ BUS BIT 6
↑ BUS BIT 5
↑ BUS BIT 4
↑ BUS BIT 3
↑ BUS BIT 2
↑ BUS BIT 1
↑ BUS BIT 0
DB7I (12 2C)
DB6I (12 2C)
DB5I (12 2C)
DB4I (12 2C)
DB3I (12 2D)
DB2I (12 2D)
DB1I (12 2D)
DB0I (12 2D)
REV
CONF
DESCRIPTION(SC)
APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
210
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSV PWA
(10/27)
FOR PWA REV.
01B
134-296090-210-0
NEC
EQUIP
Nippon Electric Co Ltd



REV	COMP	DESCRIPTION(SC)	APP
1	0	1983, 5	—
2	0	1983, 5	
3	0	1983, 5	


134-296090-212-0
(16 8C) SPP1 ↑ SPEED PULSE
(10 8D) TOG1 ↑ TQ
(09 8A) IDX0 - INDEX
(09 8G) 2BC1 ↑ 2 BYTE CLOCK
(10 8F) AD71 ↑ AD 7
(10 8G) DB71 ↑ BUS BIT 7
(10 8G) DB61 ↑ BUS BIT 6
(10 8G) DB51 ↑ BUS BIT 5
(10 8G) DB41 ↑ BUS BIT 4
(10 8H) DB31 ↑ BUS BIT 3
(10 8H) DB21 ↑ BUS BIT 2
(10 8H) DB11 ↑ BUS BIT 1
(10 8H) DB01 ↑ BUS BIT 0
(11 8B) TGT1 ↑ TIMMER GATE
(09 8D) CYP1 ↑ CYL PULSE
(09 8A) IDX0 - INDEX
(09 8G) 2B01 ↑ 2 BYTE CLOCK
(10 8F) AD11 ↑ AD 1
(10 8F) AD01 ↑ AD 0
(10 8C) RD10 - RD
(10 8D) WR10 - WR
(10 8F) AD61 ↑ AD 6
(23 9B) SVOFTK0 P52-26 - OFF TRACK
(08 8D) OCL1 ↑ ON CYLINDER
(09 8D) QLN1 ↑ Q LIN
(12 8D) SIH1 ↑ SECTOR INHIBIT
(09 8B) SEC0 - SECTOR
TIM 8253
12L
12K
- SPEED HI 1
- SPEED HI 2
SMT LS14 13D
↑ PLO GOOD
PLG1 (10 2A)
SH10 (09 2D)
SH20 (09 2E)
/ (INTERNAL USED)
↑ SECTOR INHIBIT
SIH1 (12 2H)
/ NU
LS04 12E
LS08 12G
LS32 12H
↑ QLIN/OFF TRACK
QOT1 (08 2D)
LS32 12H
- GATED SECTOR
GSC0 (06 2E)(08 2E)
EQUIP
DWG ABBR
PKG LOCATION
PKG NAME
212
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G90SV PWA
(12/27)
FOR PWA REV. 01B
134-296090-212-0
NEC
Nippon Electric Co Ltd


134-296090-213-0
(07 8A) BT8I ↑ BIT 8
(02 8C) BT7I ↑ BIT 7
(02 8D) BT5I ↑ BIT 5
(14 8H) AMMI ↑ AM MODE
(02 8F) BT1I ↑ BIT 1
(03 8A) TG3O - TAG 3
(11 8G) LRPI ↑ LOCK READ PLO
(16 8E) PMCO - POWER ON MC
(07 8B) WDOI ↑ WRITE DATA
(07 8B) WCCI ↑ WRITE CLOCK
(08 8D) WPDO - WRITE GATE OR PAD GATE
(08 8D) PADO - PAD IN PROGRESS
(08 8D) PROI ↑ WRITE PROTECT
(26 8D) WC2O - WRITE CLOCK 2F
(26 8C) SC1O - SERVO CLOCK 1F
LS00 11C
LS00 11C
LS11 12D
LS08 12B
SMT LS14 13G
LS08 12B
S04 13E
DA DF TG S74
CP MS MR 12C FO
RN 303 MC17
LS08 12B
S04 14F
S04 14F
S04 14F
GND
- DATA STROBE LATE P53-17 SVDLAT0 (305-2E)
- DATA STROBE EARLY P53-41 SVDEAR0 (305-2E)
↑ AM ENABLE P53-48 SVAMEN1 (301-2D)
↑ READ GATE P53-18 SVRDGT1 (303-2F)
↑ LOCK READ PLO P53-43 SVLRDP1 (305-2A)
↑ WRITE DATA P53-22 SVXG22O (301-2D)
↑ WRITE DATA P53-46 SVWTDT1 (301-2D)
↑ WRITE CLOCK P53-47 SVWTCK1 (301-2D)
P53-23 SVXG23O (301-2E)
- WRITE GATE P53-12 SVWTGTO (301-2C)
- PAD IN PROGRESS OR NOT WRITE ALLOW P53-25 SVPDPR1 (301-2F)
↑ PROTECT P53-38 SVPROT1 (306-2D)
- WRITE CLOCK 2F P53-45 SVWCK2O (301-2B)
P53-21 SVXG21O (301-2B)
↑ BIT CLOCK P53-44 SVBTCK1 (304-2G)
P53-20 SVXG2OO (304-2F)
↑ SERVO CLOCK SVCI (06 2B)
↑ SERVO CLOCK SCL1 (07 2D)
REV (CUST) DESCRIPTION(SC) APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
213
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G90SV PWA
(13/27)
FOR PWA REV. 01B
134-296090-213-0
NEC
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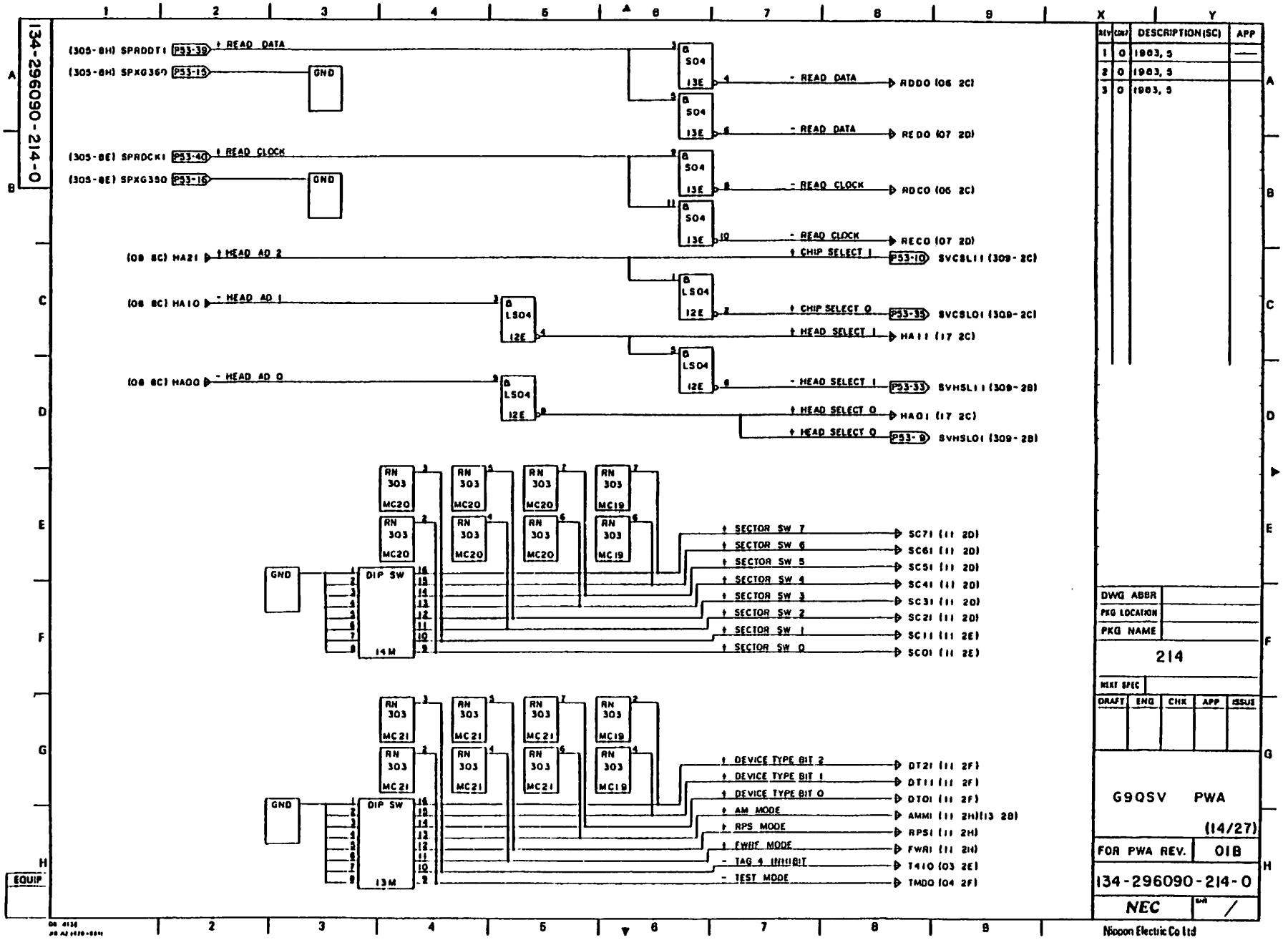
EQUIP


134-296090-214-0
(30S-8H) SPRDDT I
P53-39
↑ READ DATA
(30S-8H) SPXG36O
P53-15
GND
- READ DATA
RDDO (06 2C)
RE DO (07 2D)
(30S-8E) SPRDCK I
P53-40
↑ READ CLOCK
(30S-8E) SPXG35O
P53-16
- READ CLOCK
RDCO (06 2C)
RECO (07 2D)
(08 8C) HA2I
↑ HEAD AD 2
↑ CHIP SELECT 1
P53-10
SVCSL1 I (309-2C)
(08 8C) HA1O
- HEAD AD 1
↑ CHIP SELECT 0
P53-35
SVCSLO I (309-2C)
↑ HEAD SELECT 1
HA1 I (17 2C)
(08 8C) HAOO
- HEAD AD 0
- HEAD SELECT 1
P53-33
SVHSL1 I (309-2B)
↑ HEAD SELECT 0
HAO I (17 2C)
↑ HEAD SELECT 0
P53-9
SVHSLO I (309-2B)
S04
LS04
13E
12E
RN 303
MC20
MC19
MC21
GND
DIP SW
14M
13M
↑ SECTOR SW 7
↑ SECTOR SW 6
↑ SECTOR SW 5
↑ SECTOR SW 4
↑ SECTOR SW 3
↑ SECTOR SW 2
↑ SECTOR SW 1
↑ SECTOR SW 0
SC7I (11 2D)
SC6I (11 2D)
SC5I (11 2D)
SC4I (11 2D)
SC3I (11 2D)
SC2I (11 2D)
SC1I (11 2E)
SC0I (11 2E)
↑ DEVICE TYPE BIT 2
↑ DEVICE TYPE BIT 1
↑ DEVICE TYPE BIT 0
↑ AM MODE
↑ RPS MODE
↑ FWIF MODE
- TAG 4 INHIBIT
- TEST MODE
DT2I (11 2F)
DT1I (11 2F)
DT0I (11 2F)
AMMI (11 2H)(13 2B)
RPSI (11 2H)
FWAI (11 2H)
T4IO (03 2E)
TMDO (04 2F)
REV
CHG
DESCRIPTION(SC)
APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
214
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSV PWA
(14/27)
FOR PWA REV. 01B
134-296090-214-0
NEC
EQUIP
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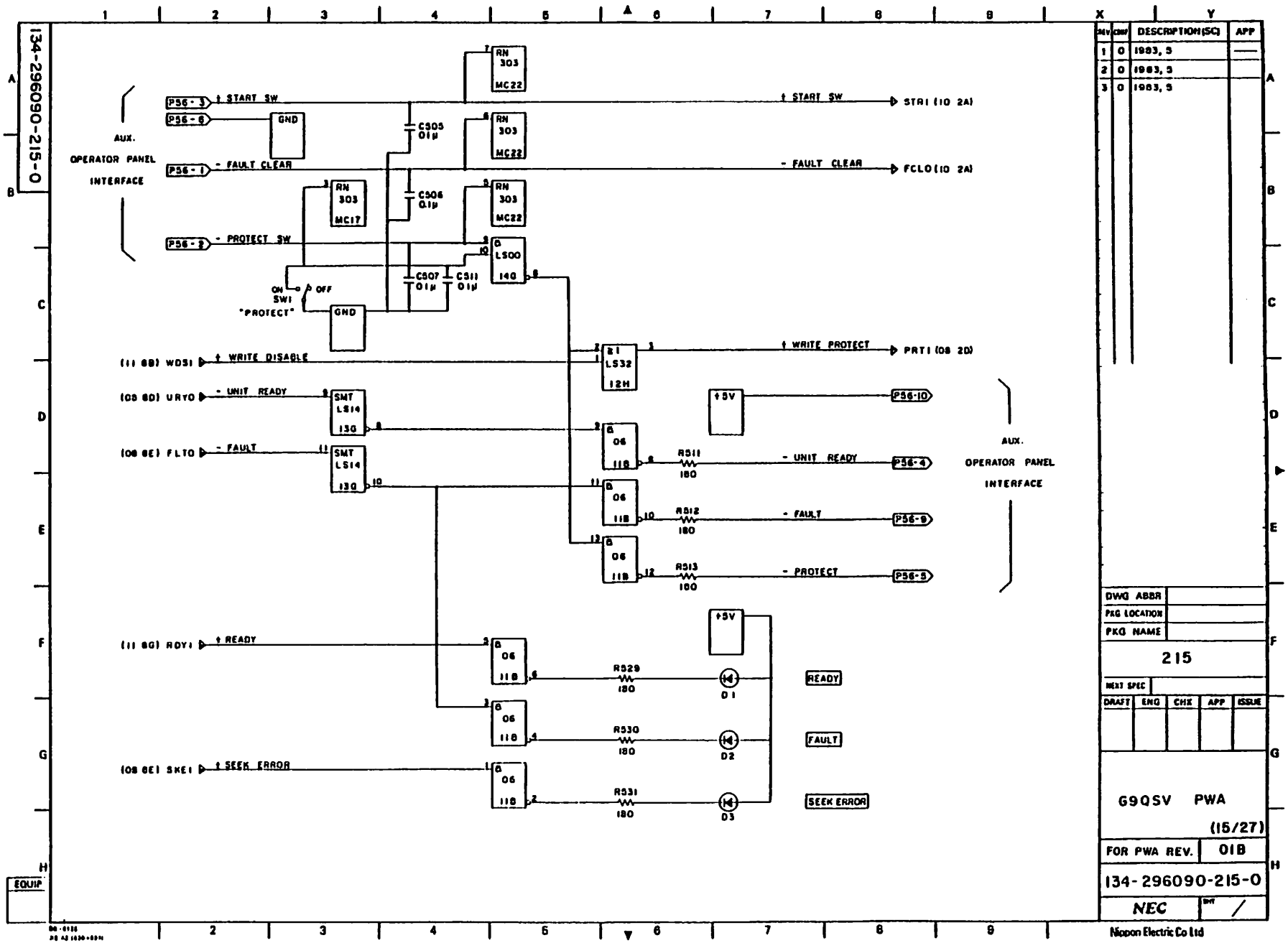
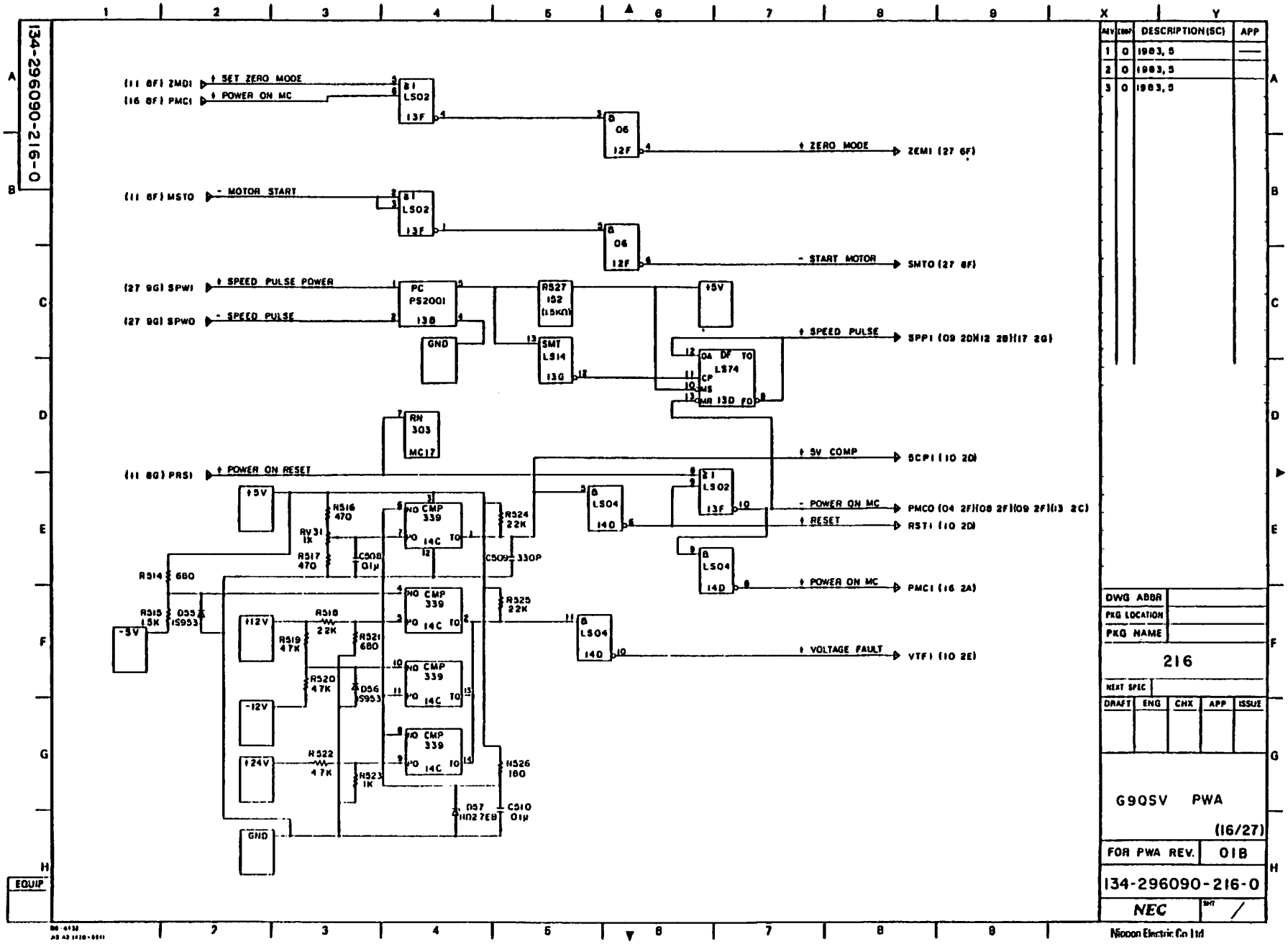
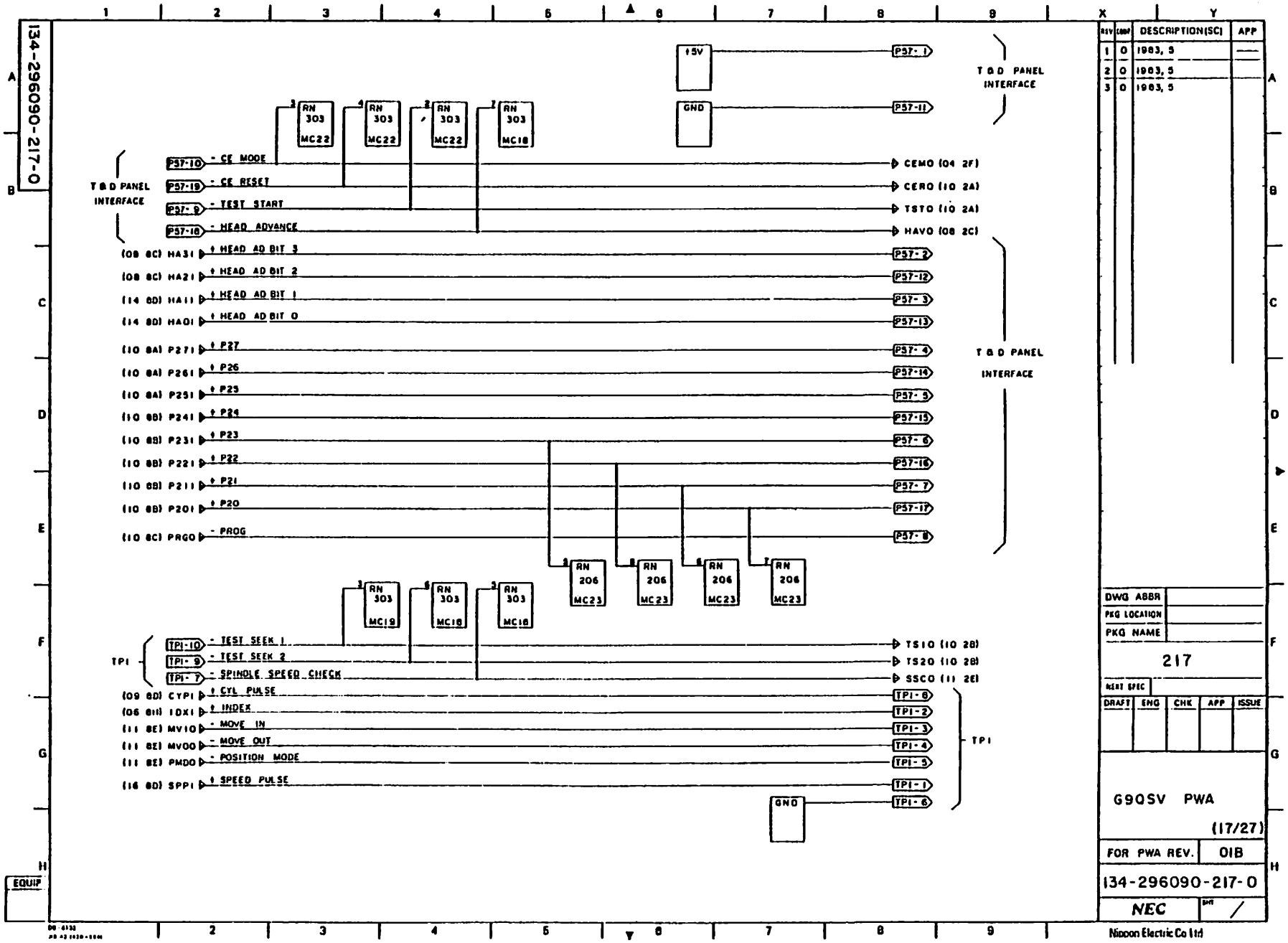
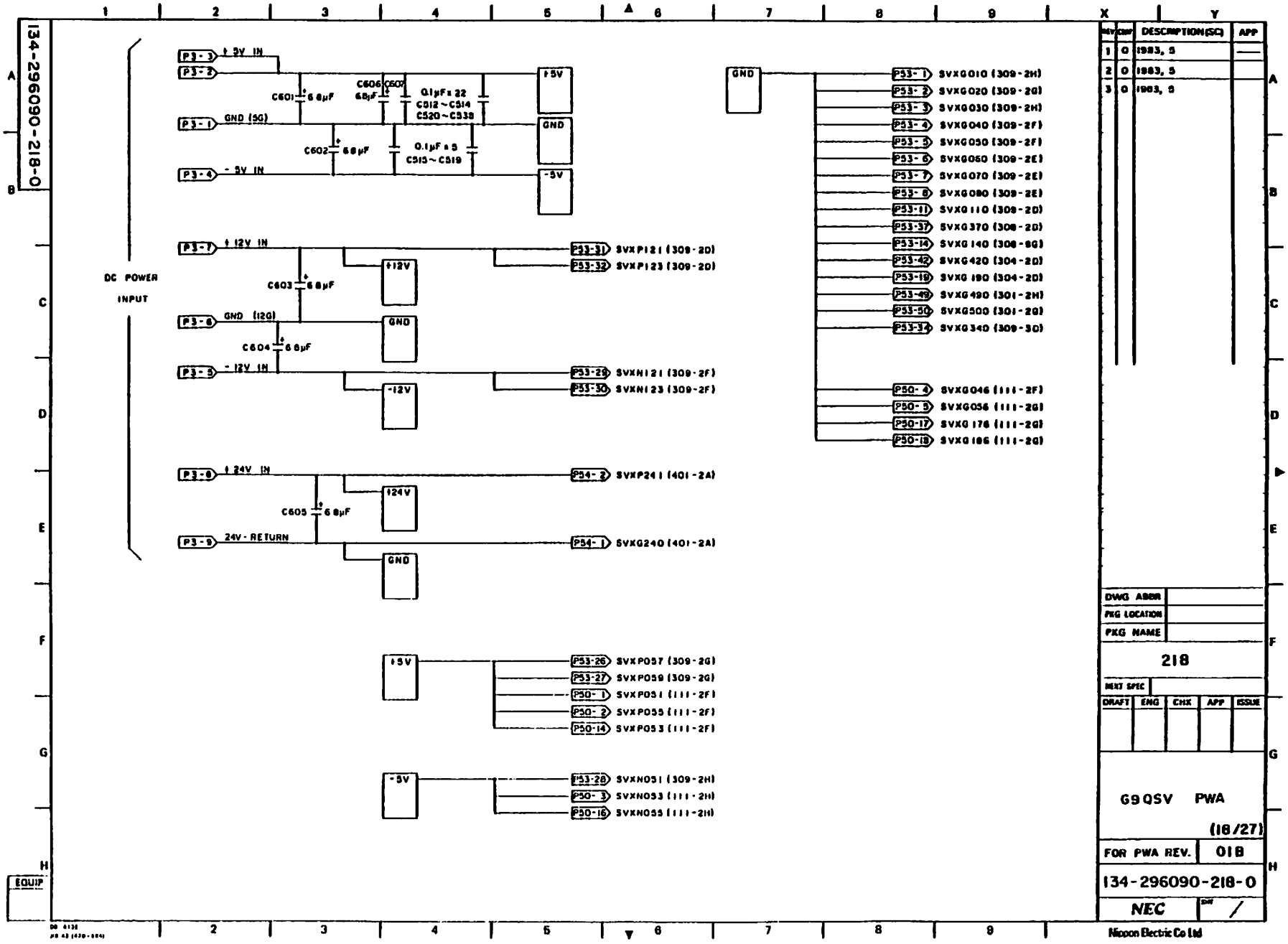
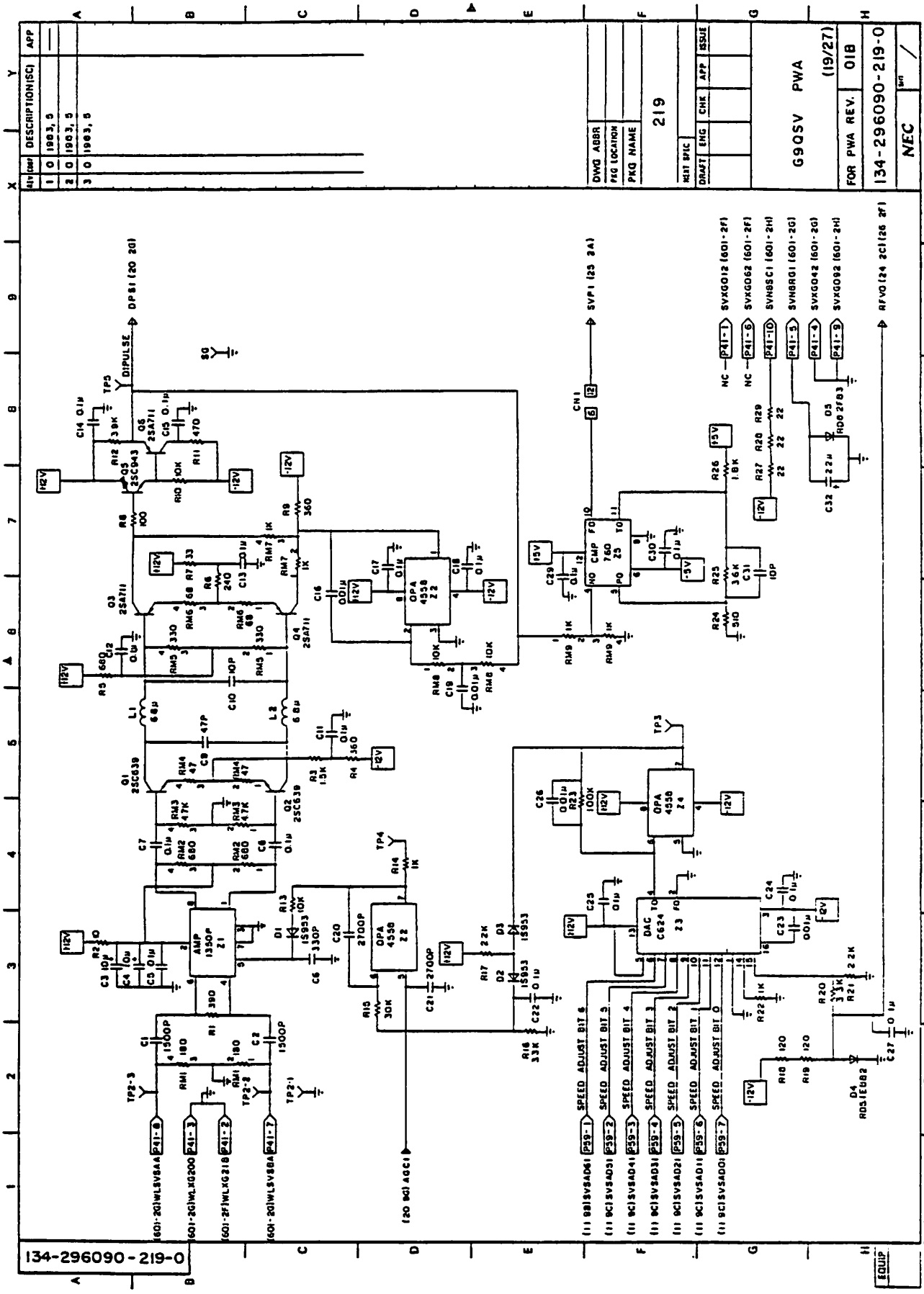
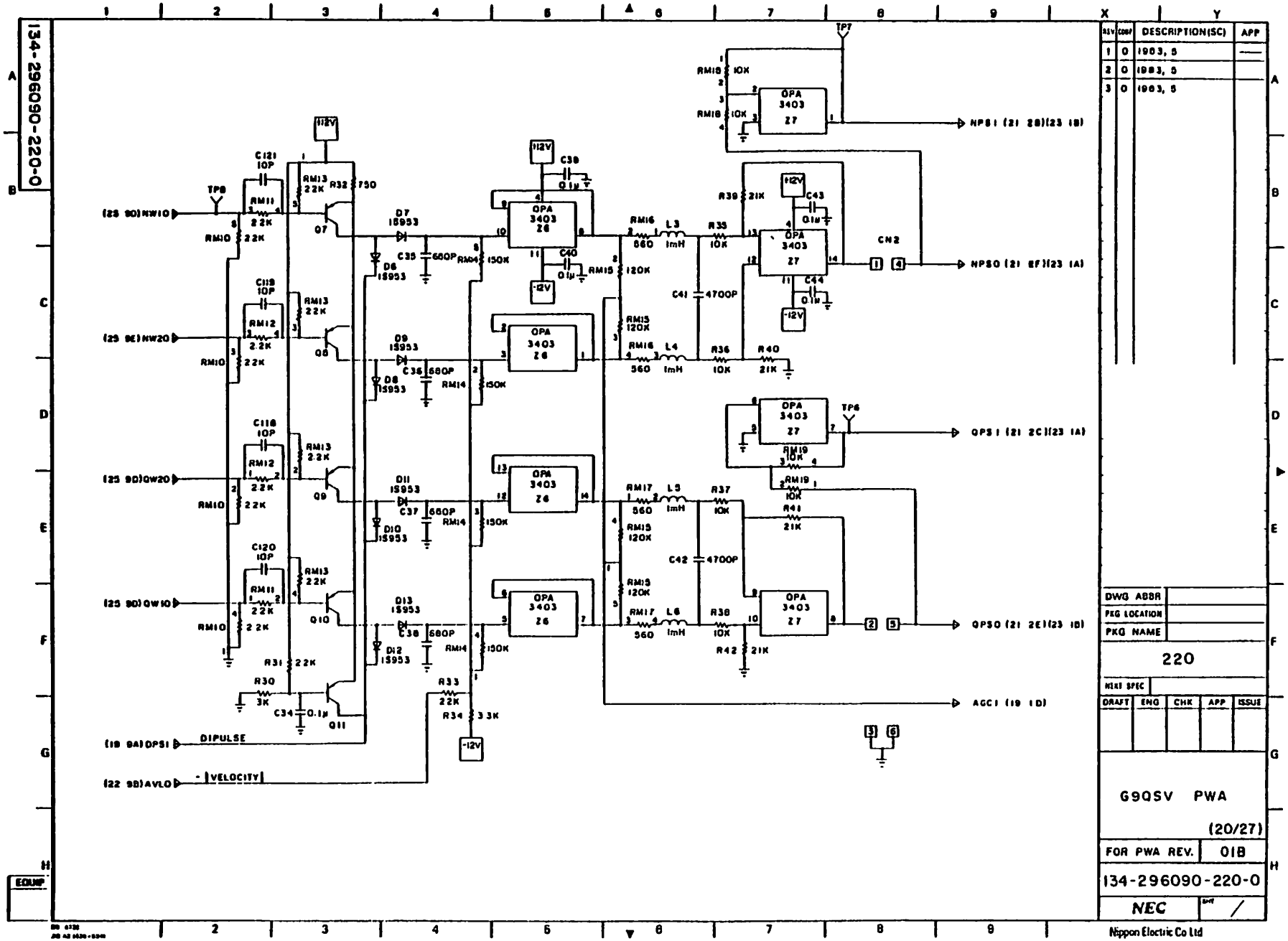

134-296090-215-0
AUX. OPERATOR PANEL INTERFACE
P56-3 ↑ START SW
P56-6 GND
P56-1 - FAULT CLEAR
P56-2 - PROTECT SW
ON SW1 OFF "PROTECT"
GND
RN 303 MC22
RN 303 MC17
C505 0.1μ
C506 0.1μ
C507 0.1μ
C511 0.1μ
LS00 14G
↑ START SW
STRI (10 2A)
- FAULT CLEAR
FCLO (10 2A)
(11 8B) WDSI ↑ WRITE DISABLE
E1 LS32 12H
↑ WRITE PROTECT
PRTI (08 2D)
(08 8D) URYO - UNIT READY
(08 8E) FLTO - FAULT
SMT LS14 13G
↑5V
P56-10
06 11B
R511 180
- UNIT READY
P56-4
R512 180
- FAULT
P56-9
R513 180
- PROTECT
P56-5
AUX. OPERATOR PANEL INTERFACE
(11 8G) RDYI ↑ READY
R529 180
D1
READY
R530 180
D2
FAULT
(08 8E) SKEI ↑ SEEK ERROR
R531 180
D3
SEEK ERROR
EQUIP
REV DIV DESCRIPTION(SC) APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
215
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9QSV PWA
(15/27)
FOR PWA REV. 01B
134-296090-215-0
NEC
Nippon Electric Co Ltd


134-296090-216-0
(11 8F) ZMDI
↑ SET ZERO MODE
(16 8F) PMCI
↑ POWER ON MC
81 LS02 13F
B 06 12F
↑ ZERO MODE
ZEMI (27 6F)
(11 8F) MSTO
- MOTOR START
81 LS02 13F
B 06 12F
- START MOTOR
SMTO (27 8F)
(27 9G) SPWI
↑ SPEED PULSE POWER
(27 9G) SPWO
- SPEED PULSE
PC PS2001 13B
GND
R527 1Ω2 (1.5KΩ)
SMT LS14 13G
↑5V
↑ SPEED PULSE
SPPI (09 2D)(12 2B)(17 2G)
QA DF TO LS74 CP MS MR 13D FD
RN 303 MC17
↑ 5V COMP
5CPI (10 2D)
(11 8G) PRSI
↑ POWER ON RESET
21 LS02 13F
- POWER ON MC
PMCO (04 2F)(08 2F)(09 2F)(13 2C)
↑ RESET
RSTI (10 2D)
B LS04 14D
↑ POWER ON MC
PMCI (16 2A)
↑5V
R516 470
RV31 1K
R517 470
C508 .01μ
NO CMP 339 14C
R524 22K
C509 330P
B LS04 14D
R514 680
R515 1.5K
D55 1SS93
-5V
↑12V
R518 22K
R519 47K
R521 680
R525 22K
B LS04 14D
↑ VOLTAGE FAULT
VTFI (10 2E)
R520 47K
D56 1SS93
-12V
↑24V
R522 47K
R523 1K
R526 180
C510 .01μ
GND
EQUIP
DESCRIPTION(SC)
1 0 1983, 5
2 0 1983, 5
3 0 1983, 9
DWG ABBR
PKG LOCATION
PKG NAME
216
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G90SV PWA
(16/27)
FOR PWA REV. 01B
134-296090-216-0
NEC
Nippon Electric Co Ltd


134-296090-217-0
+5V
GND
P57-1
P57-11
T&D PANEL INTERFACE
RN 303 MC22
RN 303 MC22
RN 303 MC22
RN 303 MC18
P57-10 - CE MODE
P57-19 - CE RESET
P57-9 - TEST START
P57-18 - HEAD ADVANCE
CEMO (04 2F)
CERO (10 2A)
TSTO (10 2A)
HAVO (08 2C)
(08 8C) HA3I - HEAD AD BIT 3
(08 8C) HA2I - HEAD AD BIT 2
(14 8D) HA1I - HEAD AD BIT 1
(14 8D) HA0I - HEAD AD BIT 0
P57-2
P57-12
P57-3
P57-13
(10 8A) P27I - P27
(10 8A) P26I - P26
(10 8A) P25I - P25
(10 8B) P24I - P24
(10 8B) P23I - P23
(10 8B) P22I - P22
(10 8B) P21I - P21
(10 8B) P20I - P20
(10 8C) PRGO - PROG
P57-4
P57-14
P57-5
P57-15
P57-6
P57-16
P57-7
P57-17
P57-8
T&D PANEL INTERFACE
RN 206 MC23
RN 206 MC23
RN 206 MC23
RN 206 MC23
RN 303 MC19
RN 303 MC18
RN 303 MC18
TPI
TPI-10 - TEST SEEK 1
TPI-9 - TEST SEEK 2
TPI-7 - SPINDLE SPEED CHECK
TS1O (10 2B)
TS2O (10 2B)
SSCO (11 2E)
(09 8D) CYPI - CYL PULSE
(06 8H) IDXI - INDEX
(11 8E) MV1O - MOVE IN
(11 8E) MV0O - MOVE OUT
(11 8E) PMDO - POSITION MODE
(16 8D) SPPI - SPEED PULSE
TPI-6
TPI-2
TPI-3
TPI-4
TPI-5
TPI-1
TPI-8
GND
TPI
EQUIP
REV | COMP | DESCRIPTION(SC) | APP
1 | 0 | 1983, 5
2 | 0 | 1983, 5
3 | 0 | 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
217
NEXT SPEC
DRAFT | ENG | CHK | APP | ISSUE
G90SV PWA
(17/27)
FOR PWA REV. 01B
134-296090-217-0
NEC
Nippon Electric Co Ltd


134-296090-218-0
DC POWER INPUT
P3-3 +5V IN
P3-2
P3-1 GND (5G)
P3-4 -5V IN
C601 6.8μF
C606 C607 6.8μF
C612~C614 C520~C538 0.1μF×22
C602 6.8μF
C515~C519 0.1μF×5
+5V
GND
-5V
P3-7 +12V IN
P3-8 GND (12G)
C603 6.8μF
C604 6.8μF
+12V
GND
P3-5 -12V IN
-12V
P53-31 SVXP121 (309-2D)
P53-32 SVXP123 (309-2D)
P53-29 SVXN121 (309-2F)
P53-30 SVXN123 (309-2F)
P3-6 +24V IN
P3-9 24V-RETURN
C605 6.8μF
+24V
GND
P54-2 SVXP241 (401-2A)
P54-1 SVXG240 (401-2A)
+5V
-5V
P53-26 SVXP057 (309-2G)
P53-27 SVXP059 (309-2G)
P50-1 SVXP051 (111-2F)
P50-2 SVXP055 (111-2F)
P50-14 SVXP053 (111-2F)
P53-28 SVXN051 (309-2H)
P50-3 SVXN053 (111-2H)
P50-16 SVXN055 (111-2H)
GND
P53-1 SVXG010 (309-2H)
P53-2 SVXG020 (309-2G)
P53-3 SVXG030 (309-2H)
P53-4 SVXG040 (309-2F)
P53-5 SVXG050 (309-2F)
P53-6 SVXG060 (309-2E)
P53-7 SVXG070 (309-2E)
P53-8 SVXG080 (309-2E)
P53-11 SVXG110 (309-2D)
P53-37 SVXG370 (309-2D)
P53-14 SVXG140 (309-6G)
P53-42 SVXG420 (304-2D)
P53-19 SVXG190 (304-2D)
P53-49 SVXG490 (301-2H)
P53-50 SVXG500 (301-2D)
P53-34 SVXG340 (309-3D)
P50-4 SVXG046 (111-2F)
P50-5 SVXG056 (111-2G)
P50-17 SVXG176 (111-2G)
P50-18 SVXG186 (111-2G)
REV DIF DESCRIPTION(SC) APP
1 0 1983, 9
2 0 1983, 9
3 0 1983, 9
DWG ABBR
PKG LOCATION
PKG NAME
218
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9QSV PWA
(18/27)
FOR PWA REV. 01B
134-296090-218-0
NEC
EQUIP
Nippon Electric Co Ltd


134-296090-219-0
G90SV PWA
(19/27)
FOR PWA REV. 018
134-296090-219-0
NEC
Nippon Electric Co.Ltd
DESCRIPTION(SC)
1983, 5
DRAFT
ENG
CHK
APP
ISSUE
DWG ABBR
PKG LOCATION
PKG NAME
219
DIPULSE
SG
AMP 1350P 21
OPA 4558 22
DAC C624 23 P0
SPEED ADJUST BIT 6
SPEED ADJUST BIT 5
SPEED ADJUST BIT 4
SPEED ADJUST BIT 3
SPEED ADJUST BIT 2
SPEED ADJUST BIT 1
SPEED ADJUST BIT 0
EQUIP



REV	CONF	DESCRIPTION(SC)	APP
1	0	1983, 5	
2	0	1983, 5	
3	0	1983, 5	

DWG ABBR	
PKG LOCATION	
PKG NAME	
220	
NEXT SPEC	

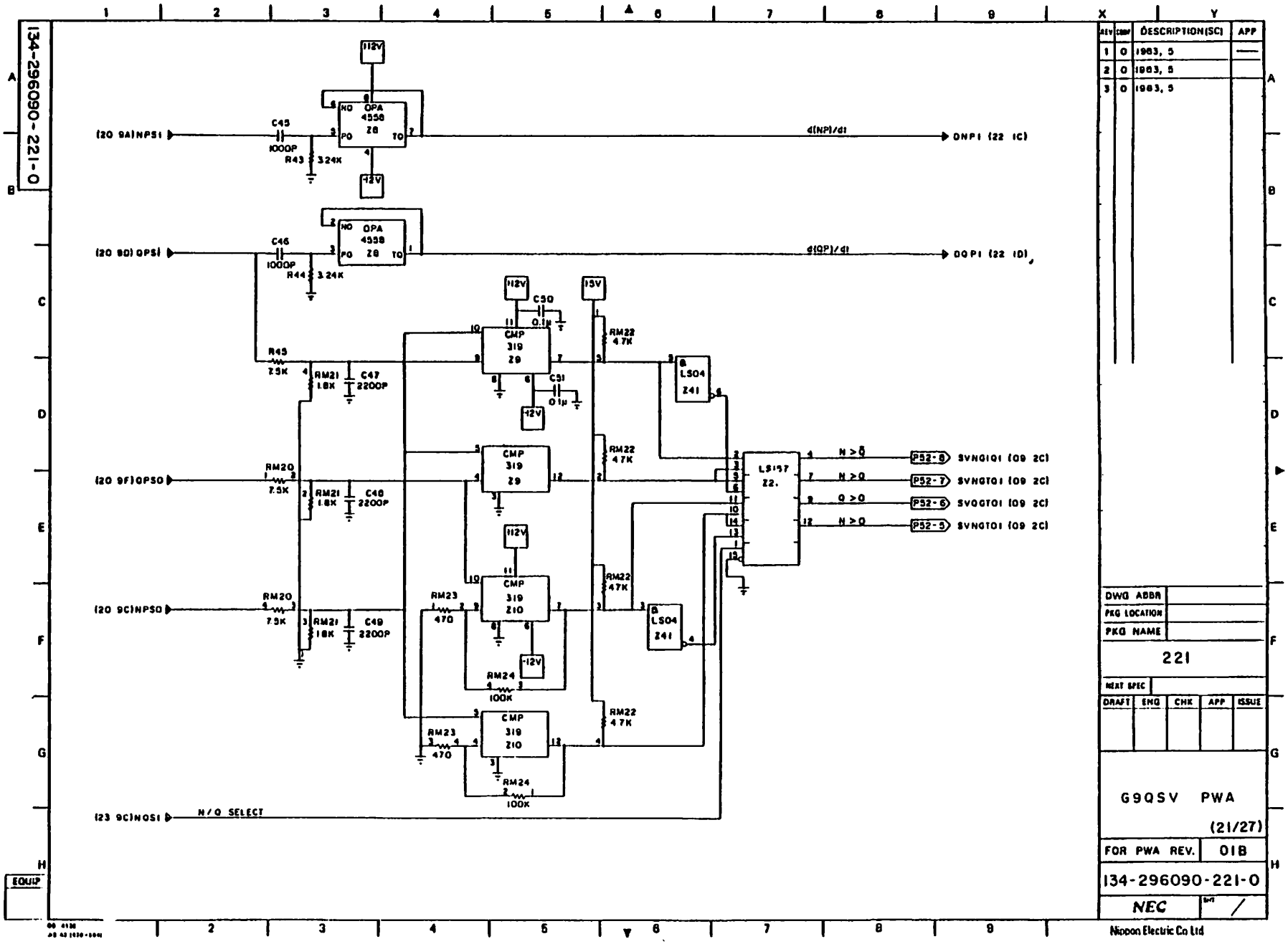
DRAFT	ENG	CHK	APP	ISSUE

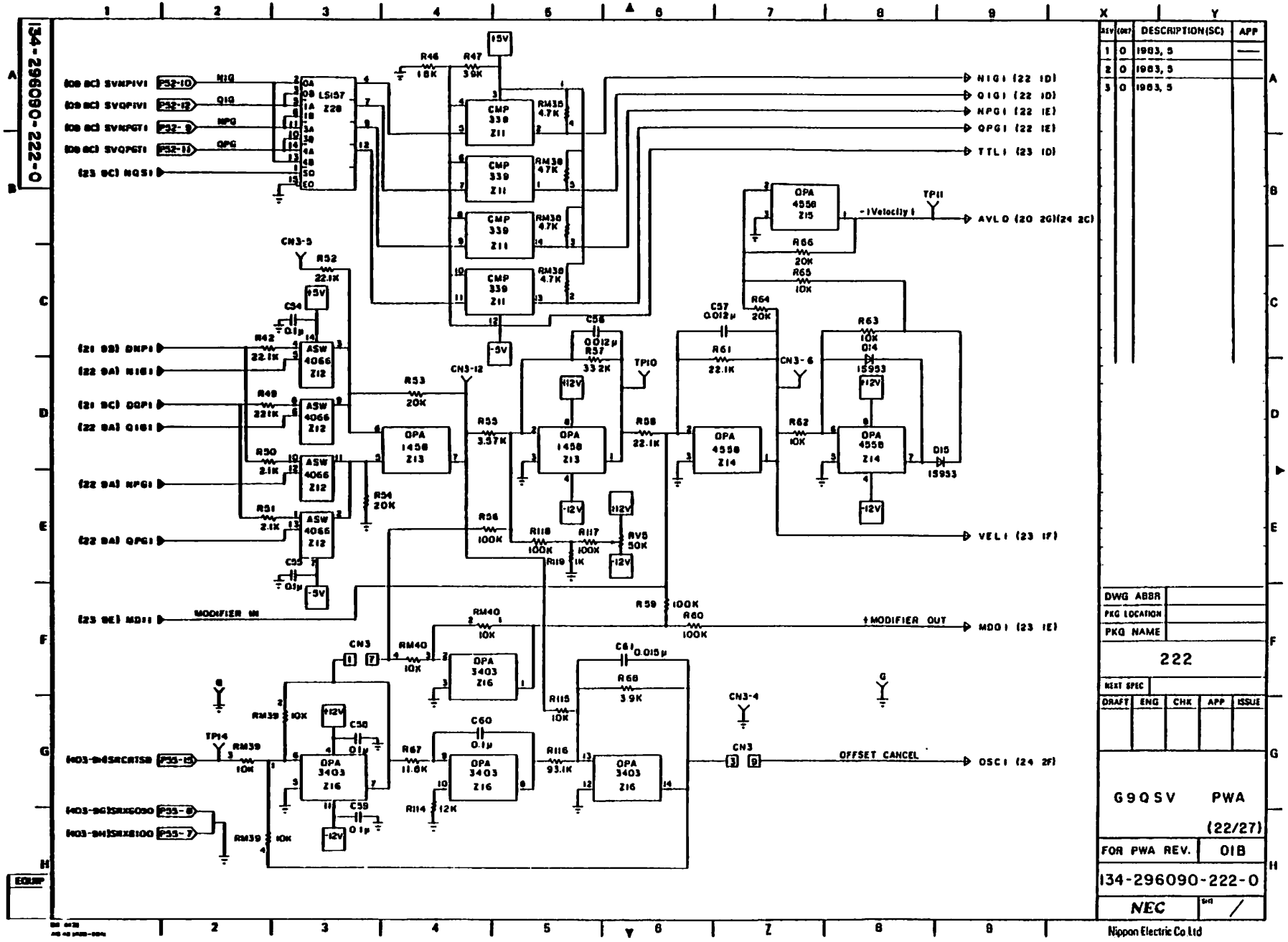
G9QSV PWA

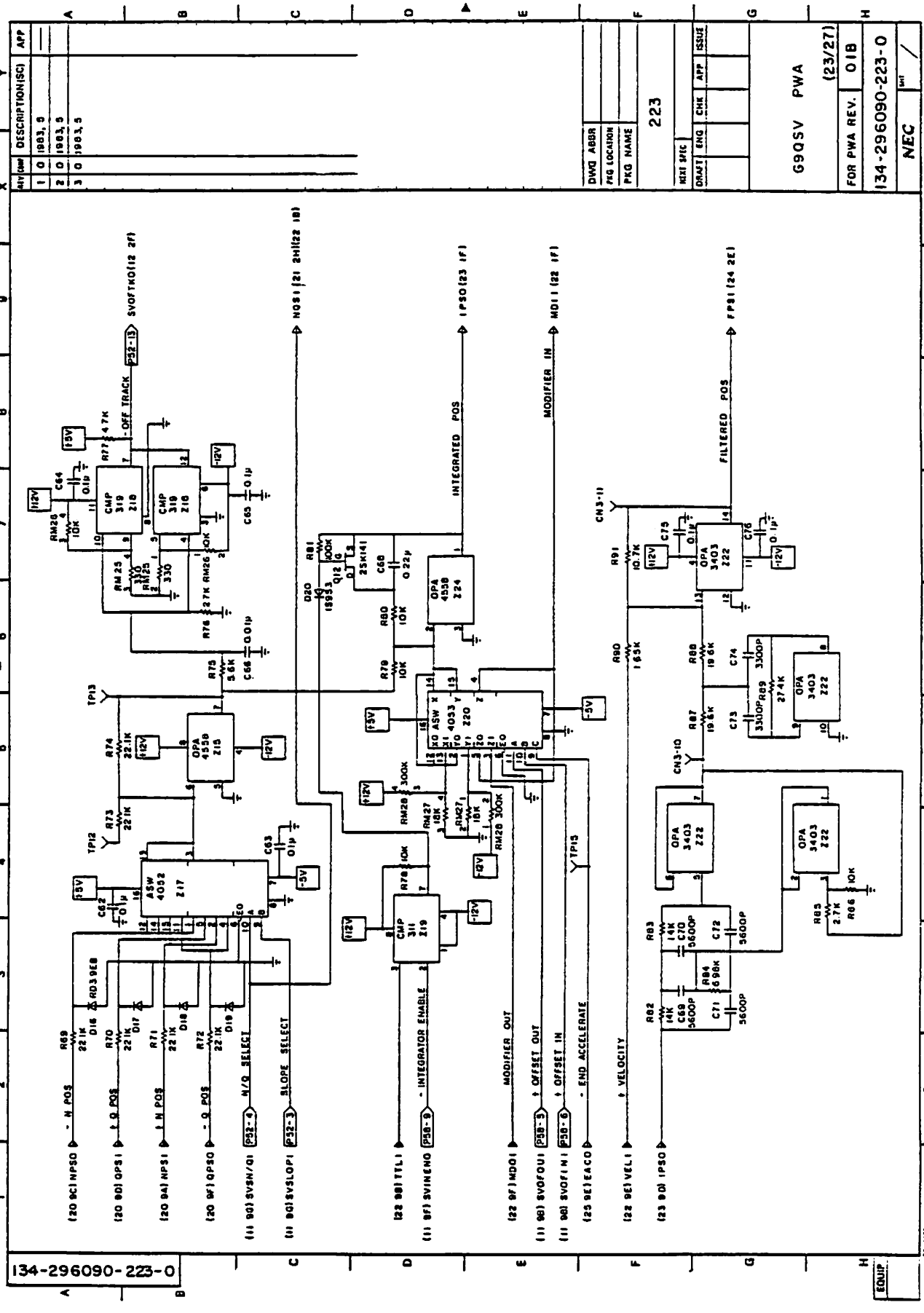
(20/27)

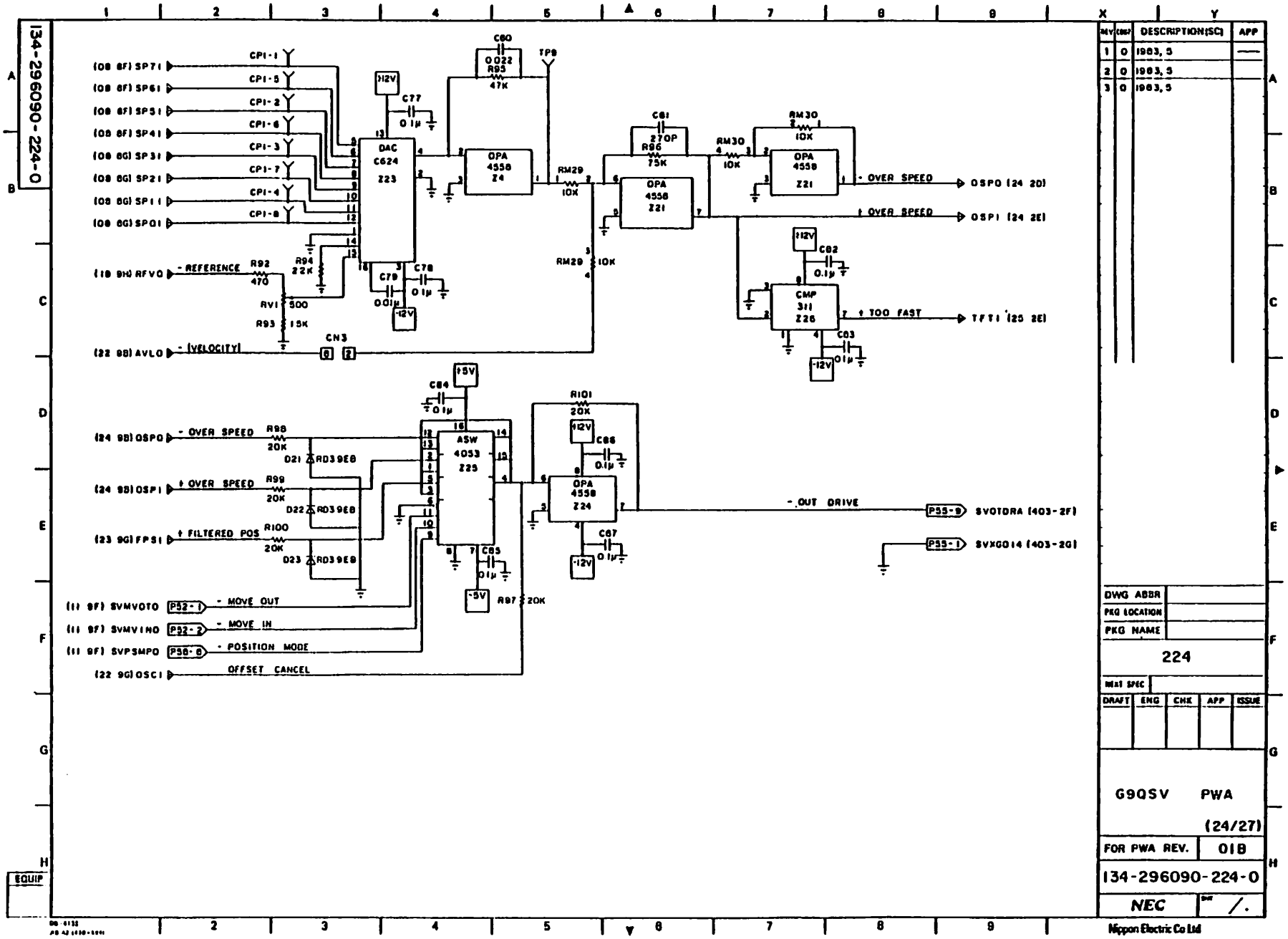
FOR PWA REV.	01B
134-296090-220-0	
NEC	SHT /

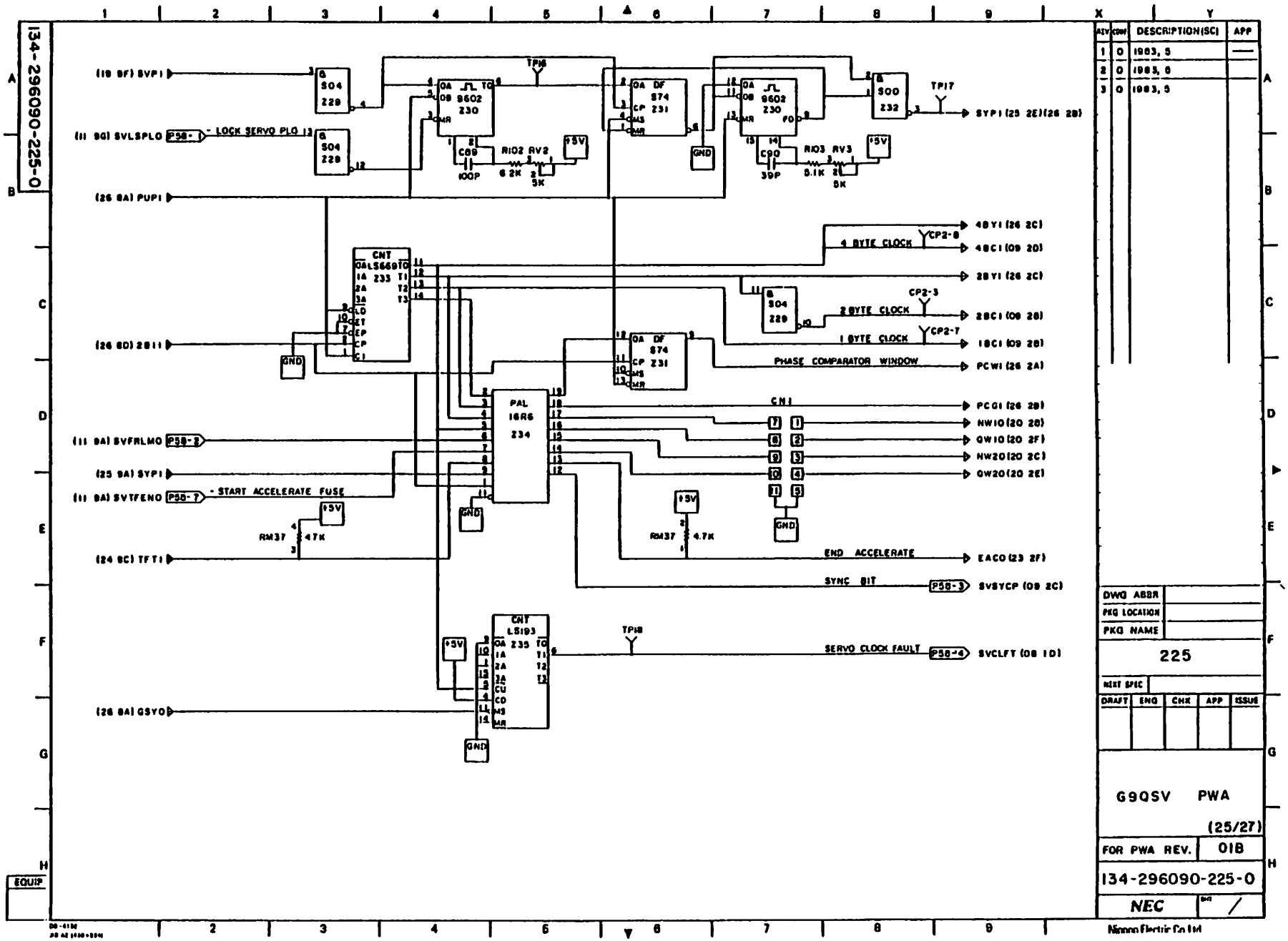
Nippon Electric Co Ltd

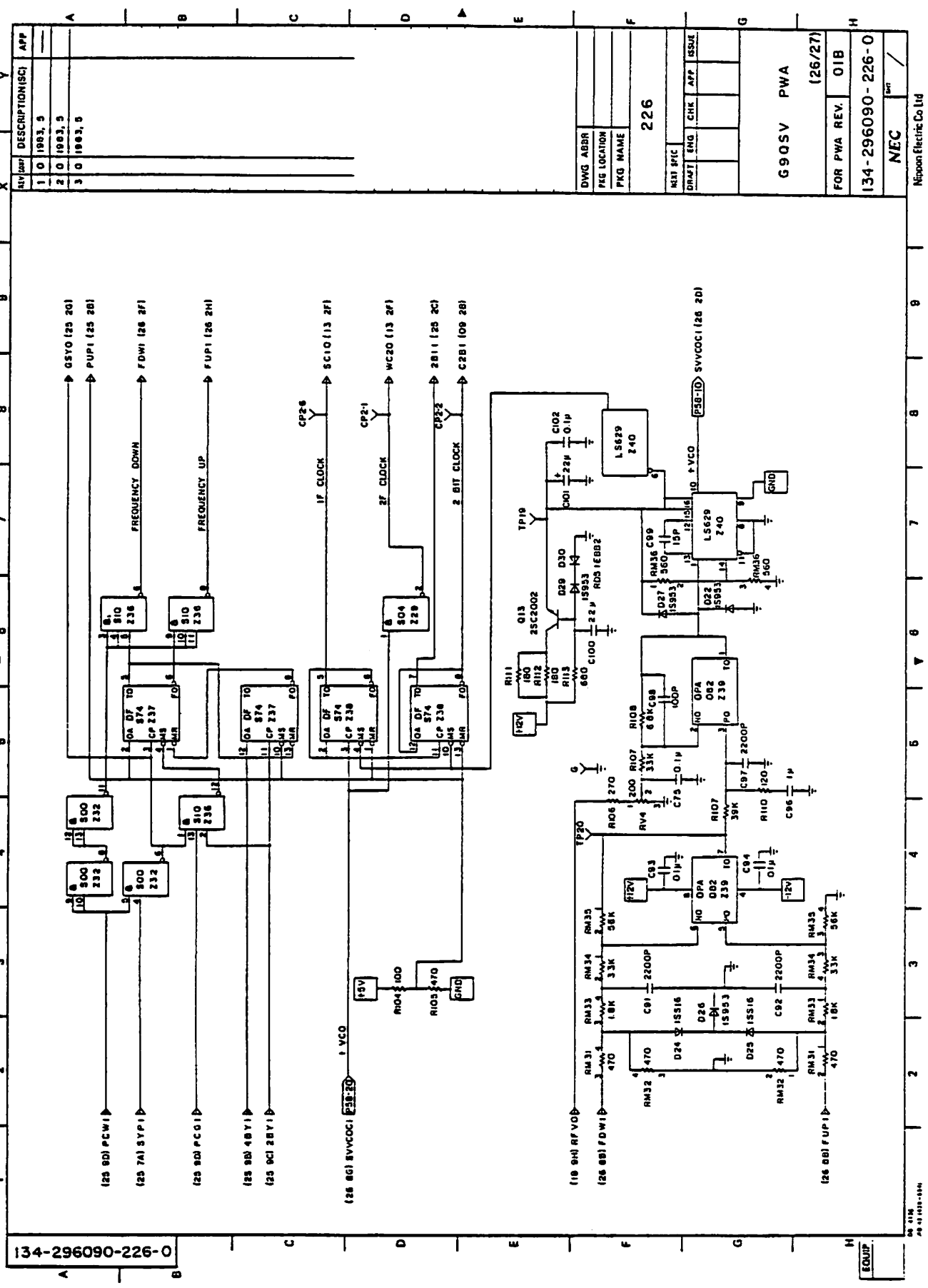

134-296090-221-0
(20 9A)NPS1
C45
1000P
R43
3.24K
OPA
4558
Z8
+12V
-12V
d(NP)/dt
DNP1 (22 1C)
(20 9D)OPS1
C46
1000P
R44
3.24K
d(OP)/dt
DOP1 (22 1D)
CMP
319
Z9
Z10
C50
0.1μ
C51
R45
7.5K
RM21
1.8K
C47
2200P
C48
C49
RM20
RM22
4.7K
RM23
470
RM24
100K
LS04
Z41
LS157
Z2.
(20 9F)OPS0
(20 9C)NPS0
(23 9C)NOS1
N/O SELECT
N>0
O>0
P52-8
P52-7
P52-6
P52-5
SVNG1O1 (09 2C)
SVNGTO1 (09 2C)
SVOGTO1 (09 2C)
REV
CHNG
DESCRIPTION(SC)
APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
221
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSV PWA
(21/27)
FOR PWA REV.
01B
134-296090-221-0
NEC
EQUIP
Nippon Electric Co Ltd

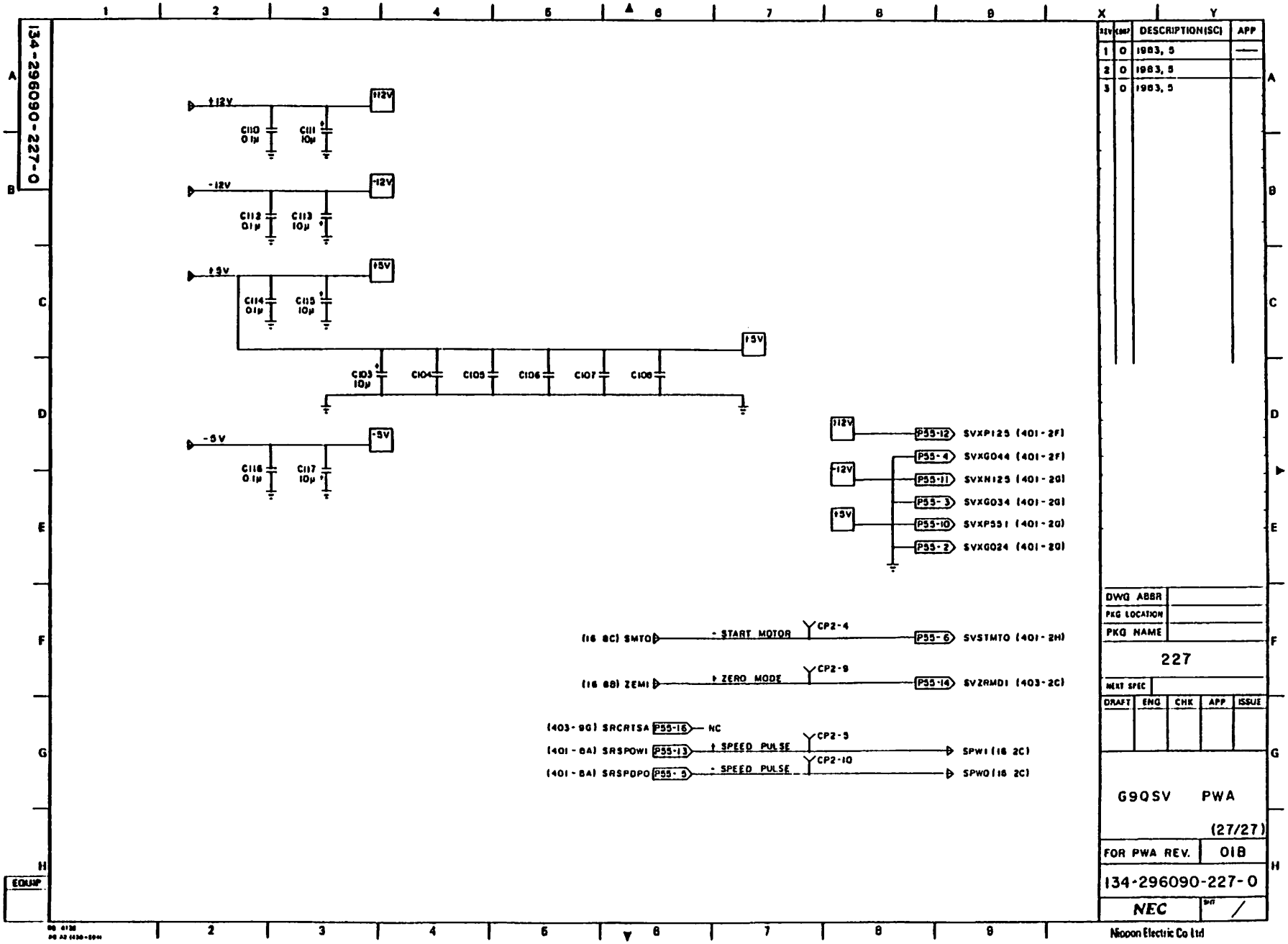

134-296090-222-0
DESCRIPTION(SC)
APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
222
NEXT SPEC
DRAFT ENG CHK APP ISSUE
G9QSV PWA
(22/27)
FOR PWA REV. 01B
134-296090-222-0
NEC
Nippon Electric Co Ltd
EQUIP
+15V
-15V
+5V
-5V
+12V
-12V
R46 18K
R47 39K
RM35 4.7K
RM36 4.7K
RM37 4.7K
RM38 4.7K
CMP 339 Z11
LS157 Z28
ASW 4066 Z12
OPA 1458 Z13
OPA 4558 Z14
OPA 4558 Z15
OPA 3403 Z16
R52 22.1K
R53 20K
R54 20K
R55 3.57K
R56 100K
R57 33.2K
R58 22.1K
R59 100K
R60 100K
R61 22.1K
R62 10K
R63 10K
R64 20K
R65 10K
R66 20K
R67 11.8K
R68 39K
R114 12K
R115 10K
R116 93.1K
R117 100K
R118 100K
R119 1K
RV5 50K
RM39 10K
RM40 10K
C54 0.1μ
C55 0.1μ
C56 0.012μ
C57 0.012μ
C58 0.1μ
C59 0.1μ
C60 0.1μ
C61 0.015μ
D14 1S933
D15 1S933
TP10
TP11
TP14
CN3-5
CN3-12
CN3-6
CN3-4
CN3
(23 9C) NQS1
(23 9E) MDI1
MODIFIER IN
+MODIFIER OUT
MDO1 (23 1E)
NIG1 (22 1D)
QIG1 (22 1D)
NPG1 (22 1E)
QPG1 (22 1E)
TTL1 (23 1D)
AVLO (20 2G)(24 2C)
-1Velocity 1
VEL1 (23 1F)
OSC1 (24 2F)
OFFSET CANCEL
(22 9A) NIG1
(22 9A) QIG1
(22 9A) NPG1
(22 9A) QPG1
(21 9B) DNP1
(21 9C) DQP1
P52-10
P52-12
P52- 9
P52-11
P55-15
P55- 9
P55- 7

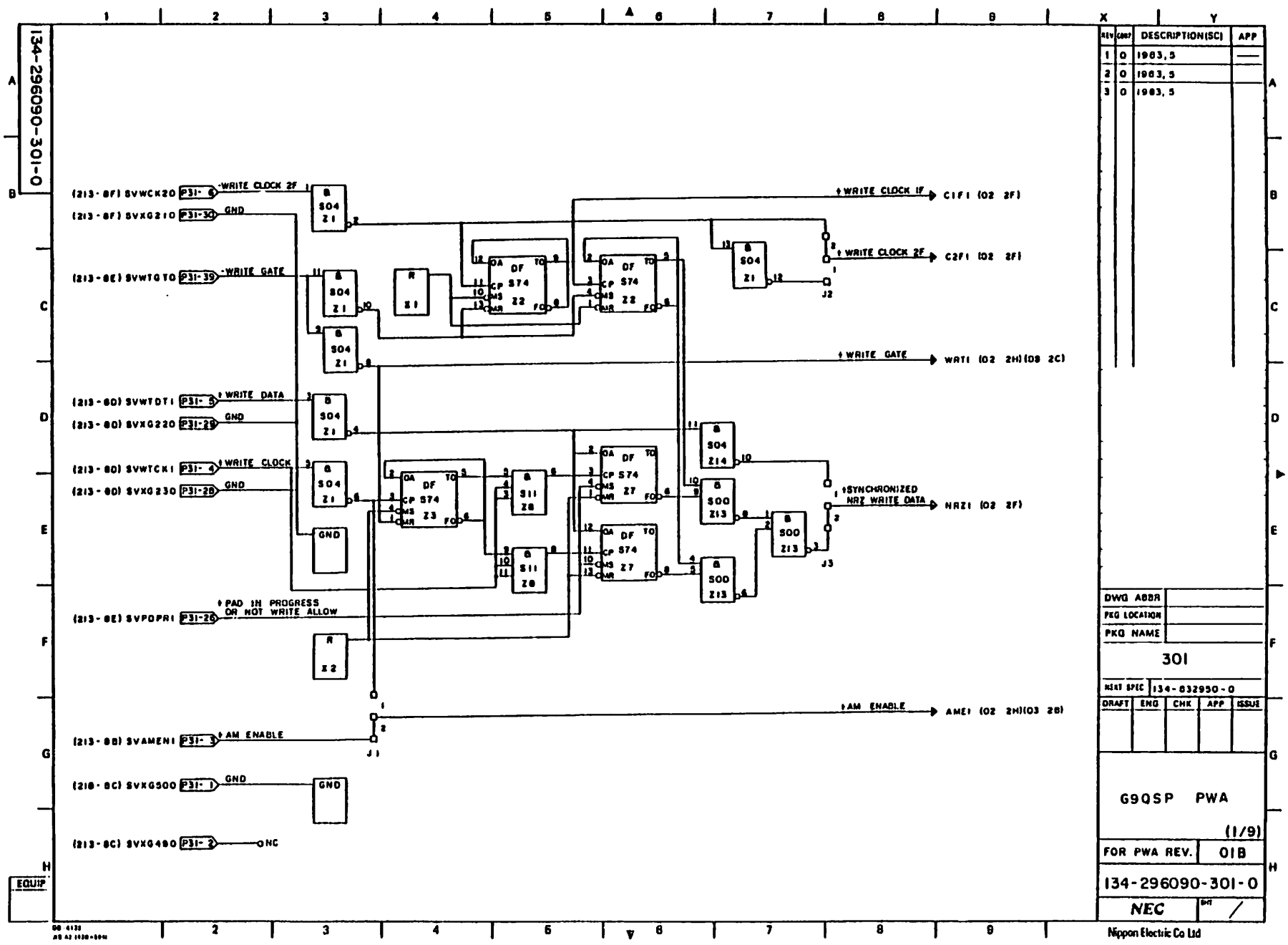

134-296090-223-0
69SV PWA
(23/27)
FOR PWA REV. 018
134-296090-223-0
NEC
Nippon Electric Co.ltd
223
DRAFT
ENG
CHK
APP
ISSUE
- N POS
+ Q POS
+ N POS
- Q POS
H/Q SELECT
SLOPE SELECT
- INTEGRATOR ENABLE
MODIFIER OUT
+ OFFSET OUT
+ OFFSET IN
- END ACCELERATE
+ VELOCITY
- OFF TRACK
INTEGRATED POS
MODIFIER IN
FILTERED POS
OPA 4556 Z15
ASW 4052 Z17
CMP 319 Z18
CMP 311 Z19
ASW 4053 Z20
OPA 4558 Z24
OPA 3403 Z22

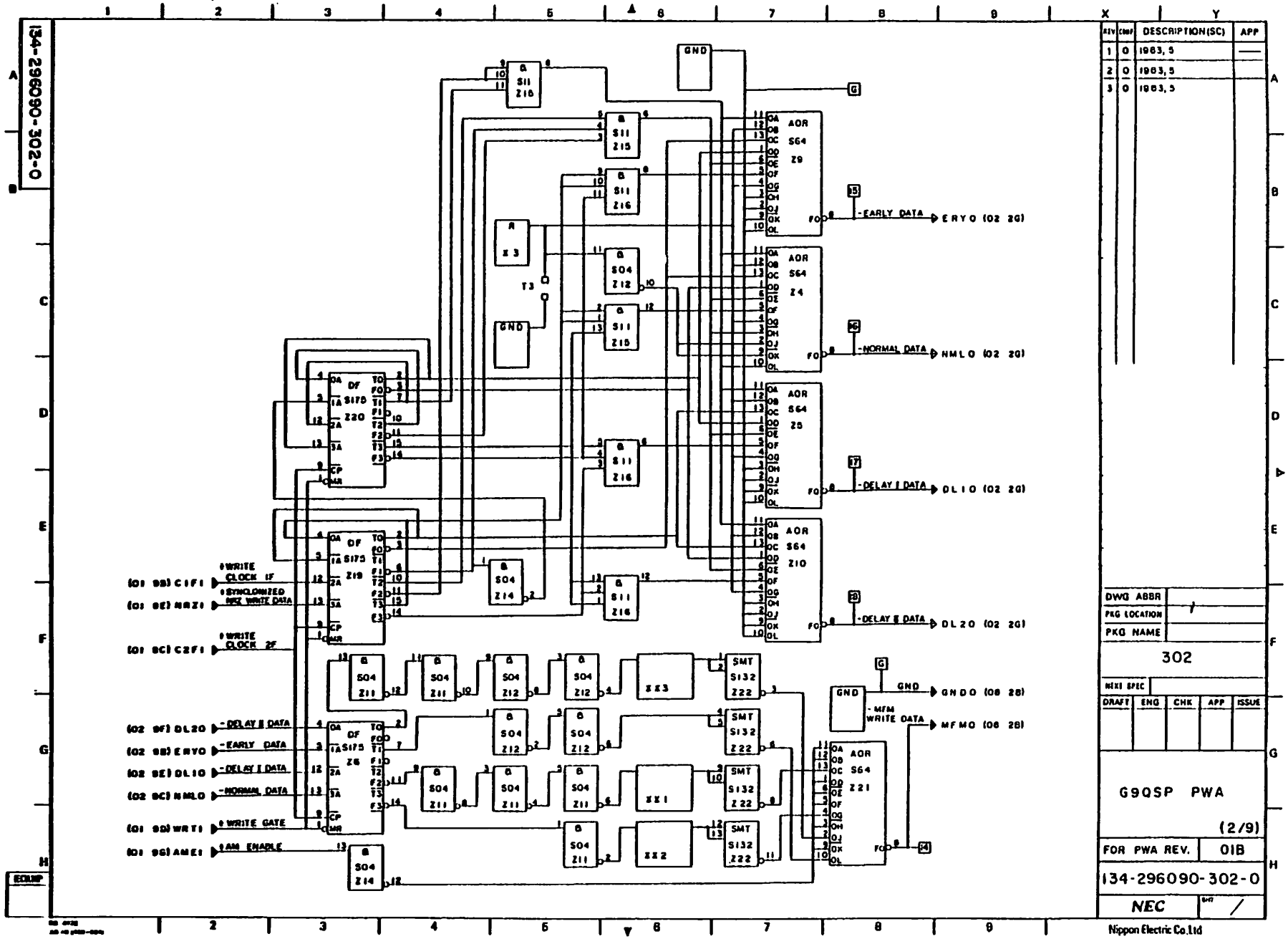

134-296090-224-0
DAC C624 Z23
OPA 4558 Z4
OPA 4558 Z21
OPA 4558 Z21
OPA 4558 Z24
CMP 311 Z26
ASW 4053 Z25
- OVER SPEED
+ OVER SPEED
+ TOO FAST
- OUT DRIVE
- REFERENCE
- VELOCITY
+ FILTERED POS
- MOVE OUT
- MOVE IN
- POSITION MODE
OFFSET CANCEL
OSPO (24 2D)
OSP1 (24 2E)
TFT1 (25 2E)
SVOTDRA (403-2F)
SVXGO14 (403-2G)
DWG ABBR
PKG LOCATION
PKG NAME
224
DRAFT
ENG
CHK
APP
ISSUE
G9QSV PWA
(24/27)
FOR PWA REV. 01B
134-296090-224-0
NEC
Nippon Electric Co Ltd

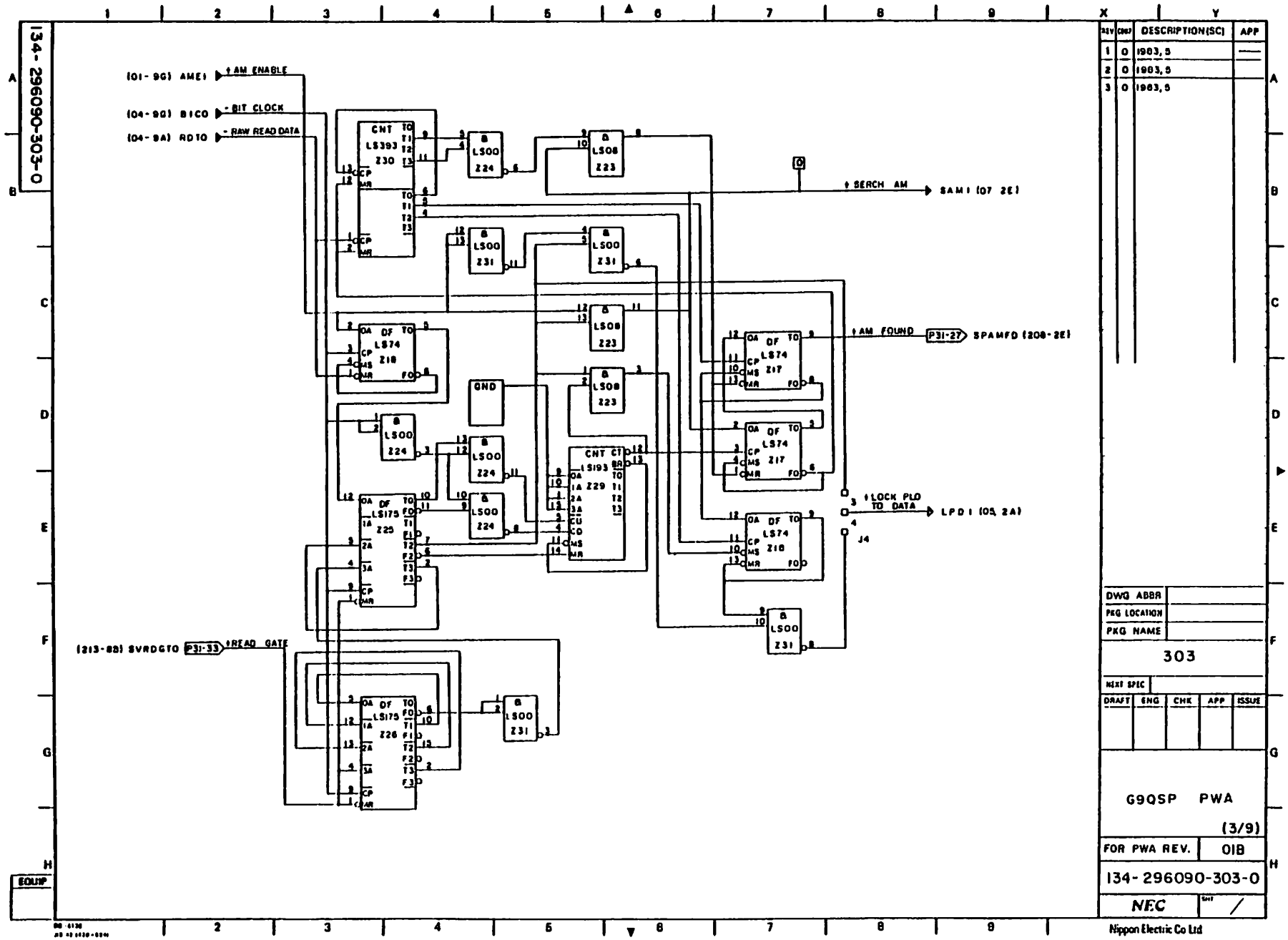

134-296090-225-0
(19 9F) SVP1
(11 9G) SVLSPLO
P58-1
- LOCK SERVO PLO
(25 9A) PUP1
(26 8D) 2B11
(11 9A) SVFRLMO
P58-2
(25 9A) SYP1
(11 9A) SVTFENO
P58-7
- START ACCELERATE FUSE
(24 9C) TFT1
(26 8A) GSY0
TP16
TP17
TP18
+5V
GND
RM37
4.7K
C89
100P
R102
6.2K
RV2
5K
C90
39P
R103
5.1K
RV3
5K
CNT
LS669
233
CNT
LS193
235
PAL
16R6
234
DF
S74
231
9602
230
S04
229
S00
232
4 BYTE CLOCK
CP2-0
2 BYTE CLOCK
CP2-3
1 BYTE CLOCK
CP2-7
PHASE COMPARATOR WINDOW
CN1
END ACCELERATE
SYNC BIT
P58-3
SERVO CLOCK FAULT
P58-4
4BY1 (26 2C)
4BC1 (09 2D)
2BY1 (26 2C)
2BC1 (09 2B)
1BC1 (09 2B)
PCW1 (26 2A)
PCG1 (26 2B)
NW10 (20 2B)
QW10 (20 2F)
NW20 (20 2C)
QW20 (20 2E)
EAC0 (23 2F)
SVSYCP (09 2C)
SVCLFT (08 1D)
SYP1 (25 2E)(26 2B)
EQUIP
REV
COM
DESCRIPTION(SC)
APP
1 0 1983, 5
2 0 1983, 6
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
225
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSV PWA
(25/27)
FOR PWA REV.
018
134-296090-225-0
NEC
Nippon Electric Co Ltd

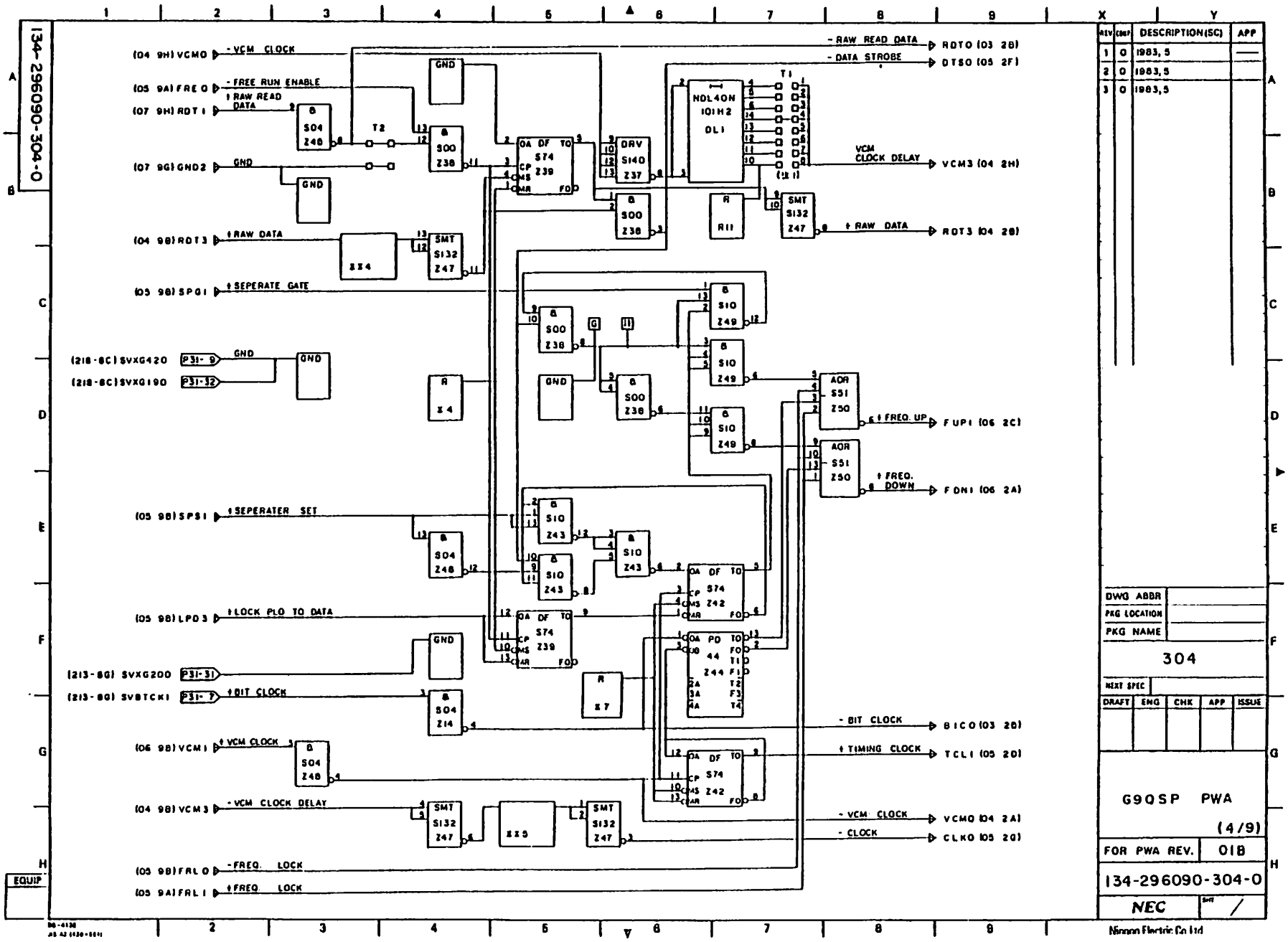

G90SV PWA
(26/27)
134-296090-226-0
NEC
Nippon Electric Co.Ltd
FOR PWA REV. 018
DWG ABBR
PKG LOCATION
PKG NAME
226
FREQUENCY DOWN
FREQUENCY UP
IF CLOCK
2F CLOCK
2 BIT CLOCK
+VCO
134-296090-226-0

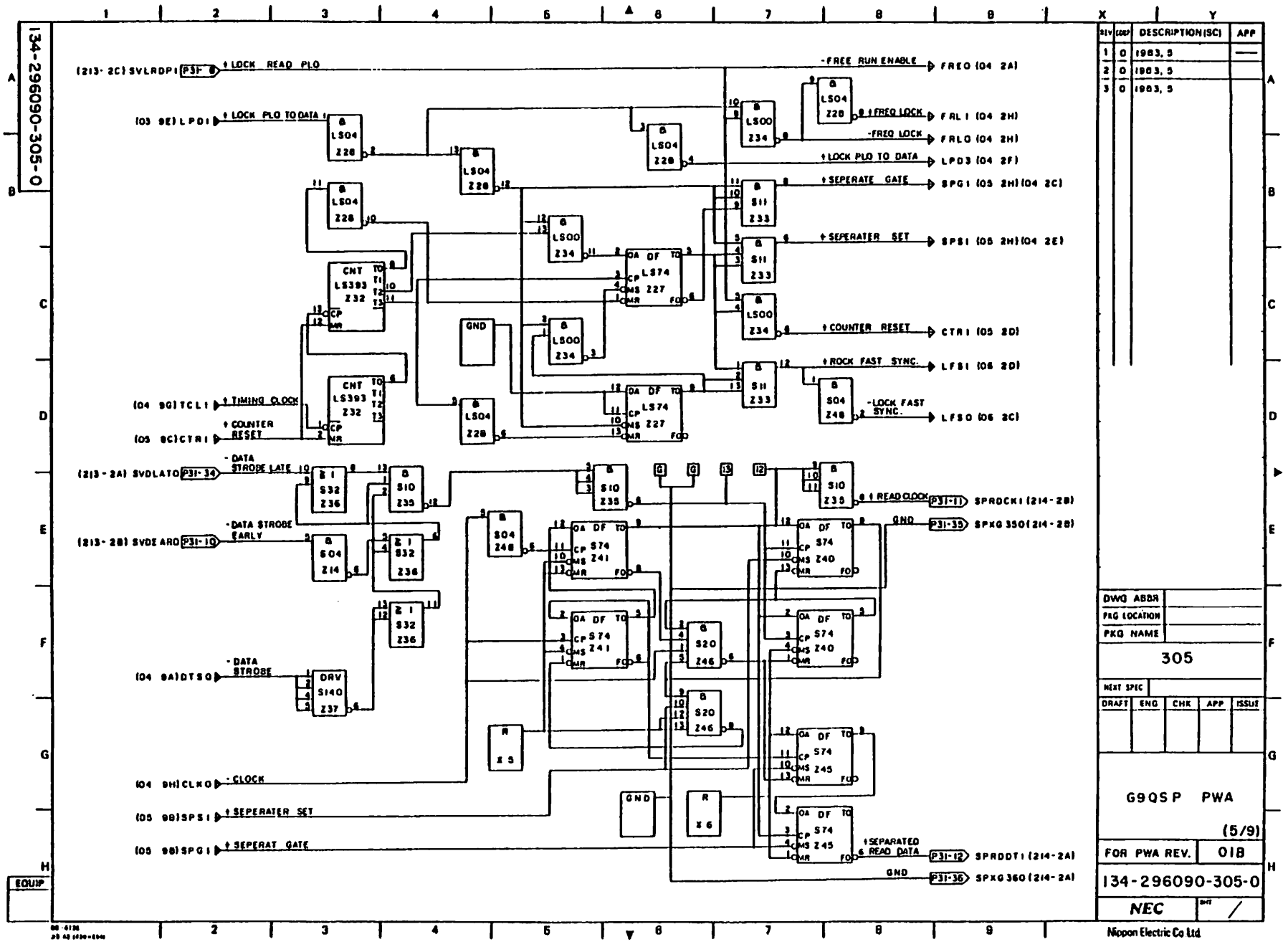

134-296090-227-0
+12V
-12V
+5V
-5V
C110 0.1μ
C111 10μ
C112 0.1μ
C113 10μ
C114 0.1μ
C115 10μ
C103 10μ
C104
C105
C106
C107
C108
C116 0.1μ
C117 10μ
P55-12 SVXP12S (401-2F)
P55-4 SVXG044 (401-2F)
P55-11 SVXN12S (401-2G)
P55-3 SVXG034 (401-2G)
P55-10 SVXP55I (401-2G)
P55-2 SVXG024 (401-2G)
(16 8C) SMTO - START MOTOR CP2-4 P55-6 SVSTMTO (401-2H)
(16 8B) ZEMI + ZERO MODE CP2-9 P55-14 SVZRMDI (403-2C)
(403-9G) SRCRTSA P55-16 NC
(401-8A) SRSPOWI P55-13 + SPEED PULSE CP2-3 SPWI (16 2C)
(401-8A) SRSPOPO P55-5 - SPEED PULSE CP2-10 SPWO (16 2C)
REV
CHNG
DESCRIPTION(ISC)
APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
227
MFRT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSV PWA
(27/27)
FOR PWA REV. 01B
134-296090-227-0
NEC
Nippon Electric Co Ltd
EQUIP

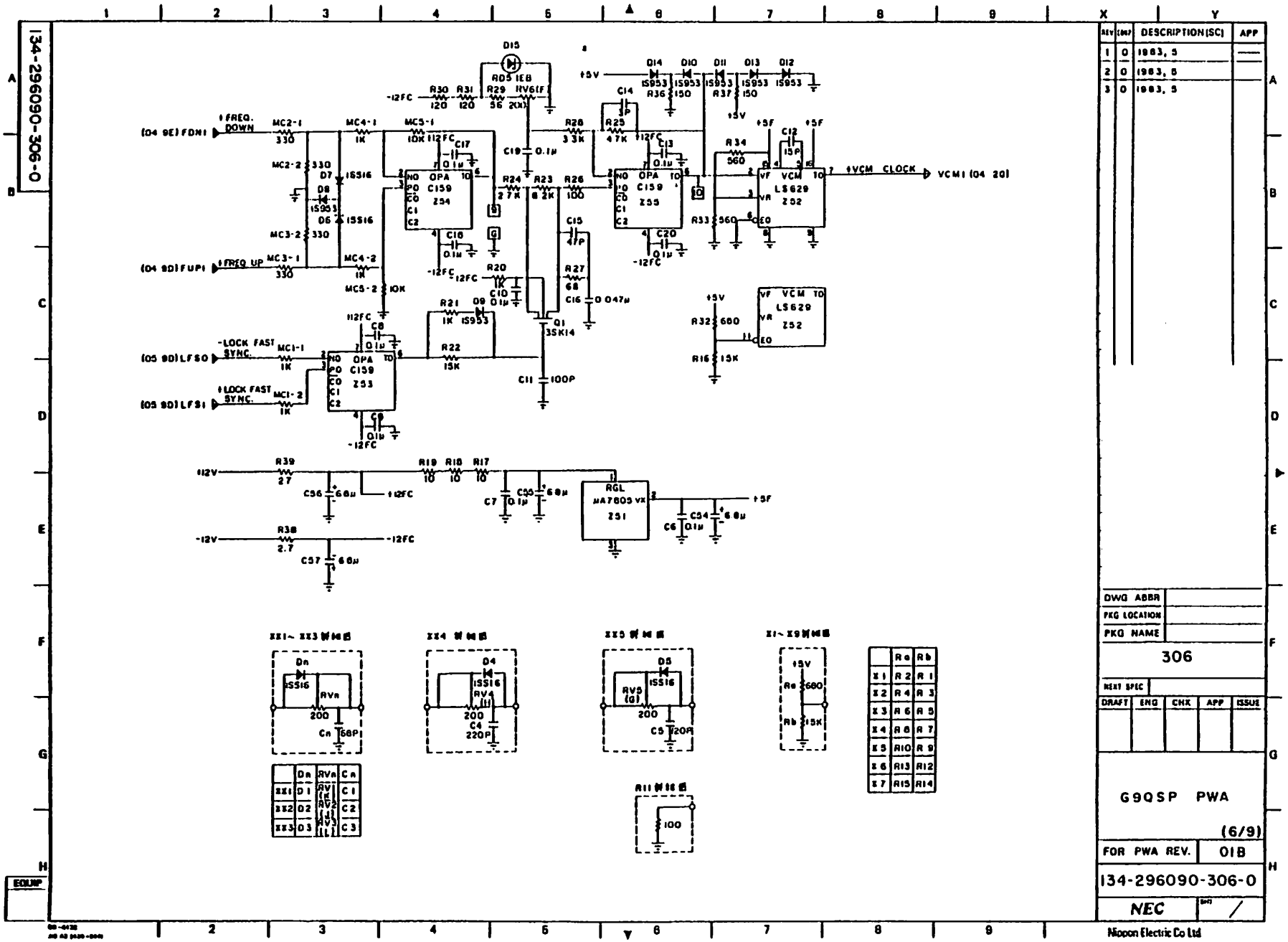

134-296090-301-0
(213-8F) SVWCK20 P31-6 -WRITE CLOCK 2F
(213-8F) SVXG210 P31-30 GND
(213-8E) SVWTG10 P31-39 -WRITE GATE
(213-8D) SVWTDT1 P31-5 +WRITE DATA
(213-8D) SVXG220 P31-29 GND
(213-8D) SVWTCK1 P31-4 +WRITE CLOCK
(213-8D) SVXG230 P31-28 GND
(213-8E) SVPDPR1 P31-26 +PAD IN PROGRESS OR NOT WRITE ALLOW
(213-8B) SVAMEN1 P31-3 +AM ENABLE
(218-8C) SVXG500 P31-1 GND
(213-8C) SVXG490 P31-2 NC
+WRITE CLOCK 1F
C1F1 (02 2F)
+WRITE CLOCK 2F
C2F1 (02 2F)
+WRITE GATE
WRT1 (02 2H)(08 2C)
+SYNCHRONIZED NRZ WRITE DATA
NRZ1 (02 2F)
+AM ENABLE
AME1 (02 2H)(03 2B)
J1
J2
J3
GND
EQUIP
REV
CORP
DESCRIPTION(SC)
APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
301
NEXT SPEC 134-832950-0
DRAFT ENG CHK APP ISSUE
G9QSP PWA
(1/9)
FOR PWA REV. 01B
134-296090-301-0
NEC
Nippon Electric Co Ltd

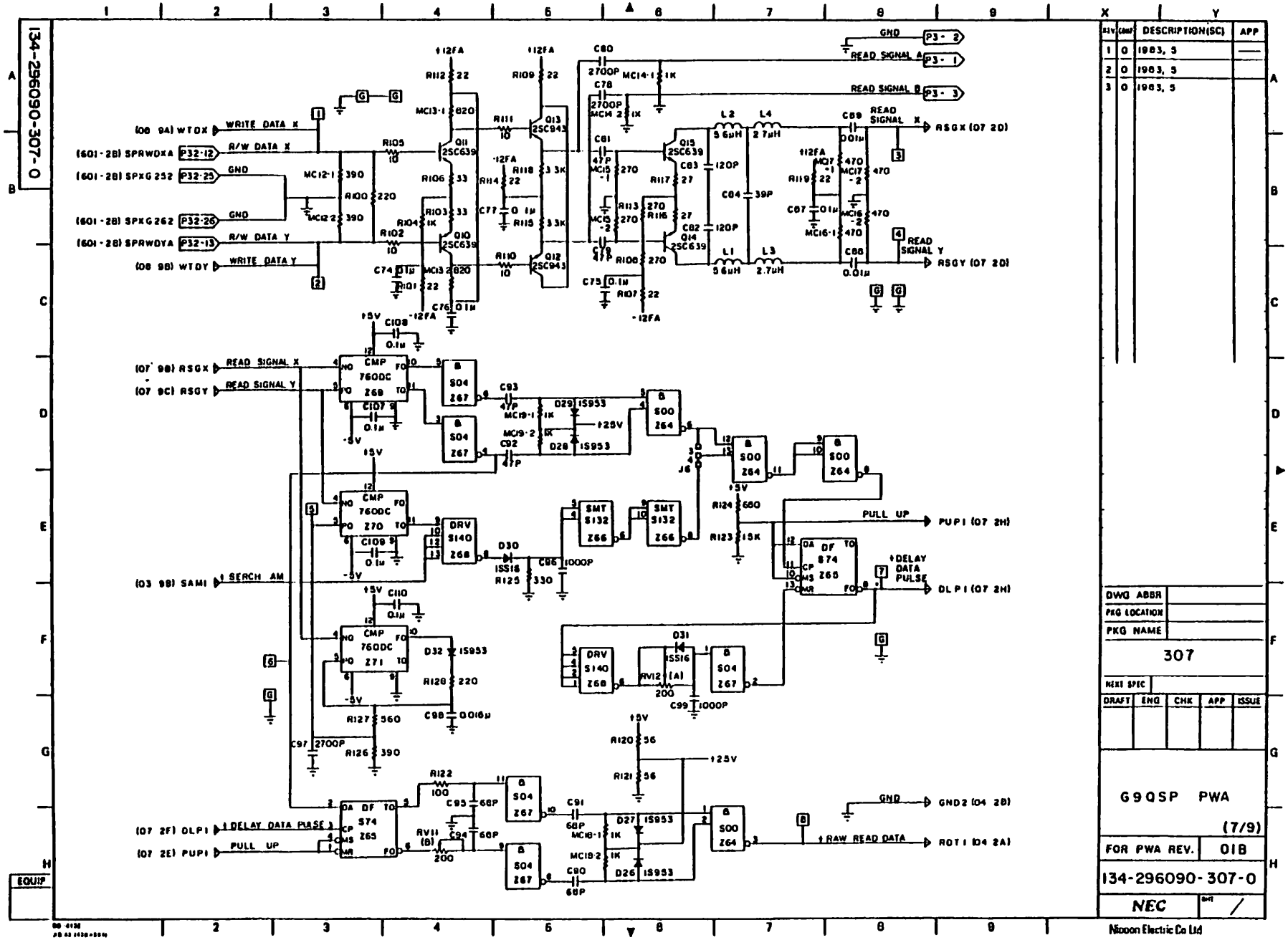

134-296090-302-0
GND
AOR S64 Z9
AOR S64 Z4
AOR S64 Z5
AOR S64 Z10
AOR S64 Z21
-EARLY DATA
ERYO (02 2G)
-NORMAL DATA
NMLO (02 2G)
-DELAY I DATA
DL1O (02 2G)
-DELAY II DATA
DL2O (02 2G)
GNDO (08 2B)
-MFM WRITE DATA
MFMO (08 2B)
WRITE CLOCK 1F
SYNCHRONIZED NRZ WRITE DATA
WRITE CLOCK 2F
-DELAY II DATA
-EARLY DATA
-DELAY I DATA
-NORMAL DATA
WRITE GATE
AM ENABLE
DF S175 Z20
DF S175 Z19
DF S175 Z6
S11 Z15
S11 Z16
S04 Z12
S11 Z15
S04 Z14
S11 Z16
S04 Z11
S04 Z12
S04 Z12
XX3
SMT S132 Z22
S04 Z12
S04 Z12
S04 Z11
S04 Z11
S04 Z11
XX1
SMT S132 Z22
S04 Z11
XX2
SMT S132 Z22
S04 Z14
R Z3
T3
GND
GND
- MFM WRITE DATA
REV
CONF
DESCRIPTION(SC)
APP
1 0 1983, 5
2 0 1983, 5
3 0 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
302
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSP PWA
(2/9)
FOR PWA REV.
01B
134-296090-302-0
NEC
Nippon Electric Co.Ltd


134-296090-303-0
(01-9G) AME1
↑AM ENABLE
(04-9D) BICO
- BIT CLOCK
(04-9A) RD1O
- RAW READ DATA
↑SERCH AM
SAM1 (07 2E)
↑AM FOUND
P31-27
SPAMFD (208-2E)
GND
↑LOCK PLO TO DATA
LPD1 (05 2A)
J4
(213-8B) SVRDGTO
P31-33
↑READ GATE
CNT LS393 Z30
CNT LS193 Z29
OF LS74 Z18
OF LS74 Z17
OF LS74 Z16
OF LS175 Z25
OF LS175 Z26
LS00 Z24
LS00 Z31
LS08 Z23
REV
CHG
DESCRIPTION(SC)
APP
1 0 1983.5
2 0 1983.5
3 0 1983.5
DWG ABBR
PKG LOCATION
PKG NAME
303
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSP PWA
(3/9)
FOR PWA REV.
01B
134-296090-303-0
NEC
Nippon Electric Co Ltd
EQUIP


134-296090-304-0
(04 9H) VCMO
- VCM CLOCK
(05 9A) FREO
- FREE RUN ENABLE
↑ RAW READ DATA
(07 9H) RDT1
(07 9G) GND2
GND
(04 9B) RDT3
↑ RAW DATA
(05 9B) SPG1
↑ SEPERATE GATE
(218-8C) SVXG420
(218-8C) SVXG190
P31-9
P31-32
(05 9B) SPS1
↑ SEPERATER SET
(05 9B) LPD3
↑ LOCK PLO TO DATA
(213-8G) SVXG200
P31-31
(213-8G) SVBTCK1
P31-7
↑ BIT CLOCK
(06 9B) VCM1
↑ VCM CLOCK
(04 9B) VCM3
- VCM CLOCK DELAY
(03 9B) FRLO
-FREQ. LOCK
(05 9A) FRL1
↑ FREQ. LOCK
EQUIP
- RAW READ DATA
RDTO (03 2B)
- DATA STROBE
DTSO (05 2F)
VCM CLOCK DELAY
VCM3 (04 2H)
↑ RAW DATA
RDT3 (04 2B)
↑ FREQ. UP
FUP1 (06 2C)
↑ FREQ. DOWN
FDN1 (06 2A)
- BIT CLOCK
BICO (03 2D)
↑ TIMING CLOCK
TCL1 (05 2D)
- VCM CLOCK
VCMO (04 2A)
- CLOCK
CLKO (05 2D)
REV
CONF
DESCRIPTION(SC)
APP
1 0 1983.5
2 0 1983.5
3 0 1983.5
DWG ABBR
PKG LOCATION
PKG NAME
304
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G90SP PWA
(4/9)
FOR PWA REV. 018
134-296090-304-0
NEC
Nippon Electric Co Ltd


134-296090-305-0
(213-2C) SVLRDPI P31-8 ↑LOCK READ PLO
(03 9E) LPDI ↑LOCK PLO TO DATA
-FREE RUN ENABLE FREO (04 2A)
↑FREQ LOCK FRLI (04 2H)
-FREQ LOCK FRLO (04 2H)
↑LOCK PLO TO DATA LPD3 (04 2F)
↑SEPERATE GATE SPGI (05 2H) (04 2C)
↑SEPERATER SET SPSI (05 2H) (04 2E)
↑COUNTER RESET CTRI (05 2D)
↑ROCK FAST SYNC. LFSI (06 2D)
-LOCK FAST SYNC. LFSO (06 2C)
(04 9G) TCLI ↑TIMING CLOCK
(03 9C) CTRI ↑COUNTER RESET
(213-2A) SVDLATO P31-34 -DATA STROBE LATE
(213-2B) SVDEARO P31-10 -DATA STROBE EARLY
(04 9A) DTSO -DATA STROBE
↑READ CLOCK P31-11 SPRDCKI (214-2B)
GND P31-35 SPXG350 (214-2B)
↑SEPARATED READ DATA P31-12 SPRDDTI (214-2A)
GND P31-36 SPXG360 (214-2A)
(04 9H) CLKO -CLOCK
(05 9B) SPSI ↑SEPERATER SET
(05 9B) SPGI ↑SEPERAT GATE
GND
CNT LS393 Z32
LS74 Z27
LS74 Z41
LS74 Z40
LS74 Z45
LS04 Z28
LS00 Z34
S11 Z33
S04 Z48
S04 Z14
S10 Z35
S32 Z36
S20 Z46
S140 Z37
R X5
R X6
EQUIP
REV | COMP | DESCRIPTION(SC) | APP
1 | 0 | 1983, 9
2 | 0 | 1983, 9
3 | 0 | 1983, 9
DWG ABBR
PKG LOCATION
PKG NAME
305
NEXT SPEC
DRAFT | ENG | CHK | APP | ISSUE
G9QSP PWA
(5/9)
FOR PWA REV. 018
134-296090-305-0
NEC
Nippon Electric Co Ltd


134-296090-306-0
REV | CNG | DESCRIPTION(SC) | APP
1 | 0 | 1983. 5
2 | 0 | 1983. 6
3 | 0 | 1983. 9
DWG ABBR
PKG LOCATION
PKG NAME
306
NEXT SPEC
DRAFT | ENG | CHK | APP | ISSUE
G9QSP PWA
(6/9)
FOR PWA REV. 01B
134-296090-306-0
NEC
Nippon Electric Co Ltd
EQUIP
+FREQ. DOWN
+FREQ UP
-LOCK FAST SYNC.
+LOCK FAST SYNC.
+VCM CLOCK
VCM1 (04 20)
(04 9E) FDN1
(04 9D) FUP1
(05 9D) LFS0
(05 9D) LFS1
-12FC
+12FC
+5V
+5F
+12V
-12V
A-50



REV	CHNG	DESCRIPTION(SC)	APP
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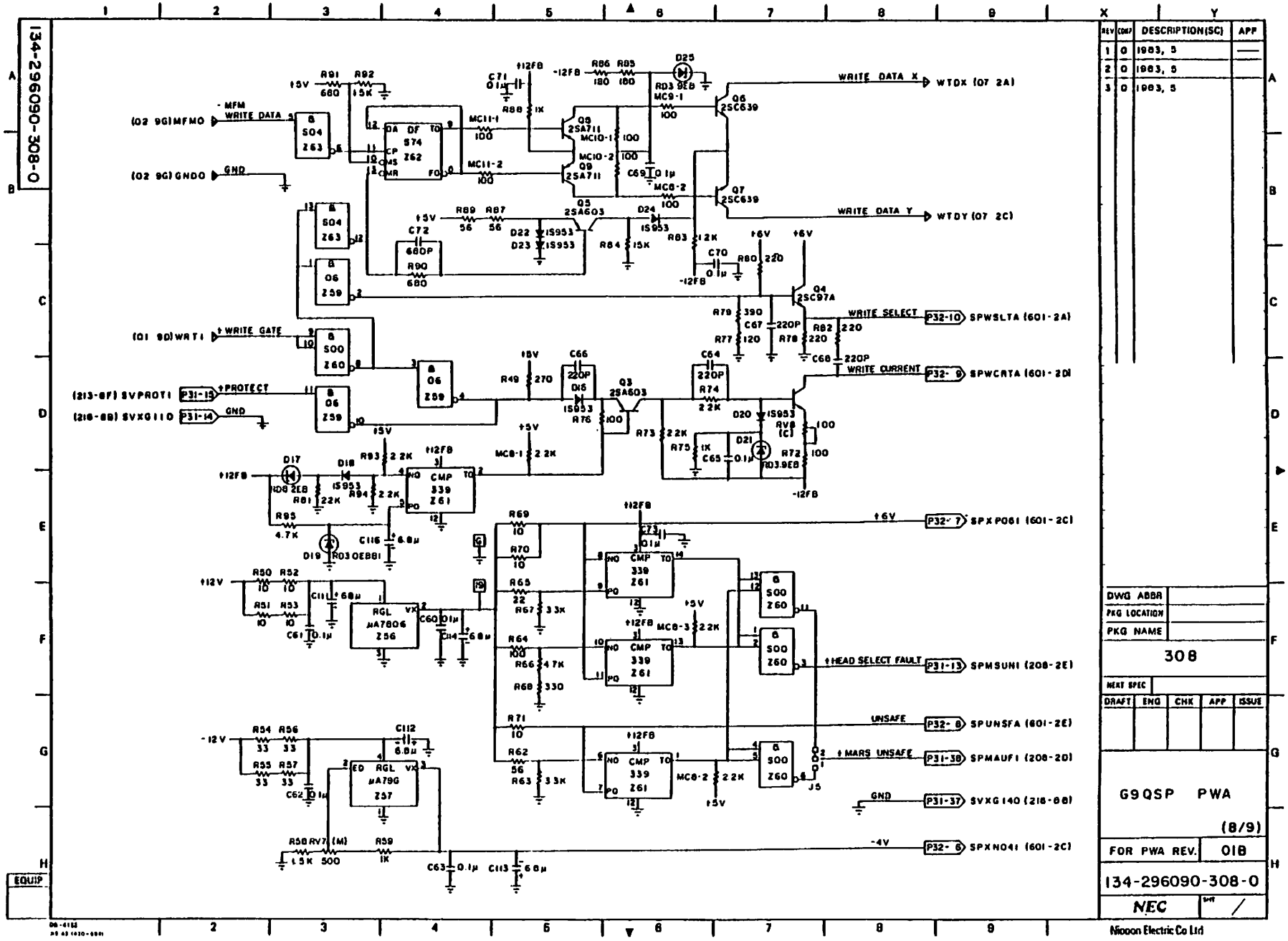
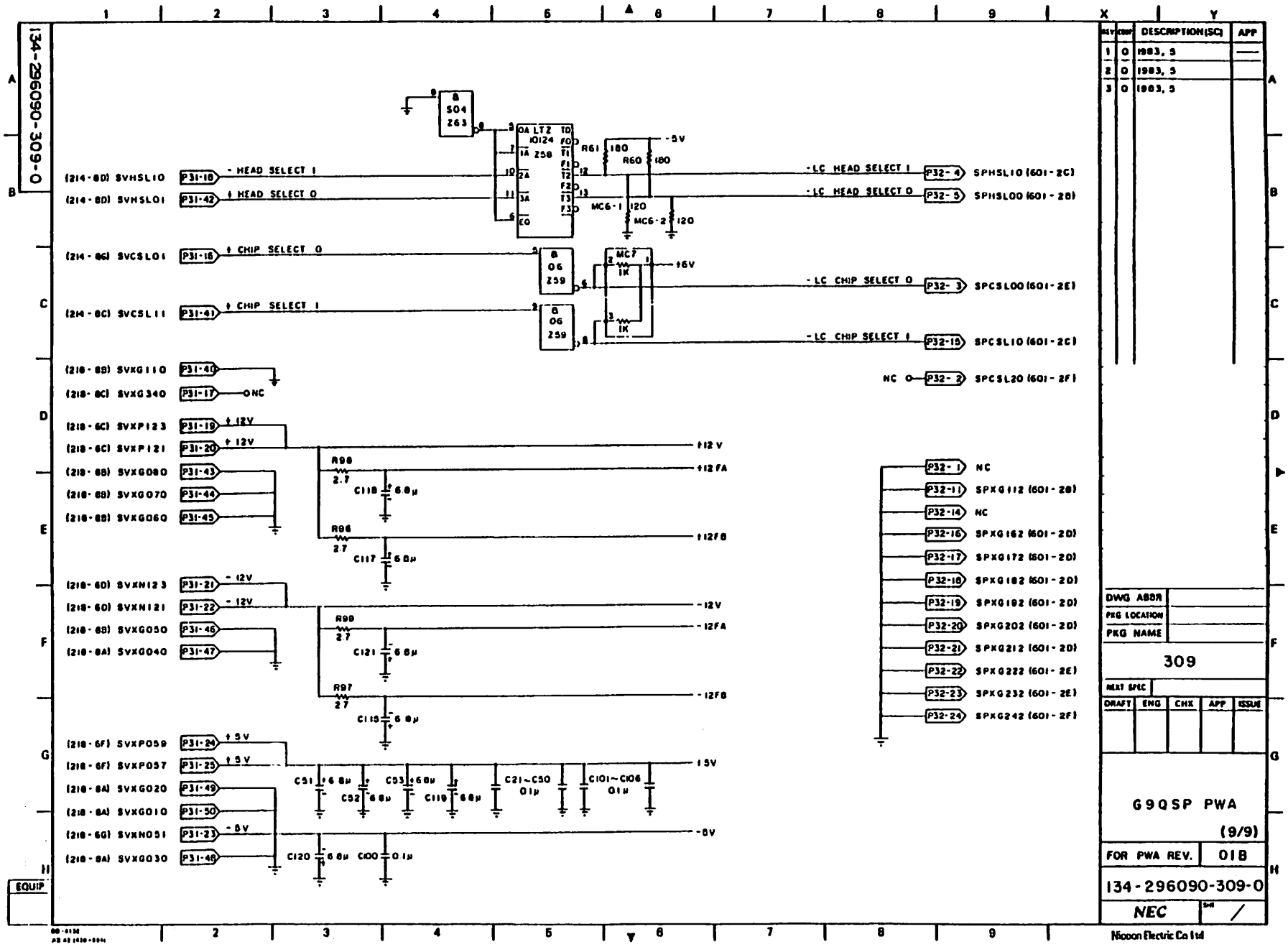
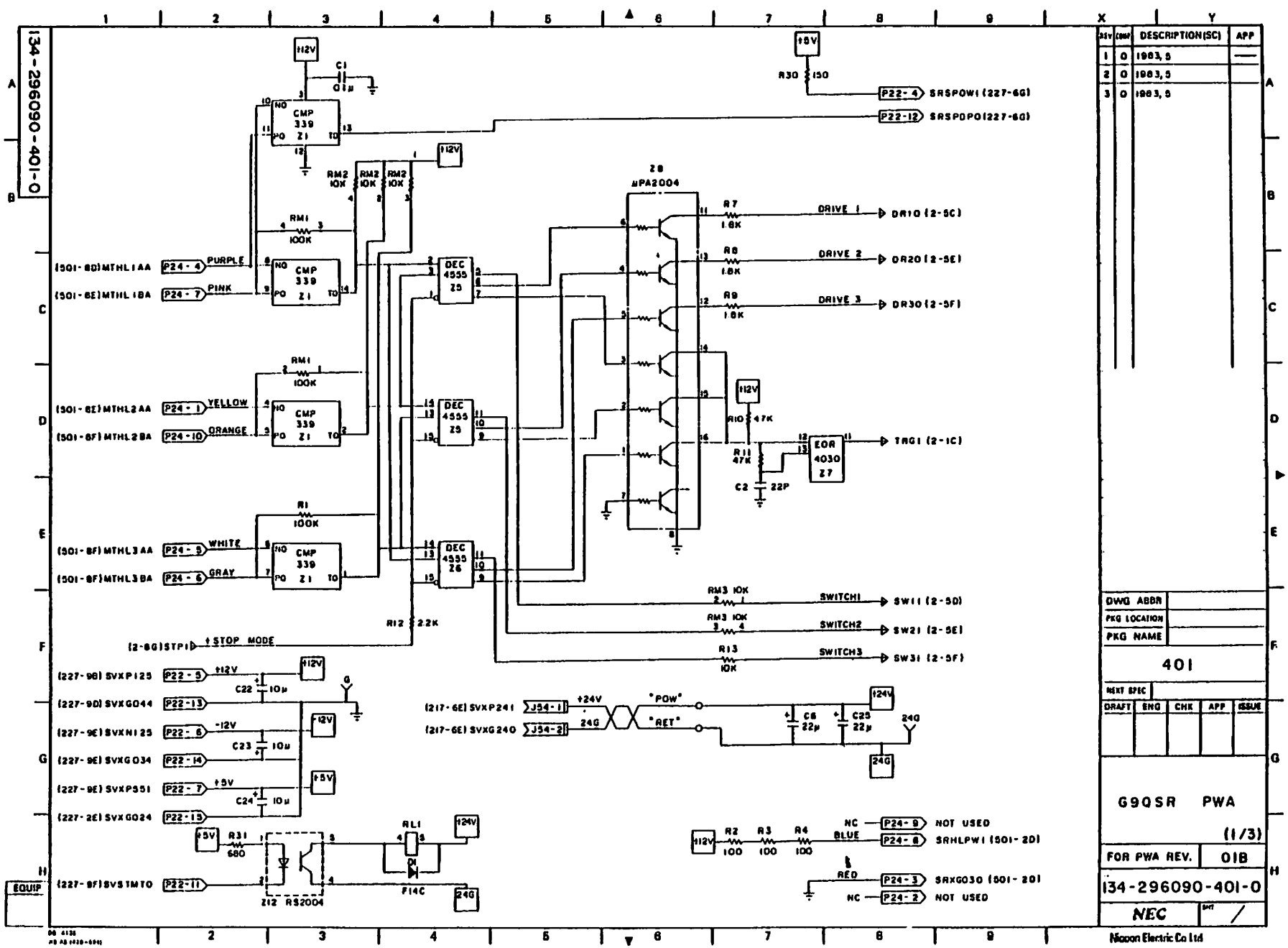
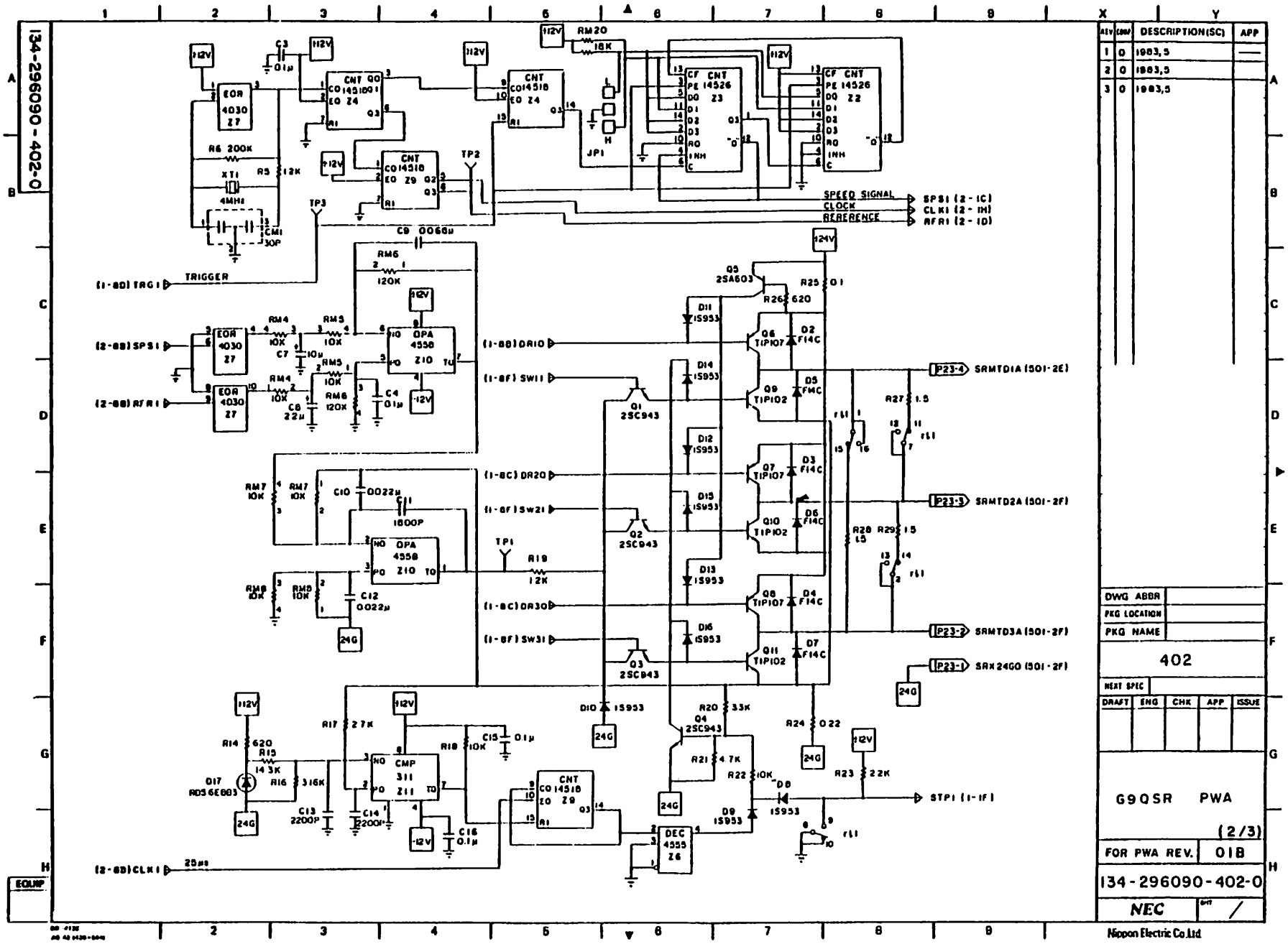
2	0	1983. 5	
3	0	1983. 5	

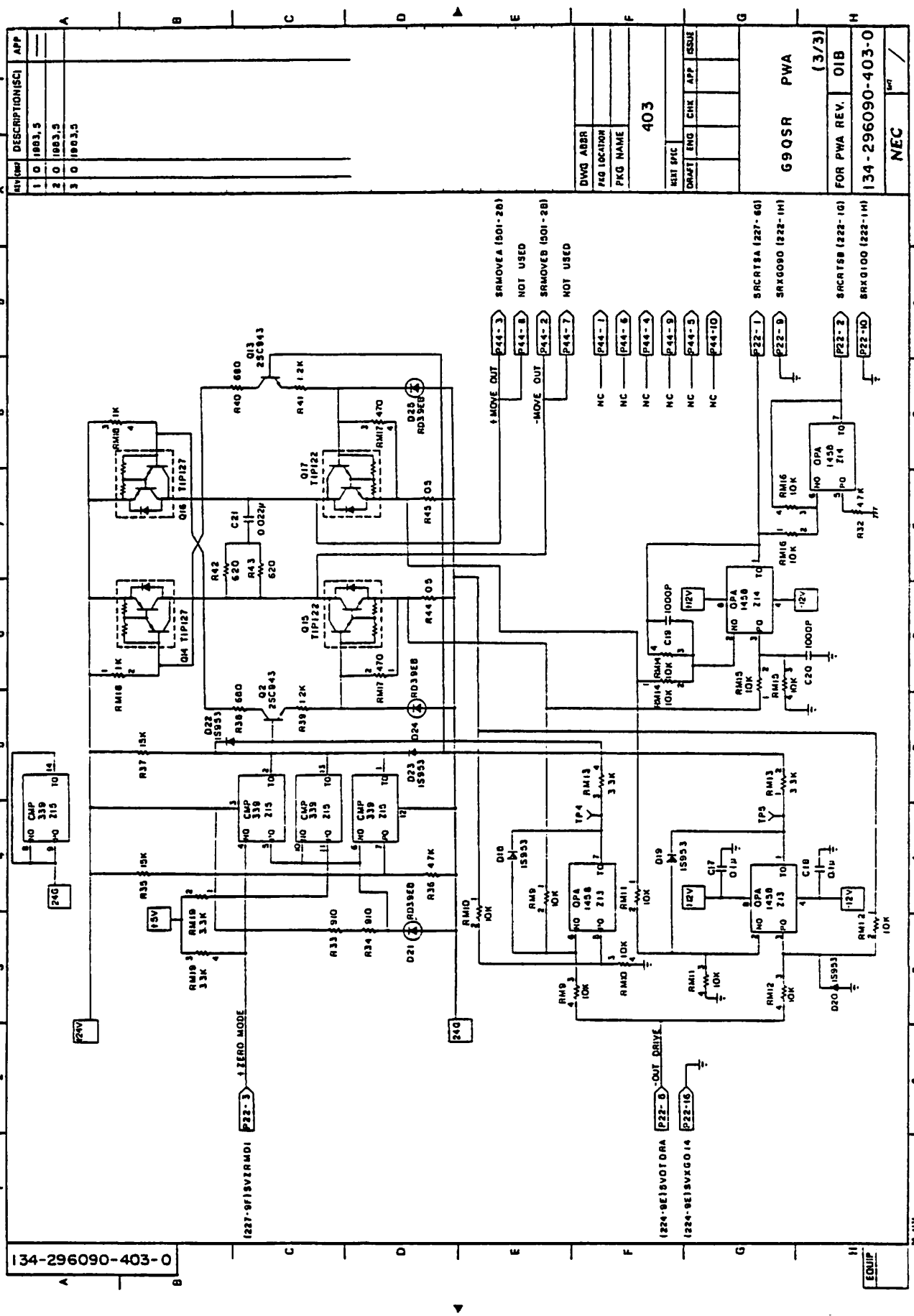


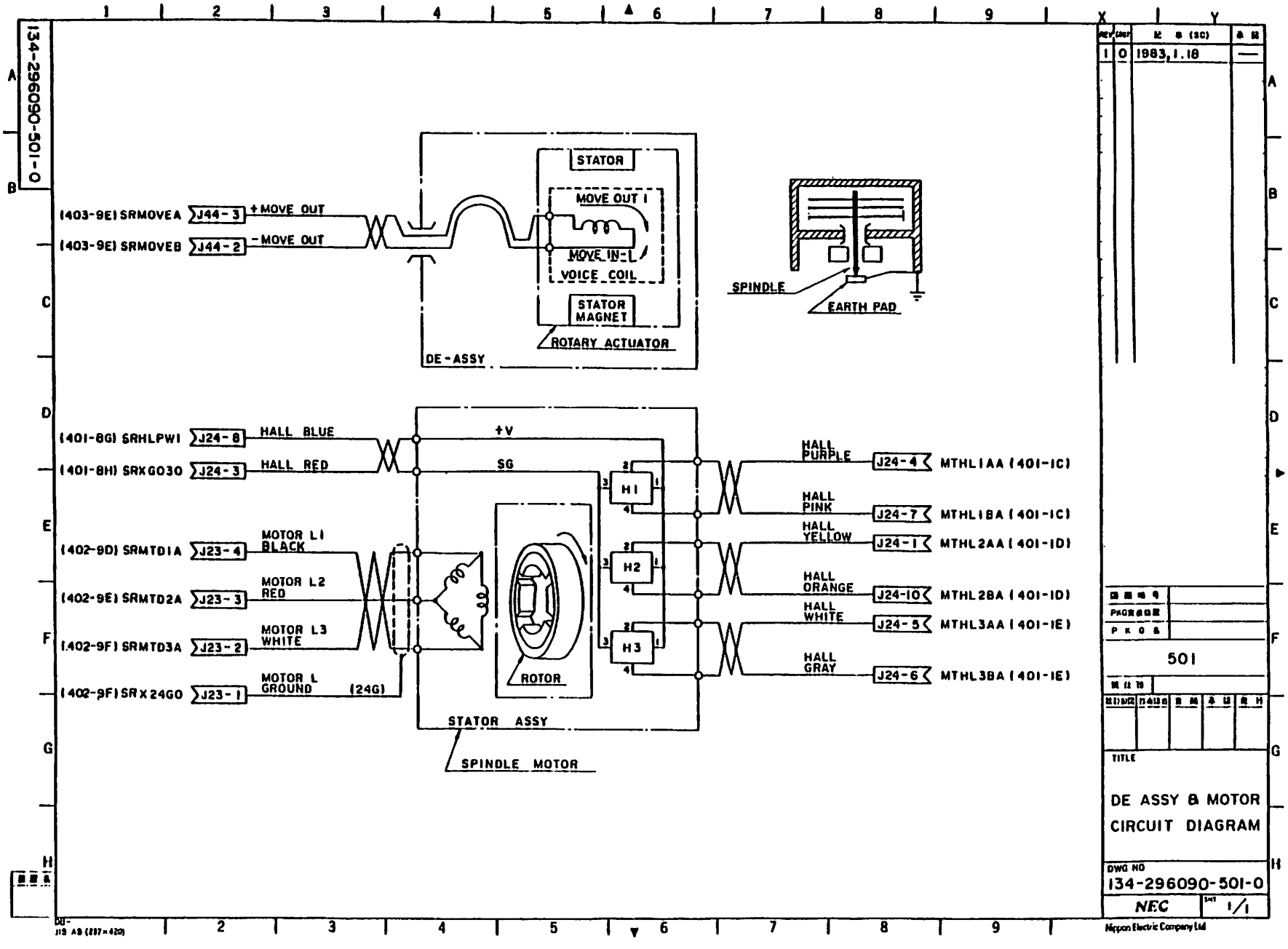
REV	COMP	DESCRIPTION(SC)	APP
1	0	1983, 5	
2	0	1983, 5	
3	0	1983, 5	

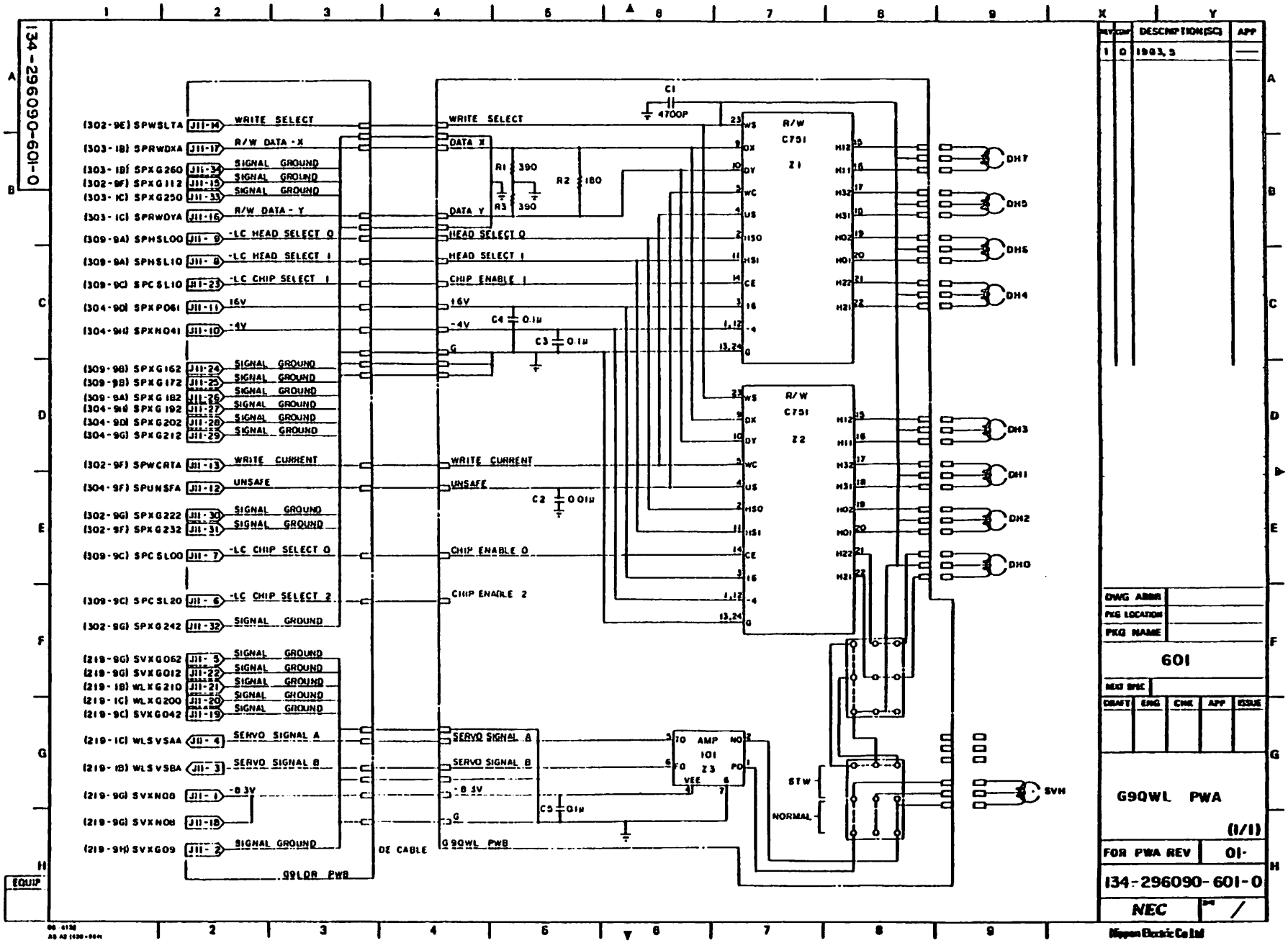

134-296090-309-0
(214-8D) SVHSL10
(214-8D) SVHSL01
(214-8C) SVCSL01
(214-8C) SVCSL11
(218-8B) SVXG110
(218-8C) SVXG340
(218-6C) SVXP123
(218-6C) SVXP121
(218-8B) SVXG080
(218-8B) SVXG070
(218-8B) SVXG060
(218-6D) SVXN123
(218-6D) SVXN121
(218-8B) SVXG050
(218-8A) SVXG040
(218-6F) SVXP059
(218-6F) SVXP057
(218-8A) SVXG020
(218-8A) SVXG010
(218-6G) SVXN051
(218-8A) SVXG030
P31-18
P31-42
P31-16
P31-41
P31-40
P31-17
P31-19
P31-20
P31-43
P31-44
P31-45
P31-21
P31-22
P31-46
P31-47
P31-24
P31-25
P31-49
P31-50
P31-23
P31-48
- HEAD SELECT 1
+ HEAD SELECT 0
+ CHIP SELECT 0
+ CHIP SELECT 1
NC
+ 12V
+ 12V
- 12V
- 12V
+ 5V
+ 5V
- 5V
8 S04 Z63
8 06 Z59
8 06 Z59
OA LT2 IO124 Z58
R61 180
R60 180
MC6-1 120
MC6-2 120
MC7 1K
1K
-5V
+5V
R98 2.7
R96 2.7
R99 2.7
R97 2.7
C118 6.8μ
C117 6.8μ
C121 6.8μ
C115 6.8μ
+12V
+12FA
+12FB
-12V
-12FA
-12FB
C51 6.8μ
C52 6.8μ
C53 6.8μ
C119 6.8μ
C21~C50 0.1μ
C101~C106 0.1μ
+5V
C120 6.8μ
C100 0.1μ
-5V
-LC HEAD SELECT 1
-LC HEAD SELECT 0
-LC CHIP SELECT 0
-LC CHIP SELECT 1
NC
P32-4 SPHSL10 (601-2C)
P32-5 SPHSL00 (601-2B)
P32-3 SPCSL00 (601-2E)
P32-15 SPCSL10 (601-2C)
P32-2 SPCSL20 (601-2F)
P32-1 NC
P32-11 SPXG112 (601-2B)
P32-14 NC
P32-16 SPXG162 (601-2D)
P32-17 SPXG172 (601-2D)
P32-18 SPXG182 (601-2D)
P32-19 SPXG192 (601-2D)
P32-20 SPXG202 (601-2D)
P32-21 SPXG212 (601-2D)
P32-22 SPXG222 (601-2E)
P32-23 SPXG232 (601-2E)
P32-24 SPXG242 (601-2F)
EQUIP
REV
CHNG
DESCRIPTION(SC)
APP
1 0 1983. 3
2 0 1983. 3
3 0 1983. 3
DWG ABBR
PKG LOCATION
PKG NAME
309
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSP PWA
(9/9)
FOR PWA REV. 01B
134-296090-309-0
NEC
Nippon Electric Co ltd


134-296090-401-0
+12V
C1
0.1μ
CMP 339 Z1
+5V
R30 150
P22-4 SRSPOW1 (227-6G)
P22-12 SRSPOP0 (227-6G)
RM2 10K
RM1 100K
Z8 μPA2004
R7 1.8K
R8 1.8K
R9 1.8K
DRIVE 1
DRIVE 2
DRIVE 3
DR10 (2-5C)
DR20 (2-5E)
DR30 (2-5F)
(501-8D)MTHL1AA
(501-8E)MTHL1BA
P24-4 PURPLE
P24-7 PINK
DEC 4555 Z5
(501-8E)MTHL2AA
(501-8F)MTHL2BA
P24-1 YELLOW
P24-10 ORANGE
R10 47K
R11 47K
C2 22P
EOR 4030 Z7
TRG1 (2-1C)
R1 100K
(501-8F)MTHL3AA
(501-8F)MTHL3BA
P24-9 WHITE
P24-6 GRAY
DEC 4555 Z6
RM3 10K
SWITCH1
SWITCH2
SWITCH3
SW1 (2-5D)
SW2 (2-5E)
SW3 (2-5F)
R12 2.2K
(2-8G)STP1 ↑STOP MODE
(227-9B)SVXP125 P22-5 +12V
(227-9D)SVXG044 P22-13
(227-9E)SVXN125 P22-6 -12V
(227-9E)SVXG034 P22-14
(227-9E)SVXP351 P22-7 +5V
(227-2E)SVXG024 P22-15
C22 10μ
C23 10μ
C24 10μ
(227-8F)SVS1MTO P22-11
+5V R31 680
Z12 RS2004
RL1
F14C
(217-6E)SVXP241 J54-1 +24V
(217-6E)SVXG240 J54-2 24G
"POW"
"RET"
C6 22μ
C25 22μ
+12V R2 100 R3 100 R4 100
NC P24-9 NOT USED
BLUE P24-8 SRHLPW1 (501-2D)
RED P24-3 SRXG030 (501-2D)
NC P24-2 NOT USED
DIV | COMP | DESCRIPTION(SC) | APP
1 | 0 | 1983, 5
2 | 0 | 1983, 5
3 | 0 | 1983, 5
DWG ABBR
PKG LOCATION
PKG NAME
401
NEXT SPEC
DRAFT | ENG | CHK | APP | ISSUE
G90SR PWA
(1/3)
FOR PWA REV. 018
134-296090-401-0
NEC
Nippon Electric Co Ltd
EQUIP


134-296090-402-0
SPEED SIGNAL
CLOCK
REFERENCE
SPSI (2-1C)
CLKI (2-1H)
RFRI (2-1D)
TRIGGER
(1-8D) TAG I
(2-8B) SPS I
(2-8B) RF R I
(2-8B) CLK I
(1-8B) DRI0
(1-8C) DR20
(1-8C) DR30
(1-8F) SWI I
(1-8F) SW21
(1-8F) SW31
P23-4 SRMTD1A (501-2E)
P23-3 SRMTD2A (501-2F)
P23-2 SRMTD3A (501-2F)
P23-1 SRX 24GO (501-2F)
STPI (1-1F)
DWG ABBR
PKG LOCATION
PKG NAME
402
NEXT SPEC
DRAFT
ENG
CHK
APP
ISSUE
G9QSR PWA
(2/3)
FOR PWA REV. 01B
134-296090-402-0
NEC
Nippon Electric Co.Ltd
EQUIP

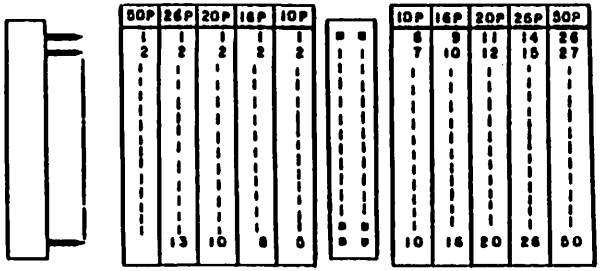

134-296090-403-0
G9QSR PWA (3/3)
134-296090-403-0
NEC
Nippon Electric Co ltd
403
+MOVE OUT
-MOVE OUT
SRMOVEA (501-28)
SRMOVEB (501-28)
NOT USED
SRCRTSA (227-6G)
SRCRTSB (222-1G)
SRXG090 (222-1H)
SRXG100 (222-1H)
+ZERO MODE
-OUT DRIVE
24V
24G
15V
-12V
+12V


134-296090-501-0
(403-9E) SRMOVEA
J44-3
+MOVE OUT
(403-9E) SRMOVEB
J44-2
-MOVE OUT
STATOR
MOVE OUT I
MOVE IN-L
VOICE COIL
STATOR MAGNET
ROTARY ACTUATOR
DE-ASSY
SPINDLE
EARTH PAD
(401-8G) SRHLPWI
J24-8
HALL BLUE
(401-8H) SRXG030
J24-3
HALL RED
+V
SG
H1
H2
H3
(402-9D) SRMTD1A
J23-4
MOTOR L1 BLACK
(402-9E) SRMTD2A
J23-3
MOTOR L2 RED
(402-9F) SRMTD3A
J23-2
MOTOR L3 WHITE
(402-9F) SRX24GO
J23-1
MOTOR L GROUND
(24G)
ROTOR
STATOR ASSY
SPINDLE MOTOR
HALL PURPLE
J24-4
MTHL1AA (401-1C)
HALL PINK
J24-7
MTHL1BA (401-1C)
HALL YELLOW
J24-1
MTHL2AA (401-1D)
HALL ORANGE
J24-10
MTHL2BA (401-1D)
HALL WHITE
J24-5
MTHL3AA (401-1E)
HALL GRAY
J24-6
MTHL3BA (401-1E)
1 0 1983.1.18
501
TITLE
DE ASSY & MOTOR CIRCUIT DIAGRAM
DWG NO
134-296090-501-0
NEC
1/1
Nippon Electric Company Ltd

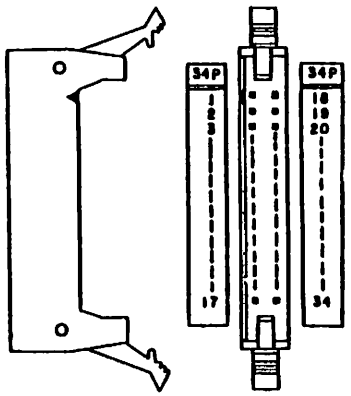

134-296090-601-0
WRITE SELECT
R/W DATA - X
SIGNAL GROUND
R/W DATA - Y
-LC HEAD SELECT 0
-LC HEAD SELECT 1
-LC CHIP SELECT 1
16V
-4V
WRITE CURRENT
UNSAFE
-LC CHIP SELECT 0
-LC CHIP SELECT 2
SERVO SIGNAL A
SERVO SIGNAL B
-8.3V
DATA X
DATA Y
HEAD SELECT 0
HEAD SELECT 1
CHIP ENABLE 1
CHIP ENABLE 0
CHIP ENABLE 2
C1 4700P
C2 0.01μ
C3 0.1μ
C4 0.1μ
C5 0.1μ
R1 390
R2 180
R3 390
R/W C751 Z1
R/W C751 Z2
TO AMP 101 Z3
DH7
DH6
DH5
DH4
DH3
DH2
DH1
DH0
SVH
STW
NORMAL
OE CABLE
G90WL PWB
G90LOR PWB
EQUIP
G90WL PWA
(1/1)
FOR PWA REV 01-
134-296090-601-0
NEC
Nippon Electric Co Ltd

134-296090-021-0

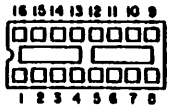
CONNECTORS PIN LAYOUT



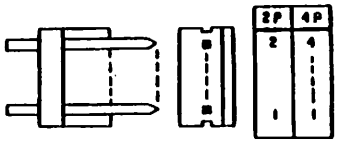
PWA	10P	16P	20P	26P	50P
G9TXW				P60	
G9QSV	P56	P55	P59 P58 P57	P50	P53
G9QSP				P32	P31
G9QSR	P24 P44	P22			



DE ASSY (P11)



PWA	16P
G9QSV	J15C J15D
G9TXW	J15A J15B



PWA	2P	4P
G9QSV	P54	
G9QSR		P23

ALV	CONF	DESCRIPTION(SC)	APP
1	0	1983.6.1	

DWG ABBR	
PKG LOCATION	
PKG NAME	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE

I/O CONNECTORS

134-296090-021-0

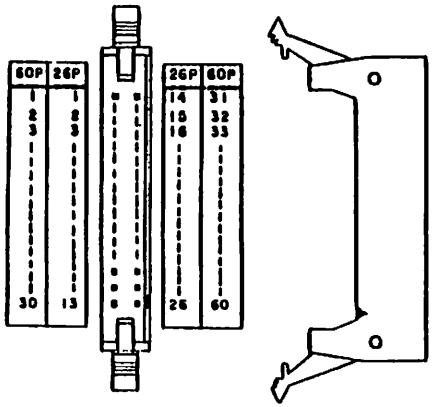
NEC SHT 1/1

Nippon Electric Co.,Ltd

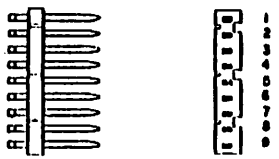
EQUIP

134-296090-022-0

INTERFACE CONNECTORS



POWER CONNECTOR



3-DC INPUTS OPTION

REV	CHNG	DESCRIPTION(SC)	APP
1	0	1983.9.	—

DWG ABBR	
PKG LOCATION	
PKG NAME	
NEXT SPEC	

DRAFT	ENG	CHK	APP	ISSUE

INTERFACE CONNECTOR
&
POWER CONNECTOR

134-296090-022-0

NEC SHT 1/1

Nippon Electric Co.Ltd

EQUIP

Appendix B

Specifications

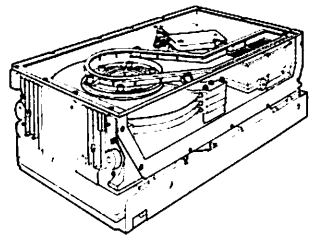


Table B-1 Operating Specifications

FEATURE	SPECIFICATION
General	
Start Time	Less than 35 seconds
Stop Time	Less than 25 seconds
Recording Mode	MFM
Interface Mode	NRZ
Head Positioning	Closed servo rotary actuator
Track Following	Modified-dipulse pattern
Basic Power Requirements	
Voltage and Current	+5 Vdc, 4.0 A -5 Vdc, 0.5 A +12 Vdc, 0.6 A -12 Vdc, 0.5 A +24 Vdc, 2.7 A (average) 5.0 A (peak)
Power Dissipation	100 W (average) 150 W (peak)
Heat Generation	86 BTU/hour

Table B-1 Operating Specifications (cont'd)

FEATURE	SPECIFICATION
Environmental	
Temperature (Ambient)	
Operating	41° to 104° F (5° to 40° C)
Nonoperating	14° to 140° F (-10° to 60° C)
Storage*	-40° to 158° F (-40° to 70° C)
Temperature (Gradient/maximum)	
Operating	18°F per hour (10°C per hour)
Nonoperating	27°F per hour (15°C per hour)
Storage	45°F per hour (25°C per hour)
Relative Humidity (No Condensation)	
Operating	20% to 80% relative humidity
Nonoperating	10% to 90% relative humidity
Storage	5% to 95% relative humidity
Vibration	
Operating	0.2G
Nonoperating	0.5G
Storage	1.5G
Shock	
Operating	2G (20 ms)
Nonoperating	5G (10 ms)
Storage	15G (30 ms)
Altitude (Maximum)	
Operating	10,000 feet (3,048 meters)
Nonoperating	40,000 feet (12,192 meters)
Storage	40,000 feet (12,192 meters)
*Storage-unopened, as shipped from factory	

Table B-2 Design Specifications

FEATURE	MODEL D2257	MODEL D2247E
Unformatted Storage Capacity		
Per Unit (MB)	167.7	103.2
Per Cylinder (bytes)	163,840	100,800
Per Track (bytes)	20,480	20,480
General		
Recording Disks	5	3
Data Heads	8	5
Servo Heads	1	1
Cylinders	1,024	1,024
Track Density (tracks/inch)	960	960
Bit Density (bits/inch)	9,420	8,670
Data Transfer Rate (MB/second)	1.19	1.20
Spindle Rotation (RPM)	3,510	3,600
Average Latency Time (ms)	8.55	8.33
One Cylinder Seek Time (ms)	5	5
Average Seek Time (ms)	20.0	20.0
Maximum Seek Time (ms)	40.0	40.0
Sectors per Track	Switch Selectable	
Reliability		
Mean Time-Between-Failures (MTBF)	12,000 hours	
Mean Time-to-Repair (MTTR)	less than one hour	
Service Life	approximately 5 years	

Table B-3 Physical Dimensions

DIMENSIONS	BASIC UNIT	STANDARD ASSEMBLY*
Width	8.54 in. (217 mm)	8.89 in. (226 mm)
Height	5.47 in. (139 mm)	5.62 in. (143 mm)
Depth	16.53 in. (420 mm)	18.50 in. (470 mm)
Weight	30.46 lbs. (13.8 kg)	32.45 lbs. (14.7 kg)

*The standard assembly includes a frame bracket.

Table B-4 Interface Cable Descriptions

SPECIFICATION	CABLE A	CABLE B
TYPE	Flat cable, 30 twisted pairs	Flat cable, 9 twisted pairs with ground plane and drain wire
IMPEDANCE	100 Ω ± 10 Ω	130 Ω ± 15 Ω
WIRE	28 AWG, 7 strands	28 AWG, 7 strands
PROPAGATION DELAY TIME	5.6 ns/meter (nominal)	5.5 ns/meter (nominal)
MAXIMUM CABLE LENGTH	98.4 ft. (30 m)	49.2 ft. (15 m)
VOLTAGE RATING	300 V (RMS)	300 V (RMS)
PART NUMBER	Spectra Strip SS-455-248-60	3 M 3476-26

Table B-5 Power Cable Descriptions

CABLE	DESIGNATION	NEC PART NUMBER	WIRE SIZE
DC Cable	0X7 DC Cable	134-233535-GRP-0	AWG 18
AC Cable	DKU000-HAC1	134-232903-GRP-0	AWG 18

Table B-6 Option Cable Descriptions

CABLE	DESIGNATION	NEC PART NUMBER	WIRE SIZE
3-DC Option Cable Operator Panel Cable	DKU000-H3P7	806-942333-200-0	 AWG 22-32

Table B-7 Interface Connector Descriptions

CABLE	CABLE CONNECTOR ASSEMBLY	G9QSV PCB CONNECTOR ASSEMBLY
A	60-pin connector 3 M, #3334-6000 (or equivalent)	60-pin vertical adapter TPD, #R60L NEC, #802-710100-560 (or equivalent)
B	26-pin connector 3 M, #3399-3000 (or equivalent)	26-pin vertical adapter TPD, #R26L (or equivalent)

Table B-8 DC Power Cable Connector Descriptions

CONNECTOR	NEC PART NUMBER	VENDOR/PART NUMBER
Disk Side Housing	806-927329-009-0	AMP Ltd./87159-9
Disk Side Contact	806-927329-571-0	AMP Ltd./87027-1
Power Supply Side Housing	802-710113-009-0	AMP Ltd./1-480706-0
Power Supply Side Contact	802-710114-002-0	AMP Ltd./350705-1

Table B-9 AC Power Cable Connector Descriptions

CONNECTOR	NEC PART NUMBER	VENDOR/PART NUMBER
Distributor Side Housing	802-710113-503-0	AMP Ltd./350766-1
Distributor Side Contact	802-710114-002-0	AMP Ltd./350705-1
Power Side Housing	802-710113-503-0	AMP Ltd./350766-1
Power Side Contact	802-710114-102-0	AMP Ltd./350550-1

Table B-10 3-DC Option Cable Connector Descriptions

CONNECTOR	NEC PART NUMBER	VENDOR/PART NUMBER
Disk Side Housing	806-927329-009-0	AMP Ltd./87159-9
Disk Side Contact	806-927329-571-0	AMP Ltd./87027-1
Power Supply Side Housing		AMP Ltd./1-480270-0
Power Supply Side Contact		AMP Ltd./60617-4

Table B-11 Operator Panel Cable Connector Descriptions

CONNECTOR	VENDOR	PART NUMBER
Disk Side Housing	Berg	65043-032
Disk Side Contact	Berg Berg	47744 (for AWG 28, 30, 32) 47745 (for AWG 22, 24, 26)

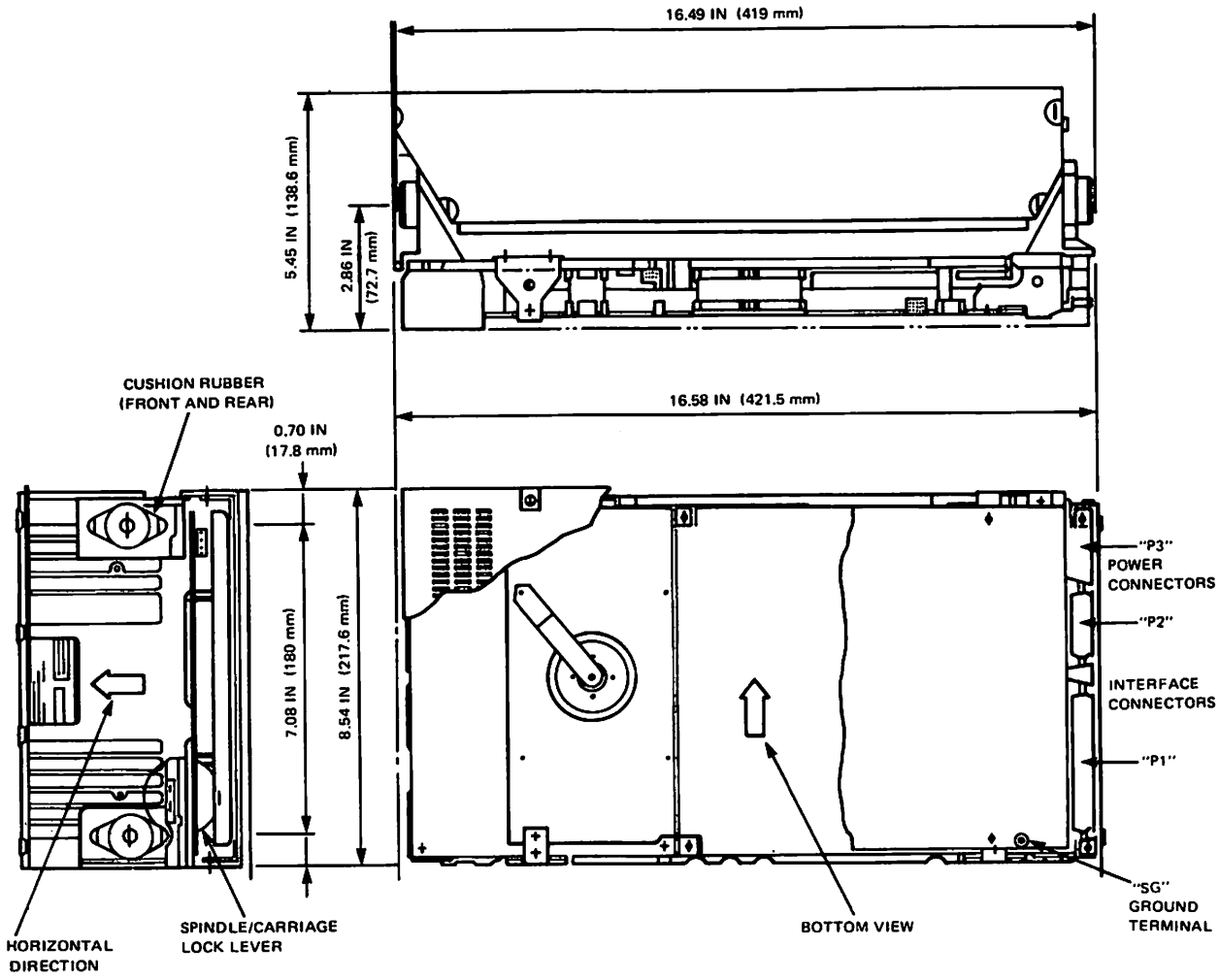


Figure B-1 D22x7 Basic Assembly Dimensions

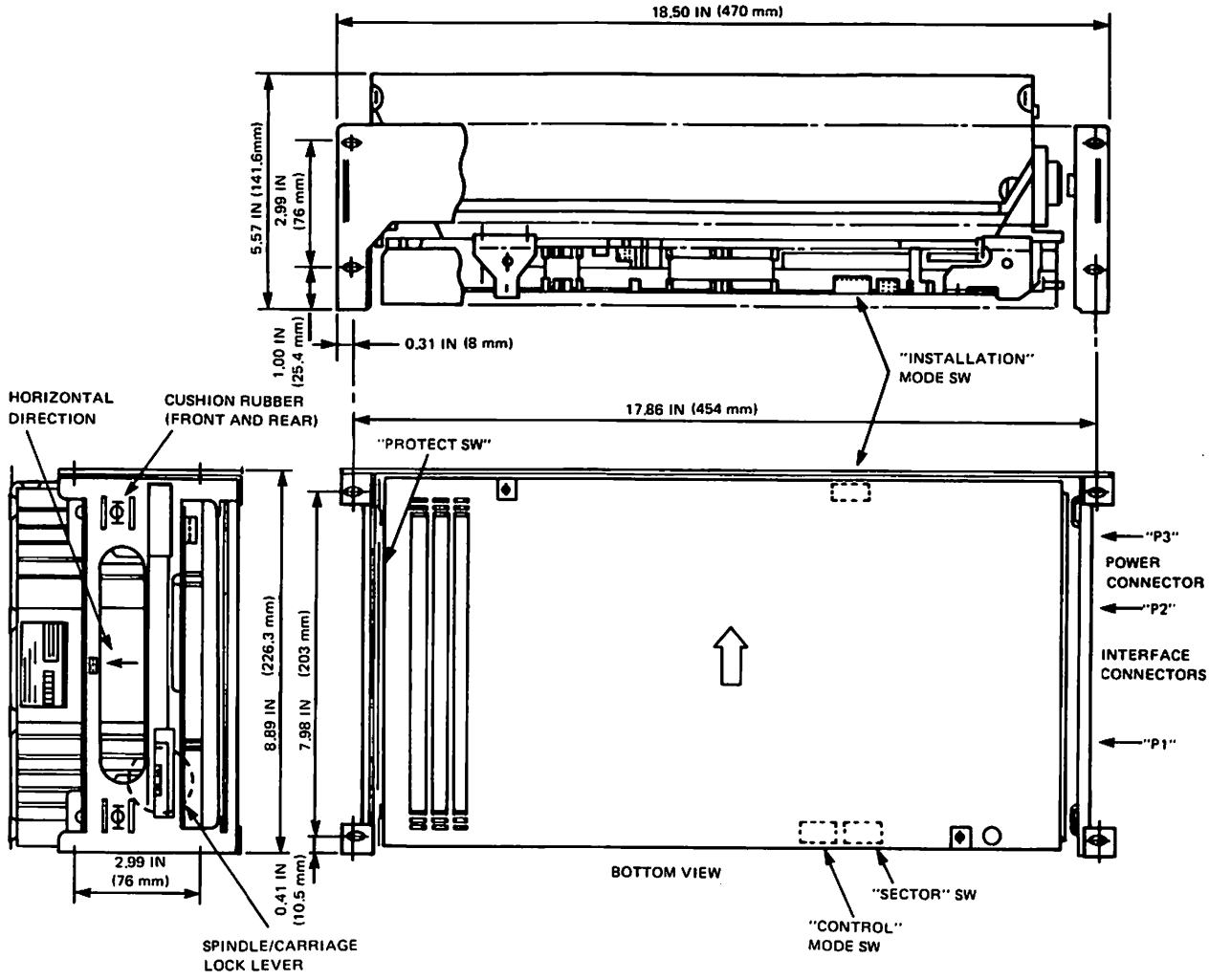


Figure B-2 D22x7 Standard Assembly Dimensions

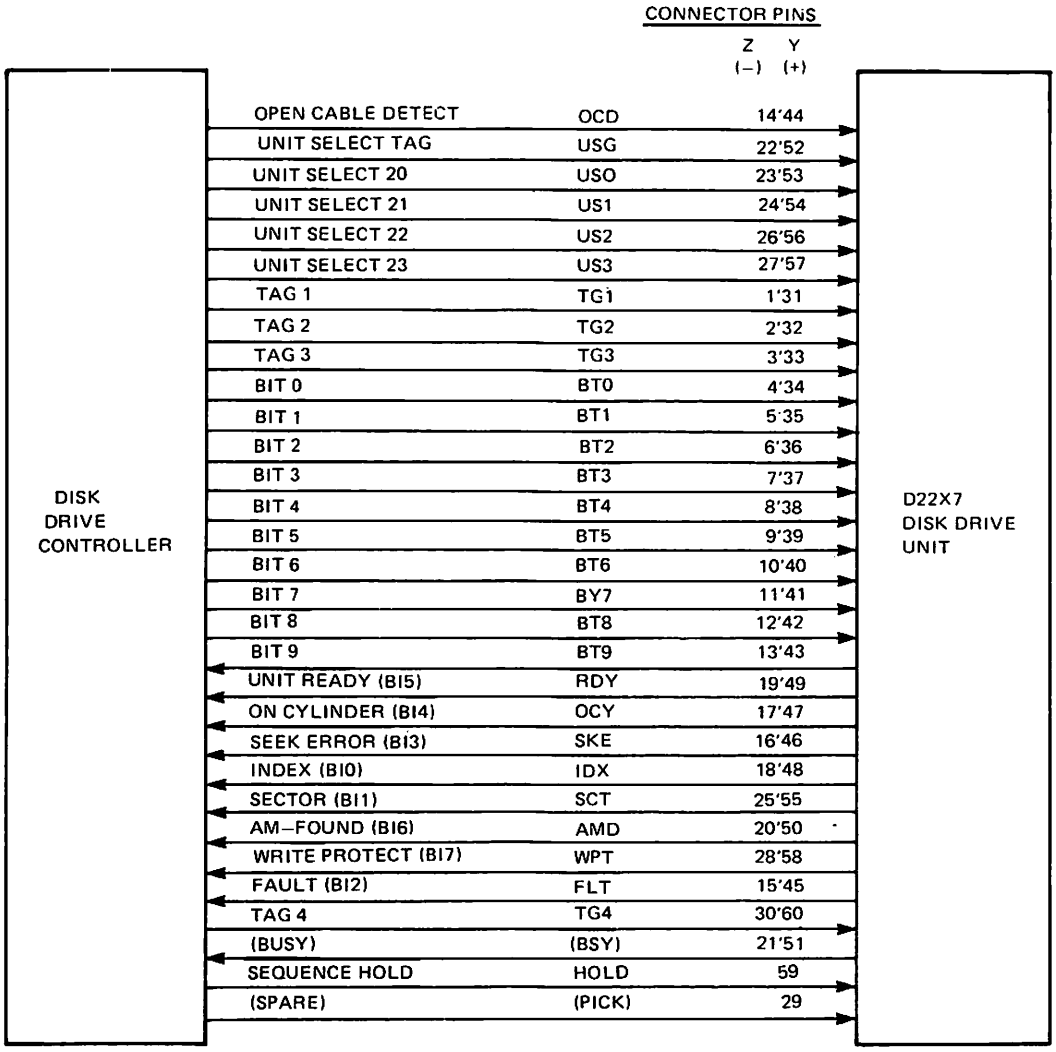


Figure B-3 Cable A Signals

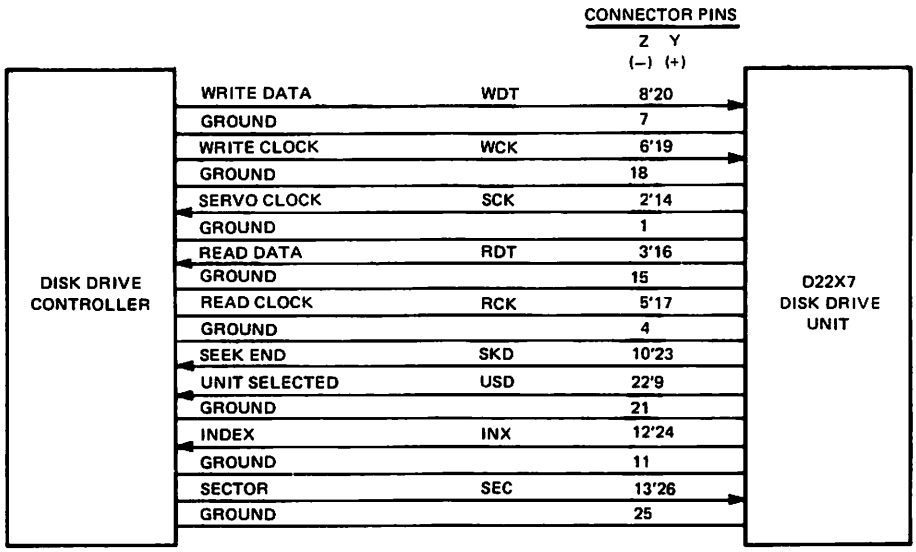
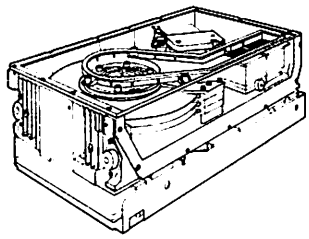


Figure B-4 Cable B Signals

Appendix C



DKU000-HLOG Diagnostic Panel

The DKU000-HLOG Diagnostic Panel tests D22x7 disk drives. When the disk drive is offline, the panel simulates an interface controller and functions as a drive exerciser. When the disk drive is online, the panel functions as a status monitor. All errors detected by the panel are encoded and logged in its internal memory and retained for more than 100 hours after power has been turned off.

C.1 CONTROL PANEL

The diagnostic panel is shown in Figure C-1. The panel contains a 25-key keypad, five LED status indicators, a six-digit liquid crystal display (LCD) window, and two summary charts. A mounting spring on each end attaches the panel to the disk drive as shown in Figure C-2.

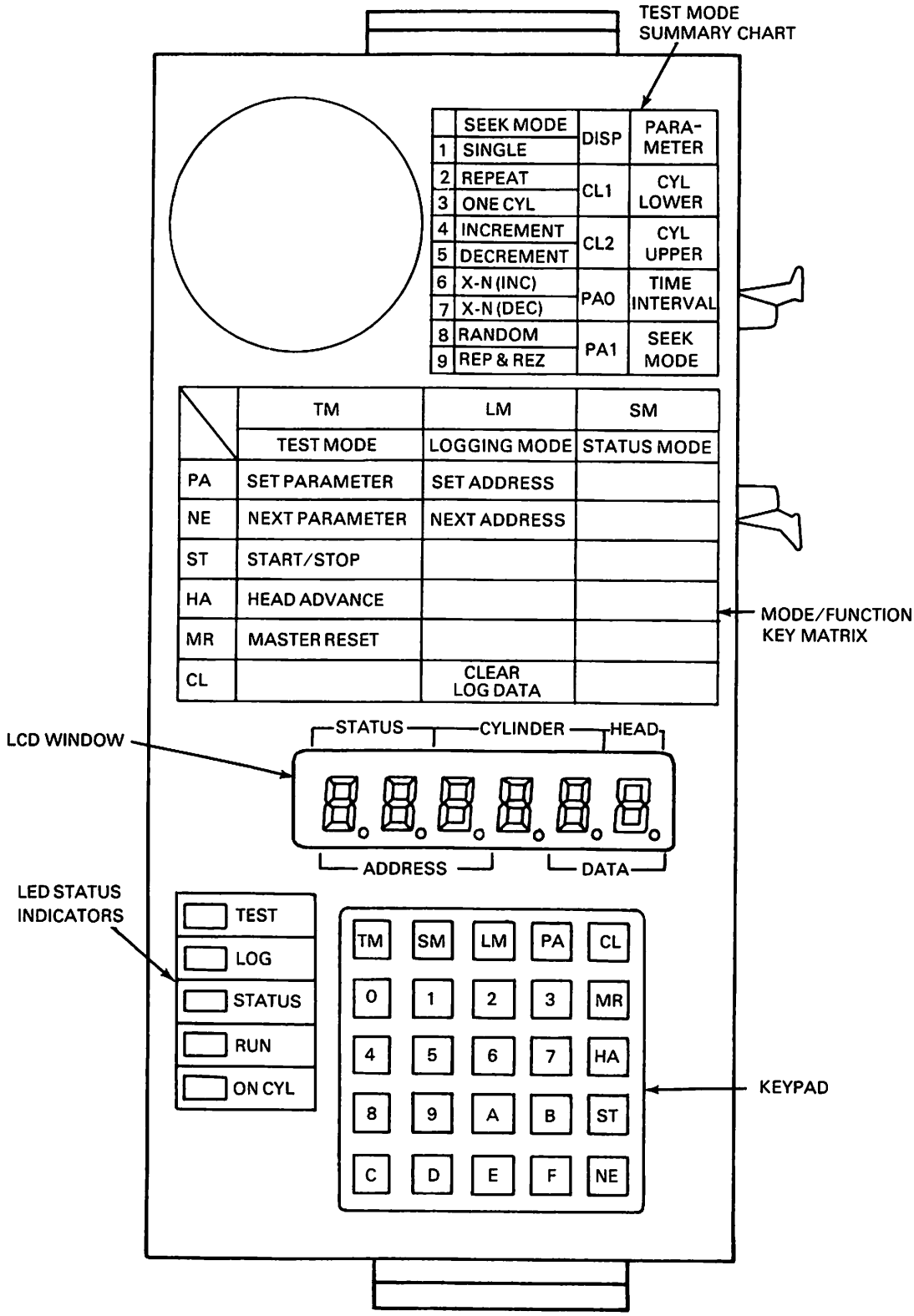


Figure C-1 Diagnostic Panel

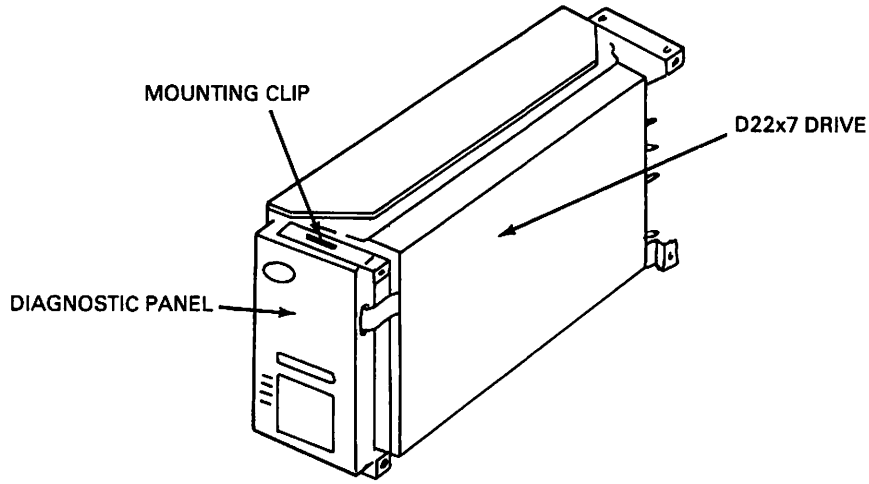


Figure C-2 Attaching the Diagnostic Panel to the Drive

A 0.4 Farad capacitor provides nonvolatile memory for the logging function. The diagnostic panel is connected to the disk drive by an interface cable as shown in Figure C-3.

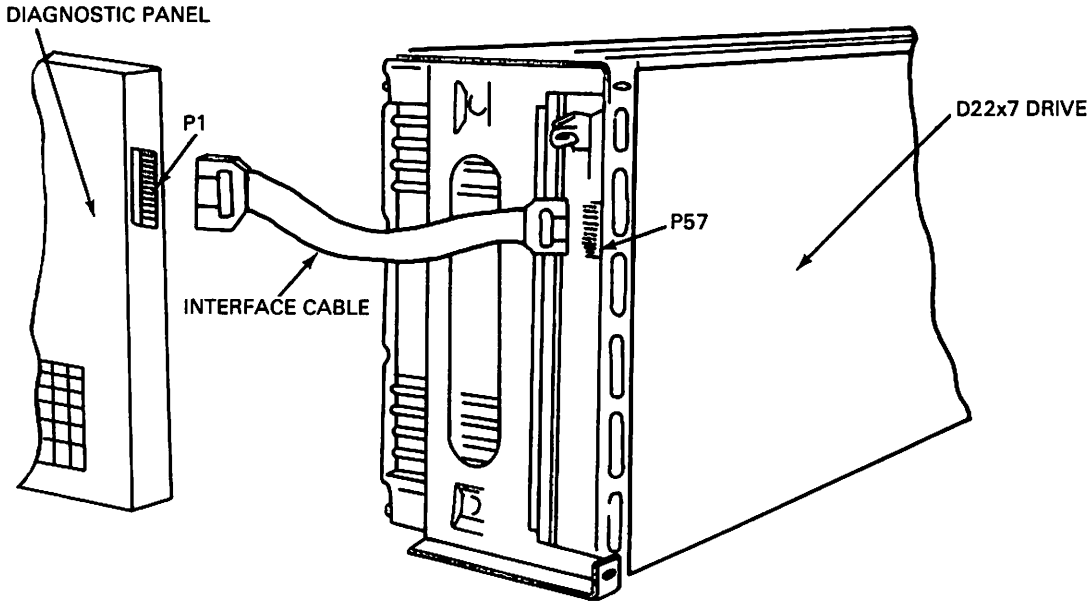


Figure C-3 Diagnostic Panel Cable and Connector

C.1.1 Keypad

The keypad contains 25 keys. Sixteen of these keys, representing hexadecimal digits 0 to F, are used to enter exercise parameters when Test mode is selected.

Three keys select the operational mode of the diagnostic panel. The functions of these keys are listed in Table C-1.

Table C-1 Mode Selection Keys

KEY	MODE SELECTED	DESCRIPTION
TM	Test Mode	Test mode places the disk drive offline. The diagnostic panel simulates an interface controller, and exercises the drive.
SM	Status Mode	Status mode monitors the online operation of the drive. The LCD window displays the current drive status, as well as the current head and cylinder address.
LM	Log Read Mode	Log Read mode provides a record of status or error information. Errors are logged sequentially and by type.

The six remaining keys enable specific diagnostic panel functions as listed in Table C-2.

Table C-2 Diagnostic Panel Functions

KEY	FUNCTION	MODE	DESCRIPTION
PA	Parameter Input	TM	Enables entry of seek test parameters from the panel keypad. See Section C.3.1.1.
		LM	Enables entry of sequential record address from the keypad. See Section C.4.2.
CL	Clear	LM	Clears the logging area. See Section C.4.3
MR	Master Reset	TM	Performs a return-to-zero (RTZ) operation. See Section C.3.1.

Table C-2 Diagnostic Panel Functions (cont'd)

KEY	FUNCTION	MODE	DESCRIPTION
HA	Head Advance	TM	Increases the head address by one each time the key is pressed. See Section C.3.1.
ST	Start/Stop	TM	Starts or stops the selected operation.
NE	Next Parameter	TM	Enters the parameter value selected by the PA key and brings up the next parameter. See Section C.3.1.1.
		LM	Initiates and advances search routine through error logs. See Sections C.4.1 and C.4.2.

C.1.2 LED Status Indicators

Three LEDs, labelled TEST, LOG, and STATUS, indicate the operational mode of the diagnostic panel. Two additional LEDs, labelled RUN and ON CYL, indicate the operational mode of the disk drive.

C.1.3 LCD Display Window

The six-digit LCD window displays status or error information. Depending upon the selected operational mode, the following information is displayed:

- cylinder address
- head address
- drive status
- error count.

C.1.4 Diagnostic Panel Summary Charts

Two charts, a Mode/Function Key Matrix and a Test Mode Summary, are included on the diagnostic panel. The Mode/Function Key Matrix lists the function performed by each of the six function keys in the three operational modes. The Test Mode Summary lists the nine seek operations and four parameters used in Test mode.

C.2 STATUS MODE

In Status mode, the diagnostic panel displays the current status of the disk drive. When an error occurs, data is logged in the diagnostic panel's internal memory and simultaneously displayed in the six-digit LCD window. Subsequent errors are logged in memory. The panel display, however, remains unchanged. Status information is formatted as shown in Figure C-4.

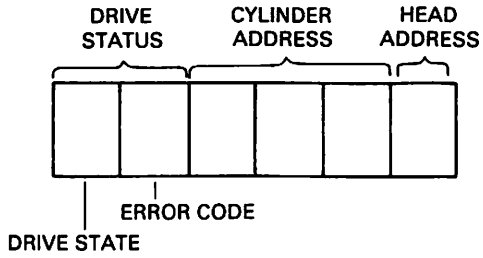


Figure C-4 Status Mode Display Format

C.2.1 Starting Status Mode

Pressing the SM key starts Status mode. When Status mode is selected, the STATUS and ON CYL LEDs light. The data window displays the drive status, consisting of the operational state of the disk drive and an associated error code, the current cylinder address, and the current head address.

C.2.1.1 DRIVE STATUS

The two-digit drive status display lists the operational state of the disk drive along with an encoded error report. Table C-3 lists the drive state displays and the corresponding state of operation.

Table C-3 Disk Drive Operational States

LCD DISPLAY	OPERATIONAL STATE
1	Power On/Initialization Sequence
2	Stop State
3	Start Delay
4	Motor Start (90% RPM attained)
5	Motor Speed Increase (97% RPM attained)
6	Full Motor Speed
7	Phase-Locked Oscillator
8	Recalibrate Out
9	Recalibrate In
A	Ready (On Cylinder)
B	Heads Out
C	Interface Check
D	Heads In
E	Fault (Not Ready)
F	Fault (Ready)

Table C-4 lists all drive status reports, along with suggested troubleshooting procedures.

Table C-4 Drive Status Reports

DISPLAY		ERROR CONDITION	SUGGESTED PROCEDURES
DRIVE STATE	ERROR CODE		
1	1	Voltage Fault	Check source voltage.
1	2	Read-only-memory (ROM) fault	Replace G9QSV PCB.
1	4	Fault latch	Replace G9QSV PCB.
2	1	Voltage fault	Check source voltage.
3	1	Voltage fault	Check source voltage.
4	1	Voltage fault	Check source voltage.
4	3	Insufficient motor speed	Check motor rotation. Replace G9QSR PCB.
4	4	No motor rotation	Check lock control lever. Replace G9QSR PCB.
5	1	Voltage fault	Check source voltage.
5	2	Insufficient motor speed	Check source voltage. Check cable connector. Replace G9QSR PCB. Replace G9QSV PCB. Replace the unit.
5	3	Excessive motor speed	See Fault 52.
6	1	Voltage fault	Check source voltage.
6	3	Excessive motor speed	See Fault 52.
7	1	Voltage fault	Check source voltage.
7	2	Motor speed loss	Restart motor. If Fault 43 or 44 occurs, replace G9QSR PCB. Replace G9QSV PCB. Replace unit.
7	4	Loss of index	Check the tripulse output. If tripulse is available, replace G9QSV PCB. Replace unit. If tripulse is not available, replace G9QSR PCB. Replace unit.

Table C-4 Drive Status Reports (cont'd)

DISPLAY		ERROR CONDITION	SUGGESTED PROCEDURES
DRIVE STATE	ERROR CODE		
7	5	Inner guard band (IGB) not found	Replace G9QSV PCB. Replace unit.
8	1	Voltage fault	Check source voltage.
8	2	Motor speed loss	See Fault 72.
8	4	Loss of index	See Fault 74.
8	5	Outer guard band (OGB) not found	Check lock control lever. Verify current flow in the voice coil. Replace G9QSV PCB. Replace unit.
8	6	No N linearity found	Replace G9QSV PCB. Replace unit.
8	7	No half track found	Replace G9QSV PCB.
8	8	No Q linearity found	Replace G9QSV PCB.
8	9	No zero difference found	Replace G9QSV PCB.
8	A	Target velocity not obtained	Replace G9QSV PCB.
8	B	Servo circuit fault	See Fault 8A.
8	C	Over-shoot check	See Fault 8A.
8	D	Over-shoot check (time out)	See Fault 8A.
9	1	Voltage fault	Check source voltage.
9	2	Motor speed loss	See Fault 72.
9	4	Loss of index	See Fault 74.
9	5	Only OGB detected	Replace G9QSV PCB. Replace unit.
9	9	No N linearity found	See Fault 86.
9	A	Target velocity not obtained	See Fault 8A.
9	C	Over-shoot check	See Fault 8A.
9	D	Over-shoot check (time out)	See Fault 8A.

Table C-4 Drive Status Reports (cont'd)

DISPLAY		ERROR CONDITION	SUGGESTED PROCEDURES
DRIVE STATE	ERROR CODE		
A	1	Voltage fault	Check the source voltage.
A	2	Motor speed loss	See Fault 72.
A	3	Excessive motor speed	See Fault 52.
A	4	Loss of index	Check the tripulse or cylinder concerned. If index signal found, replace G9QSV PCB. If index signal missing, replace unit.
A	C	R/W positioner off track	Replace G9QSV PCB. Replace unit.
B	1	Voltage fault	Check the source voltage.
B	4	Loss of index	See Fault A4.
B	9	No zero difference found	Replace G9QSV PCB.
B	A	Target velocity not obtained	See Fault 8A.
B	C	Over-shoot check	See Fault 8A.
B	D	Over-shoot check (time out)	See Fault 8A.
B	E	OGB detected during seek	See Fault 8A.
B	F	IGB detected during seek	See Fault 8A.
C	1	More than 1024 cylinders detected	
C	2	Tag 1 received when not on cylinder	
C	3	Tag 1 received when not ready	
D	1	Voltage fault	Check the source voltage.
D	4	Loss of index	See Fault A4.
D	9	No zero difference found	Replace G9QSV PCB.
D	A	Target velocity not obtained	See Fault 8A.

Table C-4 Drive Status Reports (cont'd)

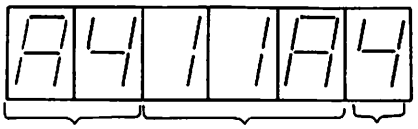
DISPLAY		ERROR CONDITION	SUGGESTED PROCEDURES
DRIVE STATE	ERROR CODE		
D	C	Over-shoot check	See Fault 8A.
D	D	Over-shoot check (time out)	See Fault 8A.
D	E	OGB detected during seek	See Fault 8A.
D	F	IGB detected during seek	See Fault 8A.
E	1	Seek error	
E	2	Excessive seek velocity	
E	3	Seek velocity too low	
E	4	PLO fault	
E	5	R/W positioner off track	See Fault AC.
E	6	Offset command error	
E	7	Faulty RTZ operation	
F	1	Write protect violation	Check for defective interface.
F	2	Write gate while not ready	Check for defective interface. Replace G9QSV PCB. Replace unit.
F	3	Write clock fault	Replace G9QSV PCB. Replace unit.
F	4	Write head off track	Replace G9QSV PCB.
F	5	Abnormal write operation	Replace G9QSP PCB. Replace G9QSV PCB. Replace unit.
F	6	Abnormal read operation	See Fault F5.

C.2.1.2 CYLINDER AND HEAD ADDRESSES

When the diagnostic panel is in Status mode, the current cylinder address is displayed in three digit hexadecimal notation. The current head address is displayed as a single digit.

C.2.2 Using Status Mode

Status mode displays the current status of the disk drive. If an error occurs, the corresponding drive status report is displayed. Simultaneously, the displayed data is logged in the diagnostic panel's internal memory. The presence of a non-zero digit in the right position of the drive status display, or the presence of a "00" code in the drive status display indicates an error condition (see Figure C-5).



THE SAMPLE DISPLAY INDICATES THAT THE INDEX SIGNAL WAS NOT DETECTED AT CYLINDER $11A_H$, HEAD 4.

Figure C-5 Status Mode Error Display Format

The panel's internal memory records subsequent errors as they occur. The LCD display, however, remains unchanged until the SM key is pressed. Pressing the SM key displays the latest drive status report.

C.2.3 Ending Status Mode

Pressing the TM or LM key ends Status mode.

C.3 TEST MODE

In Test mode, the diagnostic panel places the disk drive offline; that is, the interface between the drive and the drive controller is disabled. The diagnostic panel simulates the drive controller, and enables nine different seek operations to test the drive.

C.3.1 Starting Test Mode

Select Test mode by pressing the TM key and then pressing the 9 key. Pressing the 9 key acts as a safety device that prevents the disk drive moving from an online to an offline condition when the TM key is accidentally pressed.

After Test mode is selected, press the MR key to perform a return-to-zero (RTZ) operation. This operation moves the read/write heads to Cylinder 000.

Press the HA key to select the desired read/write head. The head address appears in the rightmost character position of the LCD display. The address is incremented by one each time the HA key is pressed.

C.3.1.1 INPUT PARAMETERS

After the read/write head is selected, three parameters (low cylinder address, high cylinder address, and interval timing) are set. Press the PA key to begin setting parameters for seek operations. The resulting LCD display is shown in Figure C-6.

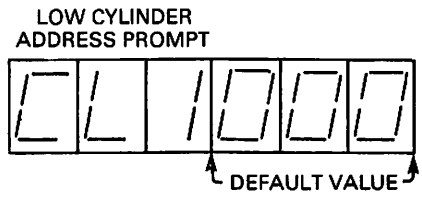


Figure C-6 Low Cylinder Parameter Display

The low cylinder address (CL1) default value (Cylinder 000) appears in the address field as shown. To set a new low cylinder address, enter three hexadecimal digits from the numeric keypad. Press the NE key to accept the default value or to accept the new value as entered from the keypad.

When the NE key is pressed, the LCD display appears as shown in Figure C-7.

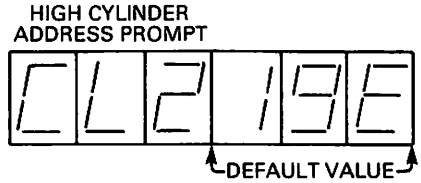


Figure C-7 High Cylinder Parameter Display

The high cylinder address (CL2) default value (Cylinder 19E) occupies the address field. To set a new high cylinder address, enter three hexadecimal digits from the keypad. The high cylinder address must be greater than the low cylinder address. Press the NE key to accept the default value or to accept the new value as entered from the keypad.

After pressing the NE key, the LCD display appears as shown in Figure C-8.

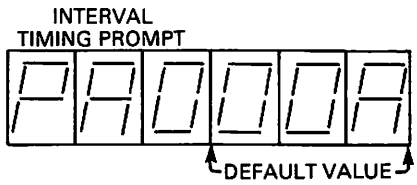


Figure C-8 Interval Timing Parameter Display

The interval timing default value, expressed in milliseconds, is recorded in the address field. To set a new interval timing, enter three hexadecimal digits from the keypad. Press the NE key to accept the default value or to accept the new value as entered from the keypad.

C.3.1.2 SEEK MODES

After the interval timing value is entered and the NE key pressed, the following display appears.

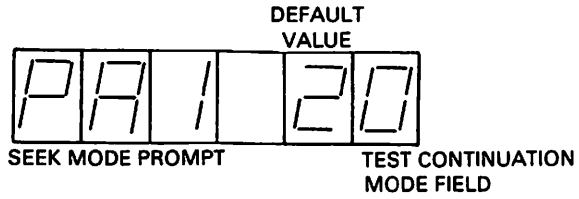


Figure C-9 Seek Mode Display

The seek mode digit selects one of the nine seek operations listed on the Test Mode Summary chart. The test continuation digit determines the conditions under which a seek test is halted. When a zero is displayed, seek operations are halted if an error occurs. When any other digit is displayed, seek operations continue to completion.

The seek mode default value is recorded in the address field. To set a new seek mode and test continuation condition, enter two digits from the keypad. Press the NE key to accept the default value or to accept the new value as entered from the keyboard.

Table C-5 summarizes the nine seek modes that can be selected.

Table C-5 Seek Modes

MODE NUMBER	SEEK MODE	DESCRIPTION
1	Single Seek	Seeks to destination cylinder (CL2) and stops. To repeat, press the MR key and wait until the read/write heads return to cylinder 000. Then press the ST key.
2	Repeat Seek	Seeks directly from the low cylinder address to the high cylinder address, and then from the high cylinder to the low cylinder. The cycle is repeated.
3	One Cylinder	Seeks one cylinder at a time from the low cylinder (CL1) to the high cylinder (CL2), and then from the high cylinder to the low cylinder. The cycle repeats. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 001, to 002, to ..., to 100. Then seeks to 099, to 098, to ..., to 000.
4	Increment Seek	Seeks one cylinder at a time from the low cylinder (CL1) to the high cylinder (CL2), and then returns directly to the low cylinder to repeat the cycle. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 001, to 002, to ..., to 100. Returns to CL1 and repeats.

Table C-5 Seek Modes (cont'd)

MODE NUMBER	SEEK MODE	DESCRIPTION
5	Decrement Seek	Seeks one cylinder at a time from the high cylinder (CL2) to the low cylinder (CL1), and then returns directly to the high cylinder to repeat the cycle. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 099, to 098, to ..., to 000. Returns to CL2 and repeats.
6	X + N (INC)	Seeks incrementally from the low cylinder (CL1) to the high cylinder (CL2), and then returns directly to CL1 to repeat the cycle. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 001 and returns to CL1; seeks to 002 and returns to CL1; seeks to ... and returns to CL1; seeks to 100. Returns to CL1 and repeats cycle.
7	X - N (DEC)	Seeks decrementally from the high cylinder (CL2) to the low cylinder (CL1), and then returns directly to CL2 to repeat the cycle. For example, with CL1 equal to 000 and CL2 equal to 100, seeks to 099 and returns to CL2; seeks to 098 and returns to CL2; seeks to ... and returns to CL2; seeks to 000. Returns to CL2 and repeats cycle.
8	Random	Seeks randomly within the parameters set by the low and high cylinder addresses.
9	Repeat and RTZ	Seeks to high cylinder (CL2), returns to cylinder 000, and repeats cycle.

C.3.2 Using Test Mode

When all parameters are set, press the ST key to enter Test mode. The RUN LED lights and the selected seek operation is performed. If an error occurs while a seek test is running, the diagnostic panel displays the status of the drive just as it does in Status mode (see Section C.2).

C.3.3 Ending Test Mode

Seek operations are halted before completion by a seek error (depending on the status of the test continuation condition), or by pressing the ST key. When seek operations stop, the RUN LED goes out. The panel remains in the Test mode. To end Test mode press the SM or LM key.

C.4 LOG READ MODE

The diagnostic panel stores specific information on each error that occurs during either Status or Test mode. Information is logged into a dedicated 640-byte memory that consists of two sections. The first section (memory addresses 000_H through $0FF_H$) records the number of times a specific error occurs. The second section (memory addresses 100_H through $27F_H$ provides a sequential log of drive operations. The Log Read mode provides access to both of these memory areas.

C.4.1 Error/Count Log

Press the LM key to start the Log Read mode. The LOG and the ON CYL LEDs light. When using the Error/Count Log, the LCD display is formatted as shown in Figure C-10.

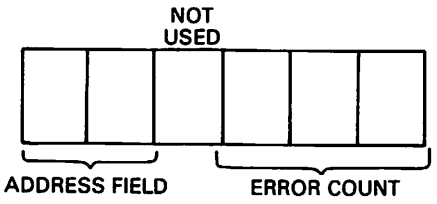


Figure C-10 Error/Count Log Display Format

When the LM key is pressed, the three-digit address field displays memory location 000 and the two-digit data field displays the total number of recorded errors.

Subsequent entries in the Error/Count Log are displayed by pressing the NE key. In most instances, pressing the NE key results in the following LCD display.

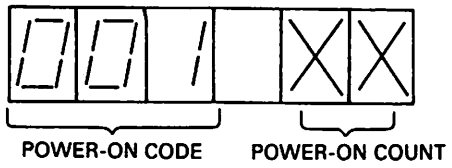


Figure C-11 Error/Count Log Power-On Count

The address field displays memory location 001 signifying power-on. The data field displays the power-on count.

Pressing the NE key again initiates a search through the Error/Count Log. When an error is detected, a drive status report (listed in Table C-3) is displayed in the address field. The number of times the error occured is displayed in the data field. A sample LCD display is shown in Figure C-12.

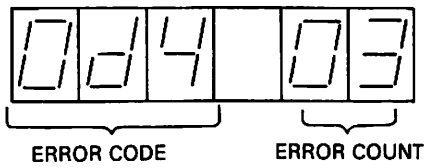


Figure C-12 Error/Count Log Error Display Format

The above display indicates that the d4 error (loss of Index signal) occured three times.

Each time the NE key is pressed, the display advances to the next error. When all errors have been displayed, or if no errors have occured, the display returns to the 000 memory address and the total count of logged errors.

C.4.2 Sequential Operations Log

Memory addresses 100 through 27F are assigned to the Sequential Operations Log. This log records errors and power-on and power-off operations. To access the Sequential Operations Log press the LM key to start Log Read mode, and then press the PA key.

Use the numeric keypad to initiate a search through the Sequential Operations Log. To examine the entire log, enter 100 from the keypad. Any other memory address from 101 through 27F can be entered. When the address has been entered, press the NE key to display the contents of the address location. The LCD display format is shown in Figure C-13.

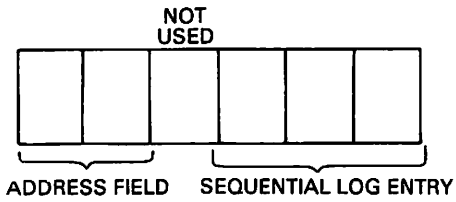


Figure C-13 Sequential Operations Log Display Format

Each time the NE key is subsequently pressed, the address field is incremented by one and the contents of that memory location are displayed in the data field. Figure C-14 shows sequential log entries.

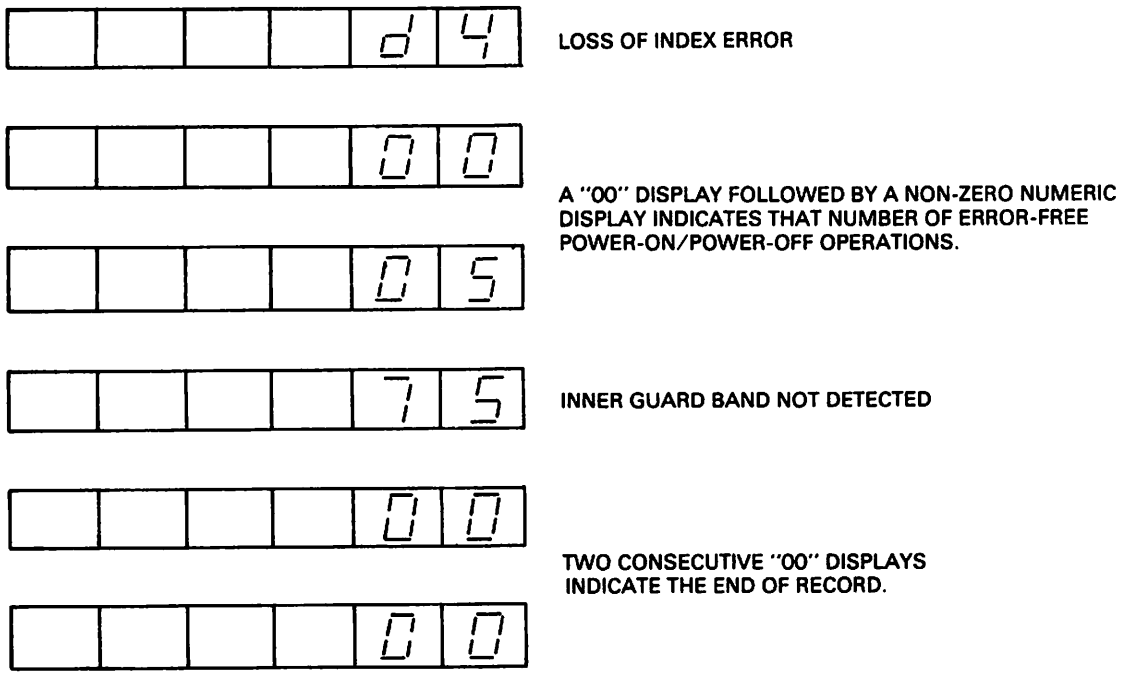
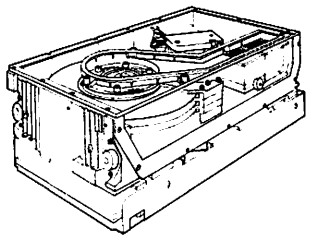


Figure C-14 Sequential Operations Log Entries

C.4.3 Ending Log Read Mode

Press the CL key to clear both the error/count log and the sequential log. Press the LM or SM key to end Log Read mode.

Appendix D



DKU000-H3P7 3-Input DC Regulator Option

This appendix assumes familiarity with the operation of the 3-Input DC Regulator option. It describes only the regulator's electrical input requirements and its physical dimensions.

D.1 GENERAL DESCRIPTION

The 3-Input DC Regulator requires an input set of three dc voltages: +24V, +5V, and -12V. From this input set, the regulator supplies the power set of dc voltages required by the D22x7 disk drive: +24V, +12V, +5V, -5V, and -12V.

The regulator contains an input connector, a signal ground terminal, voltage converters, and an output cable that connects to the D22x7 disk drive. The 3-Input DC Regulator is mounted within the D22x7 and does not affect its exterior dimensions.

Figure D-1 diagrams the 3-Input DC Regulator and Figure D-2 shows its physical dimensions.

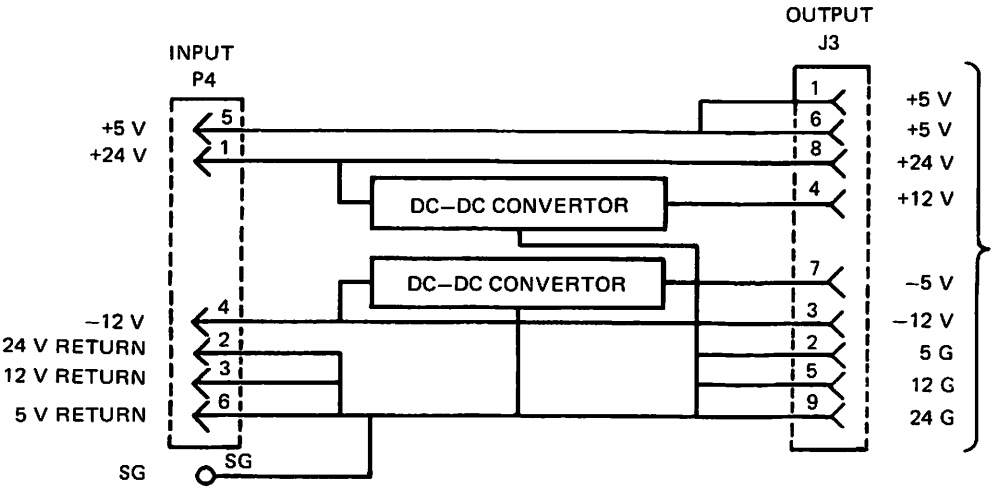


Figure D-1 Block Diagram: 3-Input DC Regulator

D.2 INTERFACE REQUIREMENTS

The following three sections describe specific interface requirements.

D.2.1 DC Power Connector (P4)

A six-pin AMP connector (No. 1-380999-0) is used for power input. Figure D-3 shows this connector, and Table D-1 lists its pin functions.

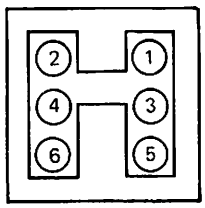


Figure D-2 P4 Connector

Table D-1 P4 Pin Assignments

PIN NUMBER	FUNCTION
1	+24 V dc
2	24 V return
3	12 V return
4	-12 V dc
5	+5 V dc
6	5 V return

The recommended mating connector for P4 is described below.

- Cable side housing— AMP P/N 1-480270-0
- Receptacle contact— AMP P/N 60617-4
  AMP P/N 60619-4
- Cable wire — No. 18 AWG standard wire

D.2.2 Signal Ground Terminal

The signal grounding wire is connected to the SG terminal. The recommended mating connector for the SG terminal is described below.

- Cable side housing— AMP Plasti-Grip Terminal
- Receptacle contact— AMP P/N 170782-1
- Cable wire — No. 18 AWG standard wire

D.2.3 DC Power Input Requirement

Table D-2 lists dc input requirements.

Table D-2 DC Power Requirements

VOLTAGE (VOLTS-DC)	TOLERANCE (+VOLTS-DC)	CURRENT (AMPERES-DC)	RIPPLE (MILLIVOLTS P-P)
+5.0	0.25	4.0	100
-12.0	0.60	1.0	100
+24.0	2.40	3.0 average 5.5 peak	240

D.3 INSTALLING THE 3-INPUT DC POWER REGULATOR

Figure D-4 shows how to install the regulator.

D.4 ELECTRICAL SPECIFICATIONS

Table D-3 lists the electrical specifications of the 3-Input DC Regulator.

Table D-3 Electrical Specifications

Input Voltage	+5V	+24V	-12V		
Input Regulation	±5%	±10%	±5%		
Output Voltage	+5V (through)	+24V (through)	-12V (through)	+12V	-5V
Output Current	5 Amax	5 Amax	1 Amax	0.6 Amax	1.2 Amax
Load Regulation +12V: 0.2A < Io < 0.6A -5V: 0.3A < Io < 1.2A	—	—	—	±3%	±3%
Total Variation	—	—	—	±5%	±5%
Ripple	—	—	—	100 mVP-P	
Protection	—	—	—	Short-circuit protection	
Ambient Temperature	5°C to 50°C				

D.5 PHYSICAL DIMENSIONS

Figure D-3 shows the dimensions of the **3-Input** DC Regulator Option.

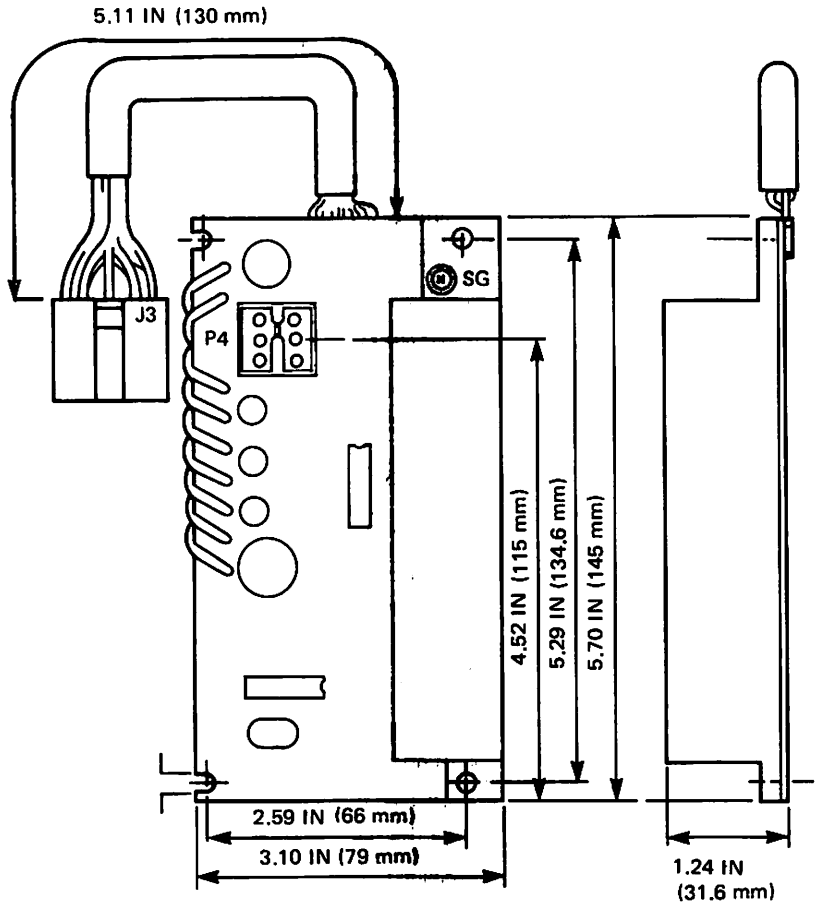


Figure D-3 3-Input DC Regulator Dimensions

Figure D-4 shows how to mount the 3-Input DC Regulator on a D22x7 disk drive.

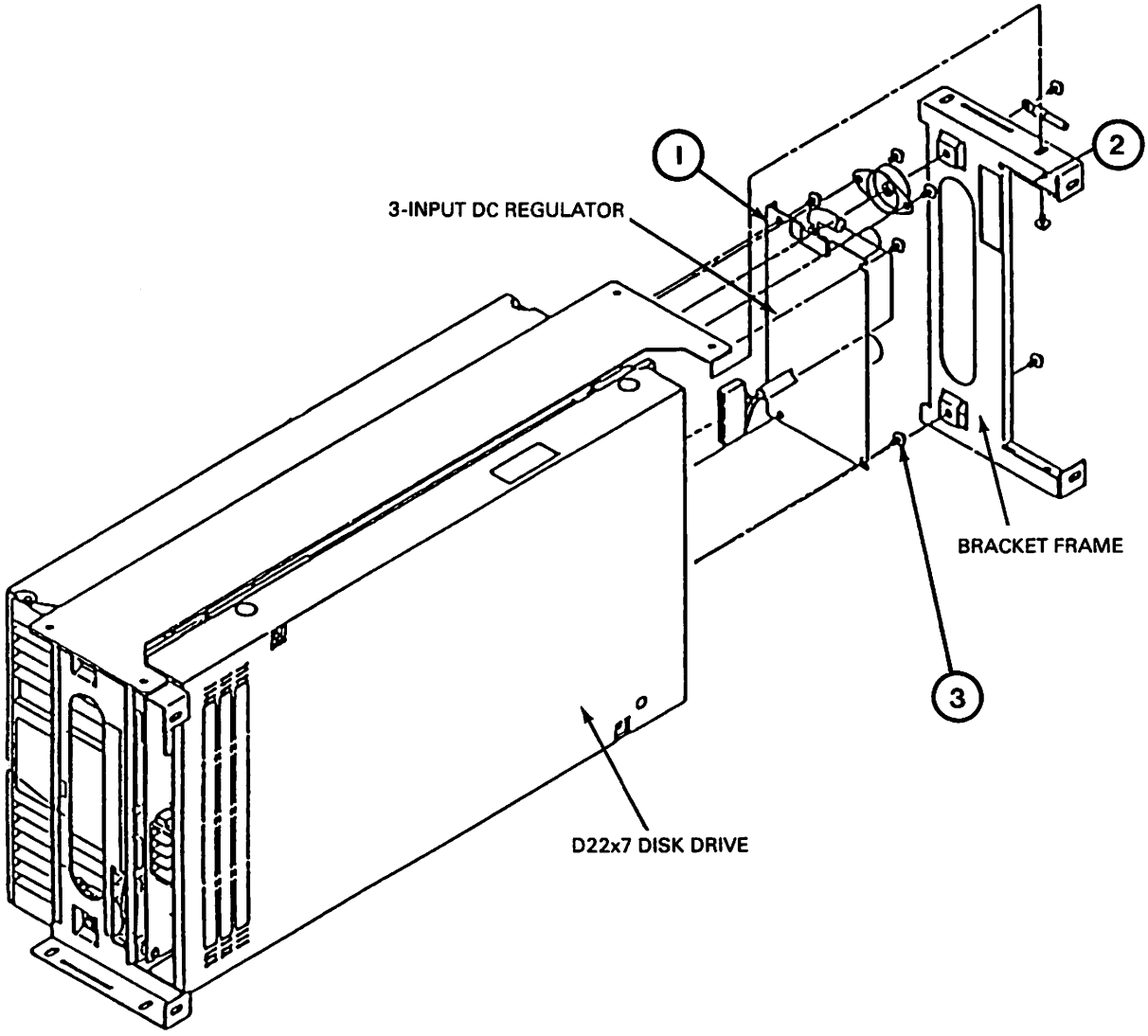
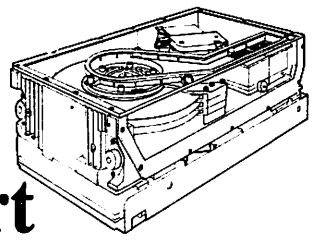


Figure D-4 3-Input DC Regulator Mounting.

Table D-4 DKU000-H3P7 3-Input DC Regulator Parts

ITEM	DESCRIPTION	PART NUMBER	QUANTITY
1	DKU000-H3P7 Regulator	806-942333-200	1
2*	Edging	806-935002-016-0	5 cm
3*	Screw	805-300004-010-0	4
*Items 2 and 3 are shipped with Item 1.			

Appendix E



DKU000-HDP2 Dual-Port Interface Option

SEE TSB 12/2/86, MATRIX ID 3112, HWT 6292 FOR INSTALL PROCEDURE.

This appendix assumes familiarity with the operation of the Dual-Port Interface, and describes only certain of its features.

E.1 GENERAL DESCRIPTION

The Dual-Port Interface allows access to one drive by two controllers. In allowing dual access, the interface functions as a switch that routes the necessary control and data signals to and from the correct controller.

The electrical specifications of the Dual-Port Interface (including line receivers and transmitters, cables and cable connectors, signal definitions, and pin assignments) are the same as those of a standard D22x7. The only difference is that D22x7 disk drives equipped with this option have two identical interfaces providing communications channels with two controllers.

These two identical interfaces are designated port A and port B. Communication links into and from port A are designated route 0; communication links into and from port B are designated route 1. Each port is physically connected to its controller by an A and a B cable.

SCREWS SECURING DUAL PORT BRD TO SERVO/LOGIC ALSO SERVE TO BRING 5V & GRND TO BRD.

Figure E-1 shows a dual-port cabling diagram.

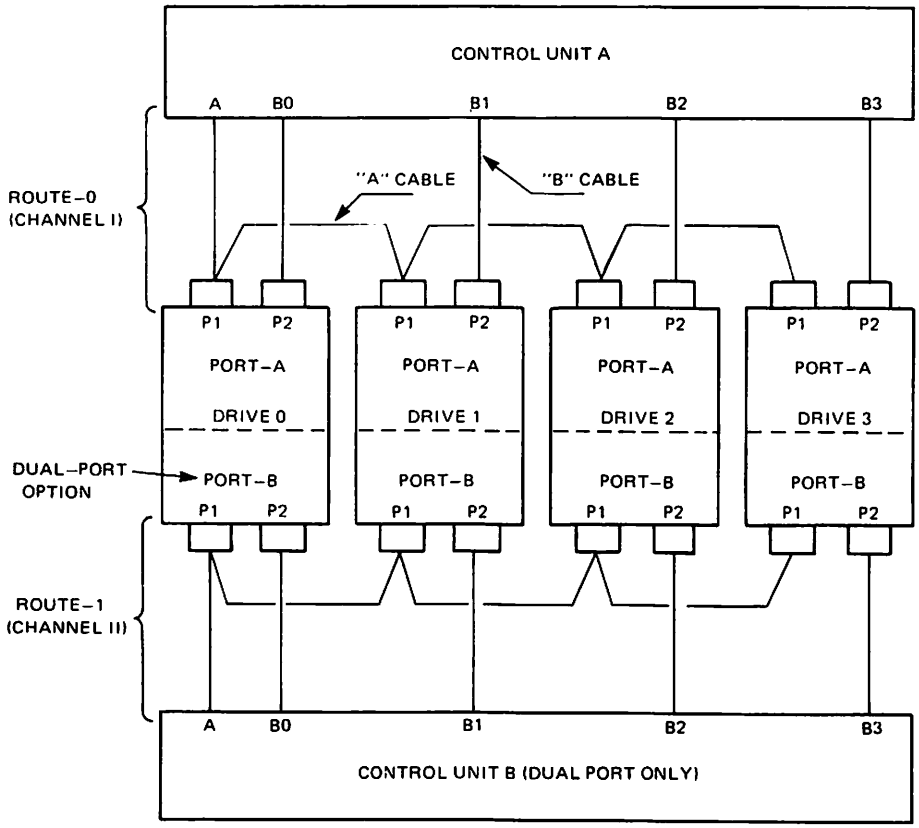


Figure E-1 Dual-Port System Cabling

E.2 SWITCHES AND INDICATORS

Three switches and four LED indicators located on the interface G9TXW PCB control its functions and provide status information. These switches and indicators are shown in Figure E-2.

E.2.1 Port A (Route 0) Switches and Indicators

- Toggle Switch — In the "E" (Enable) position, this switch establishes a communications channel (route 0) between the disk drive and a drive controller.

  In the "D" (Disable) position, no communications channel is established between the disk drive and the drive controller.

- RSV (LED) — When lit, indicates that the D22x7 is priority-selected by the route 0 controller.

- SEL (LED) — When lit, indicates that the D22x7 is selected by the route 0 controller.

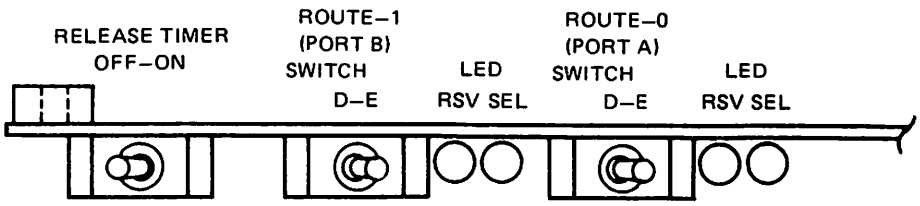


Figure E-2 Dual-Port Control Switches and Indicators

E.2.2 Port B (Route 1) Switches and Indicators

- Toggle Switch — In the "E" (Enable) position, this switch esablishes a communications channel (route 1) between the disk drive and a drive controller.

  In the "D" (Disable) position, no communications channel is established between the disk drive and the drive controller.

- RSV (LED) — When lit, indicates that the D22x7 is priority-selected by the route 1 controller.

- SEL (LED) — When lit, indicates that the D22x7 is selected by the route 1 controller.

E.2.3 Release Timer: ON/OFF Switch

This switch controls the release timer, a device that allows alternate controller access to the drive. With this switch in the OFF position, a drive remains selected until specifically released by the controller (see Section E.5.1).

With this switch in the ON position, the release timer automatically manages controller access. Each controller is allowed approximately 500 milliseconds of disk time. After that period, the communications channel is disabled and drive access is granted to the other controller.

E.3 DRIVE SELECTION

Drive selection is controlled by the G9TXW PCB on the Dual-Port Interface. When no controller has the drive reserved, the drive is available and can be selected or reserved by either controller. The interface recognizes and engages with the first controller to complete a drive selection. The drive is reserved by the selecting controller, and remains reserved until a Release signal, a release timer function, or a dc power-down occurs.

If the drive is already reserved or selected, a Busy signal is issued on cable A of the controller attempting the select. This Busy signal is issued within 600 ns of the selection attempt and remains until the drive is no longer reserved or selected.

E.4 INTERFACE

The dual-port read/write cable (cable B) is identical to the standard D22x7 cable B. The dual-port control cable (cable A), however, provides one additional status line. This line, Busy, issues a status reponse to a controller attempting to select a reserved or selected drive.

E.5 STATUS COMMANDS

The Dual-Port Interface provides two additional status commands.

E.5.1 Release Command

This command (bus bit 9 and Tag 3) is transmitted to the drive from the controller. It releases controller reserve and priority select, freeing the drive for use by the other controller.

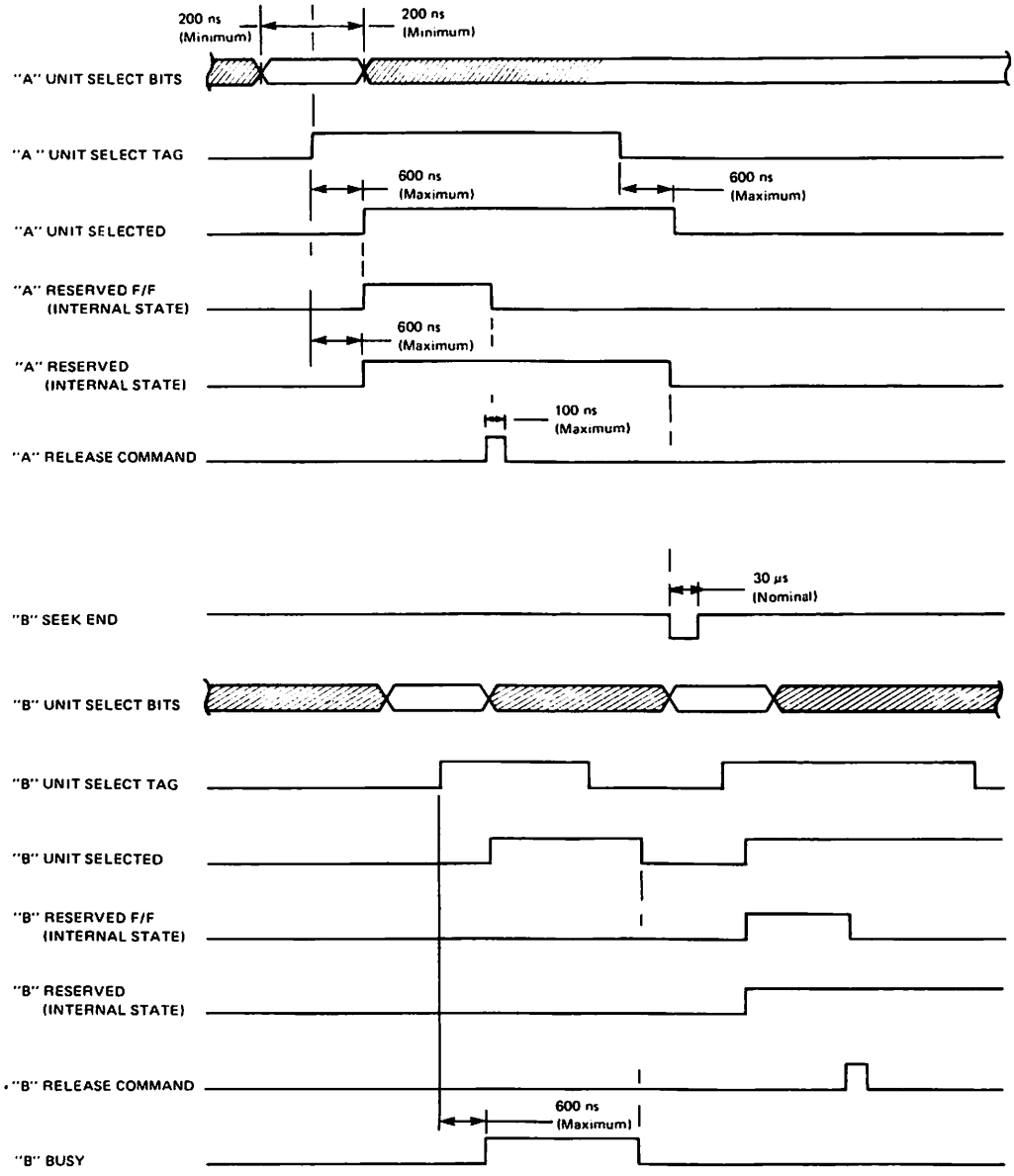


Figure E-3 Unit Select Timing for Dual-Port Option

E.5.2 Priority Select

The Priority Select signal (bus bit 9, Unit Select lines, and Unit Select Tag) is issued by a controller. This signal forces the drive to become unconditionally selected and absolutely reserved by the controller issuing the Priority Select signal. While this signal is active, the second controller is denied access to the drive. A Priority Select signal is not disabled by the release timer function.

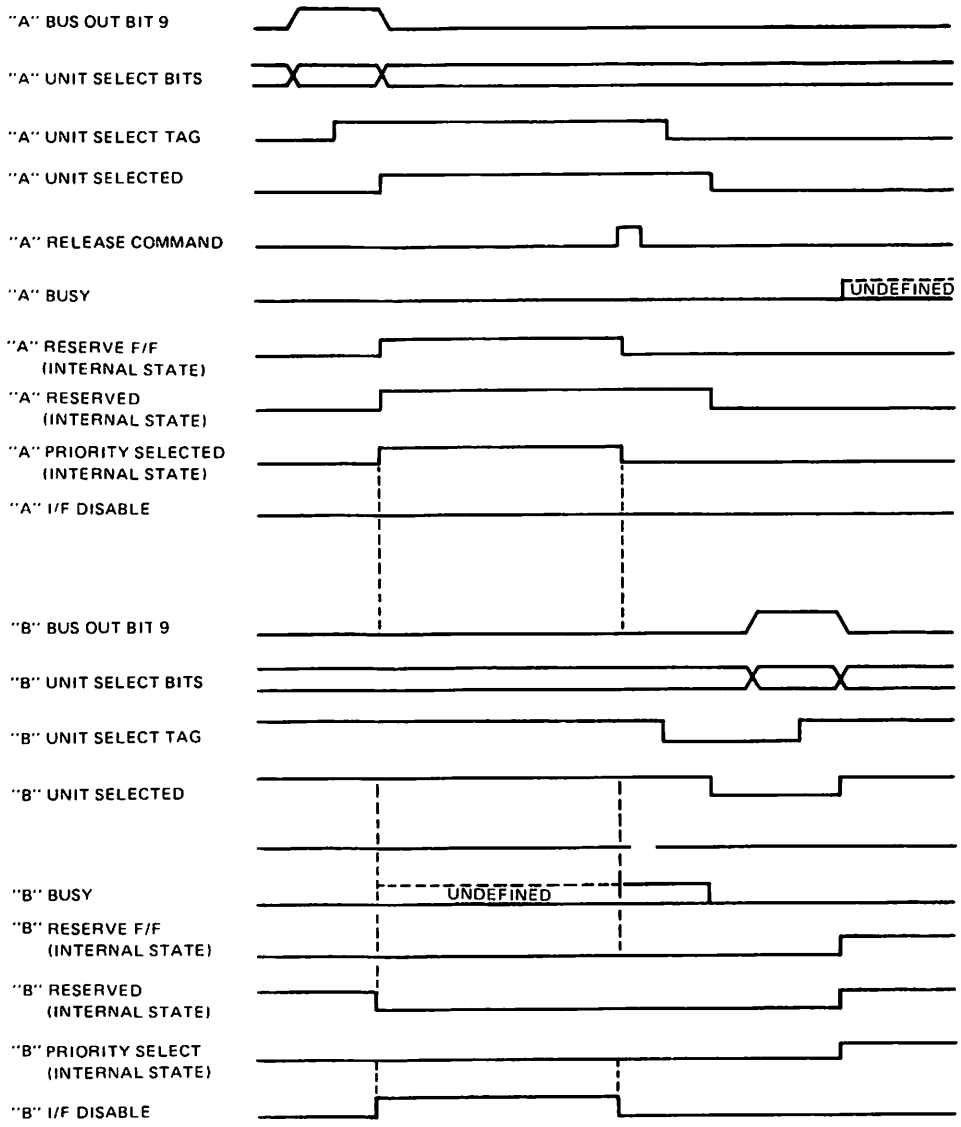


Figure E-4 Sample Priority Select Timing

CROSS REFERENCED LISTING

This page contains a brief cross referenced listing of NEC spares with their equivalent Wang part numbers on the Winchester Disk Drive Model D2257.

D2257 (167.7 MB WINCHESTER) SPARES LISTING
SORTED BY WLI #

WLI #	NEC Part Number	NEC Spare Number	Description
726-8111	134-232951	134-232951	Earth Pad Assy
726-8121	134-233100	134-832950	Read/Write PWA (G9QSP)
726-8122	134-233102	134-832952	Power Amp PWA (G9QSR)
726-8123	134-233106	134-832956	Logic & Servo PWA (G9QSV)
726-8124	134-200339-502	134-237667-057	057 DE Assy
725-0192	CAN USE EITHER W/	EITHER THE 80MB OR 167MB ONLY 1 USED	~~417 PAGE~~ DUAL PORT BRD (G9TXW)
725-0191			DUAL PORT BRD (G9QST)
725-2887			POWER SUPPLY

D2257 (167.7 MB WINCHESTER) SPARES LISTING
SORTED BY NEC PART #

NEC Part Number	WLI #	NEC Spare Number	Description
134-200339-502	726-8124	134-237667-057	057 DE Assy
134-232951	726-8111	134-232951	Earth Pad Assy
134-233100	726-8121	134-832950	Read/Write PWA (G9QSP)
134-233102	726-8122	134-832952	Power Amp PWA (G9QSR)
134-233106	726-8123	134-832956	Logic & Servo PWA (G9QSV)

Abbreviations

A	Ampere
ac	alternating current
AM	Address Mark
AWG	American Wire Gauge
CA	Cylinder Address
CRC	Cyclic Redundancy Check
dc	direct current
DE	Disk Enclosure
DIP	Dual-inline-packaged
DKC	Disk Controller
DKU	Disk Unit
ECC	Error Correction Code
EOR	End of Record
GND	Ground
HA	Head Address
HEX	Hexadecimal
IGB	Inner Guard Band
I/O	Input/Output
LED	Light emitting diode
m	meter
MB	Megabyte
MFM	Modified Frequency Modulation
MHz	Megahertz
mm	Millimeter
ms	Millisecond
mV	Millivolt
MTBF	Mean Time Between Failures
MTTR	Mean Time to Repair
NRZ	Non-Return-to-Zero
ns	Nanosecond
OGB	Outer Guard Band
PCB	Printed Circuit Board
PLO	Phase Locked Oscillator
RMS	Root-Mean-Square
ROM	Read only memory
RPM	Revolutions per Minute
R/W	Read/Write
SA	Sector Address
TTL	Transistor/Transistor Logic
V	Volt
μs	microsecond

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