

WANG

3308

**DATAPRODUCTS (300/600 LPM)
MASTER SUPPORT and LOGISTICS
VOLUME I**

**Models:
300 LPM PRINTERS**

**2273V-1
2273-1
5573**

600 LPM PRINTERS

**2273-2
5574**

**Customer Engineering Reprint
Product Maintenance Manual**

741-0434-A

PREFACE

The purpose of this manual is to provide the Wang-trained Customer Engineer (CE) with instructions to operate, troubleshoot and repair the B300 and B600 LPM Line Printers.

The following are the Wang model numbers for the B300/B600 Band Printers.

5573	300LPM	serial printer
5574	600LPM	serial printer
2273-1	300LPM	parallel printer
2273-2	600LPM	parallel printer
2273V-1	300LPM	parallel remote printer

All the printer models listed above are configured with the following options.

Maximum print columns (132)
DAVFU: Direct access vertical format unit
Standard pedestal (acoustical cabinet not used)
Universal 50/60Hz and domestic 60Hz only power supplies are used
Dataproducts Centronics compatible interface, WLI part number 726-1108, OEM part number 257265-001.

Second Edition (October 1984)

This edition of the OEM manual is the new converted number for and obsoletes 741-0434. Appendix B (OEM to Wang cross reference tables) has been added to this document. The material in this document may be used only for the purpose stated in the Preface. Updates and/or changes to this document will be published as Publications Update Bulletins (PUB's) or subsequent editions.

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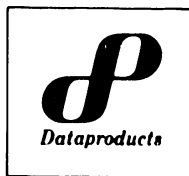
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**B-SERIES
MASTER SUPPORT
AND
LOGISTICS MANUAL**

VOLUME I

**300 LPM, 600 LPM,
AND
1000 LPM
LINE PRINTERS**

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6200 CANOGA AVENUE
WOODLAND HILLS, CALIFORNIA 91365

GENERAL DESCRIPTION

THEORY OF OPERATION

MAINTENANCE

NOVEMBER, 1982

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RELATED PUBLICATIONS

<u>Title</u>	<u>Publication Number</u>
Operator's Guide, B-Series Line Printers, Models 300 LPM/600 LPM	255136
Operator's Guide, B-Series Line Printers, with Acoustic Cabinet	267720
Maintenance Guide, B-Series Line Printers, Models 300 LPM/600 LPM	255137
Maintenance Guide, B-Series Line Printers, Models 300 LPM/600 LPM, with Acoustic Cabinet	267714
Maintenance Guide, B-Series Line Printers, Model 1000 LPM	267701
Schematics Package, B-Series Line Printers, Models 300 LPM/600 LPM	255122
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SECTION
I
GENERAL
DESCRIP-
TION

SECTION I

GENERAL DESCRIPTION

1.1 INTRODUCTION

The B-Series Band Printers, manufactured by Dataproducts Corporation in Woodland Hills, California, are medium speed, impact-type, solid font line printers that utilize a continuous character band. The Master Support and Logistics Manual describes the three printers (300 LPM, 600 LPM, and 1000 LPM) presently available in this series. See **figures 1-1 through 1-3** for photographs of the three printers available.

1.1.1 Master Support and Logistics Manual Contents and Format

Designed primarily for use by personnel at central depot-level facilities, the Master Support and Logistics Manual provides descriptive and operational information in greater depth and detail than the Operator's Guide and Maintenance Guide currently shipped with a majority of the printers. It is divided into two (2) volumes with a comprehensive alphabetical index in volume II. Volume I consists of the following sections:

- Section I - General Description
- Section II - Theory of Operation
- Section III - Maintenance
- Alphabetical Index

Volume II includes the following sections:

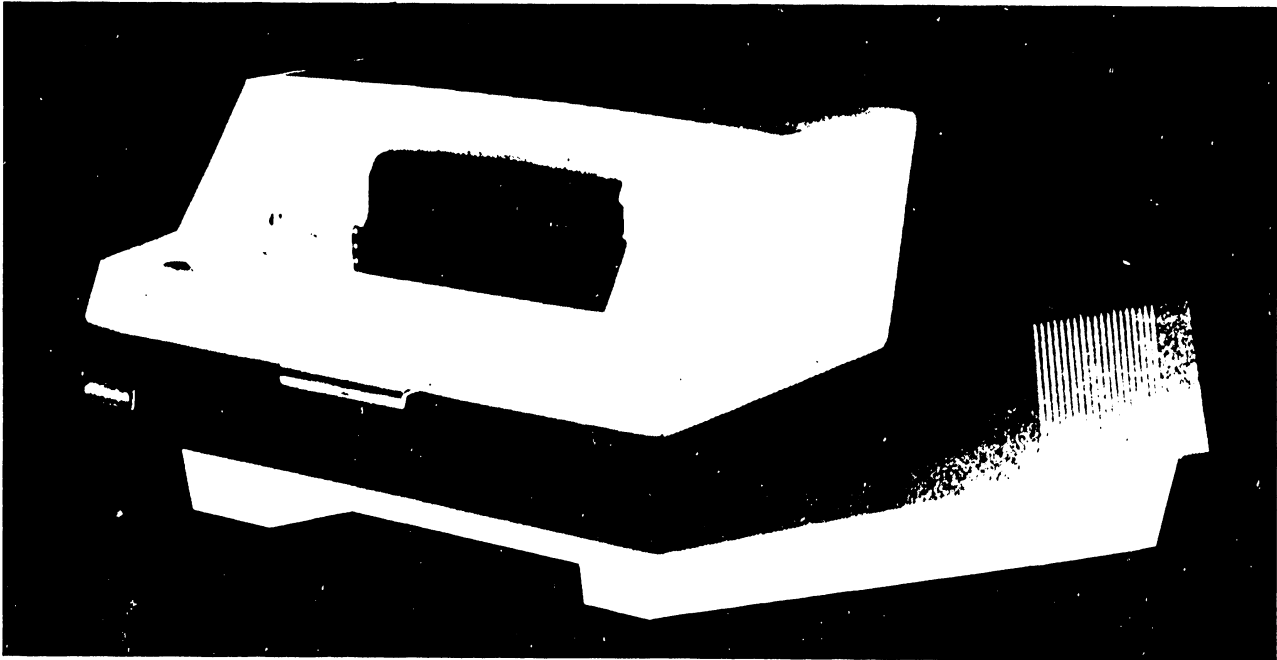
- Section IV - Troubleshooting
- Section V - Logic Diagrams
- Section VI - Illustrated Parts Lists
- Alphabetical Index

1.1.2 Section Contents

This section provides general background information on printer design, purpose and operation. The operation of major assemblies and subassemblies are discussed and available options and accessories are described.

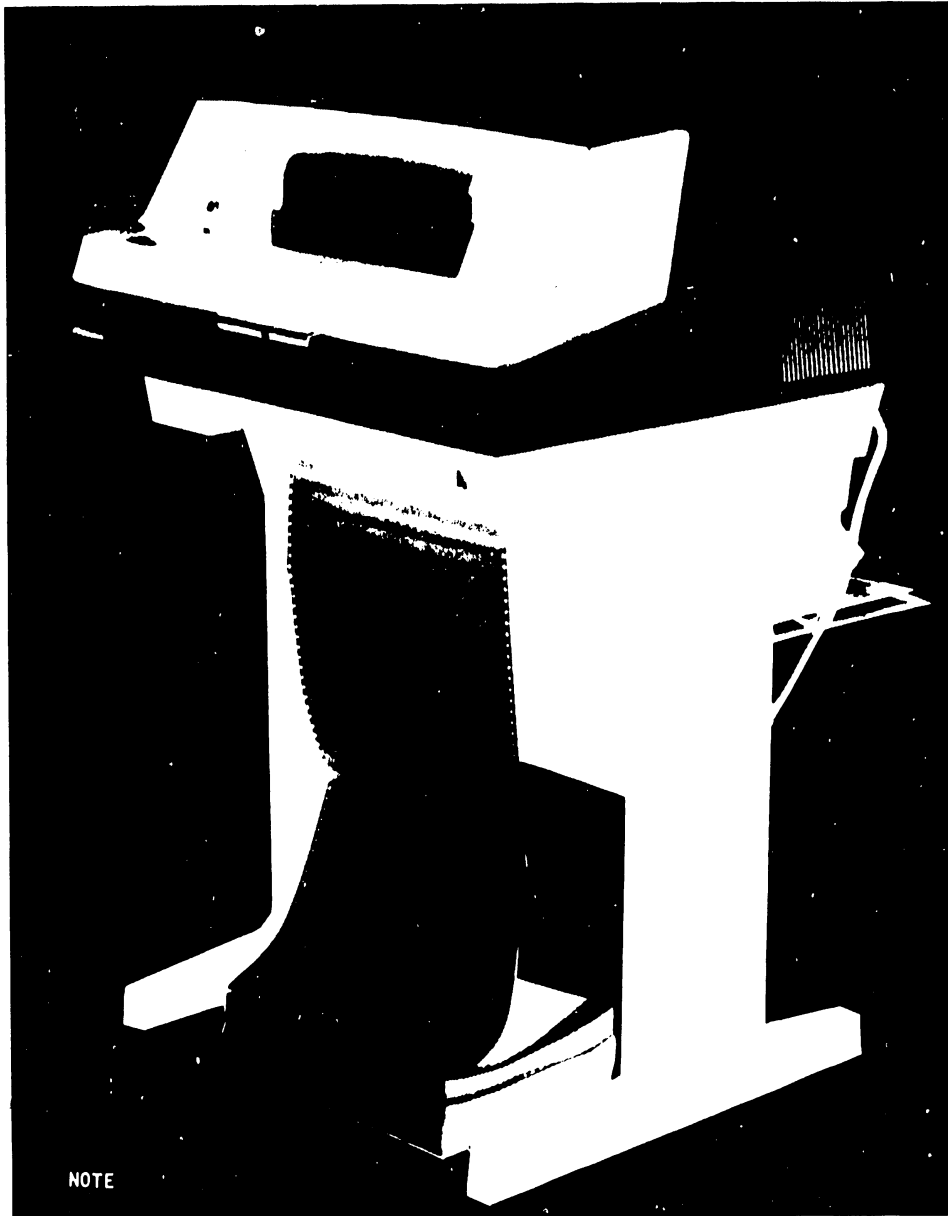
1.2 PRINTER DESIGN

The B-Series printers are compact, horizontal font, 132 column impact printers designed to provide a minimum throughput of 285 lines per minute for the 300 LPM model, 650 for the 600 LPM model, and 1000 for the 1000 LPM model when using a standard 64-character ASCII set. The operator-changeable font carrier (hereafter referred to as the character band) consists of a continuous steel band



255136.107

Figure 1-1. 300 LPM Printer

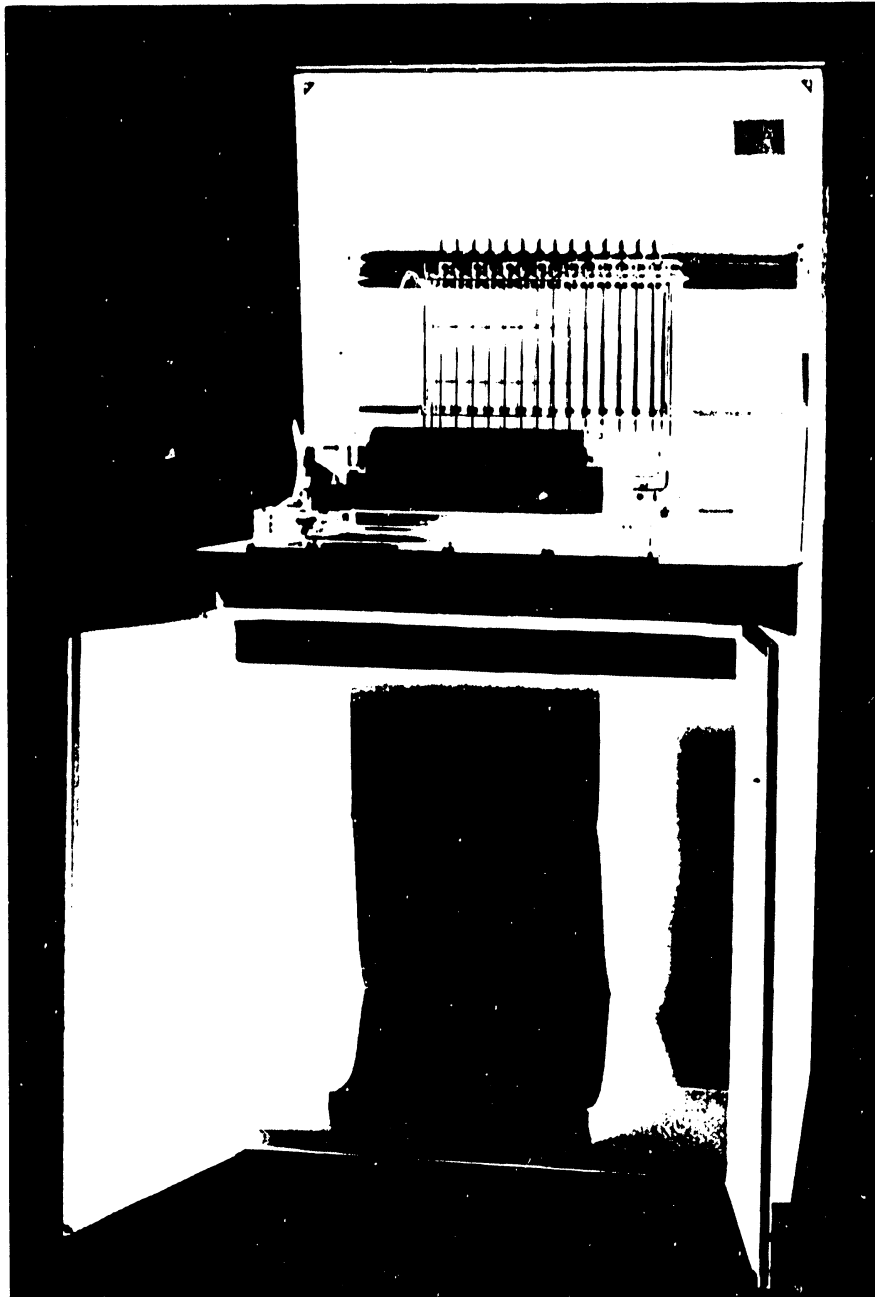


NOTE

THE PEDESTAL IS AN OPTIONAL ACCESSORY FOR THE 300 LPM PRINTER. THE STANDARD 600 LPM PRINTER IS SHIPPED WITH THE PEDESTAL, BUT MAY BE TABLE-MOUNTED.

255137.106

Figure 1-2. 600 LPM Printer with Pedestal (Front View)



NOTE: AS AN OPTION, THE
300 LPM AND 600 LPM
MAY BE ORDERED MOUNTED
IN THE ACOUSTIC CABINET.

255176.103

Figure 1-3. 1000 LPM Printer with Acoustic Cabinet

containing 208 characters for the 300 LPM and 416 characters for the 600 LPM and 1000 LPM printers. A variety of options and accessories are available to efficiently configure the printers to meet specific application requirements.

1.2.1 Purpose

The B-Series printers are general purpose output devices for use on electronic information-processing systems, such as small business applications, data communications/data entry terminals, and dedicated minicomputer based systems, where reliable operation in a heavy duty cycle environment is needed. The built-in self test and diagnostic display are designed to maximize the operator's capacity to maintain the printer and to reduce field maintenance expense.

1.2.2 Organization

The basic printer consists of seven (7) major assemblies and their related subassemblies. Each of the major assemblies is fully described in **paragraph 1.3**. **Figures 1-4 through 1-6** provide assembly block diagrams for the 300 LPM and 600 LPM printers without the acoustic cabinet, the 300 LPM and 600 LPM printers with the acoustic cabinet, and the 1000 LPM printer which is available only with the acoustic cabinet.

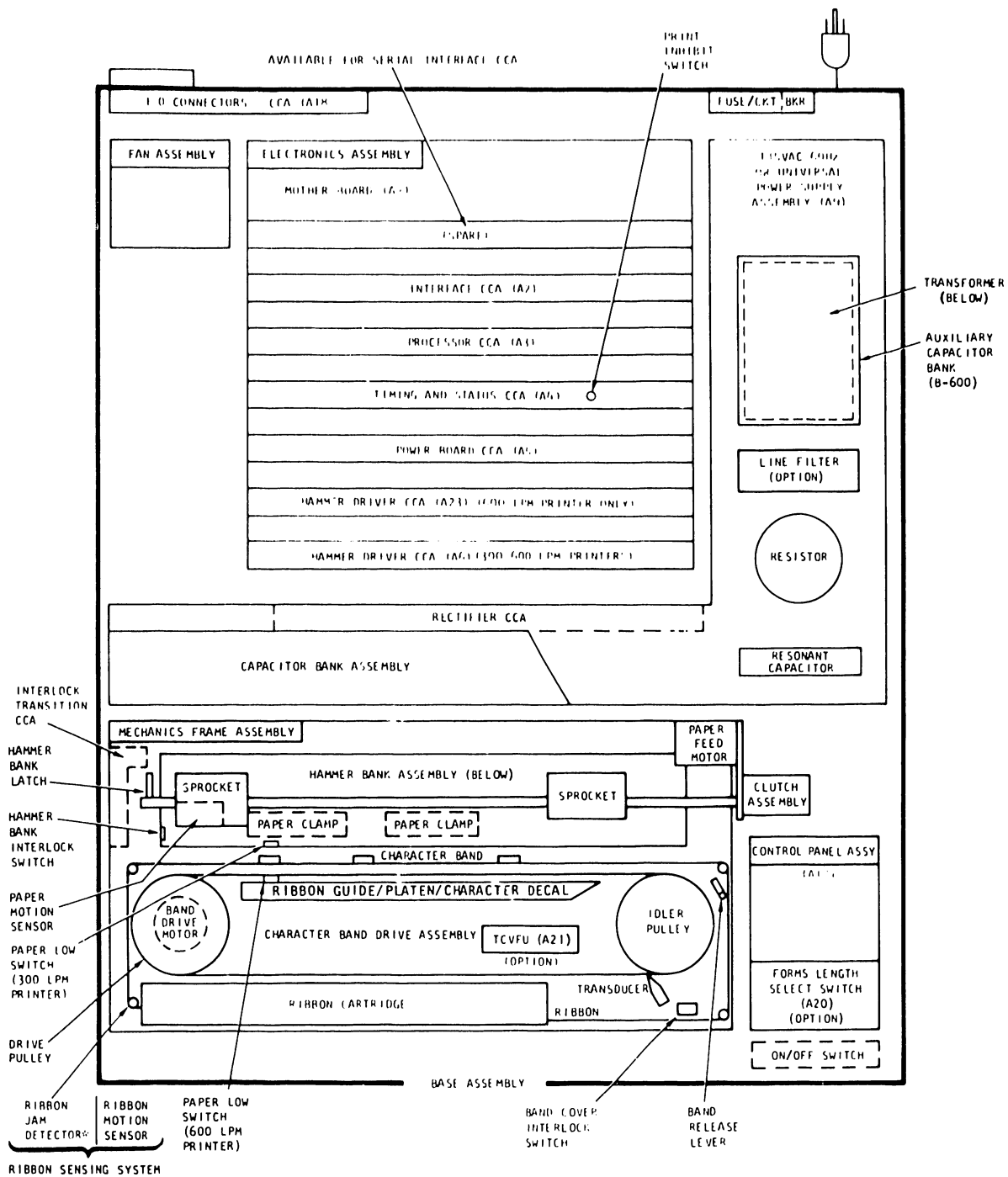
1.2.3 System Overview

The printer system, comprised of the assemblies described in **paragraph 3.1**, accepts user data, processes the data for a line of print, prints the data and moves paper according to a programmed format. A dedicated microprocessor contained on the Processor CCA controls the logical, electrical and mechanical functions of the printer and provides diagnostic testing to detect and indicate malfunctions. **Figure 1-7** furnishes an overview of the printer system in block diagram format.

Communication between the user system and the standard printer depends on an interlocked "handshaking" arrangement. After the printer has been powered up, is ready, and is placed on line, it informs the user that it is on line and ready to receive data, which it subsequently demands by raising the demand transmission line. The user system acknowledges the demand by transmitting a data or control character and a strobe or timing signal that dictates when the character should be accepted.

The printer responds to the user input by dropping its demand and accepting the data or control character. After accepting the user input, the printer loads it into memory and repeats its demand for data.

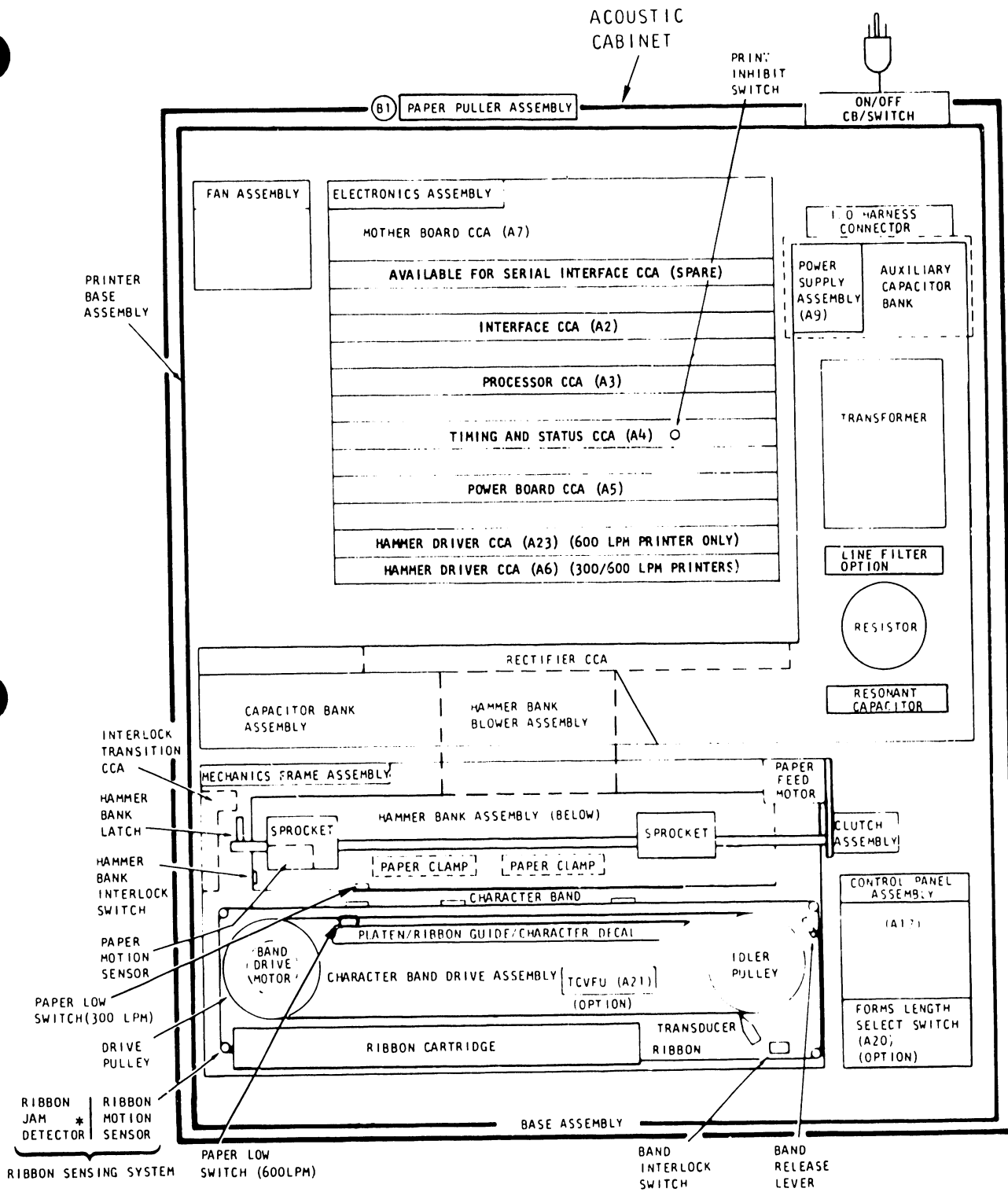
This handshaking process continues until the user transmits a control character which defines the previous data as a line of print. The printer then terminates its interfacing with the user system and proceeds to perform a series of programmed routines which will produce a line of print. These routines include Idle, Load, Edit, Print, Format, and Move Paper. A System Status Check routine periodically monitors the printer's condition in order to report any status change or fault which might interfere with printer operation. Detailed explanations of the program routines can be found in **paragraph 2.6**.



*(POSITIVE SYSTEMS ONLY)

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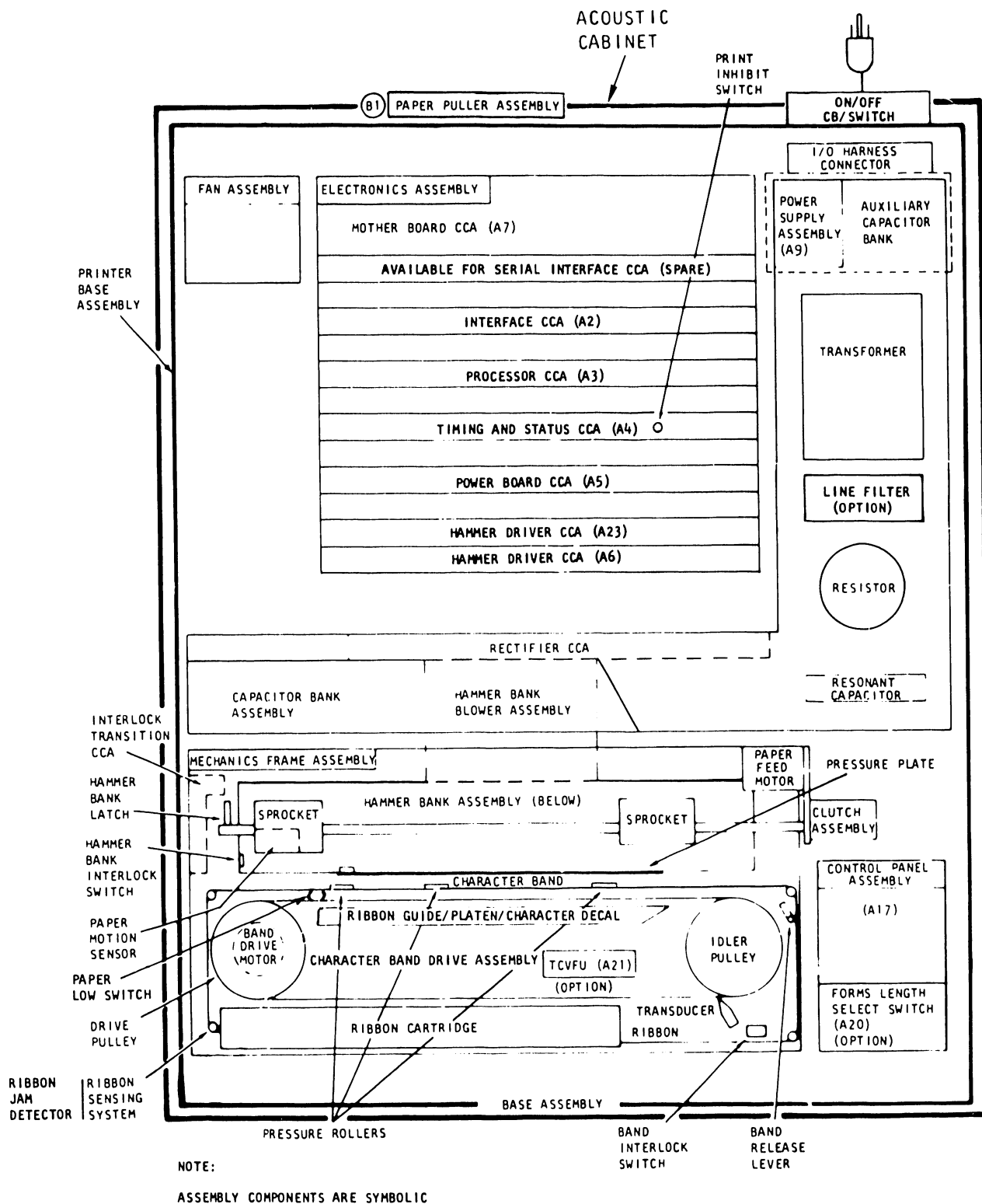
Figure 1-4. 300/600 LPM Printer without Acoustic Cabinet
Major Assemblies and Subassemblies Block Diagram



* (POSIDRIVE SYSTEM ONLY)

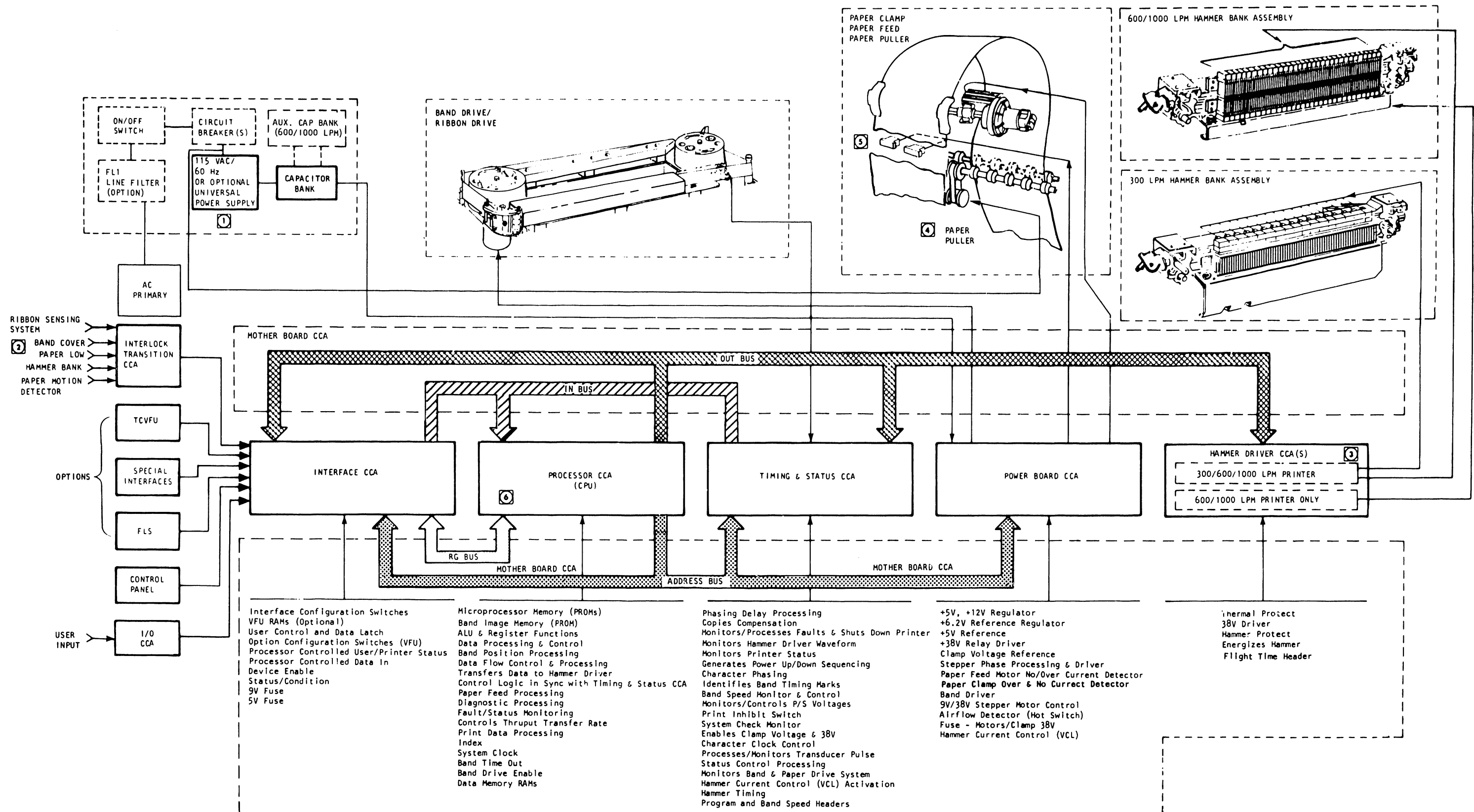
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Figure 1-5. 300/600 LPM Printer with Acoustic Cabinet
Major Assemblies and Subassemblies Block Diagram



245059.106

Figure 1-6. 1000 LPM Printer Major Assemblies and Subassemblies Block Diagram



- ① UNIVERSAL POWER SUPPLY STANDARD FOR 1000 LPM PRINTERS.
- ② RIBBON SENSING SYSTEM CONSISTS OF RIBBON MOTION SENSOR AND RIBBON JAM DETECTOR ON POSIDRIVE SYSTEMS.
- ③ 300 LPM USES ONE HAMMER DRIVER CCA; 600 LPM AND 1000 LPM USE TWO HAMMER DRIVER CCAS.

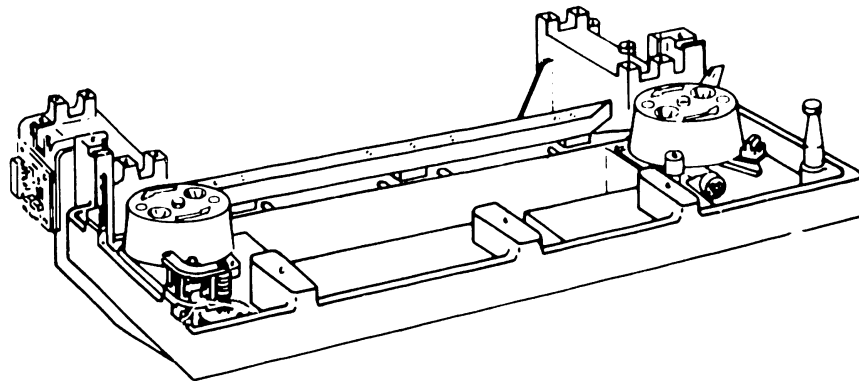
- ④ PAPER PULLER ASSEMBLY INSTALLED ONLY WHEN PRINTER IS MOUNTED IN THE ACOUSTIC CABINET.
- ⑤ PAPER CLAMPS REPLACED BY ROLLER THROAT AND PRESSURE PLATE IN 1000 LPM.
- ⑥ THE 1000 LPM PRINTER USES A 24-BIT PROCESSOR CCA.

Figure 1-7. Printer System Overview Block Diagram

1.3 ASSEMBLY DESCRIPTION

The assemblies described in the following paragraphs are the major functional components of the printer system. Illustrations and parts lists are provided in section VI of volume II.

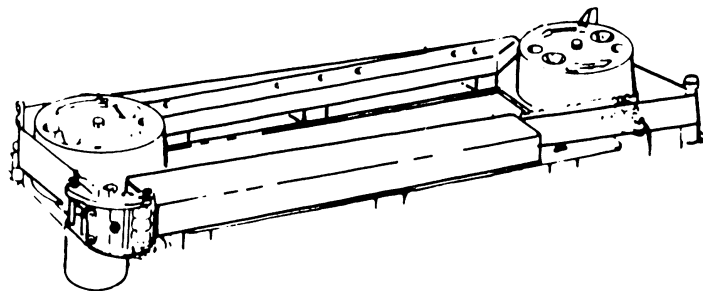
1.3.1 Mechanics Frame Assembly



The Mechanics Frame Assembly includes the Character Band/Ribbon Drive Assemblies, the Platen and the Interlock System Circuit Card Assembly, which are engaged in the mechanical tasks of moving the character band, moving the ribbon, sensing the character position, and monitoring the interlock system switches and sensors. At the present time, one of two (2) alternate Mechanic Frame Assemblies are used in 300 LPM and 600 LPM model printers. The differences between the two are most obvious in the type of character band/ribbon drive assembly installed. Each assembly is described below.

a. Character Band/Ribbon Drive Assemblies

The character band and ribbon drive components form a single subassembly with the ribbon cartridge acting as a slave to the character band drive. Movement of the ribbon is achieved with a capstan roller coupled to the band drive motor shaft. At the present time, two types of character band/ribbon drive systems may be installed in the printers. Their differences are noted in the descriptions which follow; the function of the two systems is identical.



1. Character Band Drive System- The character band drive system consists of a DC motor, a drive pulley, an idler pulley, two edge guide bearings, a character band, and a protective band cover. The DC motor is coupled directly to the drive pulley and causes the band to rotate in a counterclockwise direction at a constant velocity. The character band is mounted over the tapered drive and idler pulleys and is biased downward to ride lightly on the edge guide bearings.

The major differences between the two band drive assemblies currently installed in the B-Series printers are in the mounting of the band drive motor, the band drive motor itself, and in the construction of the drive and idler pulleys. In one, the band drive motor is fixed in the Mechanics Frame Assembly, and the band drive and idler pulleys are of solid two piece construction. This system is referred to as the O-Ring assemblies system.

In the other band drive assembly, the band drive motor and idler yoke are trunnion-mounted, and the drive and idler pulleys are solid, single piece units. This system is referred to as the Posidrive assemblies system and is installed in all 1000 LPM model printers and most later model 300 LPM and 600 LPM printers. **Figures 1-8 and 1-9** illustrate the alternate band drive assemblies.

The operator-changeable character band is a continuous steel band with raised characters and timing, index and identification marks. Perforations above and between characters provide minimum stress relief and give the top edge a scalloped appearance. An eccentric on the idler pulley allows the operator to release tension on the band for band replacement. The band transducer senses the character band identification, timing and index marks and generates a signal to the Timing and Status CCA during band motion.

2. Ribbon Drive System - The ribbon drive system consists of the ribbon cartridge, drive rollers, ribbon motion sensor, and ribbon guides. The ribbon cartridge contains a continuous loop of ribbon and snaps onto the ribbon cartridge locating buttons on the band drive casting. Ribbon is then fed around the ribbon guides, past the print station, and through the Ribbon Pivot Arm Assembly which contains the ribbon motion sensor and the ribbon rollers.

Ribbon drive is achieved by the belt-coupling of the ribbon capstan roller to the band drive motor shaft. Ribbon drive operates as a slave to the band drive and causes the ribbon to move simultaneously with the band. The driven capstan roller, along with the contra-rotating idler roller, pulls the ribbon past the print station and compresses it in even folds into the ribbon cartridge. A ribbon motion sensor located in the Ribbon Pivot Arm Assembly monitors ribbon motion.

Alternate ribbon drive systems exist for the 300 LPM and 600 LPM model printers. **Figures 1-8 and 1-9** illustrate the components of the two systems. The O-ring system uses a clear composition O-ring belt to drive the ribbon capstan roller. The Posidrive system uses a toothed drive belt, a roller arm to provide tension on the drive belt, and a microswitch to detect ribbon jams. All 1000 LPM models and most later model 300 LPM and 600 LPM printers have the Posidrive system installed.

IDLER
SHAFT
ASSEMBLY



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BAND DRIVE
MOTOR ASSEMBLY

RIBBON DRIVE
O-RING

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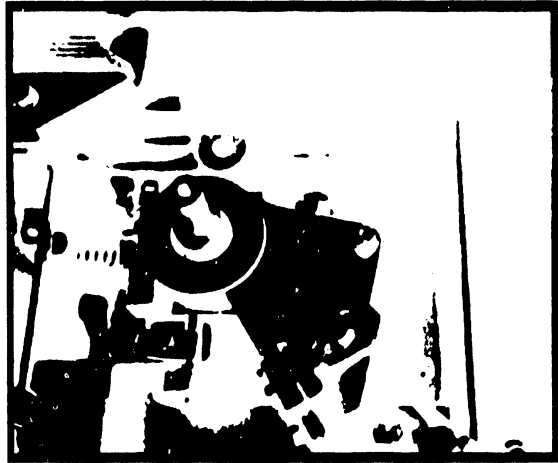
BAND
PULLEY
ASSEMBLY



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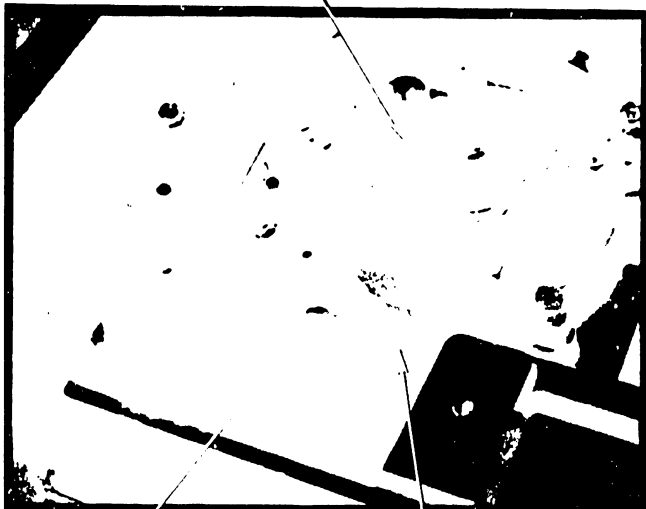
Figure 1-8. O-Ring Band Drive/Ribbon Drive Assembly

IDLER
SHAFT
ASSEMBLY



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BAND DRIVE
MOTOR ASSEMBLY

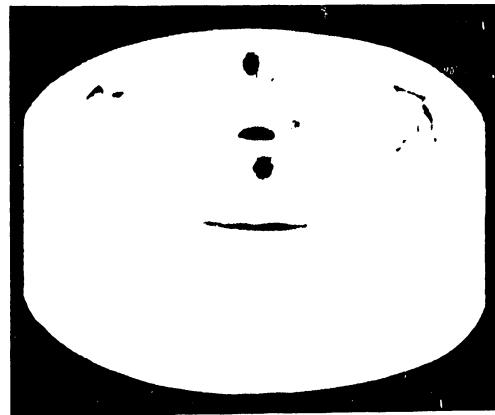


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RIBBON DRIVE
ASSEMBLY
WITH PIVOT ARM

RIBBON
DRIVE
BELT

BAND
PULLEY
ASSEMBLY



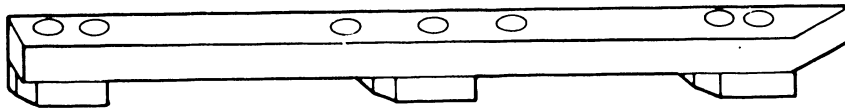
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Figure 1-9. Posidrive Band Drive/Ribbon Drive Assembly

The ribbon consists of a continuous loop of ink-impregnated nylon contained in a cartridge capable of storing the total length of the ribbon except that portion which is passing in front of the print station. The cartridge is held in place by the tension of preformed, snap action, button receptacles molded into the bottom of the cartridge. The button receptacles mate with two metal buttons mounted to the band casting.

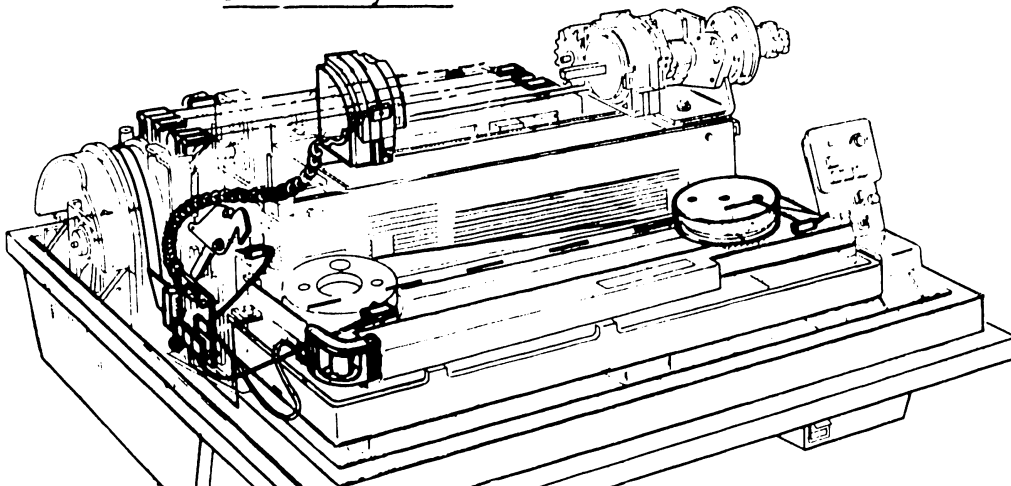
The ribbon is guided diagonally across the print station in a path determined by a ribbon guide mounted to the platen and by fixed position guides attached to the printer frame. The ribbon guide and a ribbon mask attached to the platen minimize the possibility of extraneous ink smear on paper forms.

b. Platen



The platen is a hard, chrome-plated or vespel-lined, machined steel bar precisely set on the band deck casting. It serves as a guide and impact surface when the hammer strikes against the character band during the printing operation. The position of the platen determines the throat opening for the paper path and provides a base line for setting the hammer flight time. Once adjusted, the platen should not be removed or readjusted except at a properly equipped repair depot.

c. Interlock System



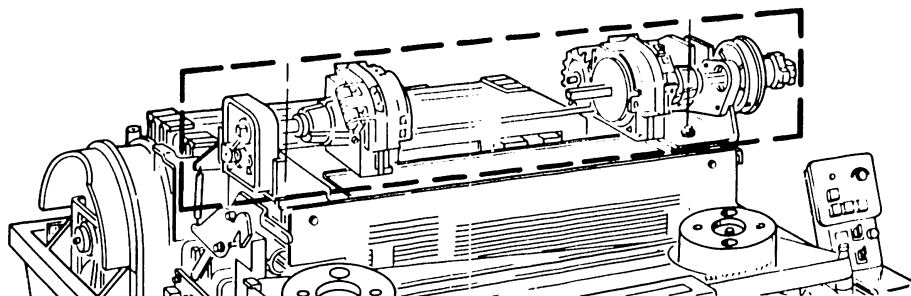
The Interlock System consists of the Interlock Transition CCA, the band cover interlock, the hammer bank interlock, the paper low switch, the paper motion sensor, and the Ribbon Sensing System. The system functions to alert the printer to a number of mechanical faults which will prevent its operation.

The Interlock Transition CCA is mounted on the Mechanics Frame Assembly to the left of the Hammer Bank Assembly. All system switches and sensors are channelled through it to the Interface CCA. The following conditions cause the control panel status indicators to display a fault code for operator interpretation and intervention: an untensioned band, an open band cover or hammer bank, printer out of paper, and lack of ribbon motion or paper motion. The Posidrive system provides an additional microswitch in the Ribbon Sensing System to detect ribbon jam.

1.3.2 Paper Feed/Paper Clamp Assemblies

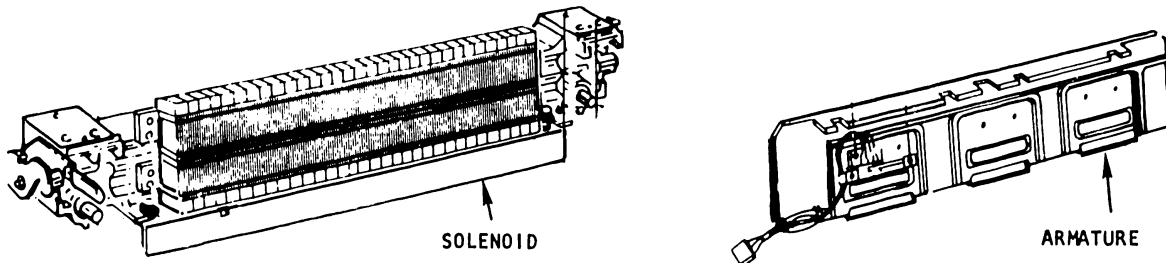
The Paper Feed and Paper Clamp Assemblies are those assemblies concerned with moving and holding the paper forms. All 1000 LPM model printers, and those 300 LPM and 600 LPM models installed in acoustic cabinets, have an additional Paper Puller Assembly to assist in uniformly feeding paper to the rear of the printer. The Paper Feed Assembly is mounted on top of the Hammer Bank Assembly, and the Paper Clamp Assembly is mounted beneath the hammer bank and the platen.

a. Paper Feed Assembly

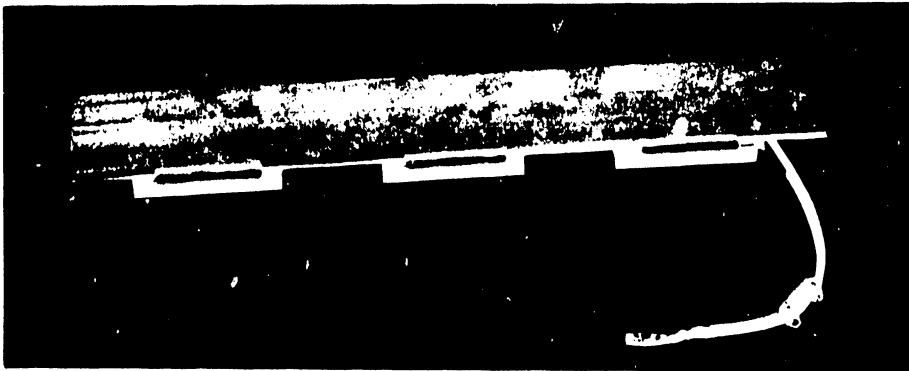


The Paper Feed Assembly consists of two (2) pin feed sprockets mounted on a drive shaft and a phase-controlled stepper motor connected to the drive shaft clutch assembly by a toothed timing drive belt. Under microprocessor control, the stepper motor advances paper forms at either single or multiple line rates. When the printer is on line, paper movement is initiated automatically when data line instruction commands, LF, FF, CR, are received by the printer. When the printer is off line, the operator can single step or slew paper by momentarily pressing the control panel PAPER STEP or TOP OF FORM switches.

b. Paper Clamp Assembly/Pressure Roller Assembly



The Paper Clamp Assembly consists of a Solenoid Clamp Assembly mounted beneath the Hammer Bank Assembly and an Armature Clamp Assembly installed beneath the platen. The armature clamps are spring-loaded and positioned to maintain a slight constant tension on the paper within the print station. The clamps are electromagnetically energized by the solenoids during the print routine to prevent blousing of multipart forms and lateral paper movement.



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The 1000 LPM model printers are equipped with a Pressure Roller Assembly and a pressure plate in place of the armature clamps and solenoids used in the 300 LPM and 600 LPM printers. The Pressure Roller Assembly is positioned beneath the platen, and under normal conditions, will never need readjustment. The pressure plate is installed beneath the Hammer Bank Assembly and adjusted to provide 500 to 750 grams of pull-through force upon the paper. No electrical current is required by this type of assembly.

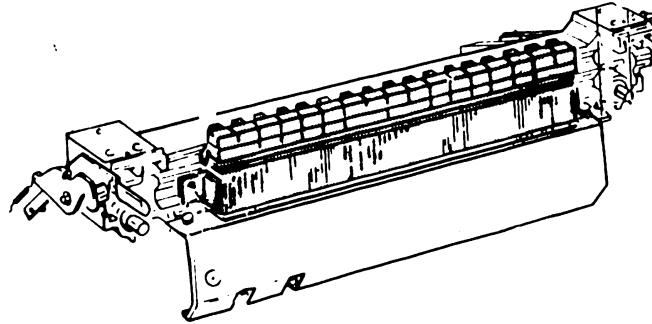
Forms are loaded from the bottom of the printer, up through the paper throat (between the platen and the hammer bank mask), and over the two (2) pin feed sprockets on the paper feed drive shaft. A Paper Support Assembly guides the paper to the paper exit at the rear of the printer. The 1000 LPM, and the 300 LPM and 600 LPM printers in acoustic cabinets, are provided with a Paper Puller Assembly. Five (5) individual, easily released rollers are used to vary tension on the paper and to ensure that forms are uniformly fed into the rear cabinet compartment.

A paper motion sensor mounted on the left hand pin feed sprocket detects lack of form motion. The paper low switch, located in the paper throat, detects paper low conditions.

1.3.3 Hammer Bank Assembly

The Hammer Bank Assembly, the Hammer Driver CCA(s), the platen, and the character band provide the mechanics for carrying out the print operation. The 300 LPM hammer bank differs from the 600 LPM and 1000 LPM hammer bank; the characteristics of each are described below.

a. 300 LPM Hammer Bank Assembly

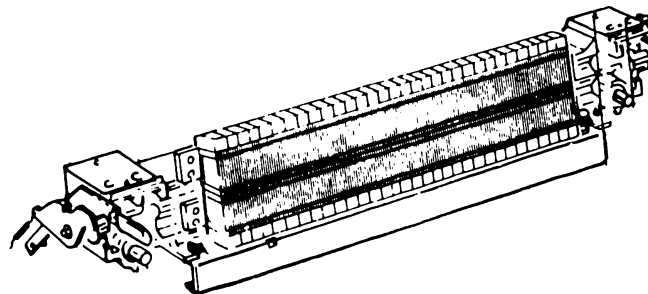


The 300 LPM Hammer Bank Assembly consists of 17 hammer modules interleaved with 17 permanent magnet modules and mounted on a common frame. There are four (4) double column spanning hammers on each of the modules. The hammer coils or flags are positioned in the gaps between the magnets. Upon application of coil current, the hammer is driven out of its slot to impact the paper for an upon the ribbon and the character band. The platen serves as a back stop for the band.

Each hammer's flight time (from excitation to impact) is determined by its interacting backstop screw located in the rear of the hammer bank. A single Hammer Driver CCA located in the electronic assembly card cage contains the current drivers for the hammers.

In the standard mode of operation (10 characters per inch), one hammer spans two column positions for a total of 132 columns. In the optional 15 characters per inch, one hammer spans three column positions. An optional 136 column printout is also available.

b. 600 LPM and 1000 LPM Hammer Bank Assembly

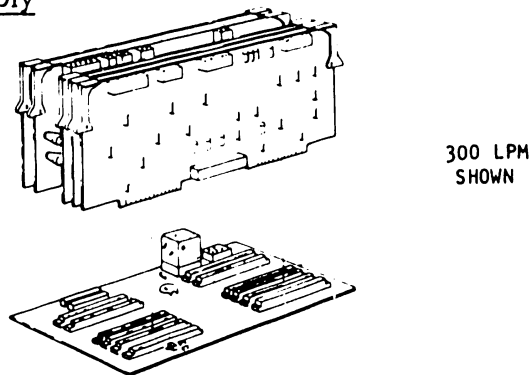


The 600 LPM and 1000 LPM Hammer Bank Assembly consists of an upper and a lower hammer bank. Each bank is made up of 17 hammer modules interleaved with 17 permanent magnet modules. There are four (4) single column spanning hammers on each of the 17 upper and 17 lower modules (34 total). The hammer coils are positioned in the gaps between the magnets. The two banks are fastened together with the hammers aligned horizontally for the odd/even print column registration. The upper bank contains the hammers for the even numbered print columns; the lower bank contains those for the odd numbered print columns.

Two Hammer Driver CCAs, located in the electronic assembly card cage, contain the current drivers for the hammers. Current is carried through the flexure springs of the hammer to its coil where the magnetic field interacts to drive the hammer toward the character band. When the current is removed, the flexure springs return the hammer to a rest position against the adjustable back-stop screw which determines the flight time of the hammer.

The 600 LPM and 1000 LPM model printers are equipped only for the standard 10 characters per inch mode of operation. A separate hammer is provided for each print column. The optional 136 column printout is made available by using two (2) Hammer Driver CCAs that contain extra current drivers for the extra columns.

1.3.4 Electronics Assembly



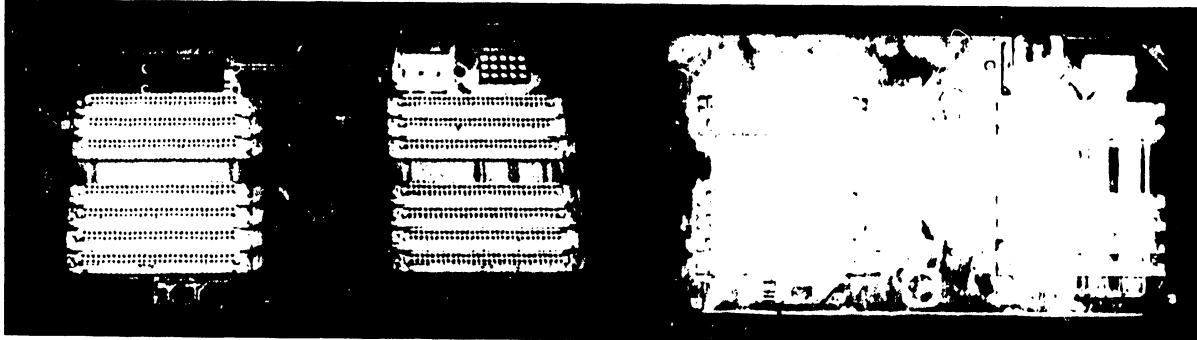
The standard Electronics Assembly (depending upon printer model) consists of five (5) or six (6) circuit card assemblies plugged into a Mother Board CCA and held in place by vertical guides. Ejector keys, attached to each CCA, aid in their removal from the Mother Board CCA connectors.

Circuitry on the circuit card assemblies processes the user data and signals, and generates internal signals to produce band/ribbon drive, paper motion, and hammer firing. **Table 1-1** lists the standard card complement for each of the printer models. The detailed operation of the CCAs is discussed in section II.

TABLE 1-1. ELECTRONICS ASSEMBLY, STANDARD CIRCUIT CARD COMPLEMENT

Circuit Card Assembly	Ref. Design.	300 LPM	600 LPM	1000 LPM
Mother Board (300 LPM)	A7	X		
Mother Board (600/1000 LPM)	A7		X	X
Interface	A2	X	X	X
20-Bit Processor	A3	X	X	
24-Bit Processor	A3			X
Timing and Status	A4	X	X	X
Power Board	A5	X	X	X
Hammer Driver	A6	X	X	X
Hammer Driver	A23		X	X

a. Mother Board CCA

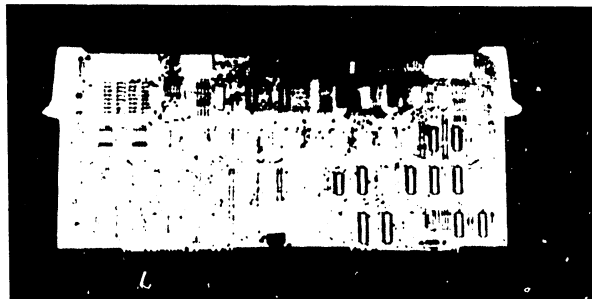


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The Mother Board CCA functions as a common bus for the transmission of required voltages and signals to and between circuit card assemblies. Two different Mother Board CCAs are used in the B-Series printers. The 300 LPM model circuit card contains six (6) pairs of 60-pin edge card connectors, XA1-XA6, into which the Electronic Assembly circuit cards are plugged. The 600 LPM and 1000 LPM circuit card contains seven (7) pairs of 60-pin edge card connectors, XA1-XA6 and XA23. The XA1 slot is reserved as a spare for use with the optional serial interface and other special customer configurations. A relay to transfer the +38 volts is also mounted on the Mother Board CCA, and connectors are provided for Capacitor Bank Harness Assembly and the optional Elapsed Time Meter Assembly.

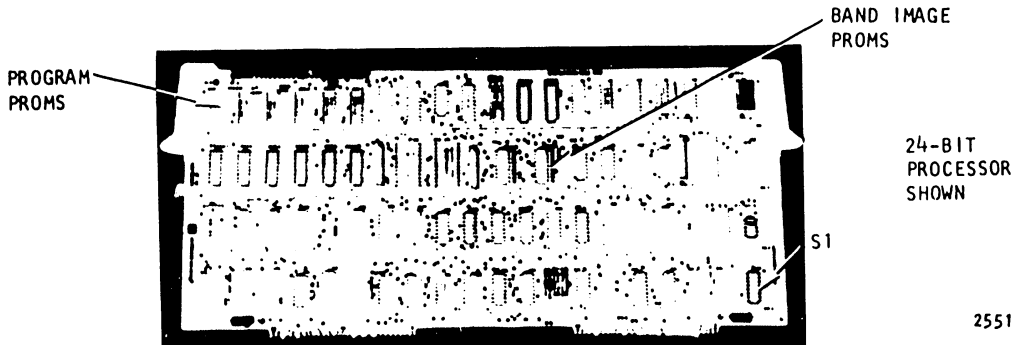
b. Interface CCA



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The Interface CCA acts as an input/output buffer to the Processor CCA for the user system, the control panel, the system interlocks, and the optional Forms Length Selector Assembly, Tape Controlled Vertical Format Unit (TCVFU) and the Direct Access Vertical Format Unit (DAVFU). A variety of logic and format options are made available by two (2) configuration switches mounted on the circuit card. Four (4) configuration switches are used when a VFU option is installed.

c. Processor CCA

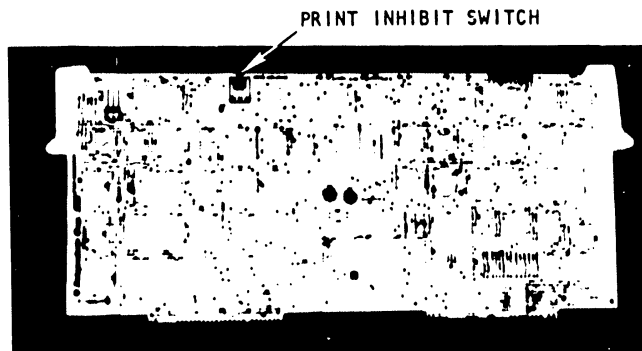


The Processor CCA functions as the computing center of the printer system and directs the printer to execute its program instructions. PROMs installed on the circuit card house the master program. Five (5) program PROMs are used in the 300 LPM and 600 LPM model printers. The 24-bit Processor CCA, used in the 1000 LPM printer, requires six (6) PROMs and has sockets for six (6) additional PROMs to meet special programming requirements.

Sockets are provided for three (3) additional PROMs which supply band image information. At least one band image PROM must be installed, and its band image code must match the code etched on the character band for the printer to initialize.

In addition, a switch (S1), mounted on the circuit card, provides for variable band time-out. Band time-out is the number of revolutions of the character band which occur between the time printable data is received and the time the band drive system is disabled because no further printable data has been transmitted.

d. Timing and Status CCA



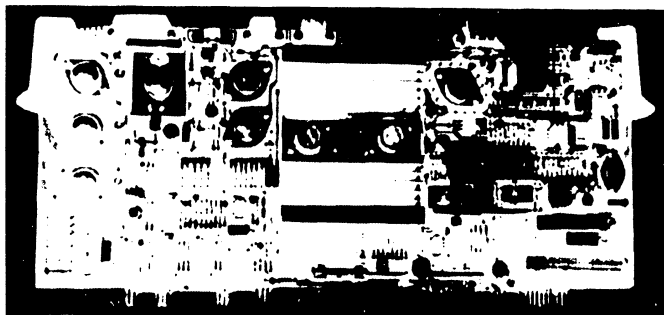
The Timing and Status CCA functions as an intermediary and monitor for the Processor CCA. It notifies the Processor CCA and the Power Board CCA of the presence or loss of power by generating the power up and power down reset sequences of the printer system. As an intermediary between the analog band drive system and the digital control of the Processor CCA, it amplifies and digitizes the transducer (character band sensor) input to provide the time base required to control hammer fire. Band speed is monitored and controlled by the high speed clock of the Processor CCA in conjunction with the band timing clock.

Status changes related to the power supply voltages, the transducer, the band drive, hammer fire, and the paper feed drive are reported to the Processor CCA for interpretation and reaction. The Timing and Status CCA will override all processor controls and automatically shut down the printer system, if monitoring of the airflow, the 5 volts or the system clock indicates a fault condition.

In addition, timing and status circuitry provides for character phasing and copies compensation for optimum print output. Under program direction, correct column spacing control is furnished for the 300 LPM model printers which have double spanning hammers and the 10/15 character per inch option. The circuitry is disabled in 600 LPM and 1000 LPM model printers which use single column spanning hammers. Changeable band speed and program headers, installed on the circuit card, program the printer for 300 LPM, 600 LPM, or 1000 LPM operation.

A print inhibit switch, mounted on the circuit card, can be used to disable the paper faults and the hammer driver(s), and prevent firing of hammers. Since the printer continues to function, the print inhibit mode is useful for most maintenance and troubleshooting procedures.

e. Power Board CCA



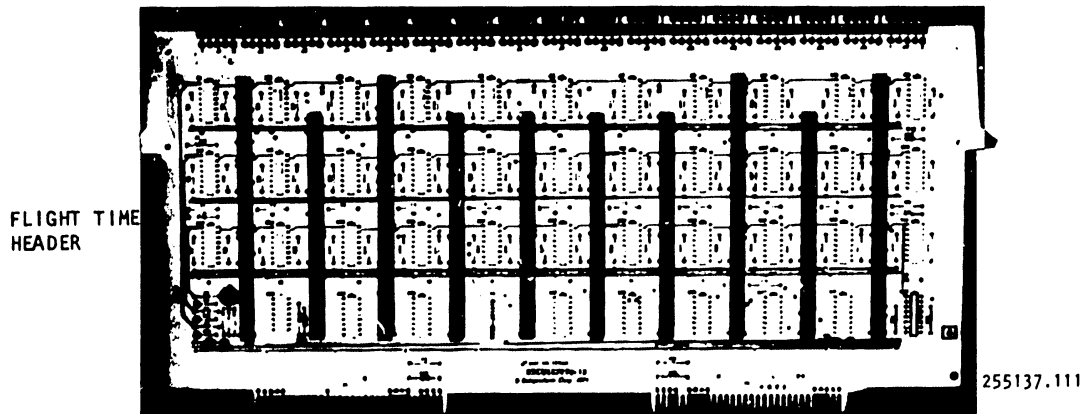
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The Power Board CCA interfaces the Processor CCA to the paper feed drive system and the Timing and Status CCA to the band drive system. It also provides regulated voltages to the printer's analog and digital circuits. By monitoring all voltages, it protects against over-voltage and over-current conditions in the printer system. An air flow monitor senses the presence of moving air within the electronics assembly and signals the Timing and Status CCA when airflow drops below a specified minimum. Regulated voltages are then shut down.

By varying the VCL output in accordance with the control panel copies potentiometer, the current to the hammer drivers, and thus the impact energy of the hammers, is regulated for penetration control.

In 300 LPM and 600 LPM model printers, the two (2) paper clamp solenoid assemblies are plugged into the Power Board CCA. Under program control, the Power Board CCA turns the clamp solenoids on or off as required during the printing and move paper sequences. The 1000 LPM model printer's paper throat assembly requires no electrical connections or control.

f. Hammer Driver CCA



The Hammer Driver CCA is the interface between the Processor CCA and the hammer bank. It contains the circuitry for firing the hammers and detecting hammer misfire. Print data from the Processor CCA is latched and decoded to enable selected hammers to fire. A header, plugged into a socket on the CCA, controls hammer flight time.

The 300 LPM printer has only one (1) Hammer Driver CCA installed in the electronic assembly card cage. The 600 LPM and 1000 LPM printers use two (2) CCAs, one for the upper hammers (A23) and one for the lower hammers (A6). The connectors for the hammer modules are mounted on the top edge of the Hammer Driver CCAs. White and blue module connectors are used to distinguish between upper and lower modules in the 600 LPM and 1000 LPM printers.

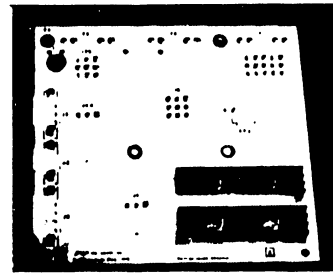
1.3.5 Power Supply

The power requirements of the printer system are met by the Power Supply Assembly which provides the following output voltages: Raw +38V, +38V, +9V, -9V, and +9VEW (Early Warning). Overload protection is furnished by the circuit breaker(s) and three (3) fuses mounted on the Rectifier CCA. Two assemblies are currently available for B-Series printers--the standard 115 VAC, 60 Hz or a universal power supply (a 300 LPM and 600 LPM option). Component differences between the two assemblies are detailed in the following paragraphs. Operating descriptions can be found in section II. All 1000 LPM models are equipped with the Universal Power Supply Assembly.

a. Standard 115 VAC, 60 Hz Power Supply Assembly



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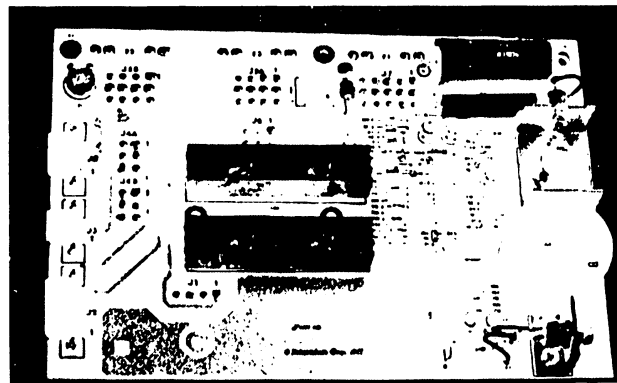
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RECTIFIER CCA

The Standard 115 VAC, 60 Hz Power Supply Assembly requires an input of 90 to 132 VAC at 60 Hz. The assembly consists of a constant voltage transformer, resonant capacitor, 38 volt preload resistor, AC Power switch, a single circuit breaker, a Rectifier CCA, and a Capacitor Bank Assembly. All 600 LPM models are also equipped with an Auxiliary Capacitor Bank Assembly to handle the additional power requirements of the second Hammer Driver CCA.

When 300 LPM or 600 LPM model printers with the standard power supply are installed in the optional acoustic cabinet, the standard switch and circuit breaker are replaced by a combination switch/circuit breaker mounted in the rear of the cabinet. The Hammer Bank Blower Assembly, utilized in acoustic cabinets, derives its power from the Rectifier CCA. Note that the Paper Puller Assembly motor wiring must be compatible with the 115 VAC, 60 Hz input.

b. Universal Power Supply Assembly



RECTIFIER CCA

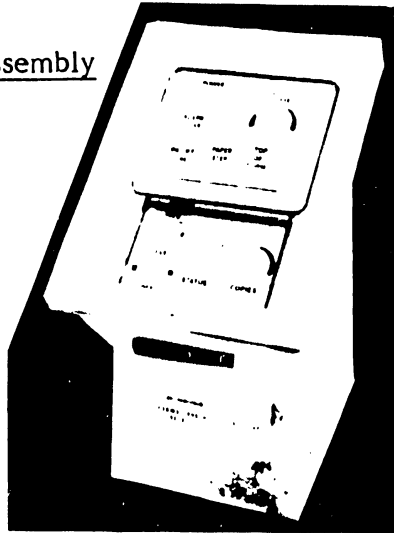
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The Universal Power Supply Assembly is designed to operate with inputs of 115 VAC or 230 VAC and 50 Hz or 60 Hz. The assembly consists of a constant voltage transformer, resonant capacitor, 38 volt preload resistor, AC Power Switch, two (2) circuit breakers, a Universal Rectifier CCA with a 38V regulator, and a Capacitor Bank Assembly. All 600 LPM and 1000 LPM models are also equipped with an Auxiliary Capacitor Bank Assembly. The Universal Power Supply Assembly is a standard feature on 1000 LPM printers.

Double sets of plugs and jacks are provided with the universal power supply transformer and Rectifier CCA to accommodate the four (4) combinations of input voltage and frequency. For all printers installed in acoustic cabinets, a reconfiguration of the power supply requires reconfiguration of the Paper Puller Assembly motor wiring to the same voltage and frequency.

When 300 LPM or 600 LPM printers with the universal power supply are installed in the optional acoustic cabinet, the standard switch and circuit breakers are replaced by a combination switch/circuit breaker mounted in the rear of the printer. The cabinet's Hammer Bank Blower Assembly is plugged into the Rectifier CCA.

1.3.6 Control Panel Assembly

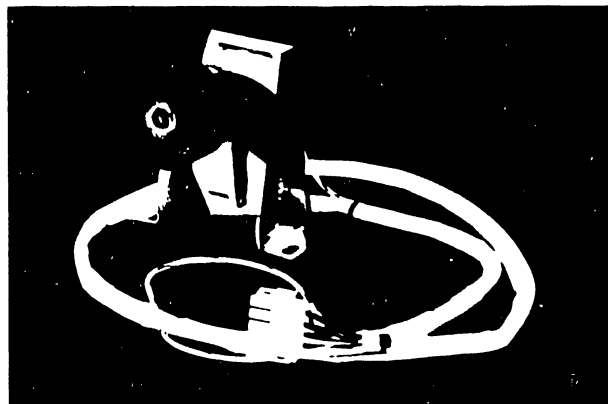


ACOUSTIC
CABINET
CONTROL
PANEL
SHOWN

267700.146

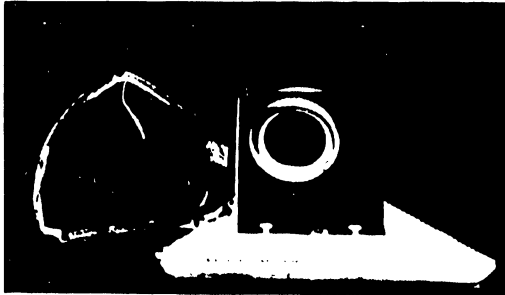
Operator monitoring and control of the printer is aided by the indicators, switches and potentiometers mounted on the Control Panel Assembly. The POWER indicator, ON/OFF LINE switch/indicator, ALARM/CLEAR switch/indicator, PAPER STEP switch, TOP OF FORM switch, and PHASE potentiometer are readily accessible to the operator. By raising the cover door, the COPIES potentiometer, 6/8 LINES switch, TEST (self-test) switch, and STATUS indicators are also accessible. The digital STATUS indicator facilitates diagnosis and identification of problems and malfunctions.

1.3.7 Fan Assemblies

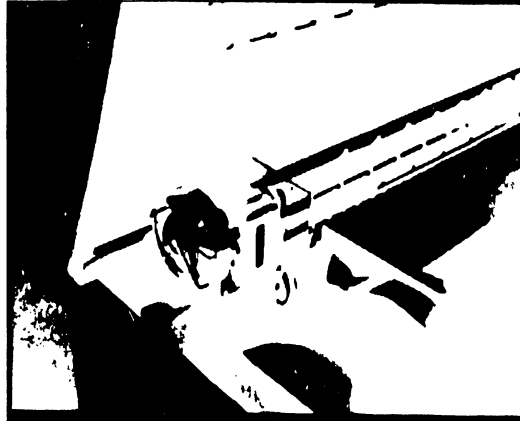


245058A.1003/3

The standard 300 LPM and 600 LPM printers have a single Fan Assembly located in the rear of the printer to provide a constant flow of air over and around the Electronic Assembly card cage and to maintain the operating temperature within a specified range. Failure of the fan to maintain the temperature within the required temperature range will cause an immediate reflex fault that will power down the printer. Power for the Fan Assembly is provided by the AC power source. Printer operation is prevented if the Fan Assembly is not plugged into the Rectifier CCA.



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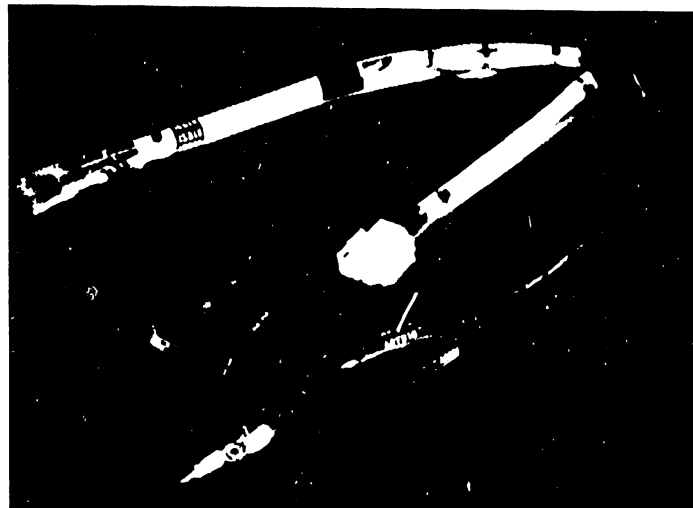


255176.258

All printers installed in an acoustic cabinet have two (2) additional fan assemblies. A Hammer Bank Blower Assembly, positioned over the hammer bank, expels the heat generated by the printing operation. A plenum chamber directs the air flow to the hammer modules. The blower motor is plugged into the Rectifier CCA.

The Paper Puller Assembly motor is cooled by an axial fan attached to the motor assembly. Air is pulled from the cabinet duct and forced over and around the motor to prevent overheating.

1.3.8 Harness Assemblies



STANDARD POWER SUPPLY
HARNESS ASSEMBLY SHOWN

255137.133

The printer employs a number of harness and cable assemblies to interconnect the major assemblies, subassemblies and circuit card assemblies. Interconnection diagrams are provided in **section V** of volume II.

1.4 OPTIONS AND ACCESSORIES

A variety of options and accessories are available to efficiently configure the printer to meet specific application requirements. The following paragraphs briefly describe those options and accessories currently obtainable.

1.4.1 Multiple Band Sensing and Character Sets

A printer is normally provided with one (1) character band and a code-correlated band image PROM. By installing two (2) additional band image PROMs on the Processor CCA, a maximum of three (3) differently configured character bands may be used on the same printer without electronic changes. Note that the character bands and band image PROMs must be matched and that printers cannot be equipped with both USA and UK PROMs.

Standard character bands are available in 48, 64, upper and lower case 96, and 128 character sets. An optional automatic foldover of lower case character codes into appropriate upper case characters may be provided with the 64 character utility band sequence. Consult the appropriate table in **section VI** of volume II for a descriptive list of the standard character band/PROM sets. Printers configured with the Centronics-Compatible Interface CCA cannot use the 128 character set and do not print the 96th character in the 96 character set. See **paragraph 1.4.4, subparagraph b**.

A variety of special character and font styles is also available. Unique characters can be designed upon customer request.

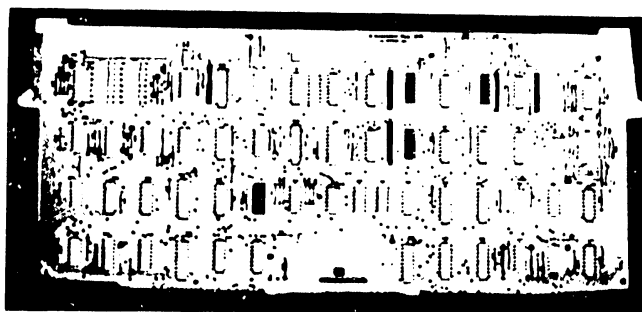
1.4.2 Condensed Print

Standard horizontal character spacing for all printer models is ten (10) characters per inch (CPI). The 300 LPM models can be configured to use the condensed print fifteen (15) CPI band/PROM sets. Changing from standard to condensed printing can then be simply a matter of changing the character band when the Multiple Band sensing option is also installed. Since 136 columns are the maximum accepted by the printer, the 15 CPI option reduces the width of the printout.

1.4.3 136 Column Print Capability

A 136 column print capability is available as an option for all standard printer models. Additional circuitry on the Hammer Driver CCA(s) is required to implement the option. This option is not available for 300 LPM and 600 LPM printers configured with either the Centronics-Compatible Interface CCA or the Serial Interface CCA with VFU.

1.4.4 Interface Options



SERIAL INTERFACE
CCA SHOWN

255137.124

In addition to the standard Short Line Interface CCA, optional interface configurations are available to meet special customer requirements. Operation of the most widely used optional interfaces is discussed in **section II** of this volume.

a. Long Line Interface

The Long Line Interface allows the interface lines to be extended from the standard 15 meters (49 feet) to 150 meters (492 feet). Integrated circuit differential transmitters and receivers of the DM 8830/8820 class are used. The user must supply similar long line devices at the controller end.

b. Centronics-Compatible Interface

The Centronics-Compatible Interface permits operation on most Centronics-Compatible controllers. The VFU option is standard with this interface. In addition, any character set used must be limited to 95 characters maximum; octal 177 is used as a delete code in 300 LPM and 600 LPM models and is switch-selectable in 1000 LPM printers. 300 LPM and 600 LPM printers configured with the Centronics-Compatible Interface CCA cannot support the optional 136 column print capability.

c. Serial Interface

The Serial Interface utilizes standard RS232C receivers and drivers, or 20 MA current loops, to receive and transmit data in serial format. The front-ended circuit card assembly is plugged into the spare slot of the Mother Board CCA. The printer can be configured for the VFU option by replacing the standard non-VFU Short Line Interface CCA with the Centronics-Compatible Interface CCA. Since the maximum baud rate available is 19,200, the Serial Interface cannot support the full 1000 lines per minute print rate of the 1000 LPM printer. However, the 300 LPM and 600 LPM printers with the VFU serial configuration cannot support the optional 136 print column.

d. Low True and Buffer Clear Invert Interfaces

To meet customer requirements for low true interfacing, a configuration switch mounted on the Short Line Interface CCA allows all received and transmitted signals, except Buffer Clear, to be inverted. The low true interface capability is currently available only with the standard short line configuration.

The standard low active BUFFER CLEAR can be inverted to high active by another configuration switch mounted on the interface circuit card assembly. The high true BUFFER CLEAR option is currently available in either short line or long line configured printers.

e. Customer Interfaces

In addition to the Long Line, Centronics-Compatible, and Serial interfaces already described, other system-compatible interfacing options are available upon request. When required, parity checking and automatic line feed on carriage return can also be provided. Custom interface requirements can be implemented by special request to the DPC Sales Administrator.

1.4.5 Input/Output Harness Assemblies

Non-standard I/O harness assemblies are provided as required for each of the interface options described above. User pin assignments for these I/O assemblies are discussed in **section II** of this volume. In addition, the following options are available:

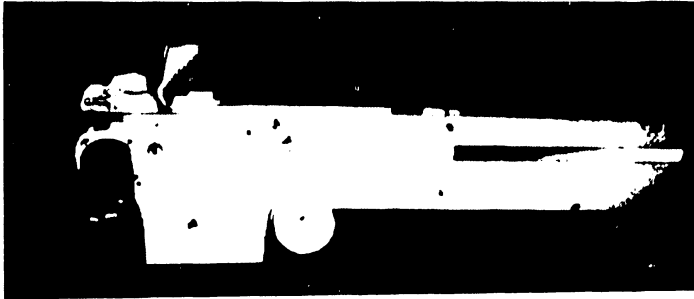
a. Pull Up/Pull Down Resistors

Custom termination resistors on the receiver lines may be provided upon request. Minimum acceptable value is 200 ohms. When both pull up and pull down resistors are installed, 470 ohms is the optimum value for each resistor. A table of the pull up and pull down resistor configurations is provided in **section VI** of volume II.

b. Winchester Connector

An optional 50-pin Winchester connector, a mating connector, and fifty crimp-type pins may be supplied with the printer instead of the standard AMP connector. A twisted pair is used for each signal. The pin assignments for the Winchester connector are shown in **section II** of this volume.

1.4.6 Tape Controlled Vertical Format Unit (TCVFU)



245059.184

The 12-channel Tape Controlled Vertical Format Unit, consisting of an optical paper tape reader and related electronics, is offered as an option to allow handling of a variety of form lengths and to enable rapid paper slewing within individual forms. The Processor CCA firmware (PROMs) and the Interface CCA configuration switch set-up must be compatible with the VFU function. Operation of the TCVFU is described in **section II** of this volume.

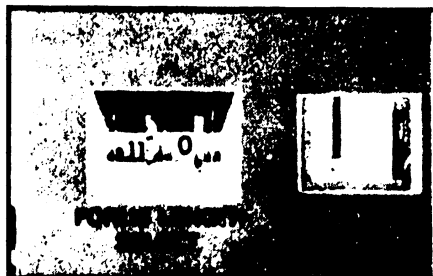
The tape reader uses a 12 channel paper tape, of a maximum length of 144 lines (24 inches at 6 LPI; 18 inches at 8 LPI). Each tape loop should have only one hole punched in the channel 1 position to designate Top of Form. Bottom of Form may be punched in either channel 2, 8, 11, or 12 as required by the Interface CCA configuration switch settings.

Multiple forms may be punched into one tape if the format is short, and if each repetition of the format pattern is identical to all other format patterns on the tape. Tape punching procedures are provided in the Operator's Guide and the Maintenance Guide which are shipped with the printer.

1.4.7 Direct Access Vertical Format Unit (DAVFU)

The Direct Access Vertical Format Unit provides the same form handling and movement capability as the TCVFU, but functions under direct user control. The Processor CCA PROMs and the Interface CCA configuration switch set-up must be compatible with VFU operation. The DAVFU function is described in **section II** of this volume.

1.4.8 Forms Length Selector Assembly



2450448.239

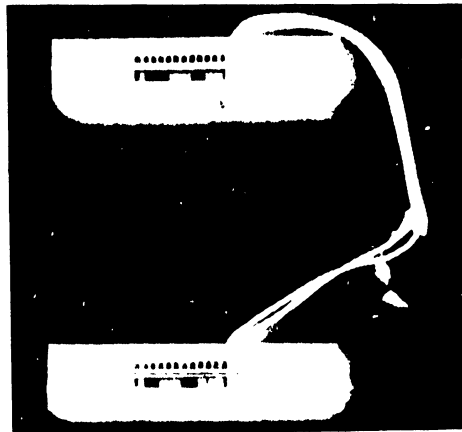
The Forms Length Selector Assembly, consisting of two (2) thumbwheel switches, is mounted on the base of the Control Panel Assembly. Setting of the two switches allows the operator to handle a variety of commonly used form lengths and to advance paper the appropriate number of lines to Top of Form by pressing the control panel TOP OF FORM switch. A user-transmitted form feed code will also advance paper to the top of form designated by the switch settings.

Switch number one (1) defines a form length from 3 to 14 inches. Switch number two (2) designates fractions of an inch from 0, 1/4, 1/3, 1/2, 2/3, to 3/4. Fourteen inches is the maximum selectable form length. If a form length is selected which is not divisible by the current lines per inch setting (6 or 8), a fault code will appear on the STATUS indicator display. When a printer is also configured with the optional DAVFU and/or TCVFU, an additional switch is provided on the Form Length Selector Assembly to permit the operator to select either the form length selector or VFU option.

1.4.9 Ground Isolation

The standard printer is shipped with the logic and frame grounds tied together. An isolated ground configuration is available as an option.

1.4.10 Elapsed Time Meter Assembly



245058.907

The Elapsed Time Meter Assembly consists of two (2) chemical type meters, accurate within $\pm 10\%$, which measure power on and print time. "Power On" time is recorded with a 0 to 10,000 hour meter, and "Print Time" is recorded with a 0 to 1,000 hour meter. Intended for historical recording purposes only, the meters are not visible without lifting or removing the top cover of the printer.

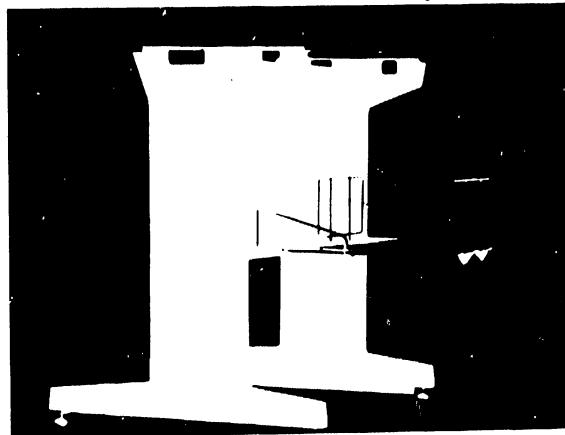
1.4.11 Line Filter Assembly

The Line Filter Assembly can be installed to attenuate high frequency noise from the power line. The low-pass filter is mounted on the power supply chassis and wire-connected between the power cord and the power switch.

1.4.12 Pedestal Assembly and Paper Shelf Assembly (Figure 1-2)

For the 300 LPM model printer, which cannot be conveniently mounted on a table top, a Pedestal Assembly is available as an accessory. The Pedestal Assembly is normally included with all 600 LPM models. **Figure 1-2** illustrates a 600 LPM printer mounted on the pedestal.

The Pedestal Assembly is shipped, disassembled, in a separate container and must be assembled at the site. Assembly instructions are provided in the Maintenance Guide.



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A Paper Shelf Assembly, which attaches to the rear of the pedestal, is also available. The shelf is designed to passively stack various form sizes and paper lengths.

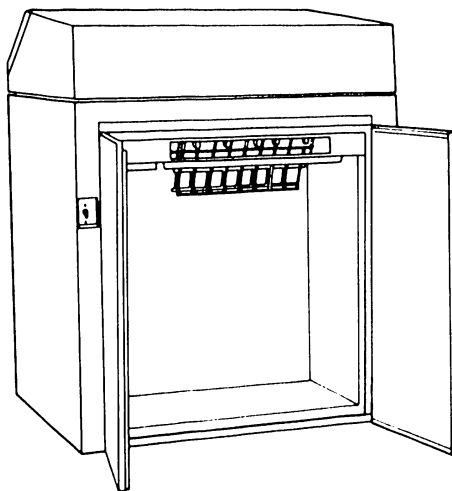
1.4.13 Full Length Cabinet Assembly

Both 300 LPM and 600 LPM printers can be mounted on a Full Length Cabinet Assembly. Hinged doors provide access to the interior of the enclosed cabinet for paper loading and storage. A paper shelf, attached to the rear of the cabinet, passively stacks paper as it emerges from the printer.

1.4.14 Acoustic Cabinet Assembly (Figure 1-3)

The 300 LPM and 600 LPM model printers can be ordered mounted in the same Acoustic Cabinet Assembly that is a standard accessory for the 1000 LPM printers. Retrofitting of printers in the field is not possible because of the component and wiring changes required by the acoustic cabinet configuration.

The Acoustic Cabinet Assembly fully encloses the printer's electro-mechanical assemblies and, therefore, reduces noise levels to 60 dBA during printer operation. Double doors, front and rear, afford easy access for paper loading and removal. An optional right rear door viewing window allows the operator to monitor paper stacking without opening the cabinet.



A Paper Puller Assembly, mounted in the rear of the cabinet, ensures that paper is uniformly fed into the rear of the cabinet. Paper stacking is facilitated by an adjustable paper stacking shelf mounted on rails in the rear cabinet or by a paper stacking base placed on the floor of the rear cabinet.

1.4.15 Paint Schemes

Special paint colors for the exterior skins of the printer may be supplied on request. Usually a paint chip is required at the time of order. Contact the DPC Sales Administrator for details.

SECTION

II

THEORY

OF

OPERA-

TION

SECTION II

THEORY OF OPERATION

2.1 INTRODUCTION

This section discusses in detail the operation of the standard B-Series printer and the most common variants and options. The topics include descriptions of the system interface, the circuit card assemblies (CCAs), the printer subsystems, the format control systems and program overviews.

2.2 SYSTEM INTERFACE

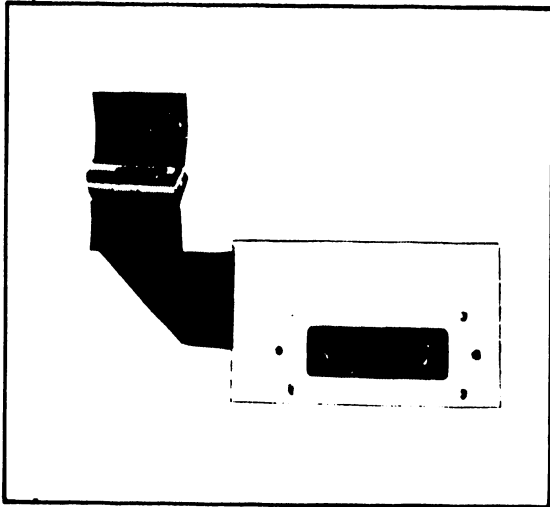
The Input/Output Harness Assembly interfaces the user system to the printer and provides the necessary lines for transmission of data, control, status, and strobe signals. The user's I/O cable connector is plugged into an I/O receptacle (J1) located at the rear of the printer. The I/O CCA, containing any needed resistor networks, is plugged into J5 of the Interface CCA. The resistor networks pull-up and/or pull-down the user-to-printer signals to the required logic levels and provide the source current for driving the printer-to-user signals. The Serial I/O has no CCA.

With the exception of the Serial system interface, the following logic levels are used by all interface configurations:

- | | | |
|---------|---|---|
| Logic 1 | - | Must be greater than 2.4 VDC and less than 5.0 VDC. |
| Logic 0 | - | Must be greater than 0.0 VDC and less than 0.4 VDC. |

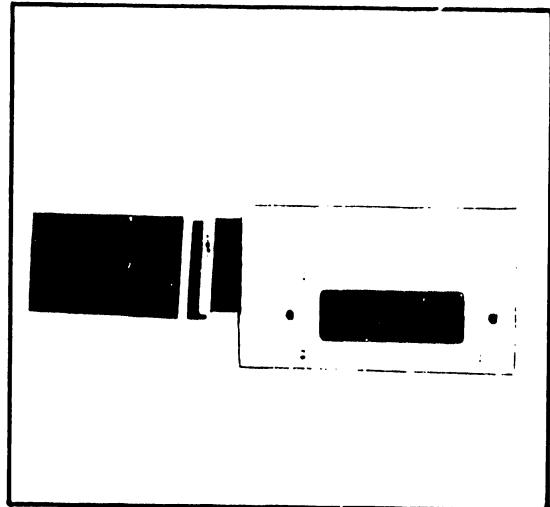
Currently, four (4) different interface configurations are commonly installed in the B-Series printers. The standard short line and the long line interfaces are available with an AMP or optional Winchester I/O connector. The Centronics-Compatible and Serial interface configurations have unique I/O connectors which are not interchangeable with the other systems.

Figure 2-1 illustrates the four (4) types of connectors. Logic diagrams for all I/O CCAs, except Serial which has no CCA, are included in **section V**. The interfacing conditions, such as handshaking routines, timing, and connector pin assignments are individually described in **paragraphs 2.2.1 through 2.2.4**. **Paragraph 2.3** describes each type of Interface CCA in detail.



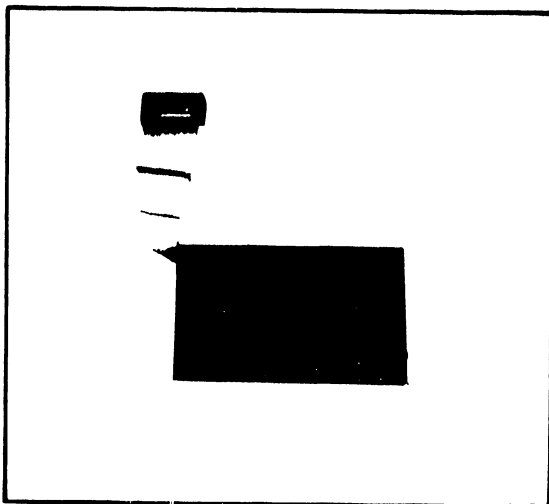
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A. SHORT/LONG LINE AMP
TYPE CONNECTOR



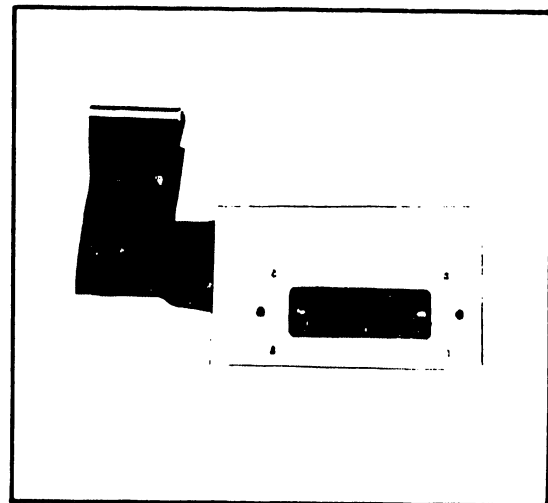
255176.315

B. SHORT/LONG LINE WINCHESTER
TYPE CONNECTOR



255176.314

C. SERIAL TYPE CONNECTOR



255176.313

D. CENTRONICS-COMPATIBLE
TYPE CONNECTOR

Figure 2-1. I/O Harness Assembly Connector Types

2.2.1 Short Line System Interface

The Short Line system interface uses a demand/response handshake routine and a bit parallel data transfer format. **Figure 2-2** provides a flow diagram of the Short Line system interface handshaking mode of operation. **Figure 2-3** supplies the timing diagram. When the printer is ready, on line, and able to load data, the handshaking sequence proceeds as follows:

1. If the STROBE signal is inactive (low), the DEMAND line can go active (high) to request data from the user. DEMAND will remain high until STROBE is received by the printer.
2. When DEMAND is high and the data lines are stable, STROBE can go active.
3. When the data lines have been sampled by the printer, DEMAND goes inactive (low).
4. When the user detects that DEMAND is inactive, STROBE should go low (inactive).
5. When the printer detects the inactive STROBE, the next DEMAND can be generated.

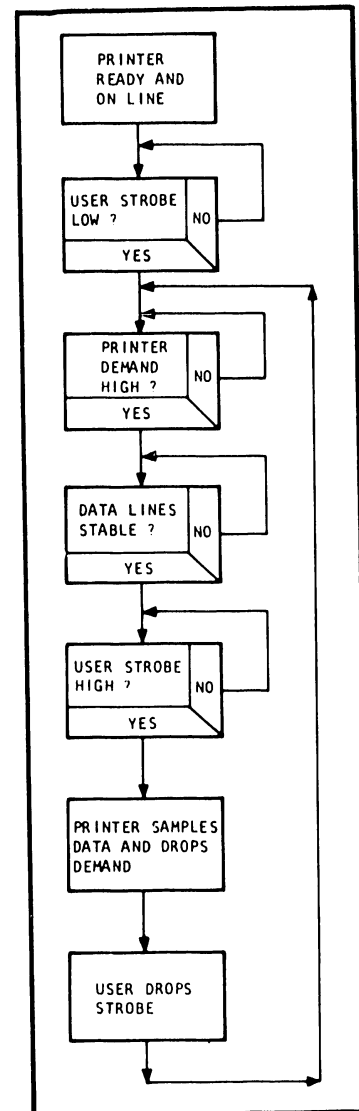
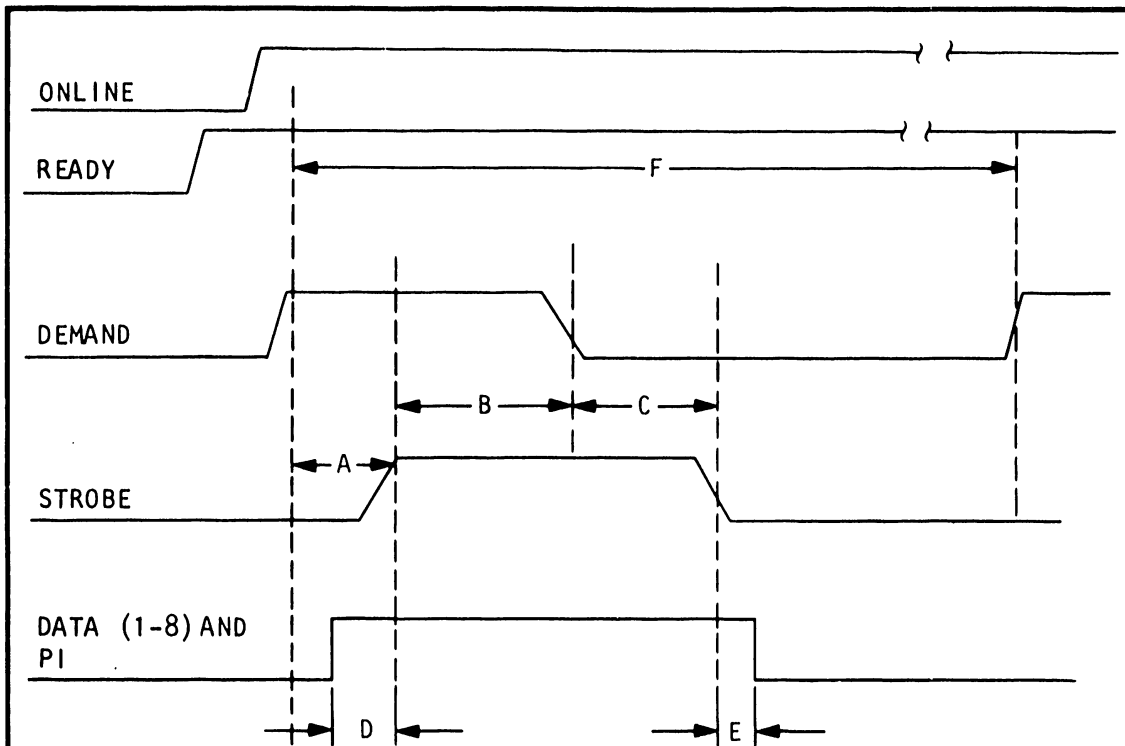


Figure 2-2. Flow Diagram Short Line/Long Line Handshake Routine



NOTE	SIGNAL ACTIVITY	MAX	MIN
A	STROBE PRESENT AFTER DEMAND PRESENT	250 NS	50 NS
B	DEMAND REMOVED AFTER STROBE PRESENT	143 NS	N/A
C	STROBE REMOVED AFTER DEMAND REMOVED	800 NS	50 NS
D	SETTLING TIME	N/A	50 NS
E	DATA HOLD TIME	N/A	50 NS
F	CHARACTER TRANSFER	N/A	1.95 μ S

NOTES:

- A THIS IS THE TIME RANGE THE USER MAY TAKE TO RAISE STROBE FOLLOWING THE LEADING EDGE OF THE DEMAND TO GUARANTEE THE MAXIMUM TRANSFER RATE.
- B THIS IS THE TIME THE PRINTER WILL TAKE TO DROP THE DEMAND AFTER THE LEADING EDGE TO THE STROBE.
- C THIS IS THE TIME RANGE THE USER MAY TAKE TO REMOVE STROBE FOLLOWING THE TRAILING EDGE OF THE DEMAND TO GUARANTEE THE MAXIMUM TRANSFER RATE.
- D THIS IS THE MINIMUM DATA SETTling TIME THE USER MUST GUARANTEE PRIOR TO RAISING THE STROBE.
- E THIS IS THE MINIMUM DATA HOLD TIME THE USER MUST GUARANTEE AFTER REMOVAL OF THE STROBE.
- F THIS IS THE MINIMUM CHARACTER TRANSFER PERIOD IF THE TIMING SPECIFIED IN DEFINITIONS A THROUGH E ARE MET.

Figure 2-3. Short Line and Long Line Interface Timing Diagram

Table 2-1 lists and briefly defines the interfacing signals as they appear at the J1 connector located at the rear of the printer. Pin assignments are given for both the standard AMP and the optional Winchester connectors.

In addition to the standard signal lines, **Table 2-1** lists as optional those signals and pins designated for special features. Internally used equivalents to the user signals are listed in parentheses. More detailed definitions can be found in **section V**, the Glossary of Mnemonic Terms. See also **logic diagram sheet numbers 58 and 59**.

TABLE 2-1. SHORT LINE AND LONG LINE I/O CONNECTOR PIN ASSIGNMENTS

Signal Mnemonic	Amp Connector (J1)		Winchester Connector (J1)		Definition															
	Signal Pin	Ground Pin	Signal Pin	Ground Pin																
Standard Signal Lines																				
READY (RDY)	22	6	CC	EE	Printer-generated to indicate it is ready to be placed on line.															
ON LINE (ONLN)	21	5	y	AA	Printer-generated to indicate it is on line.															
DEMAND (DEM)	23	7	E	C	Printer-generated to request data from user. Only active when ONLINE is active except in the Print Inhibit Mode.															
STROBE	38	37	i	m	User-generated to indicate stable data on the data lines.															
DATA Lines 1-8					User-generated data lines for transmission of print data and format control codes.															
DATA 1	19	3	B	D																
DATA 2	20	4	F	J																
DATA 3	1	2	L	N																
DATA 4	41	40	R	T																
DATA 5	34	18	V	X																
DATA 6	43	42	Z	b																
DATA 7	36	35	n	k																
DATA 8	28	44	u	w	(Option)															
IDENT 0 (IDNT 0)	50	32	d	f	Printer-generated to identify the characteristics of the band currently installed.															
IDENT 1 (IDNT 1)	49	16	a	c	<table border="1"> <thead> <tr> <th>IDENT 0</th> <th>IDENT 1</th> <th>BAND</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>EDP (300 LPM Only)</td> </tr> <tr> <td>1</td> <td>1</td> <td>48 or 128 Character Set</td> </tr> <tr> <td>1</td> <td>0</td> <td>64 Character Set</td> </tr> <tr> <td>0</td> <td>1</td> <td>96 Character Set (U/L Case)</td> </tr> </tbody> </table>	IDENT 0	IDENT 1	BAND	0	0	EDP (300 LPM Only)	1	1	48 or 128 Character Set	1	0	64 Character Set	0	1	96 Character Set (U/L Case)
IDENT 0	IDENT 1	BAND																		
0	0	EDP (300 LPM Only)																		
1	1	48 or 128 Character Set																		
1	0	64 Character Set																		
0	1	96 Character Set (U/L Case)																		
INTERFACE CONN VERIFY	46 45		v x																	
+5V (Test only)	12		HH																	
Ground		39		K																

TABLE 2-1. SHORT LINE AND LONG LINE I/O CONNECTOR
PIN ASSIGNMENTS (Cont'd)

Signal Mnemonic	Amp Connector (J1)		Winchester Connector (J1)		Definition
	Signal Pin	Ground Pin	Signal Pin	Ground Pin	
<u>Optional Signal Lines</u>					
PPR INST (PI)	30	14	p	s	User-generated to inform printer that format data is on the data lines used with TCVFU or DAVFU options only.
BOF	25	9	M	P	Printer-generated to inform user that the bottom of form position has been reached.
TOF	24	8	S	U	Printer-generated to inform user that the top of form position has been reached.
PRMVG/ VFURDY	26 48	10 17	W FF	Y DD	Printer-generated to inform user that paper is moving. In VFU units, it indicates that the VFU memory is loaded.
PARITY BIT (PARBIT)	29	13	z	BB	User-generated to provide the parity bit for the pre-set parity option.
BUFFER CLR (BUFCLR)	31	15	A	H	User-generated to clear all data stored in the printer buffer before starting a new data transfer.
PARITY ERR (PARERR)	27	11	r	t	Printer-generated to inform the user of a parity error on the last data transfer.
NOT VFU	47		e		
VFU VERIFY	33		h		
NOTE: AMP connector pins 26 and 48 and Winchester connector pins W and FF are internally connected on the I/O connector.					

2.2.2 Long Line System Interface

The Long Line system interface functions in the same way as the short line system described in **paragraph 2.2.1**. **Table 2-1** and **figures 2-2 and 2-3** also apply to the Long Line system interface. Note that the Long Line I/O CCA contains no-pull up or pull-down resistor networks. See **logic diagram sheet numbers 60 and 61** in **section V**.

2.2.3 Centronics-Compatible System Interface

The Centronics-Compatible system interface uses a pulsed handshaking routine rather than an interlocked handshaking mode of operation. Data is transferred in a bit parallel format on a Strobe/Acknowledge basis.

Before the printer can receive print or format data, it must be selected by pressing the ON/OFF LINE switch on the control panel or by the user transmitting a DC1 (Hex 11) control code on the data lines. The SLCT (Select) line to the user is then set active, and BUSY, which is activated during power up, is inactivated. An ACK* (Acknowledge) pulse of 2.5 microseconds is immediately sent to the user.

Figure 2-4 provides a flow diagram of the selection and handshaking routines for the Centronics-Compatible system interface. Select and data transfer timing diagrams are supplied by figures 2-5 through 2-8.

Table 2-2 lists and briefly defines the interfacing signals as they appear at the J1 connector located at the rear of the printer. More detailed definitions are listed in the Glossary of Mnemonic Terms in section V of volume II. See also logic diagram sheet number 62.

Once the printer has been selected and the BUSY signal dropped, the handshaking sequence proceeds as follows:

1. The user transmits a data STROBE of 0.5 to 1.0 microseconds to the printer.
2. The printer senses the active STROBE and stores the data in memory.
3. If BUSY is inactive, the printer waits for 2.5 microseconds and then issues a 2.5 microsecond ACK* pulse. If BUSY is active, the ACK* pulse will not be sent until BUSY becomes inactive.
4. The user system then senses the ACK* pulse and can then transmit another data STROBE to the printer.

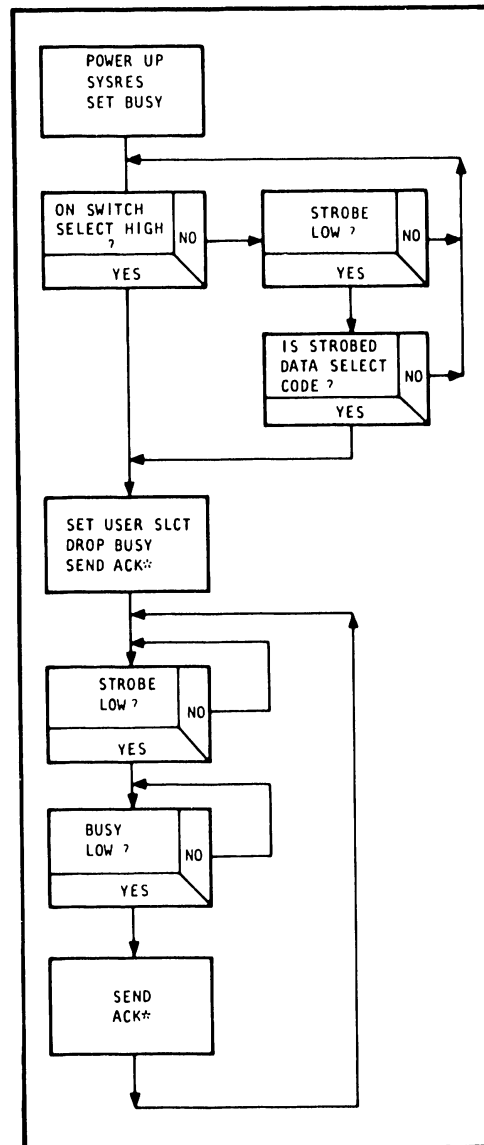


Figure 2-4. Flow Diagram
Centronics-Compatible
Handshake Routine

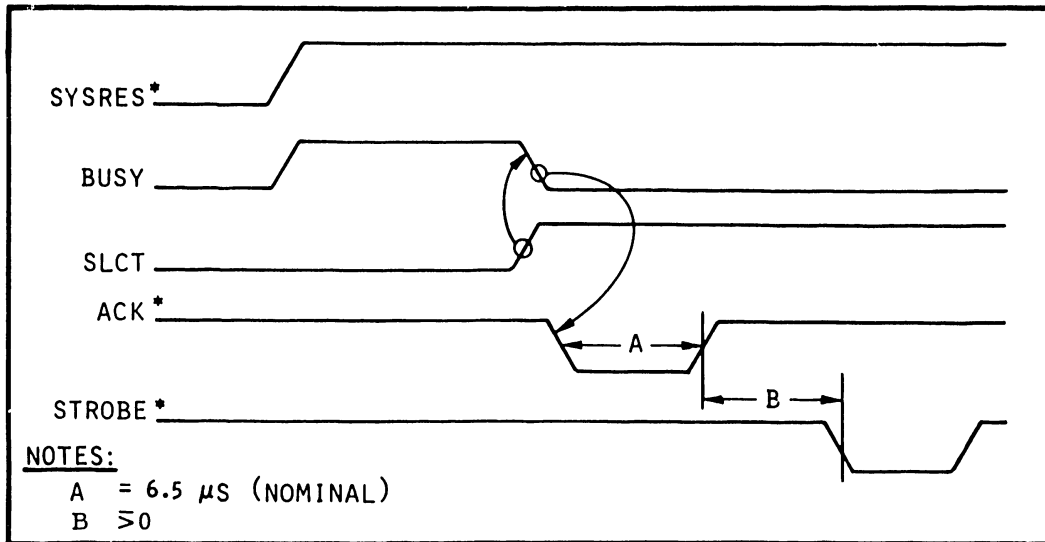


Figure 2-5. Centronics-Compatible Interface Select Timing Via ON/OFF LINE Switch

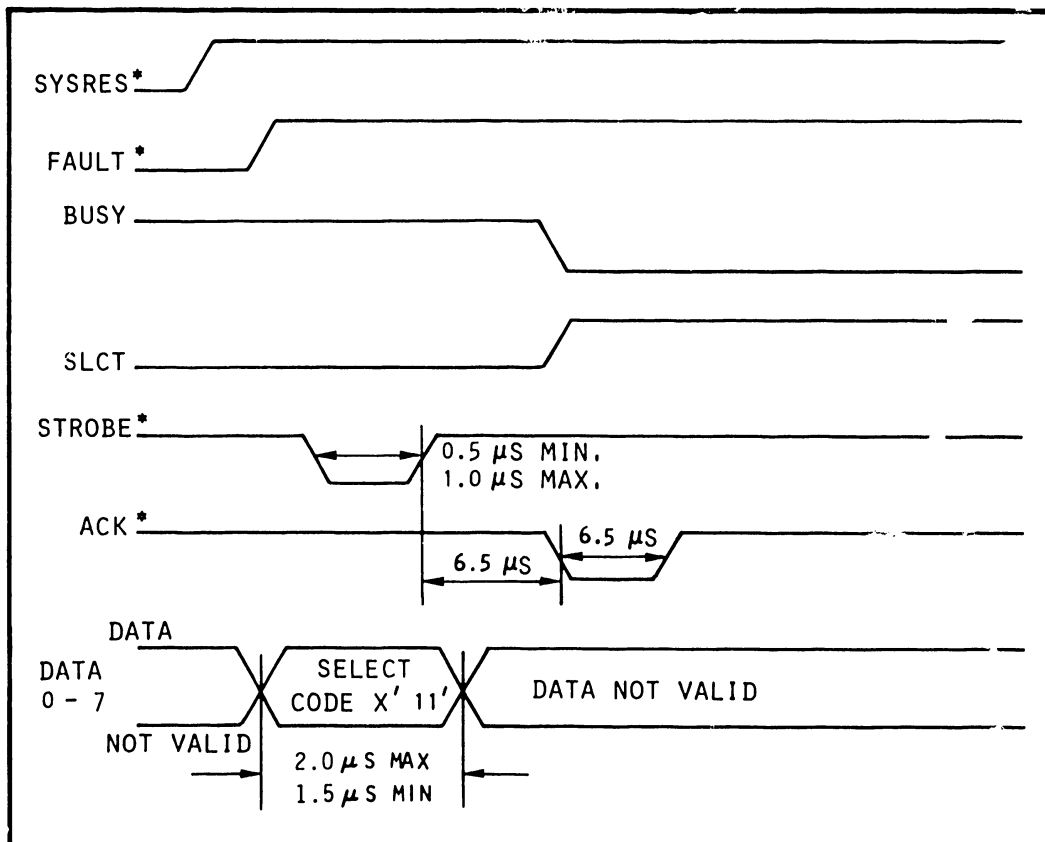


Figure 2-6. Centronics-Compatible Interface Select Timing Via Data Bus

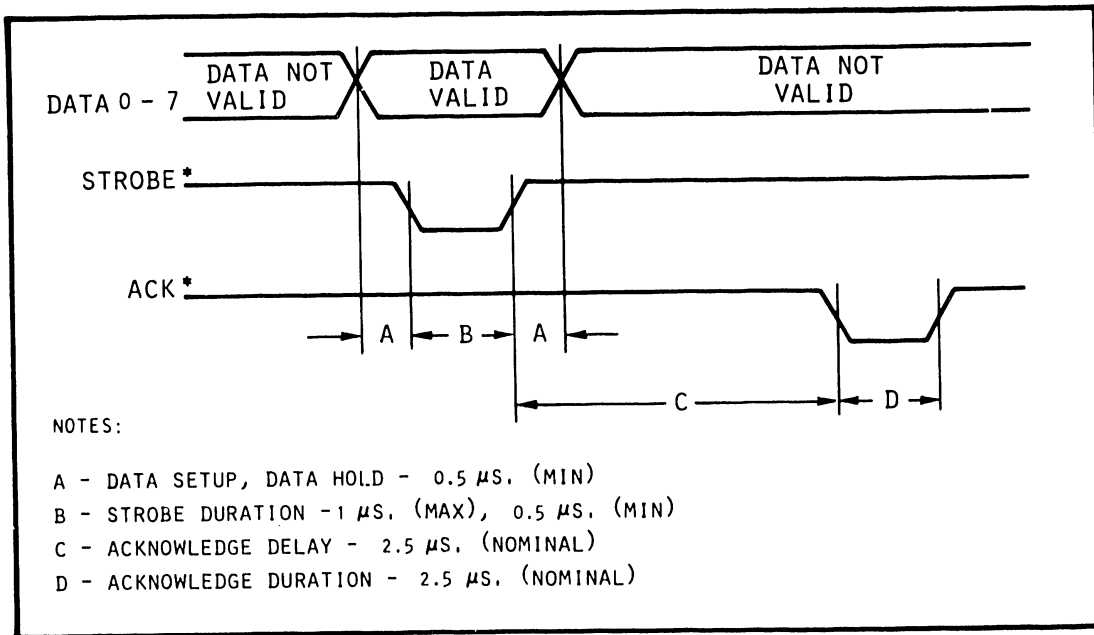


Figure 2-7. Centronics- Compatible Interface Data Transfer Timing without BUSY

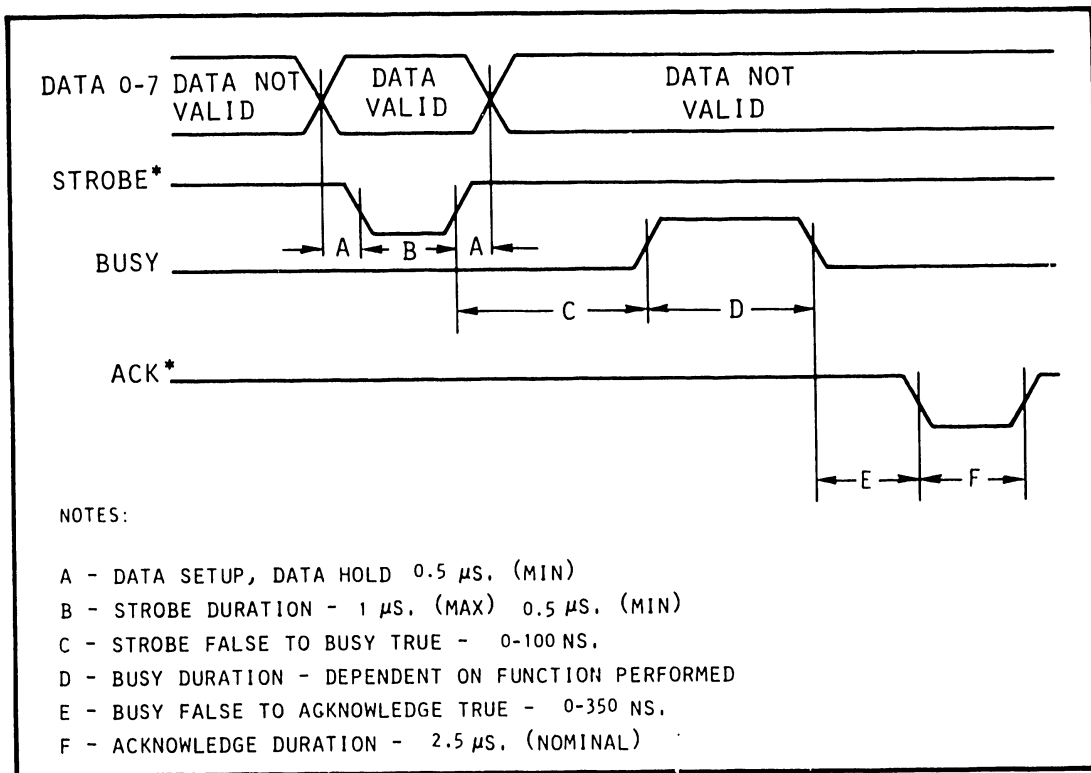


Figure 2-8. Centronics-Compatible Interface Data Transfer with BUSY

TABLE 2-2. CENTRONICS-COMPATIBLE I/O CONNECTOR PIN ASSIGNMENTS

Signal	Signal Pin	Return Pin	Definition
STROBE*	1	19	User-generated signal to inform printer that data on the data lines are stable.
DATA Lines			User-generated data lines for transmission of print data and control codes.
DATA 1	2	20	
DATA 2	3	21	
DATA 3	4	22	
DATA 4	5	23	
DATA 5	6	24	
DATA 6	7	25	
DATA 7	8	26	
DATA 8	9	27	
ACK*	10	28	Printer-generated to inform the user that a data word was received.
BUSY	11	29	Printer-generated to inform the user that the printer is not able to receive print or format data.
PE	12		Printer-generated to indicate that the printer is out of paper; also active during power up to back-up BUSY.
SLCT	13		Printer-generated to indicate that the printer has been selected.
INPUT PRIME*	31	30	User-generated to clear the printer buffer and initialize the interface logic.
FAULT*	32	33	Printer-generated to inform the user that a fault has occurred in the printer.
± 0 V	14, 16		Printer's logic ground; may be tied to chassis.
+5 V	18		Regulated five (5) volt supply.
CHAS GND	17		

2.2.4 Serial System Interface

The Serial system interface is made up of three (3) assemblies: an I/O Harness, a Serial Interface CCA which is edge-connected to the spare slot of the Mother Board CCA, and an Interconnect Cable Assembly. A parallel interface circuit card assembly, either short line for non-VFU or Centronics-Compatible for VFU operation, is also installed in its normal slot in the electronics card cage. **Figure 2-9** shows the interconnection of the components of the Serial system interface configuration.

NOTES:

- + SIGNAL OPTIONS
- * CCA EDGE CONNECTOR
- ** INTERCONNECT CABLE
- ‡ MORE THAN ONE SIGNAL LINE AND PIN CONNECTION

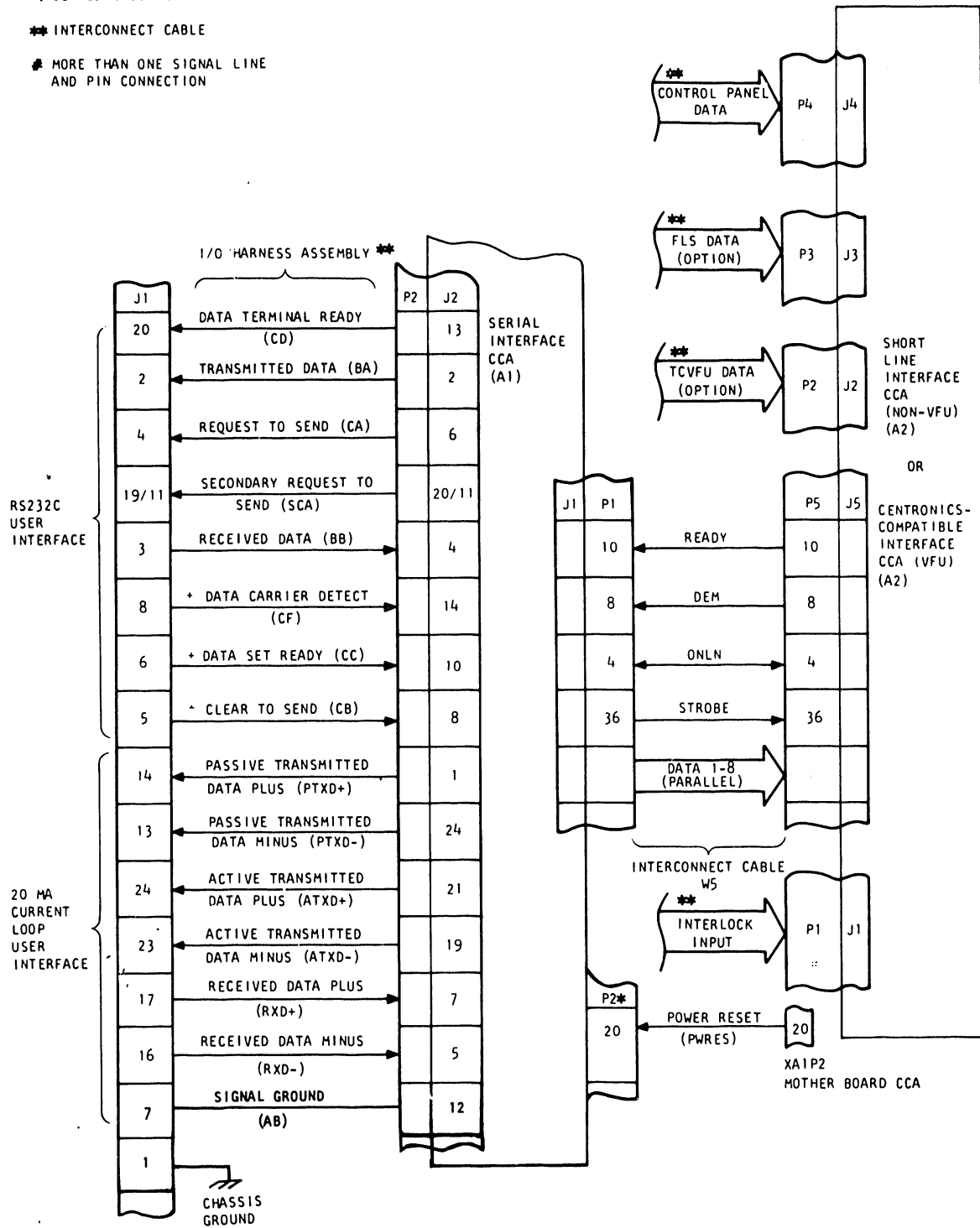


Figure 2-9. Serial System Interface Components

The user's I/O cable is plugged into the I/O Harness receptacle which is located at the rear of the printer. The printer's I/O harness cable is plugged into J2 on the Serial Interface CCA. The I/O Harness Assembly functions as a pass-through device that connects the user's system to transmitter and receiver circuits and current sensing devices mounted on the Serial Interface CCA. **Table 2-3** lists and defines the Serial system interface pin connections.

TABLE 2-3. SERIAL I/O CONNECTOR PIN ASSIGNMENTS

Signal	I/O Connector Pin No.	CCA Connector (J2) Pin No.	Definition
<u>RS232C</u>			
(AA)	1	N/C	Protective Ground
(AB)	7	12	Signal Ground (Common Return)
(BB) RXD	3	4	User-generated to transmit all print, format, and control data to the printer. (Received Data)
(CD) DTR*	20	13	Printer-generated to indicate the printer is ready to receive data. (Data Terminal Ready)
(CA) RTS*	4	6	Printer-generated to indicate the printer is ready to transmit data. (Request to Send)
(SCA) SRS*	11, 19	11, 20	Printer-generated to send busy status and to control data flow along the BB line. (Secondary Request to Send)
(BA)	2	2	Printer-generated to send information to the user. TXD(Transmitted Data)
(CC)	6	10	Optional user-generated to indicate the status of DSR*the user equipment. (Data Set Ready)
(CF)	8	14	Optional user-generated to validate data being DCD*sent to the printer. (Data Carrier Detect)
(CB)	5	8	Optional user-generated to inform the printer that CTS*the user is ready to receive data. (Clear to Send)
<u>20 mA Current Loop</u>			
(RXD+)	17	7	User-generated to transmit all print, format, and control code data and to indicate the status of the user equipment. (Received Data Plus)
(RXD-)	16	5	Current loop return for RXD+. (Received Data Minus)
(PTXD+)	14	1	Printer-generated to indicate it is able to receive data. (Passive Transmitted Data Plus)
(PTXD-)	13	24	Current loop return for PTXD+. (Passive Transmitted Data Minus)
(ATXD+)	24	21	Printer-generated to provide printer status information and allow for full duplex 20 mA current loop transmission. (Active Transmitted Data Plus)
(ATXD-)	23	19	Current loop return for ATXD+. (Active Transmitted Data Minus)

Data and status are transferred to and from the parallel interface over the Interconnect Cable Assembly which is plugged into J1 on the Serial Interface CCA and J5 on the Parallel Interface CCA. The way in which data is handled by the printer after the transfer depends on which of the two (2) Parallel CCAs is installed. See paragraphs 2.2.1 or 2.2.3 for the parallel interface handshake routines and timing. Table 2-4 lists and defines the signals between the serial and parallel interfaces.

TABLE 2-4. SERIAL TO PARALLEL INTERFACING SIGNALS

Interface CCA J5 Pin	Signal	Definition
4	ONLN	Printer On Line
8	DEM	Printer Demand
10	READY	Printer Ready
20	DATA 8	Data Information Line
22	DATA 7	Data Information Line
24	DATA 6	Data Information Line
26	DATA 5	Data Information Line
28	DATA 4	Data Information Line
30	DATA 3	Data Information Line
32	DATA 2	Data Information Line
34	DATA 1	Data Information Line
36	STROBE	Data Strobe for non-VFU Operation
	STROBE*	Data Strobe for VFU Operation

Operating in an asynchronous mode, the Serial Interface CCA accepts the user data in serial form and converts it to the parallel format recognized by the printer. Serial data can be transmitted by either the Standard RS232C Voltage or the 20 mA Current Loop method. Switch S1-5, located on the circuit card assembly, determines which method is used at any given time. The interface switches and required transmission and receiving circuits are discussed in greater detail in paragraph 2.3.1, subparagraph d.

Signal levels for the Serial interface system differ from the other three (3) system interfaces. Signals between the printer and the user should fall within the following levels:

a. RS232C Voltage

Space	-	Must be greater than +3 V and less than +25 VDC.
Mark	-	Must be more negative than -3 VDC and less negative than -25 VDC.

b. 20 mA Current Loop

Logic 1	-	Must be greater than 15 mA and less than 20 mA.
Logic 0	-	Must be greater than 0 mA and less than 3 mA.

In addition to the two (2) methods of transmitting data, the Serial Interface CCA can support three (3) different RS232C communications formats or protocols. Switches mounted on the CCA determine whether serial data transmission will be in the simplex, unblocked duplex, or blocked duplex format.

Asynchronous communication between the user system and the Serial Interface CCA is controlled by a 2651 Programmable Communications Interface integrated circuit (PCI). Communication between the Serial Interface CCA and the printer's parallel interface is controlled by an 8255 Programmable Peripheral Interface integrated circuit (PPI). Both are under the program control of an 8085A microprocessor that is mounted on the circuit card assembly.

Figure 2-10 provides a flow diagram of the user to Serial Interface CCA and serial to parallel interface communications. The operation is discussed in greater detail in paragraph 2.3.1, subparagraph d. See also logic diagram sheet numbers C1 through C5.

After the printer is turned on and the power up and switch routines are completed, the following communications occur to begin data transmission:

1. An active READY signal is transmitted from the parallel interface to the PPI on the serial CCA.
2. With READY high, an active DEM signal from the parallel interface to the PPI causes the PCI on the Serial Interface CCA to enable its receivers and transmitters and force the DTR* and RTS* signals to the user to go low.
3. Signal SCA is then set to indicate that the interface is able to receive data. Code XON (Hex 11) is also sent to the user.
4. If the optional signals Data Set Ready (DSR*) and Data Carrier Detect (DCD*) are under user control, the user must set input lines CC and CF to high before transmitting data.
5. A valid start bit must precede each byte of data. The falling edge of the normally high RXD line marks the beginning of a valid start bit which allows the PCI to load the character into its parallel to serial receive buffer.

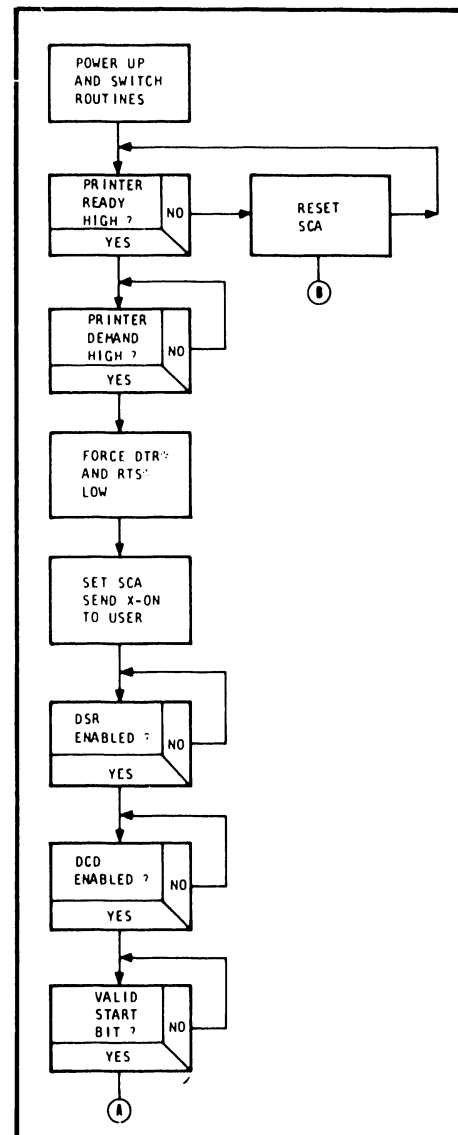


Figure 2-10A. Flow Diagram
Serial System Interface
Communications

6. The PCI's RxRDY signal is raised to initiate a RST 6.5 Interrupt to the microprocessor so that the data is written into a temporary location in the serial interface data RAM.
7. With data in the serial interface data RAM and the READY signal from the printer high active, an active DEM transmitted from the parallel interface to the PPI causes the STROBE signal to the printer to be set.
8. Data is then transferred from the PPI port to the parallel interface user data latch.

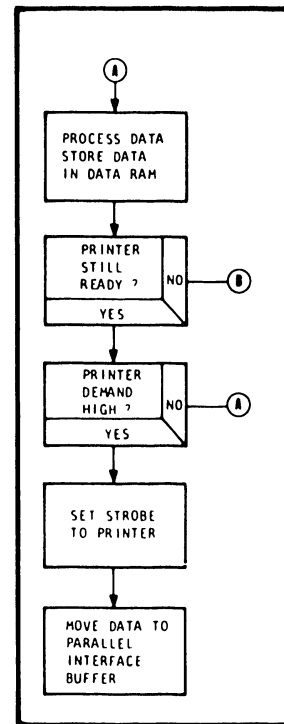


Figure 2-10B. (Cont'd)
Flow Diagram
Serial System Interface
Communications

2.3 CIRCUIT CARD ASSEMBLY ARCHITECTURE AND FUNCTIONS

The set up and function of each of the printer's major circuit card assemblies and their devices are discussed in detail in paragraphs 2.3.1 through 2.3.6 of this section. The circuit cards are dual edge-connected to the Mother Board CCA that is mounted to the printer base. The Mother Board CCA serves as a common bus for transmitting required voltages and signals to and between the CCAs.

A bus structure, made up of six (6) bus lines, supplies the paths for sending data and control information between the CCA devices. The bus structure includes the following bus lines:

1. Working Instruction Bus - This bus carries the program instructions from the instruction register section to devices throughout the Processor CCA. The bus is divided into instruction fields (groups of bits) which energize specific groups of devices.
2. Operand Bus (OBUS) - The OBUS carries the data to be processed from the Processor CCA's Arithmetic Logic Unit (ALU) instruction multiplexers to the various address or working registers that connect to the OBUS.

3. Register Bus (RGBUS) - The RGBUS serves as the pathway by which incoming user data or tape reader data is transmitted from the Interface CCA to the Processor CCA's ALU, Data RAM, and image address PROMs.
4. Input Bus (INBUS) - The INBUS carries user control, configuration switch, FLSS, and status information between the Interface CCA, the Timing and Status CCA and the Processor CCA.
5. OUTBUS - The OUTBUS transmits the last ALU-generated data from the Processor CCA to the Interface CCA, the Timing and Status CCA, and the Hammer Driver CCA(s).
6. Address Bus (ADRBS) - The ADRBS is used to send the program instructions which enable the Interface CCA, the Timing and Status CCA, and the Power Board CCA control groups.

Figure 2-11 provides a block diagram of the standard arrangement of the CCAs, the CCA devices, and the bus structure.

NOTE

In the following detailed descriptions of the CCAs, sheet number references (i.e., SH 5) are to the logic sheets provided in **section V** of volume II. The sheet number references are included to enable forward and backward tracing through the circuitry.

2.3.1 Interface CCA

In general, an interface CCA acts as an input/output buffer to the Processor CCA for the user system, the control panel, all system interlocks, the optional TCVFU, and the optional FLS switch. Under the program control of the Processor CCA, it performs the following logic functions for printer operation:

1. Determines the configuration switch settings and defines the printer system configuration for the Processor CCA.
2. Allows the user, through a single level buffer and latch, to transfer data to the printer system under program control.
3. Debounces all interlock signals going to the Processor CCA.
4. Allows the Processor CCA to monitor the control panel and provides a system status change signal to the Processor CCA when the ALARM/CLEAR switch is activated.
5. Forms a buffer and latch to the Processor CCA in order to send status or fault condition information to the STATUS indicator display.

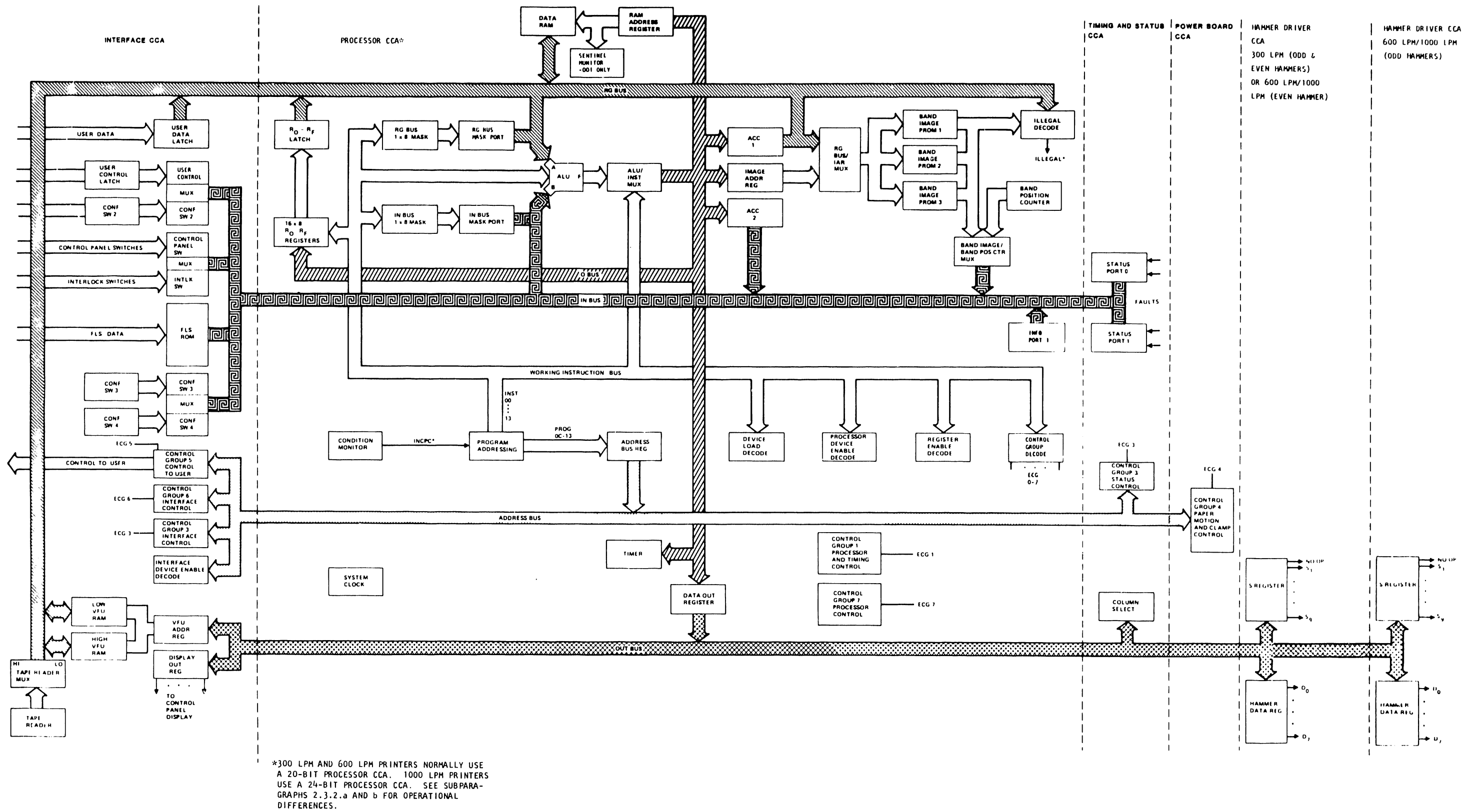


Figure 2-11. Circuit Card Assembly Device and Bus Block Diagram

6. Translates the forms length selector switch setting into the number of lines per page.
7. Forms a buffer and multiplexer for the optional TCVFU tape reader data to be stored and transmitted to the Processor CCA.
8. Monitors, under program control, the user/printer communications status.

At the present time, printers are configured with one (1) of the following four (4) circuit card assemblies: Short Line, Long Line, Centronics-Compatible, or Serial. The operation and unique devices of each CCA are described in detail in **subparagraphs a through d**.

a. Short Line Interface CCA

The following description of the Short Line Interface CCA is divided into two (2) parts. The first part discusses the major devices used on the circuit card assembly. The second part describes the operation of the devices as part of the overall printer functions. References are to **Logic Diagram Sheet Numbers 5 through 13** in section V of volume II.

1. Device Description - The Short Line Interface CCA uses low power Schottky and TTL integrated circuits to perform its functions. The following paragraphs briefly discuss the major integrated circuits and their functions. **Figure 2-17** is provided at the end of this discussion to serve as a pictorial summary of the device descriptions.

(a) Drivers and Receivers - Signals between the user and the printer are transmitted over an I/O cable of twisted pair wires by Hex Schmitt trigger Receivers U33 and U34 (**Sh 6 and SH 10**) and Hex Inverter Buffer/Drivers U31 and U32 (**Sh 7**). The driver's output impedance acts as a series terminator for the twisted pair.

Figures 2-12 and 2-13 illustrate the typical receiver and driver circuits formed by the I/O CCA and the Interface CCA.

(b) Configuration Switches - Configuration switches mounted on the Interface CCA are used to configure the printer to meet user requirements. Up to eight (8) switch-selectable configuration options are available with each switch. At the present time, not all switch positions are used.

The standard non-VFU Short Line Interface CCA has two (2) configuration switches S1 and S2. The VFU Short Line Interface CA has four (4) configuration switches S1 through S4.

Tables 2-5A through 2-5D list and define the configuration switch settings now available; **Figure 2-14** illustrates the same switch settings in diagram form for quick reference.

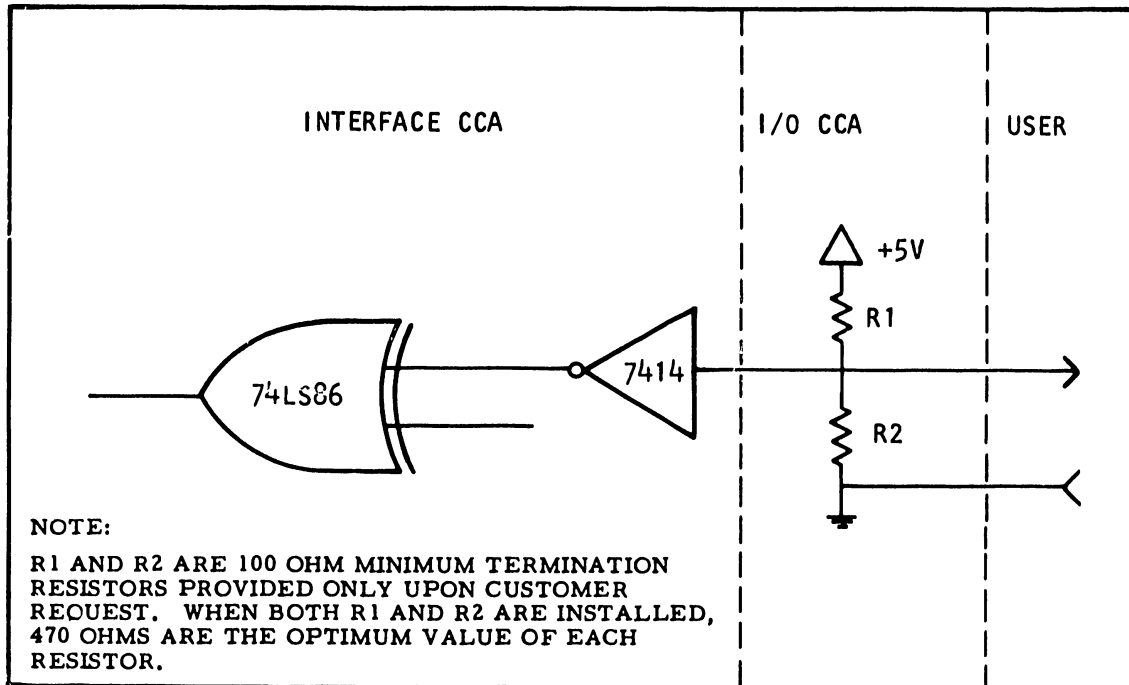


Figure 2-12. Typical Short Line Interface Receiver Circuit

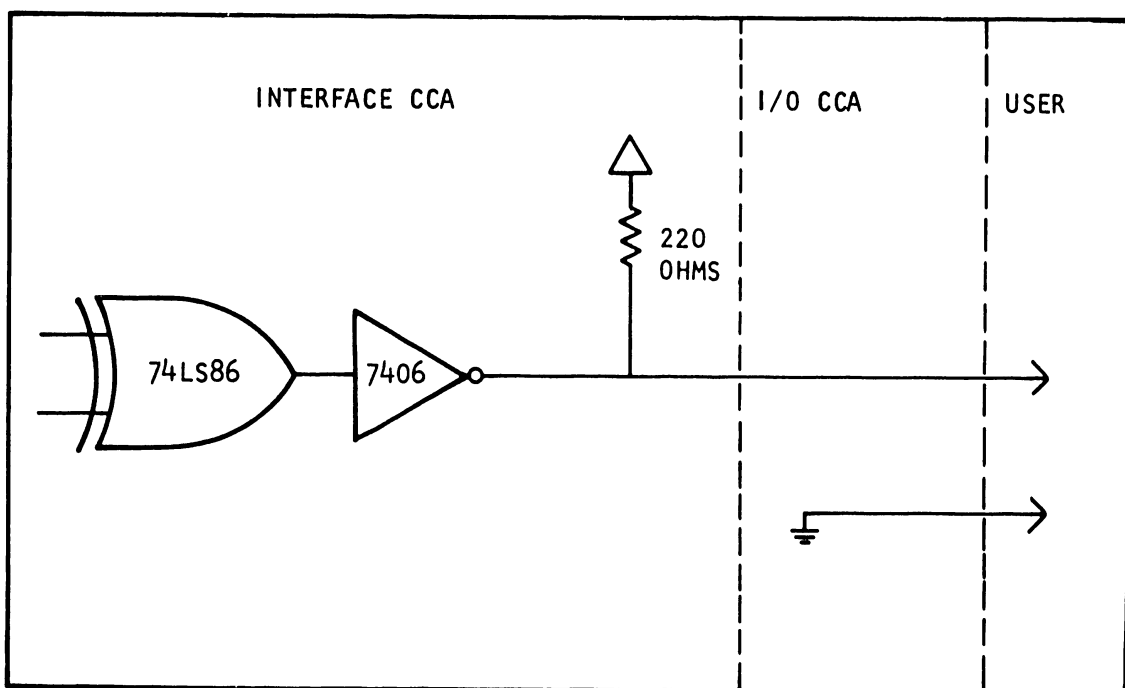
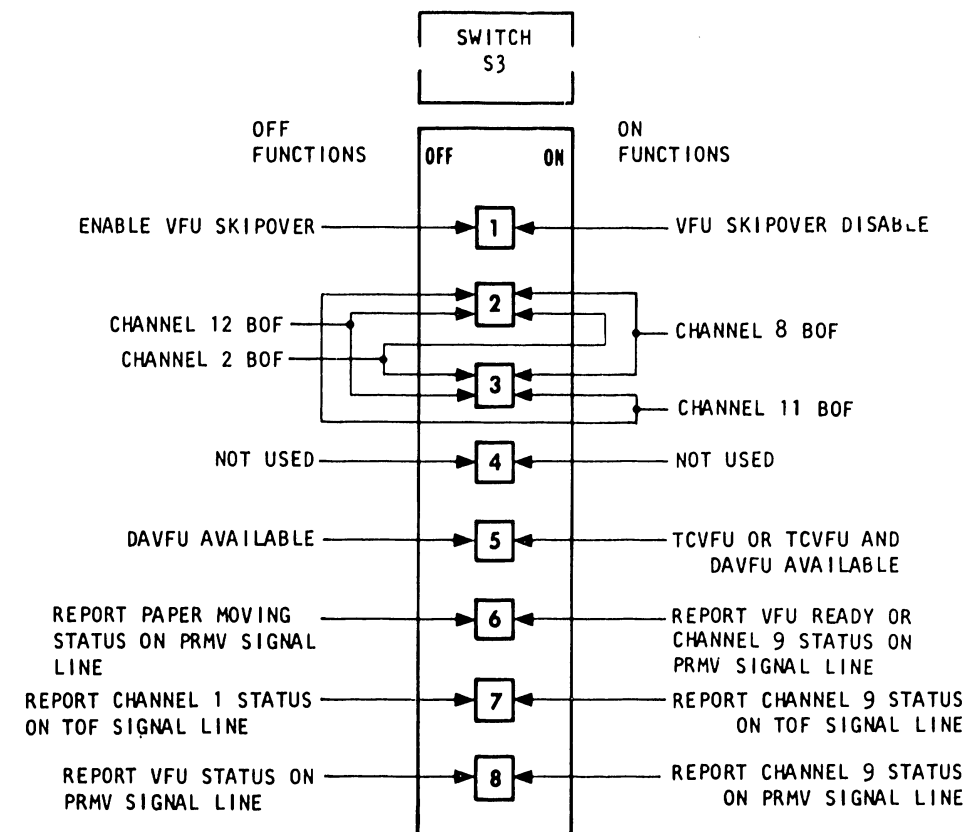
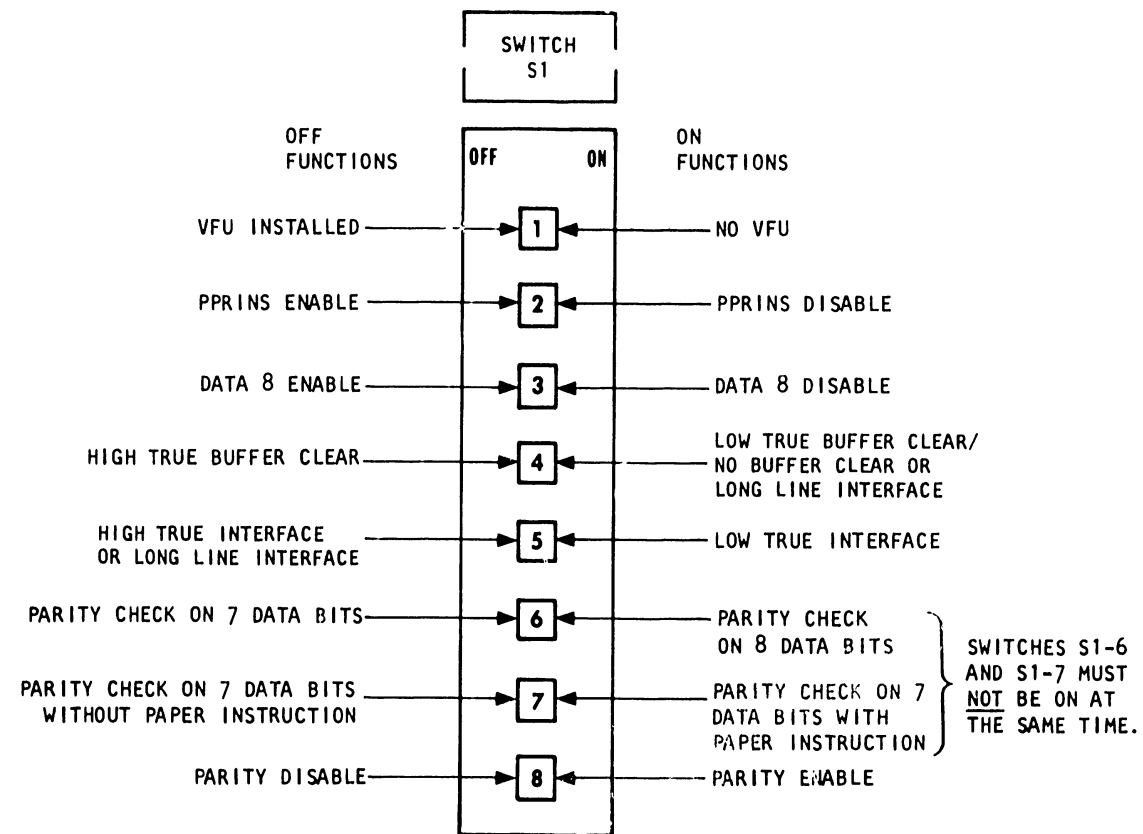
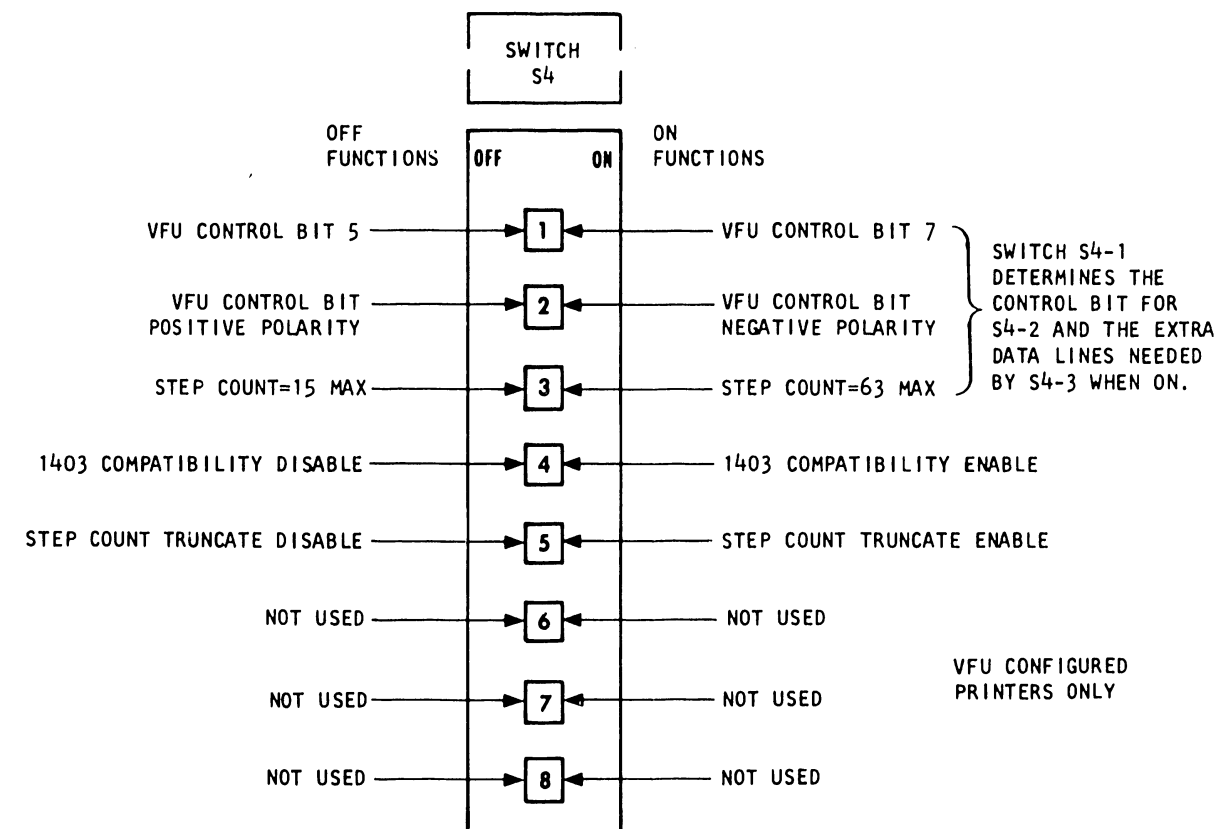
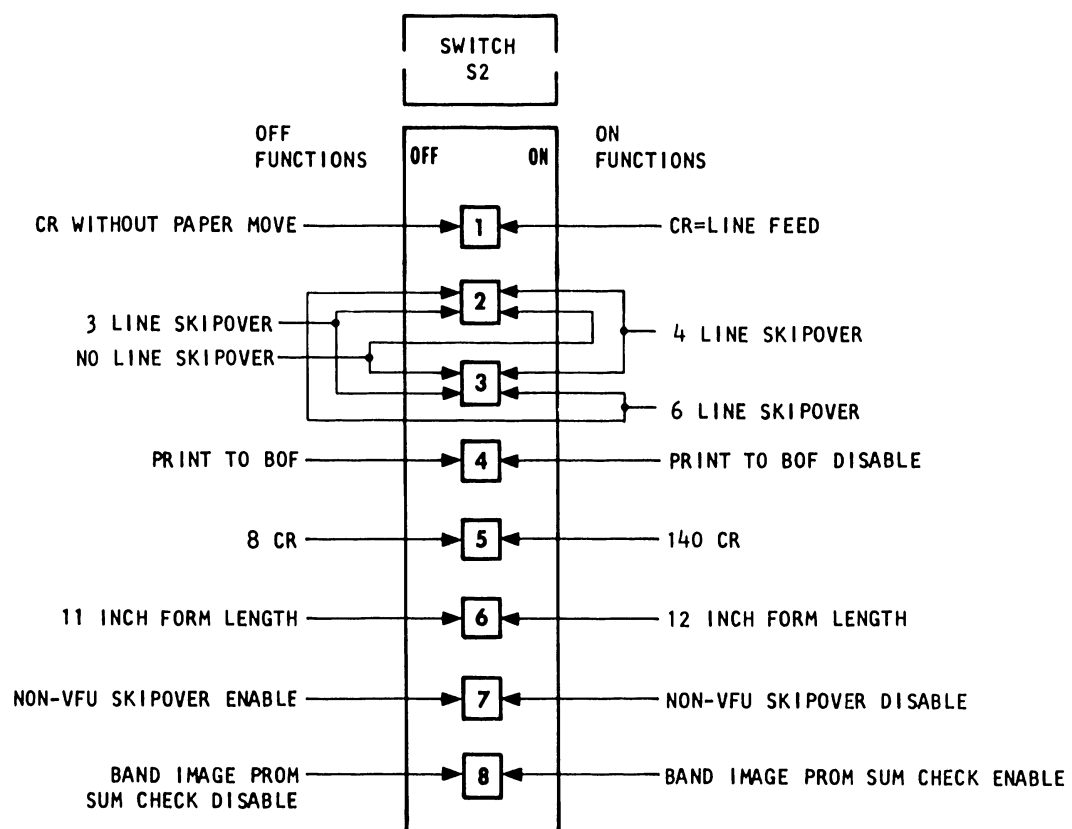


Figure 2-13. Typical Short Line Interface Driver Circuit



VFU CONFIGURED
PRINTERS ONLY



VFU CONFIGURED
PRINTERS ONLY

Figure 2-14. Configuration Switches

TABLE 2-5A. CONFIGURATION SWITCH S1 SETTINGS

NOTE

Configuration Switch S1 is installed on both non-VFU and VFU printers.

Switch	Description	Switch Function	
		When ON	When OFF
S1-1	Not VFU/VFU Verify (SH 10)	Indicates to the user that the VFU option is not installed in the printer; provides a verify path to the user system.	Indicates that the VFU option is installed in the printer; verify path to user system is open. Normal setting for a VFU-equipped printer.
S1-2	PPRINS Disable (SH 6)	Disables the paper instruction line to user control latch U3 when the VFU option is <u>not</u> installed.	Enables the paper instruction line to user control latch U3 when the VFU option is installed.
S1-3	DATA 8 Disable (SH 10)	Configures the printer for a 7-bit interface by disabling the 8th data bit to the user data latch U6.	Configures the printer for an 8-bit interface; the 8th data bit to the user data latch U6 is enabled.
S1-4	Low True BUFFER CLEAR (SH 6)	Configures the printer for a low true BUFFER CLEAR signal at U48; when the buffer clear option is not wanted, the switch is on and the BUFFER CLEAR signal floats on the I/O.	Configures the printer for a high true BUFFER CLEAR signal at U48.
S1-5	Low True Interface (SH 6)	Configures the printer for low true interface operation.	Configures the printer for high true or Line Line interface operation.
S1-6	Parity 8/ Data 8 (SH 10)	Causes the 8th input to the parity generator U20 to become Data 8.	Causes the 8th input to the parity generator U20 to be "open" or as defined by S1-7.
S1-7	Parity 8/ Paper Instruction (SH 10)	Causes the 8th input to the parity generator U20 to become Paper Instruction (P1). In a non-VFU printer with a 7-bit interface and the parity option, the switch should be on to drive a logic "0" to U20-2.	Causes the 8th input to the parity generator U20 to be "open" or as defined by S1-6.
CAUTION			
S1-6 and S1-7 should <u>never</u> be on at the same time.			
S1-8	Parity Enable (SH 10)	Enables the printer to perform a parity check on the data lines.	Disables the parity check.

TABLE 2-5B. CONFIGURATION SWITCH S2 SETTINGS

NOTE

Configuration Switch S2 is installed on both non-VFU and VFU printers.

Switch	Description	Switch Function																
		When ON	When OFF															
S2-1	CR-Line Feed (SH 8)	Causes the printer to interpret a CR code as a carriage return and line feed operation.	Causes the printer to interpret a CR code as a carriage return only.															
S2-2 S2-3	Skipover 20 Skipover 21 Select (SH 8)	<p>Used in one of the following combinations to select one of four skipover conditions.</p> <table border="1"> <thead> <tr> <th>S2-2</th> <th>S2-3</th> <th>Number of Lines Skipped</th> </tr> </thead> <tbody> <tr> <td>OFF</td> <td>OFF</td> <td>3 Lines</td> </tr> <tr> <td>OFF</td> <td>ON</td> <td>6 Lines</td> </tr> <tr> <td>ON</td> <td>OFF</td> <td>No Lines</td> </tr> <tr> <td>ON</td> <td>ON</td> <td>4 Lines</td> </tr> </tbody> </table>		S2-2	S2-3	Number of Lines Skipped	OFF	OFF	3 Lines	OFF	ON	6 Lines	ON	OFF	No Lines	ON	ON	4 Lines
S2-2	S2-3	Number of Lines Skipped																
OFF	OFF	3 Lines																
OFF	ON	6 Lines																
ON	OFF	No Lines																
ON	ON	4 Lines																
<p>NOTE</p> <p>The selection of skipover also defines the timing of the Bottom of Form (BOF) signal output to the user.</p>																		
S2-4	Disable BOF (SH 8)	Causes the printer to stop printing after detection of the paper low signal and to display a 16 STATUS condition which allows single step printing to the bottom of the paper.	Causes the printer to continue to print until the Bottom of Form (BOF) signal is generated after detection of the paper low switch. Operator intervention will allow single step printing to continue in the same way as when the switch is ON.															
S2-5	8 or 140 Carriage Returns (SH 8)	Allows a maximum of 140 consecutive carriage returns.	Allows a maximum of 8 consecutive carriage returns.															
S2-6	11" or 12" Form Length (SH 8)	Defines the form length as 12 inches. Disabled when the FLS option is used.	Defines the form length as 11 inches. Disabled when the FLS option is used.															
S2-7	Disable S2-2 and S2-3 (SH 8)	Disables the skipover as defined by S2-2 and S2-3; allows the user to control the number of lines to be printed after the BOF signal is detected.	Enables the skipover as defined by S2-2 and S2-3.															
S2-8	BIP Sum Check (SH 8)	Enables a band image PROM sum check.	Causes no band image PROM sum check to occur. Normal setting.															

TABLE 2-5C. CONFIGURATION SWITCH S3 SETTINGS

NOTE

Configuration Switch S3 is installed on VFU printers only.

Switch	Description	Switch Function																
		When ON	When OFF															
S3-1	Enable VFU Skipover (SH 11)	Enables the VFU skipover option in which a paper move command that results in a position between BOF and TOF will cause paper motion to continue until the next TOF is reached.	Disables the VFU skipover option.															
S3-2 S3-3	BOF Tape Channel Select (SH 11)	Used in one of the following combinations to select one of four possible BOF tape channels. <table border="0"> <tr> <td style="text-align: center;"><u>S3-2</u></td> <td style="text-align: center;"><u>S3-3</u></td> <td style="text-align: center;"><u>BOF Tape Channel</u></td> </tr> <tr> <td style="text-align: center;">OFF</td> <td style="text-align: center;">OFF</td> <td style="text-align: center;">12</td> </tr> <tr> <td style="text-align: center;">OFF</td> <td style="text-align: center;">ON</td> <td style="text-align: center;">11 (Reference Tape channels</td> </tr> <tr> <td style="text-align: center;">ON</td> <td style="text-align: center;">OFF</td> <td style="text-align: center;">2 1 through 12)</td> </tr> <tr> <td style="text-align: center;">ON</td> <td style="text-align: center;">ON</td> <td style="text-align: center;">8</td> </tr> </table>	<u>S3-2</u>	<u>S3-3</u>	<u>BOF Tape Channel</u>	OFF	OFF	12	OFF	ON	11 (Reference Tape channels	ON	OFF	2 1 through 12)	ON	ON	8	
<u>S3-2</u>	<u>S3-3</u>	<u>BOF Tape Channel</u>																
OFF	OFF	12																
OFF	ON	11 (Reference Tape channels																
ON	OFF	2 1 through 12)																
ON	ON	8																
S3-4	(SH 11)	Not Used	Not Used															
S3-5	TCVFU or DAVFU (SH 11)	Indicates that a Tape Control Vertical Form Unit (TCVFU) or Tape Control and Direct Access Format Unit is available. Tape is read automatically on power up.	Indicates that the Direct Access Vertical Format Unit (DAVFU) option is available.															
S3-6	Report Switch or Paper Moving Status (SH 11)	Enables reporting of the VFU Ready or Channel 9 status on the Paper Moving (PRMV) interface signal line; used with S3-8.	Enables reporting of the paper moving status on the Paper Moving (PRMV) interface signal line.															
S3-7	Channel 9 or Channel 1 Status (SH 11)	Enables reporting of Channel 9 status on the Top of Form (TOF) interface signal line.	Enables reporting of Channel 1 status on the Top of Form (TOF) interface signal line.															
S3-8	Channel 9 or VFU Ready Status (SH 11)	Enables reporting of Channel 9 status on the PRMV interface signal line when S3-6 is ON.	Enables reporting of VFU Ready Status on the PRMV interface signal line when S3-6 is ON.															

TABLE 2-5D. CONFIGURATION SWITCH S4 SETTINGS

NOTE

Configuration Switch S4 is installed on VFU printers only.

Switch	Description	Switch Function	
		When ON	When OFF
S4-1	VFU Control Bit 2 ⁶ or 2 ⁴ (SH 11)	Enables Data 7 line to be used to decode channel search or step count commands. Polarity is set by S4-2.	Enables Data 5 line to be used to decode channel search or step count commands. Polarity is set by S4-2.
S4-2	VFU Control Bit Polarity (SH 11)	Enables a negative polarity for the control bit set by S4-1. A logic "1" control bit stands for a tape channel command; a logic "0" stands for a line skip command.	Enables a positive polarity for the control bit set by S4-1. A logic "1" control bit stands for a line skip command; a logic "0" stands for a tape channel command.
S4-3	Step Count 15 or 63 Lines Select (SH 11)	Decodes a line skip command for a maximum of 63 lines. The extra data lines selected depend on S4-1.	Decodes a line skip command for a maximum of 15 lines.
S4-4	1403 VFU Compatibility (SH 11)	Enables the 1403 VFU Compatibility option. A user channel search command to advance paper to the next channel stop in a specific channel will <u>not</u> cause paper to advance <u>if</u> paper is positioned at the channel for which the search is being made and no data has been printed in that location.	Disables the 1403 VFU Compatibility option.
S4-5	Step Count Truncate (SH 11)	Enables the Step Count Truncate option. A line skip command that would place the paper past the next top of form will be shortened in order to position the paper at the next top of form.	Disables the Step Count Truncate option.
S4-6		Not Used	Not Used
S4-7		Not Used	Not Used
S4-8		Not Used	Not Used

(c) Interface Device Enable Decoder - A 3-to-8 line decoder/demultiplexer U29 (SH 7) is used to enable one (1) of seven (7) devices for output to the INBUS. When enabled by CONBIT* (Control Bit), ADRBS 12 and ADRBS 13, the decoder outputs one low active signal which then enables another interface device to transfer status or configuration information to the INBUS. Selection of the U29 output is determined by ADRBS 0F, ADRBS 10, and ADRBS 11.

A function table and loading diagram are provided in **figure 2-15** to help understand the operation of the decoder. **Table 2-6** lists the output signals of U29 and their functions.

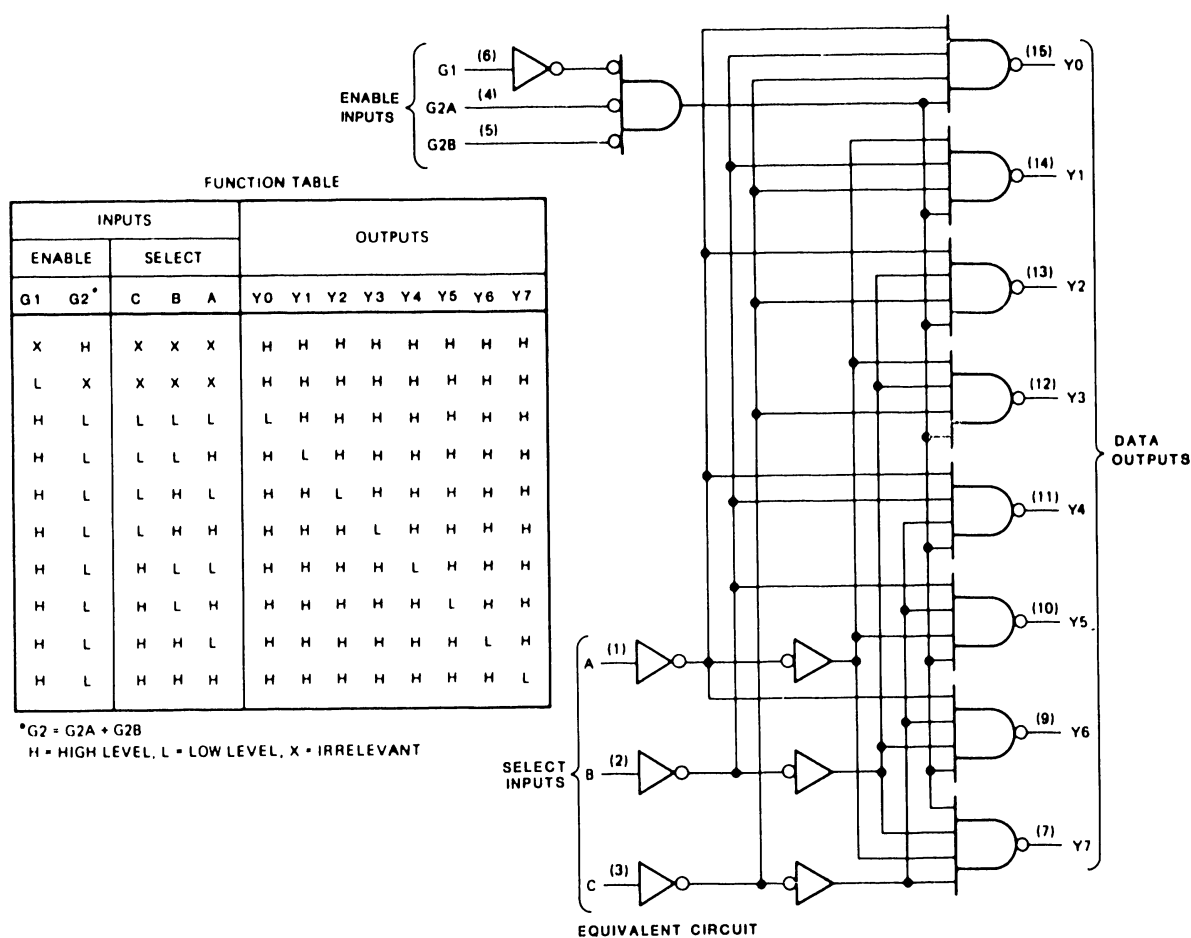


Figure 2-15. Interface Device Enable Decoder (74LS138)

TABLE 2-6. INTERFACE DEVICE ENABLE DECODER SIGNALS

Signal	Devices Enabled	Function
FLSS* (Forms Length Selector Switch)	MEM1 (SH 9)	Places the contents of MEM1, control panel forms length selector switch data, onto the INBUS.
UCL* (User Control Latch)	U7, U8 (SH 8)	Generates CG1* (Configuration Group 1) which selects the user control information (U7 and U8, A inputs) for input to the INBUS.
CG2* (Configuration Group 2)	U7, U8 (SH 8)	Provides output control to let configuration switch S2-1 through S2-8 settings (U7 and U8, B inputs) to be placed on the INBUS.
CG3* (Configuration Group 3)	U24, U53 (SH 11)	Provides the select signal to enable positions of configuration switches S3-1 through S3-4 and S4-1 through S4-4 (U24 and U53, A inputs) to be input to the INBUS.
CG4* (Configuration Group 4)	U24, U53 (SH 11)	Provides the output control signal to place the settings of configuration switches S3-5 through S3-8 and S4-5 through S4-8 (U24 and U53, B inputs) on the INBUS.
INSW* (Interlock Switch)	U2, U9 (SH 9)	Provides output control signal to allow interlock switch, paper motion, ribbon motion, and on line indicator status (U2 and U9, B inputs) on the INBUS.
CPS* (Control Panel Switches)	U2, U9 (SH 9)	Selects the status of the control panel switches (U2 and U9, A inputs) for input to the INBUS.

(d) INBUS Ports - Then INBUS Ports, consisting of quad multiplexers, enable information about the printer status, the configuration switches, forms length select switch, the control panel switches, and the interlock switches onto the INBUS for use by the Processor CCA. The device enable decoder U29 (SH 7) provides the select and output control for the INBUS Ports. A loading diagram and function table are furnished in figure 5-3 in section V.

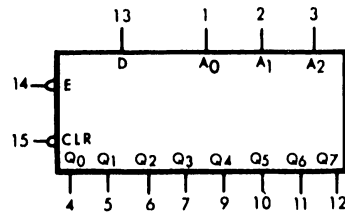
(e) Control Group Enables - The Short Line Interface CCA uses three (3) 8-bit addressable latches and a 3-to-8 line decoder demultiplexer which function as control group devices. The selection of the control group is determined by a Control Group Decoder U65 (SH 29) or U53 (Sh A32) mounted on the Processor CCA.

Under program control, each device receives program instructions over the Address Bus lines 10, 11, 12 and 13 that activate control or status signals for use by other devices on the CCA or by the user. The four (4) control groups used by the Interface CCA are:

- Control Group 0 (U47, SH 7)
- Control Group 3 (U28, SH 7)
- Control Group 5 (U14, SH 7)
- Control Group 6 (U13, SH 6)

(1) Control Group 0 - Signal ECG0* provides the enable for the 8-bit addressable latch U47 (SH 7). Address Bus lines 10, 11, and 12 select the output line and ADRBS 13 determines the logic level of the signal.

A function table and loading diagram are provided in figure 2-16 to aid in understanding the U47 latch operation. Table 2-7 lists the Address Bus lines, their functions, and the output signal conditions that are controlled by Control Group 0.



VC=Pin 16
GND=Pin 8

FUNCTION TABLE

INPUTS					OUTPUTS							
CLR*	E*	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
L	H	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	D							
H	L	H	L	L		D						
H	L	L	H	L			D					
H	L	L	L	H				D				
H	L	H	L	H					D			
H	L	L	H	H						D		
H	L	H	H	H							D	

D=ADRBS INPUT X=DO NOT CARE
OUTPUT OF UNSELECTED LINES=OUTPUT SET IN LAST CYCLE

Figure 2-16. Control Group 0 Latch (74259)

TABLE 2-7. CONTROL GROUP 0 DECODE AND FUNCTIONS

Address Bus Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	Reset User's Paper Moving Signal Reset On Line Clear	U47-4 low; PRMV at J5-16 inactive. U47-5 low; READY low to clear On Line F/F (U43).
0	0	0	1		
0	0	1	0	N/A	
0	0	1	1	N/A	
0	1	0	0	N/A	
0	1	0	1	N/A	
0	1	1	0	N/A	
0	1	1	1	N/A	
1	0	0	0	Set User's Paper Moving Signal Set On Line Clear	
1	0	0	1		
1	0	1	0	N/A	
1	0	1	1	N/A	
1	1	0	0	N/A	
1	1	0	1	N/A	
1	1	1	0	N/A	
1	1	1	1	N/A	

(2) Control Group 3 - Signal ECG3* enables one (1) output from either U28 (SH 7) on the Interface CCA or U45 (SH 36) on the Timing and Status CCA. Each active output is in a low logical state. Table 2-8 lists the Address Bus line signals, the functions, and the output signal conditions which are controlled by Control Group 3. See figure 2-15 for a function table and loading diagram for the U28 and U45 decoders' operation.

TABLE 2-8. CONTROL GROUP 3 DECODE AND FUNCTIONS

Address Bus Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	N/A	
0	0	0	1	Stepper Phase Shift Clock	STPSHF* active to the Power Board
0	0	1	0	Load Column or Print Phase	LDCOL* active to U46-9 (SH 34)
0	0	1	1	Disable VCL	VCLOFF* low to U44-3, ENVCL inactive
0	1	0	0	Enable VCL	VCLON* low to U44-4, ENVCL active
0	1	0	1	Enable +38 Volts	38VON* low to U44-10, EN38V* active
0	1	1	0	Disable +38 Volts	38VOFF* low to U44-11, EN38V* inactive
0	1	1	1	Clear System Status Faults	CLRFLT* active to U50-11 (SH 35)
1	0	0	0	Clear Ribon Motion Sensor	CLSEN* active to U49-9 (SH 9)
1	0	0	1	Load VFU Address Register	LVFUAR active to U50-11 (SH 11)
1	0	1	0	Clear Paper Motion Flag	RMTFLG* active to U43-13 (SH 8)
1	0	1	1	Set Master Clear Switch Flip-Flop	SMCSFF* active to U10-2 (SH 9)
1	1	0	0	N/A	
1	1	0	1	Load Display	LDISPY* active to enable U45
1	1	1	0	N/A	
1	1	1	1	Clear Buffer Clear Latch	RBCLRF* active to reset U21

(3) Control Group 5 - Signal ECG5* provides the enable for the 8-bit addressable latch U14 (SH 7). Address Bus lines 10, 11, and 12 select the output line, and ADRBS 13 determines the logic level of high or low.

Table 2-9 lists the Address Bus line signals, their functions, and the output signal conditions which are controlled by Control Group 5. See figure 2-16 for a function table and loading diagram for the U14 latch operation.

TABLE 2-9. CONTROL GROUP 5 DECODE AND FUNCTIONS

Address Bus Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	Reset Parity Error	U14-4 low input to U16-4 inactivates PARERR
0	0	0	1	Reset Ready	U14-5 low input to U15-9 inactivates RDY
0	0	1	0	Reset Online	U14-6 low input to U16-9 inactivates ONLN
0	0	1	1	Reset Ident 1 Data Bit	U14-7 low input to U16-12 resets IDNT1 to low
0	1	0	0	Reset Top of Form	U14-9 low input to U17-1 inactivates TOF
0	1	0	1	Reset Bottom of Form	U14-10 low input to U17-4 inactivates BOF
0	1	1	0	N/A	
0	1	1	1	Reset Demand	U14-12 low to U30-2 and U15-2 inactivates DEM
1	0	0	0	Set Parity Error	U14-4 high to U16-4 activates PARERR
1	0	0	1	Set Ready	U14-5 high to U15-9 activates RDY
1	0	1	0	Set Online	U14-6 high to U16-9 activates ONLN
1	0	1	1	Set Ident 1 Data Bit	U14-7 high to U16-12 sets IDNT1 to high
1	1	0	0	Set Top of Form	U14-9 high to U17-1 activates TOF
1	1	0	1	Set Bottom of Form	U14-10 high to U17-4 activates BOF
1	1	1	0	N/A	
1	1	1	1	Set Demand	U14-12 high to U30-2 and U15-12 activates DEM

(4) Control Group 6 - Signal ECG6* provides the enable for the 8-bit addressable latch U13 (SH 6). Address Bus lines 10, 11, and 12 select the output line and ADRBS 13 determines the logic level of the output. Table 2-10 lists the Address Bus line signals, their functions, and the output signal conditions that are controlled by Control Group 6. See figure 2-16 for a function table and loading diagram for the U13 latch operation.

TABLE 2-10. CONTROL GROUP 6 DECODE AND FUNCTIONS

Address Bus Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	Disable Tape Channel High	U13-4 low; ENTCH low to U4 and U5 to select TPCH1*-6* inputs
0	0	0	1	Disable Tape Channel Low	U13-5 low; ENTCL low to U11-11; w/U13-4 determines ENTAPE*
0	0	1	0	Select Low Byte VFU RAMs	U13-6 low; U38 and U40 select active (SH 11)
0	0	1	1	N/A	
0	1	0	0	Reset Online Light	U13-9 low; ONLNLT inactive to U2-10 (SH 9)
0	1	0	1	Tape Motor Off	U13-10 low; TMON* inactive
0	1	1	0	Disable User Data and Control	U13-11 low; ENUSER* inactive (not used in 1000 LPM printers)
0	1	1	1	Reset Ident 0 Data Bit	U13-12 low; IDNT0 low to user
1	0	0	0	Enable Tape Data High	U13-4 high; ENTCH high to U4 and U5 to select TPCH7*-12* inputs
1	0	0	1	Enable Tape Data Low	U13-5 high; ENTCL high to U11-11; ENTAPE* active
1	0	1	0	Select High Byte VFU RAMs	U13-6 high; U36 and U39 select active (SH 11)
1	0	1	1	N/A	
1	1	0	0	Set Online Light	U13-9 high; ONLNLT active to U2-10 (SH 9)
1	1	0	1	Tape Motor On	U13-10 high; TMON* active
1	1	1	0	Enable User Data and Control	U13-11 high; ENUSER* active (not used in 1000 LPM printers)
1	1	1	1	Set Ident 0 Data Bit	U13-12 high; IDNT0 high to user

(f) Addressable Latches - In addition to the latches used as control group decoders, a number of dual D-type flip-flops serve to latch data for use by other interface and printer devices. The main functions controlled by these latches include:

- Buffer Clear U21 (SH 6)
- Strobe-Respond U27 (SH 6)
- Paper Status U43 (SH 8)
- On Line Flip-Flop U43 (SH 8)

(g) User Data Latch - The User Data Latch U6 (SH 10) drives the user data on to the RGBUS for use by the Processor CCA or input to the VFU memory RAMs. The latch is enabled by ANDing UDL* and ENUSER*.

(h) Parity Checker - By setting configuration switch S1-8 to the on position, the Parity Checker U20 (SH 10) provides parity control for a maximum of eight (8) data lines. The parity code is defined by ODDPAR (Odd Parity) and the user's PARBIT (Parity Bit). The combination of data bits selected for the parity check is determined by the setting of configuration switches S1-3, S1-6, and S1-7.

(i) Display Decoders - Two (2) BCD to seven (7) segment display decoders, U1 and U12 (SH 12), are used by the Interface CCA to convert status information received from OUTBS0-7 into the appropriate LED indicator display on the control panel. Numbers 00 to 99 are generated in this way. Fault signals CLKFLT* (Clock Fault), 5VFLT* (5 Volt Fault), and HOT* are hardwired to diodes on the Interface CCA to generate the status indications C, P, and H.

(j) Forms Length Selector Switch Memory - When the optional forms length selector switch is installed, an additional PROM, MEM1 (SH 9) is mounted on the Interface CCA. The 256 x8 PROM stores the format data input from the form length select switch mounted on the control panel and, under processor control, places it on the INBUS.

(k) VFU Memory - Four (4) 256 x 4 RAMs, U36, U38, U39, and U40 (SH11), store the format data input by a 12 channel tape reader directly by the user. A D-type flip-flop U50 acts as a latched address register for the VFU memory devices.

2. Operational Description - The functions of the Interface CCA may be divided into two (2) major areas --- user printer data transfer and interface processor data transfer. (See figure 2-17.) With the exception of the hardwired CLKFLT*, HOT*, and 5VFLT*, the interface operates under processor control.

(a) User/Printer Data Transfer - Communications between the user and printer is on the demand/response handshaking basis described in paragraph 2.2.1. Data from the user is input through the I/O CCA to connector J5 (SHs 6 and 10).

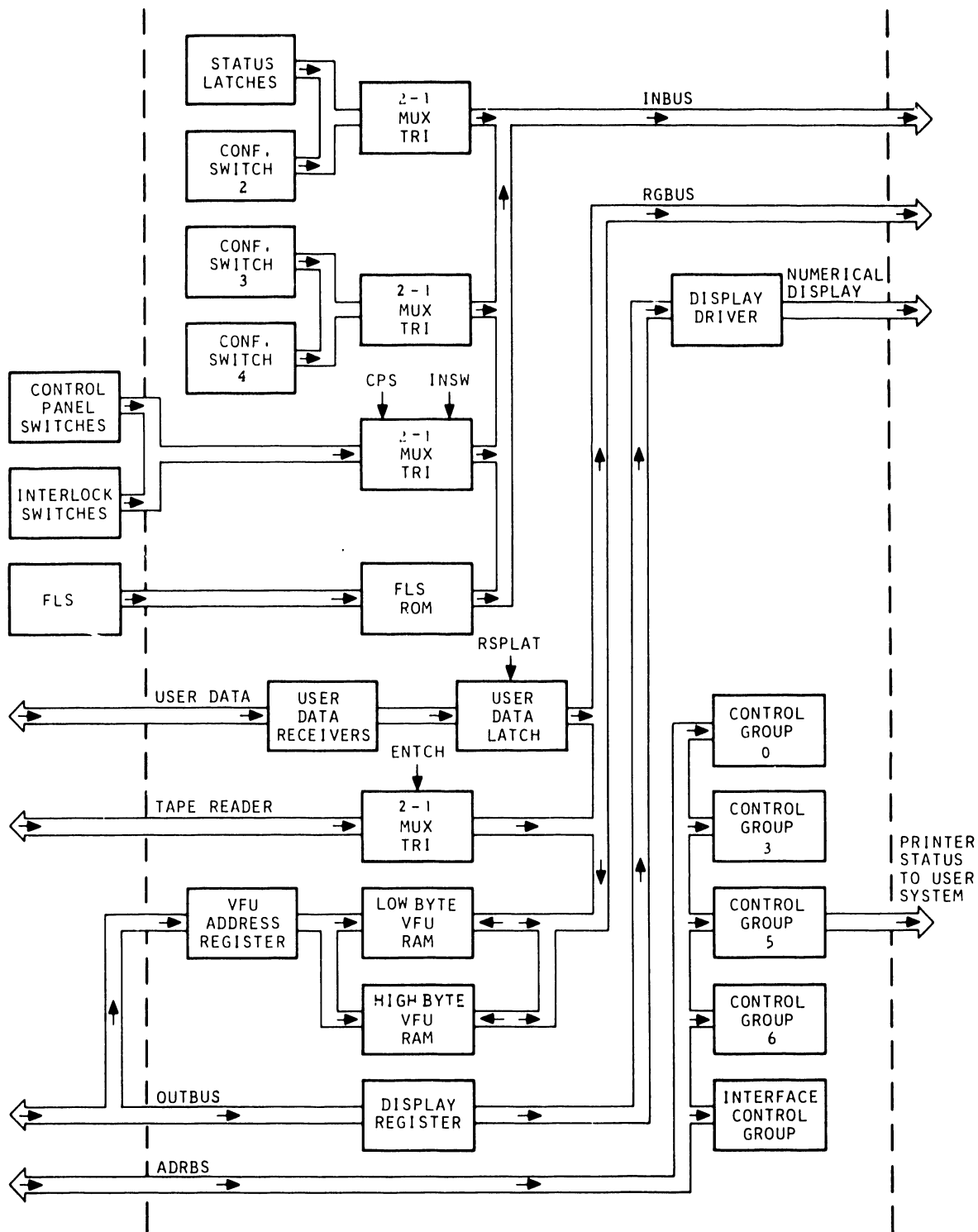


Figure 2-17. Short Line Interface CCA Block Diagram

Input data is isolated and inverted by U33 and U34 before being input to the EXCLUSIVE OR gates U17, U18, U19, and U48. If switch S1-5 (SH 6) is set to the on position, the optional LOTRU* (Low True) signal, also input to the EXCLUSIVE OR gates, will cause all incoming data to be inverted.

Data then goes to the user data latch U6 (SH 10) which, when clocked by the positive transition of the RSPLAT (Respond Latch) signal, sets the outputs to the logic state of the inputs. RSPLAT is generated by the strobe flip-flop U27 (SH 6).

If the interface switch S1-8 is in the on position, a parity check is performed upon each incoming data byte by the parity checker U20 (SH 10). Options of eight (8) data bits, seven (7) data bits, or seven (7) data bits plus Paper Instruction (PI) are available for the parity check.

If a parity error is detected during data load or DAVFU load, the Processor CCA will activate ECG3* (Control Group 3) (SH 7) in order to send the parity error status code to the Interface CCA. When enabled by LDISPY* (Load Display), latch U45 outputs the status to the control panel STATUS indicators via decoders U1 and U12. See table 2-8 for the Address Bus lines 10-13 signal levels used to activate LDISPY*.

In addition to monitoring the incoming user data, the Interface CCA is responsible for informing the user of the printer's status. The Control Group Five multiplexer U14 (SH 7) transmits, through the J5 connector, the signals which tell the user when the printer is on line (ONLN), Ready (RDY), and can receive data (DEM).

Other printer signals tell the user that paper is moving (PRMV), that the paper is at the Top or Bottom of Form (TOF, BOF), or that a Parity Error has occurred (PARERR). The two (2) signals IDENT0 and IDENT1 identify the band type for the user system. See table 2-9 for the Address Bus line 10-13 logic levels needed to activate these signals.

(b) Interface/Processor Data Transfer - Once the output logic levels of the user data latch have been set, an output control signal generated by gating ENUSER* (Enable User) and UDL* (User Data Latch) at U30 (SH 10) will transmit the data to the Processor CCA via the RGBUS. The generation of UDL* is a function of the Register Enable Decoder U5 or U34 on the Processor CCA (SH 29 or SH 32). ENUSER* is an output of the Control Group 6 circuitry.

In addition to latching the user data for transmission to the processor, the Interface CCA, under program control, multiplexes the configuration, control panel, interlock, and forms length selector switch states for use by the Processor CCA. The Device Enable Decoder, six (6) multiplexers, and a 256 x 8 RAM make up the circuitry that drives the various switch conditions onto the INBUS.

The Device Enable Decoder U29 (SH 7) is enabled by CONBIT* (Condition Bit), ADRBS 12, and ADRBS 13 from the Processor CCA. The select signals, ADRBS 0F, ADRBS 10, and ADRBS 11, determine which pair of multiplexers or MEM1 will be activated by U29's output. Multiplexers U7 and U8 (SH 8) transmit user control data, such as BFCLR* (Buffer Clear) and PINSL (Paper Instruction Latch) and configuration switch 2 settings.

Multiplexers U2 and U9 (SH 9) drive the conditions of the interlock switches or the control panel switches on to the INBUS. U24 and U53 (SH 11), which are installed on the Interface CCA when an optional VFU is used, input configuration switches 3 and 4 settings on to the INBUS.

The FLSS* (Forms Length Selector Switch) output by U29 activates the output of the form length select RAM MEM1 for input to the INBUS. MEM1 is installed as an option on the Interface CCA. See table 2-6 for the Interface Device Enable Decoder Signals and their functions.

b. Long Line Interface CCA (Option)

The Long Line Interface CCA operates in the same way as the Short Line Interface CCA. With the exception of the receivers and drivers, the devices used are the same though the reference designations may vary. By using 8820 and 8830 class line receivers and drivers, the printer may be used at an extended distance (up to 150 meters) from the user's controller.

Figures 2-18 and 2-19 illustrate the typical Long Line interface receiver and driver circuits. Logic diagram sheets 14-22 in section V of volume II provide the complete circuit plan for the Long Line Interface CCA.

c. Centronics-Compatible Interface CCA (Option)

To configure the printer for the Centronics-Compatible operation, the standard Short Line Interface CCA is replaced by the Centronics-Compatible Interface CCA. Though the overall principles of operation are similar, significant differences exist and are discussed in the following paragraphs. The first section describes the major circuitry devices used on the Centronics-Compatible CCA. The second section details the operation of the CCA.

It is suggested that the Short Line Interface CCA description in paragraph 2.3.2, subparagraph a be read for general understanding of device and interface operation. See logic diagram sheets B5 through B13 in section V of volume II.

1. Device Description - The following description of devices used by the Centronics-Compatible Interface CCA deals only with those which are unique to the CCA. The description of the control panel display devices, the form length select devices, control group and configuration group devices provided for the Short Line Interface CCA apply for the Centronics-Compatible CCA though the reference designations may vary. Figure 2-22, at the end of the device description, provides a summary of the various devices and their functions.

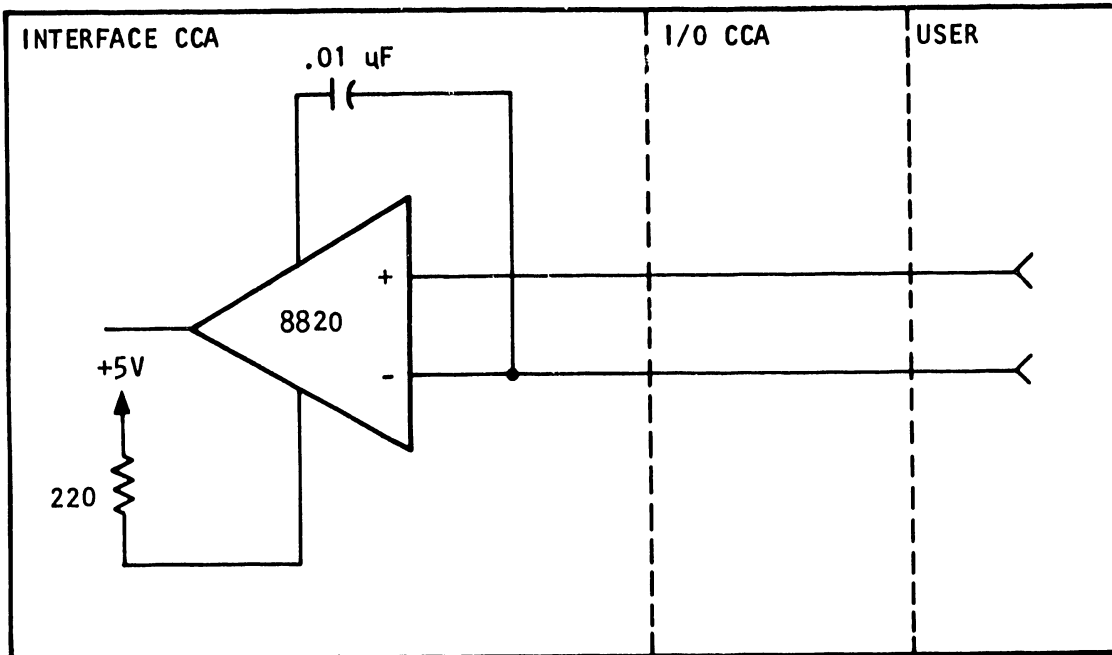


Figure 2-18. Typical Long Line Interface Receiver Circuit

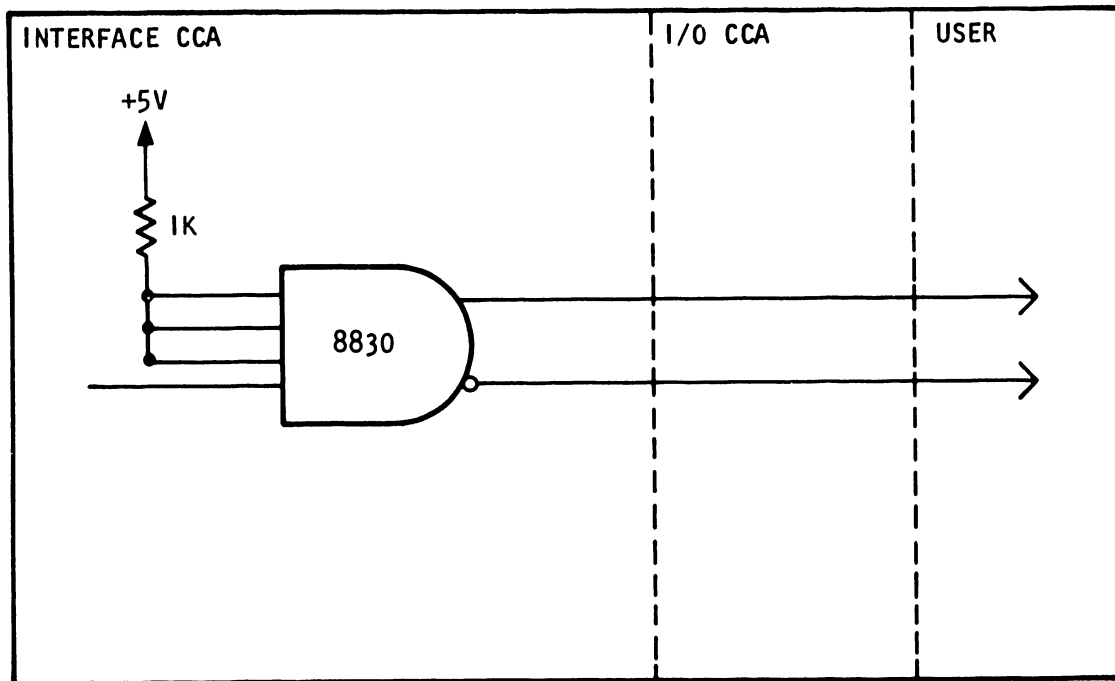


Figure 2-19. Typical Long Line Interface Driver Circuit

(a) Receiver and Transmitter Circuits - Signals between the printer and the user system are transmitted over an I/O cable of twisted pair wires by Hex Schmitt trigger receivers U30 and U31 (SHs B5, B6, B10) and by Hex Inverter Buffer/Drivers U15 and U28 (SH B7). Figures 2-20 and 2-21 illustrate the typical receiver and transmitter circuits used by the Centronics-Compatible Interface CCA.

(b) Configuration Switches - Four (4) configuration switches mounted on the CCA are used to configure the printer to meet various user requirements. Up to eight (8) switch-selectable options are available with each switch. Tables 2-11A through 2-11D define the switch settings currently available for the Centronics-Compatible CCA.

TABLE 2-11A. CENTRONICS-COMPATIBLE CONFIGURATION SWITCH S1 SETTINGS

Switch	Description	Switch Function	
		When ON	When OFF
S1-1	Not Used		
S1-2	Not Used		
S1-3	Data 8 Disable (SH B10)	Configures the printer for a 7-bit interface by disabling the 8th data bit to the user data decoder MEM2 and the user data latch U16.	Configures the printer for an 8-bit interface.
S1-4	Input Prime Enable (SH B5)	Configures the printer for input prime operation. The user-generated signal clears the printer buffer and initializes the interface logic.	Disables input prime operation.
S1-5	Not Used		
S1-6	Not Used		
S1-7	Not Used		
S1-8	Not Used		

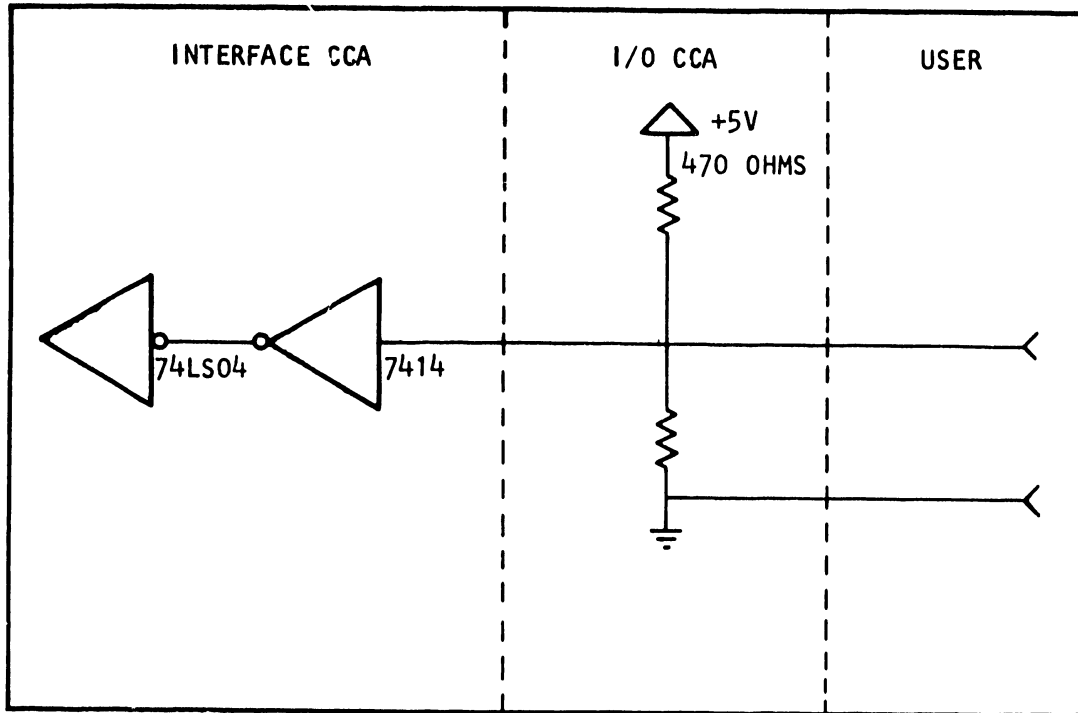


Figure 2-20. Typical Centronics-Compatible Interface Receiver Circuits

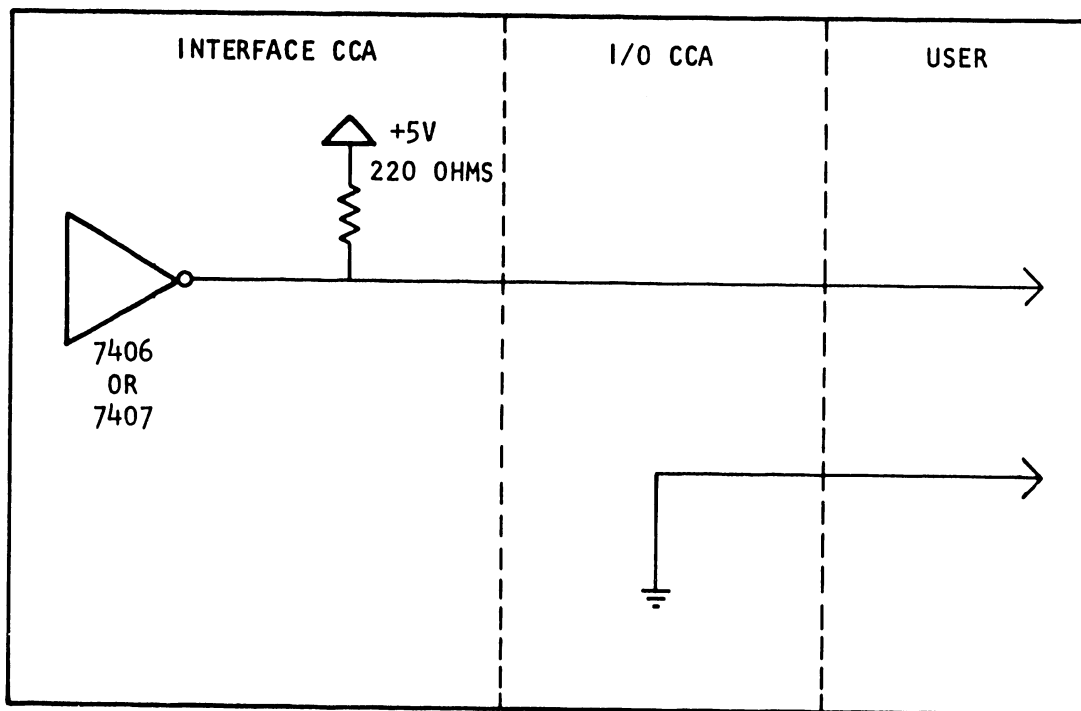


Figure 2-21. Typical Centronics-Comaptible Interface Driver Circuits

TABLE 2-11B. CENTRONICS-COMPATIBLE CONFIGURATION SWITCH S2 SETTINGS

Switch	Description	Switch Function																
		When ON	When OFF															
S2-1	CR=Line Feed (SH B8)	Causes the printer to interpret a CR code as a carriage return and line feed operation; data is printed before paper is moved.	Causes the printer to interpret a CR code as a carriage return only.															
S2-2 S2-3	Skipover 20* Skipover 21 (SH B8)	Used in one of the following combinations to select one of the following skipover conditions: <table border="0" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;">S2-2</td> <td style="text-align: center;">S2-3</td> <td style="text-align: center;"><u>Number of Lines Skipped</u></td> </tr> <tr> <td style="text-align: center;">OFF</td> <td style="text-align: center;">OFF</td> <td style="text-align: center;">3 Lines</td> </tr> <tr> <td style="text-align: center;">OFF</td> <td style="text-align: center;">ON</td> <td style="text-align: center;">6 Lines</td> </tr> <tr> <td style="text-align: center;">ON</td> <td style="text-align: center;">OFF</td> <td style="text-align: center;">No Lines</td> </tr> <tr> <td style="text-align: center;">ON</td> <td style="text-align: center;">ON</td> <td style="text-align: center;">4 Lines</td> </tr> </table>	S2-2	S2-3	<u>Number of Lines Skipped</u>	OFF	OFF	3 Lines	OFF	ON	6 Lines	ON	OFF	No Lines	ON	ON	4 Lines	
S2-2	S2-3	<u>Number of Lines Skipped</u>																
OFF	OFF	3 Lines																
OFF	ON	6 Lines																
ON	OFF	No Lines																
ON	ON	4 Lines																
S2-4	BOF Disable* (SH B8)	Causes the printer to stop printing after detection of the paper low signal and to display a 16 STATUS condition which allows single step printing to the bottom of the paper.	Causes the printer to continue printing until the BOTTOM OF FORM signal is generated after detection of the paper low switch. Operator intervention will allow single step printing to continue in the same way as when the switch is ON.															
S2-5	Line Feed on Buffer Full (SH B8)	Allows paper to move one (1) line after a buffer full condition (132) is detected and data has been printed.	Causes the printer to automatically print data when the print buffer is full (132); paper will not move unless a paper move code is received.															
S2-6	11" or 12" Form Length (SH B8)	Defines the form length as 12 inches. Disabled when the FLS option is used.	Defines the form length as 11 inches. Disabled when the FLS option is used.															
S2-7	Delete Code Enable (SH B8)	Allows the user to clear the print buffer by sending a delete code (Hex 7F).	Causes the printer to acknowledge the delete code and set busy; the printer buffer is not changed.															
S2-8	8 or 140 CR (SH B8)	Allows a maximum of 140 consecutive carriage returns.	Allows a maximum of 8 consecutive carriage returns.															

*Note that the Centronics-Compatible printer defines the bottom of form as the line following the last printable line of the page. No printing occurs on this line. The skipover condition is also affected.

TABLE 2-11C. CENTRONICS-COMPATIBLE CONFIGURATION
SWITCH S3 SETTINGS

Switch	Description	Switch Function	
		When ON	When OFF
S3-1	VFU Skipover (SH B11)	Enables the VFU Skipover option in which a paper move command that results in a position between BOF and TOF will cause paper motion to continue until the next TOF is reached.	Disables the VFU Skipover option.
S3-2	Print on Paper Feed (SH B11)	Causes printable data to be printed when a Line Feed (LF), Form Feed (FF), or Vertical Tab (VT) command is received.	Disables the Print on Paper Feed Command.
S3-3	Double Space on Line Feed or STEP Switch (SH B11)	Causes paper to advance two (2) lines for each Line Feed (LF) command received and when the STEP switch is pressed.	Disables the Double Line Feed Option.
S3-4	Not Used		
S3-5	Tape Reader Available (SH B11)	Indicates that a 12 Channel Tape Reader is available; tape is read automatically on power up if control panel FLS/VFU switch is in the VFU position.	Indicates that a 12 Channel Tape Reader is <u>not</u> available.
S3-6	Not Used		
S3-7	Not Used		
S3-8	Not Used		

TABLE 2-11D. CENTRONICS-COMPATIBLE CONFIGURATION SWITCH S4 SETTINGS

Switch	Description	Switch Function	
		When ON	When OFF
S4-1*	Enable 136 Column Printing (SH B11) (1000 LPM Only)	Allows the printing of 136 columns when the 136 print column option is installed. Without 136 print column capability, the last four characters will be lost.	Disables the printing of 136 columns and enables printing of 132 columns.
S4-2	Print Delete Code (SH B11) (1000 LPM Only)	Makes the delete code (Hex 7F) a printable character; BUSY is not set if the 250661-001 Decode PROM is installed.	Disables the print delete code option. BUSY will be set even if the 250661-001 Decode PROM is installed.
S4-3	Not Used		
S4-4	Not Used		
S4-5	Step Count Truncate (SH B11)	Enables the Step Count Truncate option. A line skip command that would place the paper past the next top of form will be shortened in order to position the paper at the next top of form.	Disables the Step Count Truncate option.
S4-6	Not Used		
S4-7	Not Used		
S4-8	Not Used		

* Automatic printing on buffer full, Switch S2-5, is dependent on the setting of this switch.

(c) Interface Device Enable Decoder and INBUS Ports -

A 3-to-8 line decoder/demultiplexer U42 (SH B7) is used to enable one (1) of seven (7) devices for input to the INBUS. INBUS Ports U7, U8, U20, U6, U17, and MEM 1 (SHs B8, B9, and B11) provide the circuitry needed to place information about printer status and configuration, interlock, control panel, and forms length selector switches onto the INBUS for use by the Processor CCA.

(d) Control Group Enables - The Centronics-Compatible Interface CCA uses three (3) 8-bit addressable latches and two (2) 3-to-8 line decoder/demultiplexers as control group enable devices. The selection of the control group is determined by the Control Group Decoder U65 (SH 29) or U53 (SH A32) mounted on the Processor CCA.

Under program control, each device receives program data over Address Bus lines 10, 11, 12 and 13 and activates control or status signals for use by other devices on the CCA or by the user. The five (5) control groups used by the Centronics-Compatible Interface CCA are:

- Control Group 0 (U27, SH B7)
- Control Group 2 (U24, SH B6)
- Control Group 3 (U43, SH B7)
- Control Group 5 (U25, SH B7)
- Control Group 6 (U14, SH B6)

(i) Control Group 0 - Signal ECG0* produces the enable for the 8-bit addressable latch U27 (SH B7). ADRBS 10, 11, and 13 select the output pin and ADRBS 13 determines the logic level of the output signal. Table 2-12 lists the Address Bus lines, their function, and the output signal conditions that are controlled by Control Group 0.

TABLE 2-12. CONTROL GROUP 0 DECODE AND FUNCTIONS

Address Bus Line				Function	Output Signal Condition	
13	12	11	10			
0	0	0	0	Set Paper Empty	U27-4 low; PE active to user. U27-5 low; BUSY D inactive.	
0	0	0	1	Disable Busy Set		
0	0	1	0	Not Used		
0	0	1	1	Not Used		
0	1	0	0	Not Used		
0	1	0	1	Not Used		
0	1	1	0	Not Used		
0	1	1	1	Not Used		
1	0	0	0	Reset Paper Empty		U27-4 high; PE inactive to user. U27-5 high; BUSY D active
1	0	0	1	Enable Busy Set		
1	0	1	0	Not Used		
1	0	1	1	Not Used		
1	1	0	0	Not Used		
1	1	0	1	Not Used		
1	1	1	0	Not Used		
1	1	1	1	Not Used		

(2) Control Group 2 - A 3-to-8 line decoder/demultiplexer U24 (SH B6) is used to enable one (1) of two (2) output signals. When enabled by ECG2* and ADRBS 13, selection of the output is determined by ADRBS 10, ADRBS 11 and ADRBS 12. Table 2-13 lists the Address Bus lines, their functions, and the output signal conditions that are controlled by Control Group 2. See figure 2-15 for a loading diagram and function table for U24 operation.

TABLE 2-13. CONTROL GROUP 2 DECODE AND FUNCTIONS

Address Bus Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	Not Used	
0	0	0	1	Not Used	
0	0	1	0	Not Used	
0	0	1	1	Not Used	
0	1	0	0	Not Used	
0	1	0	1	Not Used	
0	1	1	0	Not Used	
0	1	1	1	Not Used	
1	0	0	0	Toggle ON LINE Flip-flop	U24-15 low, TONLFF* active to U36-9
1	0	0	1	Clear Busy Latch	U24-14 low; CBUSYL* active to U38-1
1	0	1	0	Not Used	
1	0	1	1	Not Used	
1	1	0	0	Not Used	
1	1	0	1	Not Used	
1	1	1	0	Not Used	
1	1	1	1	Not Used	

(3) Control Group 3 - Signal ECG3* enables one (1) output from either U43 (SH B7) on the Centronics-Compatible Interface CCA or U45 (SH 36) on the Timing and Status CCA. Each active output is in a low logical state.

Table 2-14 lists the Address Bus line signals, the functions, and the output signal conditions controlled by Control Group 3. See figure 2-15 for a function table and loading diagram for the U43 and U45 decoder operation. Note that when ADRBS 13 is low, the output signals will be found on the Timing and Status CCA.

TABLE 2-14. CONTROL GROUP 3 DECODE AND FUNCTIONS

Address Bus Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	Not Used	
0	0	0	1	Stepper Phase Shift Clock	STPSHF* active to the Power Board CCA
0	0	1	0	Load Print Phase Column	LDCOL* active to U46-9 (SH 34)
0	0	1	1	Disable VCL	VCLOFF* low to U44-3; ENVCL inactive
0	1	0	0	Enable VCL	VCLOFF* low to U44-3; ENVCL active
0	1	0	1	Enable 38 Volts	38VON* low to U44-10; EN38V* active
0	1	1	0	Disable 38 Volts	38VOFF* low to U44-11; EN38V* inactive
0	1	1	1	Clear Fault Registers	CLRFLT* active to U50-11 (SH 35)
1	0	0	0	Clear Ribbon Motion Sensor	CLSEN* active to U9 (SH B13)
1	0	0	1**	Load VFU Address Register	LVFUAR* active to U44 (SH B11)
1	0	1	0	Clear Paper Motion Flag	RMTFLG* active to INBUS 0
1	0	1	1	Set Master Clear Switch F/F	SMCSFF* active to U9 (SH B9)
1	1	0	0	Load Ribbon Motion Sensor	LDSEN* active to U41 (SH B13)
1	1	0	1	Load Display Register	LDISPY* active to U3/U26 (SH B12)
1	1	1	0	Reset Online F/F	RONLFF* active U23 (SH B7)
1	1	1	1	Clear Strobe Latch	CSTRBL* active to U47/U48 (SH B6)

**Used only on 300 LPM and 600 LPM printers.

(4) Control Group 5 - Signal ECG* provides the enable for the 8-bit addressable latch U25 (SH B7). Address Bus lines 10, 11, and 12 select the output line, and ADRBS 13 determines the logic level of the output signal.

Table 2-15 lists the Address Bus line signal levels, their functions, and the output signal conditions that are controlled by Control Group 5. See figure 2-16 for a function table and loading diagram for the U14 latch operation.

TABLE 2-15. CONTROL GROUP 5 DECODE AND FUNCTIONS

Address Bus Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	Not Used	
0	0	0	1	Set Alarm Light; Reset Online F/F	ALRMIN* low to J4-27; RALMLT inactive
0	0	1	0	Not Used	
0	0	1	1	Reset User's Acknowledge	ACK* inactive to user
0	1	0	0	Set User's Select Line	SLCT active to user
0	1	0	1	Reset User's Fault Line	FAULT* inactive to user
0	1	1	0	Not Used	
0	1	1	1	Not Used	
1	0	0	0	Not Used	
1	0	0	1	Reset Alarm Light; Set Online F/F	ALRMIN* high to J4-27; RALMLT active if RONLFF is also high
1	0	1	0	Not Used	
1	0	1	0	Set User's Acknowledge	ACK* active to user
1	1	0	0	Reset User's Select Line	SLCT inactive to user
1	1	0	1	Set User's Fault Line	FAULT* active to user
1	1	1	0	Not Used	
1	1	1	1	Not Used	

(5) Control Group 6 - Signal ECG6* provides the enable for the 8-bit addressable latch U14 (SH B6). Address Bus lines 10, 11, and 12 select the output line, and ADRBS 13 determines the logic level of the output.

Table 2-16 lists the address bus line signal levels, their functions, and the output signal conditions that are controlled by Control Group 6. See figure 2-16 for a function table and loading diagram for the U14 latch operation.

TABLE 2-16. CONTROL GROUP 6 DECODE AND FUNCTIONS

Address Bus Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	Disable Tape Channel High	U14-4 low; ENTCH low to U4 and U5 to select TPCH1-6* inputs
0	0	0	1	Disable Tape Channel Low	U14-5 low; ENTCL low to U3-6; with U14-4 determines ENTAPE* level
0	0	1	0**	Select Low Byte VFU RAMs	U14-6 low; U33 and U34 select active (SH B11)
0	0	1	1	Set Busy and Hold	U14-7 low; U38 set (SH B6)
0	1	0	0	Reset Online Light	U14-9 low; ONLNLT inactive to U20-10 (SH B9)
0	1	0	1	Tape Motor Off	U14-10 low; TMON* inactive
0	1	1	0	Not Used	
0	1	1	1	Not Used	
1	0	0	0	Enable Tape Data High	U14-4 high; ENTCH high to U4 and U5 to select TPCH7-12* inputs
1	0	0	1	Enable Tape Data Low	U14-5 high; ENTCL high to U3-6 and ENTAPE* active
1	0	1	0**	Select High Byte VFU RAMs	U14-6 high; U45 and U46 select active (SH B11)
1	0	1	1	Reset Busy and Hold	U14-7 high to Busy Latch U38-4 (SH B6)
1	1	0	1	Tape Motor ON	U14-10 high; TMON* active
1	1	1	0	Not Used	
1	1	1	1	Not Used	

**Used only by 300 LPM and 600 LPM Centronics Compatible Printers

(e) Decode PROM - The Centronics-Compatible Interface CCA uses a 256 x 8 programmable ROM (MEM2 SH B10) to decode the user's data and generate the IBUSY (Instruction Busy) and NOP (No Operation) signals. IBUSY and NOP, with the Control Group 0, produce the BUSY D input to the Busy Latch U38 (SH B6). The Decode PROM inputs to the User Control Latch U18 (SH B10) also generate the SPINSL (Soft Paper Instruction Latch) and NOPL (No Operation Latch) signals for use by the Processor CCA.

Two Decode PROMs are available for 1000 LPM printers. The 257290-001 PROM kit, which is also used on 300 LPM and 600 LPM models, always sets the BUSY within 100 nanoseconds of receiving a delete code (Hex 7F) from the user. The 250661-001 PROM kit, which is not available for 300 LPM and 600 LPM printers, does not set BUSY when configuration switch S4-2 is placed in the on position.

S4-2 causes a delete code to be treated as a printable character when in the on position. If S4-2 is OFF, the BUSY signal to the user will be set within a maximum of three (3) microseconds. See table 2-11 for the various configuration switch settings.

2. Operational Description - The operational description for the Centronics-Compatible Interface CCA is divided into six (6) parts. The first part is a discussion of the control codes used by the printer and is followed by a description of the power up, user/interface data transfer, and interface/processor data transfer routines. The final sections deal with the STATUS Indicator displays which are unique to this interface option and the self-test mode. See paragraph 2.2.3 for a description of the Centronics-Compatible handshaking routine. Data flow is shown in figure 2-22.

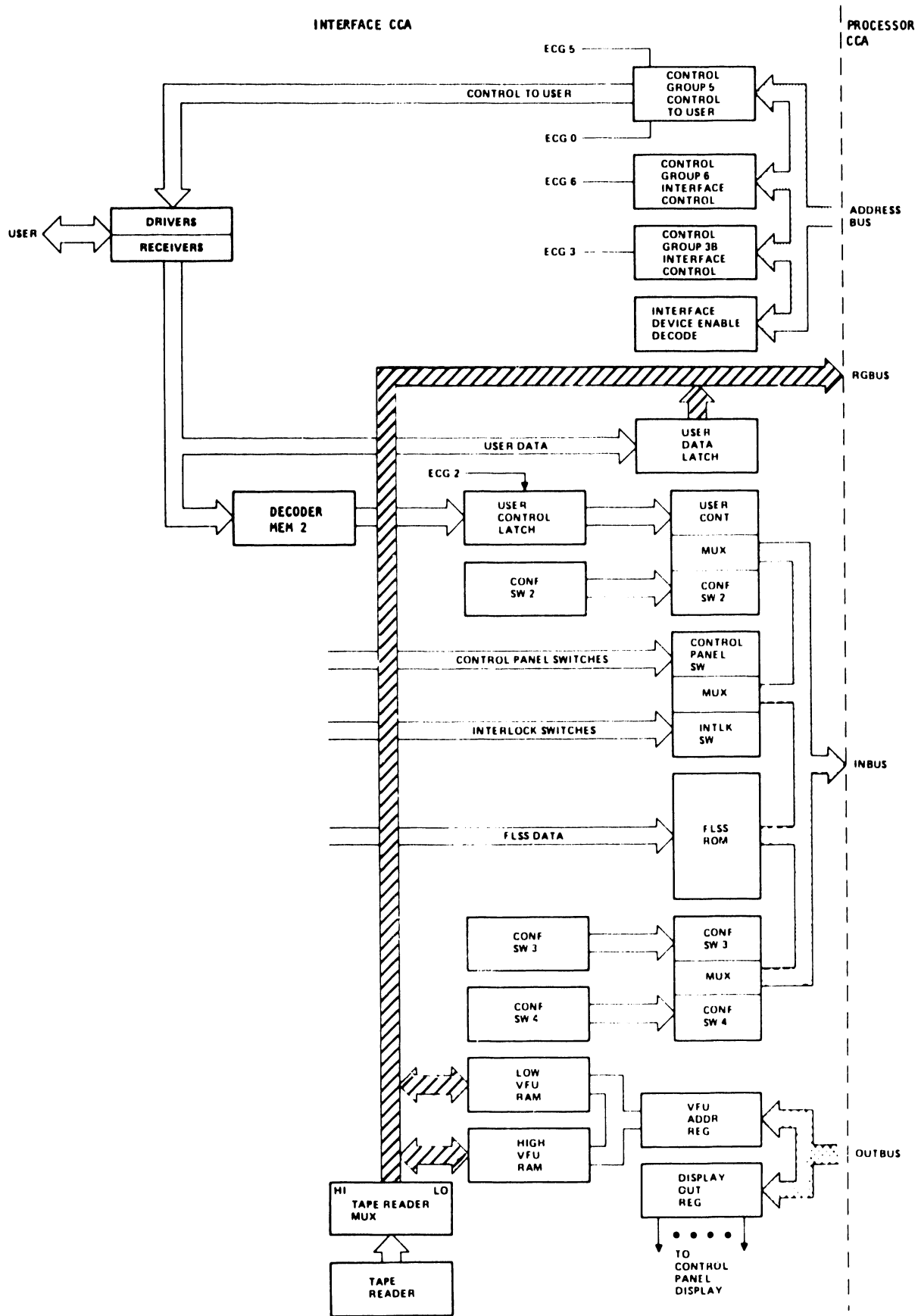


Figure 2-22. Centronics-Compatible Interface Block Diagram

(a) Control Code - Table 2-17 provides a list of the control codes used by the Centronics-Compatible Interface CCA. The unique codes are described in greater detail in the paragraphs which follow.

TABLE 2-17. CENTRONICS-COMPATIBLE PRINTER CONTROL CODES

Hex Code	Mnemonic	BUSY Set?	Description
0A	LF	YES	Paper advances one line (Line Feed)
0B	VT	YES	Skip to Channel 2 (Vertical Tab)
0C	FF	YES	Skip to Channel 1 (Form Feed)
0D	CR	YES	End of line of data - begin print cycle (Carriage Return)
11	(DC1)	NO	Remote select of printer
13	(DC3)	YES	Remote deselect of printer
1D	GS	YES	Start DAVFU load
1E	RS	YES	Stop DAVFU load
1F	US	YES	Indicates next character is VFU command
20 thru 7E	USASCII	NO (unless data buffer full)	ASCII will be printed if within the legal character-set of the band currently installed. A space will replace an illegal code.
7F	DEL	YES**	Clears data buffer if switch S2-7 is ON.

NOTE: Any code received by the printer that is not listed in this table will be treated as a no operation; i.e., will be acknowledged but will not initiate a function or a busy condition and will not move the print buffer pointer.

**When Decode PROM 250661-001 is installed in 1000 LPM printers, no BUSY is sent to the user if the delete code is a printable character. See table 2-11D for configuration switch S4-2 settings.

(1) Select (DC1, Hex 11) - If no printer fault exists, and if the printer is not in self test mode, a DC1 (Hex 11) code sent over the user data lines will select the printer and place it ON LINE. No operator intervention is required. However, the printer may be selected by pressing the ON/OFF LINE switch on the Operator Control Panel. When the Serial Interface CCA is installed with the Centronics-Compatible CCA, DC1 is not available until after the first time the ON/OFF LINE switch is pressed.

(2) Deselect (DC3, Hex 13) - A DC3 code sent over the user data lines will deselect the printer and place it OFF LINE. The printer will not respond to the deselect code if it is in the load cycle and the first character has been loaded. The printer may be deselected by pressing the ON/OFF LINE switch on the Operator Control Panel.

(3) Line Feed (LF, Hex 0A) - If the printer is in the select mode, a LF code will cause the immediate advance of paper one (1) line. The print buffer will not be affected.

(4) Carriage Return (CR, Hex 0D) - If the printer is in the select mode, and has received printable characters, a CR will cause immediate printing. A CR is not acknowledged when the printer is in the deselect mode. The maximum number of accepted carriage returns is determined by configuration switch S2-8.

(5) Vertical Tab (VT, Hex 0B) - If the VT code is received while the printer is selected, the code is processed and then acknowledged. In the deselect mode, the VT code is not processed or acknowledged.

If VFU data is loaded in RAMs U33, U34, U45, U46 (**SH B11**), a VT code will cause paper to advance to the next location punched in channel 2 of the VFU tape or in its DAVFU equivalent. If no location is designated by a punched hole, paper motion will stop at top of form. If VFU data is not loaded in the VFU RAMs, the VT code will cause paper to move to a default location. These default tabs are at one (1) inch intervals.

(6) Form Feed (FF, Hex 0C) - The FF code is processed and acknowledged if it is received while the printer is selected. While the printer is deselected the FF is not acknowledged or processed.

If VFU data is loaded in the VFU RAMs, the FF code causes paper to advance to the next top of form location. If the VFU data RAMs are not loaded, the FF code will cause paper to advance to a location selected by configuration switch S2-6 -- either 11 or 12 inches.

(7) GS and RS (Hex 1D and 1E) - During a printer load cycle, the data lines are monitored for a format control code. When the GS (DAVFU Start) code is received, the normal data load routine is left and the DAVFU load routine is begun. Once in the DAVFU load routine, all data sent by the user is considered to be tape channel data and is loaded into the VFU data RAMs. The DAVFU data load is ended when the RS (DAVFU Stop) code is received.

(8) US Sequence (Hex 1F) - If the printer is selected, the US code will cause the printer to use the next character sent by the user as a VFU skip command unless it is in the FLS mode of operation. An US code will cause a STATUS fault display of 32 while in the FLS mode. Bit 5 of the next character determines whether a line or channel skip will be done.

If bit 5 is equal to a logical one (1), the first four (4) bits of the character set the number of lines that will be skipped. A line count of zero (0) is treated as a NOP with BUSY set.

If bit 5 is equal to a logical zero (0), the first four (4) bits of the next character determine the channel number to which the printer will skip. Channel numbers other than 1-12 will cause a STATUS error display.

(9) Delete (DEL, Hex 7F) - The optional delete code is enabled by setting configuration switch S2-7 to ON. By transmitting the DEL code over the data lines, the user can clear the input data buffer. During response to the DEL code, the BUSY line to the user is set. If S2-7 is OFF and a DEL code is received, it is treated as a NOP with BUSY set.

In 1000 LPM model printers, the DEL code can be a printable character if configuration switch S4-2 is ON. The logic level of the user's BUSY signal line is determined by the Decode PROM installed on the interface CCA. See **paragraph 2.3.1, subparagraph c.1.e**, for a description of the Decode PROMs.

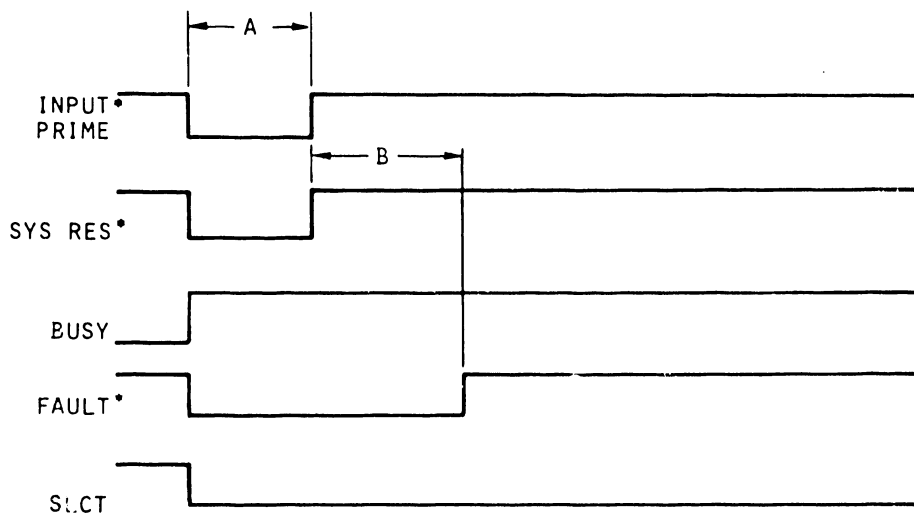
(b) Power Up - When power is applied to the printer, all interface signals are inactive except BUSY and PE (Paper Empty) (SH B7). BUSY indicates that the printer is unable to receive data. PE is active to prevent data from being transferred when the user is not monitoring the BUSY signal.

An active BUSY is generated by the BUSYL* (Busy Latch) output of U38-6 (SH B6) which also inactivates the DEM* (Demand) signal to the user. The PE signal is controlled by ECG0* and Address Bus lines 10 through 12 (U27, SH B7).

(c) User/Interface Data Transfer - Before the printer can receive print or format data, it must be selected. Selection can be done by pressing the ON/OFF LINE switch to ON or by the user sending a select code (Hex 11) over the data lines. See figures 2-5 and 2-6 for timing diagrams for the two (2) select methods. Notice that a remote select can be made even when the BUSY signal is active.

After being selected, a SLCT (Select) signal is sent to the user to indicate that the printer has been selected. Data from the user is then inverted and input to the User Data Latch (U16) and the Decode PROM MEM2 (SH B10). STB* (Strobe), generated from the user's STROBE signal (SH B6), sets the output of U16 to the logic levels of its inputs.

In addition to the STROBE* signal to indicate stable data on the data lines, the user may send an INPUT PRIME* (SH B5) signal to the printer. If configuration switch S1-4 is ON, INPUT PRIME* will clear the print buffer and initialize the printer. Functionally, INPUT PRIME* is the same as pressing the ALARM/CLEAR switch on the operators control panel. Figure 2-23 provides a timing diagram for the INPUT PRIME* signal.



- A. $\bar{>}$ 40 MICROSECONDS
- B. PRINTER INITIALIZE \approx 2 SECONDS

Figure 2-23. INPUT PRIME Timing

(d) Interface/Processor Data Transfer - Once the logic levels of the User Data Latch (UI6) have been set, an output control signal, generated by gating ENUSER* and UDL* at U23 (SH B10), will transmit the data to the Processor CCA via the RGBUS0 to 7 lines. The generation of UDL* is a function of the Register Enable Decoder, U5 or U34, on the Processor CCA (SH 29 or SH A32).

After data is received, the printer will send the user an ACK* signal. If the data word creates a busy condition, the printer will not send ACK* until BUSY is dropped.

(e) STATUS Indications - The STATUS indicators used with the Centronics-Compatible Interface CCA differ slightly from those in the standard printer configuration. Table 2-18 lists and defines only these indications. See section IV in volume II for a complete description of the standard status code displays.

TABLE 2-18. CENTRONICS-COMPATIBLE STATUS CODE DISPLAYS

Code	Definition
13	TCVFU Tape too long (Greater than 126 Lines)
17	Loss of Print Sync (600 LPM only)
23	Reserved
27	DAVFU Data Transfer More Than 126 Lines
29	DAVFU Top of Form Load Error
31	DAVFU Data Load Error
32	US Code Received While in FLS Mode
34	Illegal RAM Integrity ERROR (1000 LPM only)
68	RESERVED

(f) Self-Test Mode - When the printer is operating in the self-test mode, the BUSY and FAULT* signals to the user are active. The STROBE* signal from the user has no effect. To return the printer to user control, the TEST switch must be placed in the center position and the ON/OFF LINE switch pressed. This will place the printer off line. The printer will again respond to the user's command after it has been selected. Once the printer has been selected, it will not respond to the self test switch.

d. Serial Interface CCA

The Serial Interface CCA is edge-connected to the spare card slot of the Mother Board CCA. It interfaces the parallel Short Line Interface CCA for non-VFU, or the Centronics-Compatible Interface CCA for VFU, with the user's I/O. Operating in an asynchronous mode, with or without a modem, it accepts user data in serial form and converts it to the parallel format recognized by the printer.

The discussion of the Serial Interface CCA is divided into two (2) major sections. The first section, Device Description, includes a description of the methods of data transmission, the configuration switches, and the major integrated circuits. The second, Operational Description, deals with operating modes, communications protocols, power up, and data transfer.

Logic Diagram sheets C1 through C5 are available in section V of volume II. Paragraphs 2.3.1.a and 2.3.1.c should be consulted for a discussion of two (2) parallel interface CCAs.

1. Device Description - This section includes a description of the methods of data transmission, the interfaces' configuration switch settings, and the major integrated circuits used by the Serial Interface CCA.

(a) Methods of Transmission - The Serial Interface CCA can accept two (2) types of serial data transmission -- Standard RS232C Voltage and 20 mA Current Loop. The method of transmission is determined by setting switch S1-6 on the CCA (SH C4).

(1) RS232C Voltage - Discrete voltage levels are used for transmitting data as well as for interface communications. The single-ended RS232C compatible receivers and transmitters (SH C4) are capable of operating over a cable length of 15.3 meters (50 feet). Figures 2-24 and 2-25 illustrate the recommended RS232C receiver and transmitter circuits.

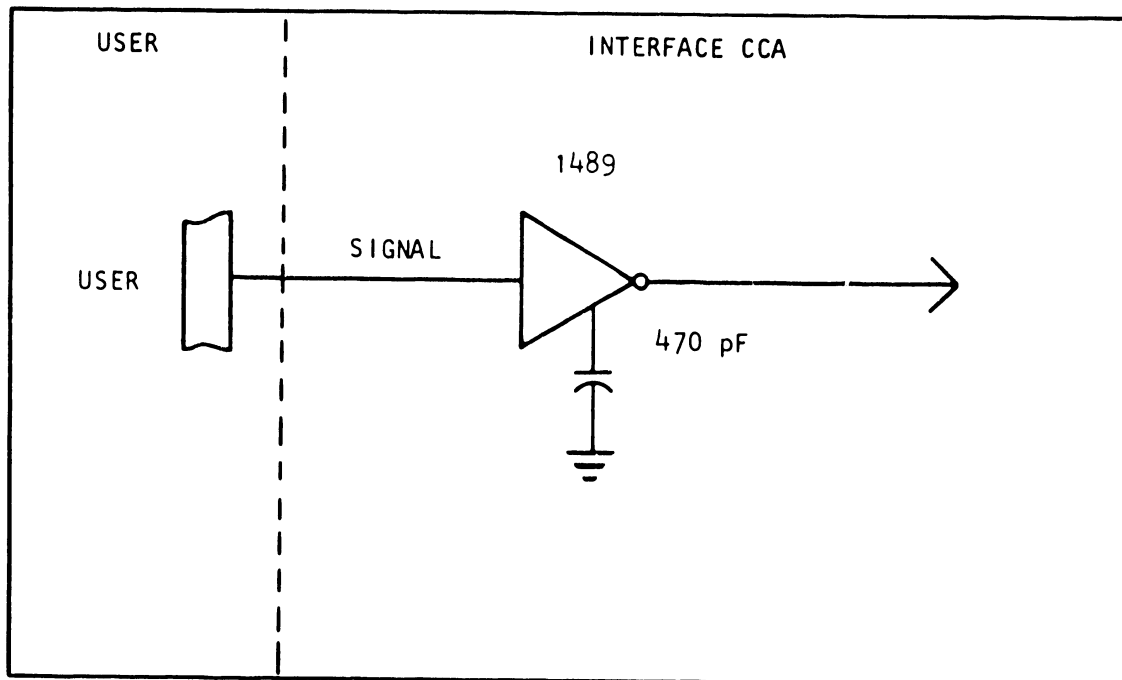


Figure 2-24. Typical RS232C Receiver Circuit

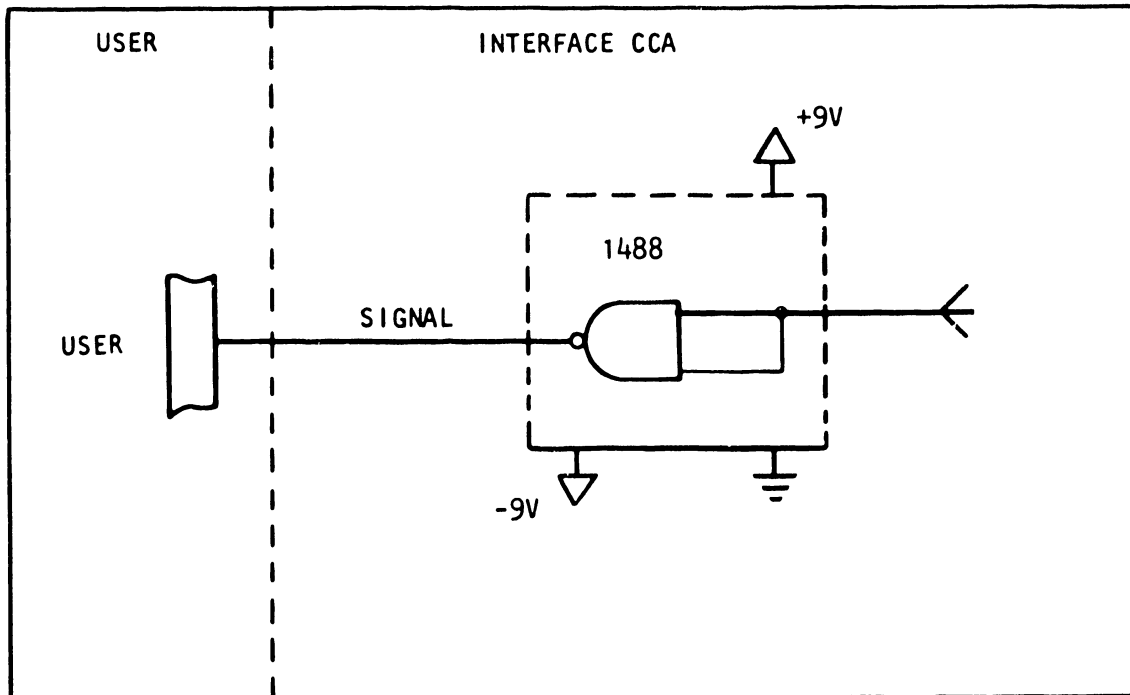


Figure 2-25. Typical RS232C Transmitter Circuit

(2) 20 mA Current Loop - Signals are transmitted by means of two (2) current loops: receive and transmit. The receive loop is made up of a two (2) wire current source (RXD+ and RXD-) supplied by the user to the CCA. Within the Serial Interface CCA, the two (2) wires of the receiver current source are terminated in a current sensing device (SH C4). Figure 2-26 illustrates the 20 mA Current Loop Receiver Circuit.

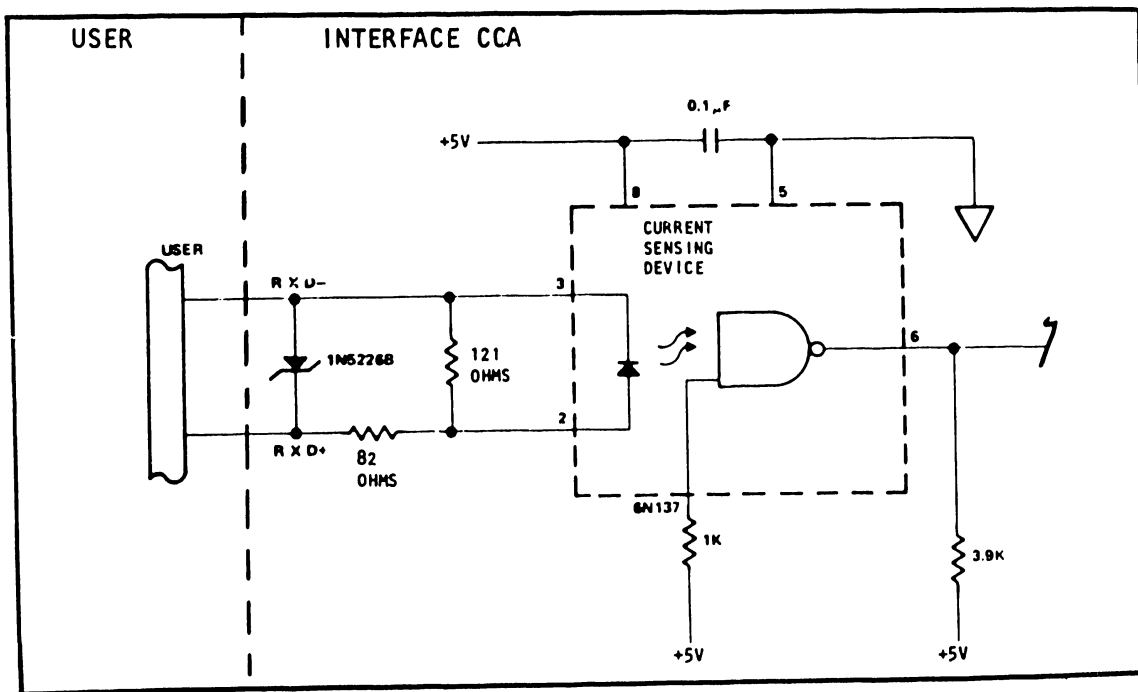


Figure 2-26. 20 mA Current Loop Receiver Circuit

The active current loop transmitter circuit (ATXD+, ATXD-) is controlled by the printer and terminated in a current-sensing device at the user end. Its purpose is to provide for full duplex 20 mA current loop transmission. Maintaining current in the loop, except during data transfer, indicates that the printer is capable of sending data to the user (SH C1).

Figure 2-27 illustrates the 20 mA current loop transmitter circuit. Communications over cable lengths of up to 460 meters (1500 feet) are possible with the use of this active transmitter circuit.

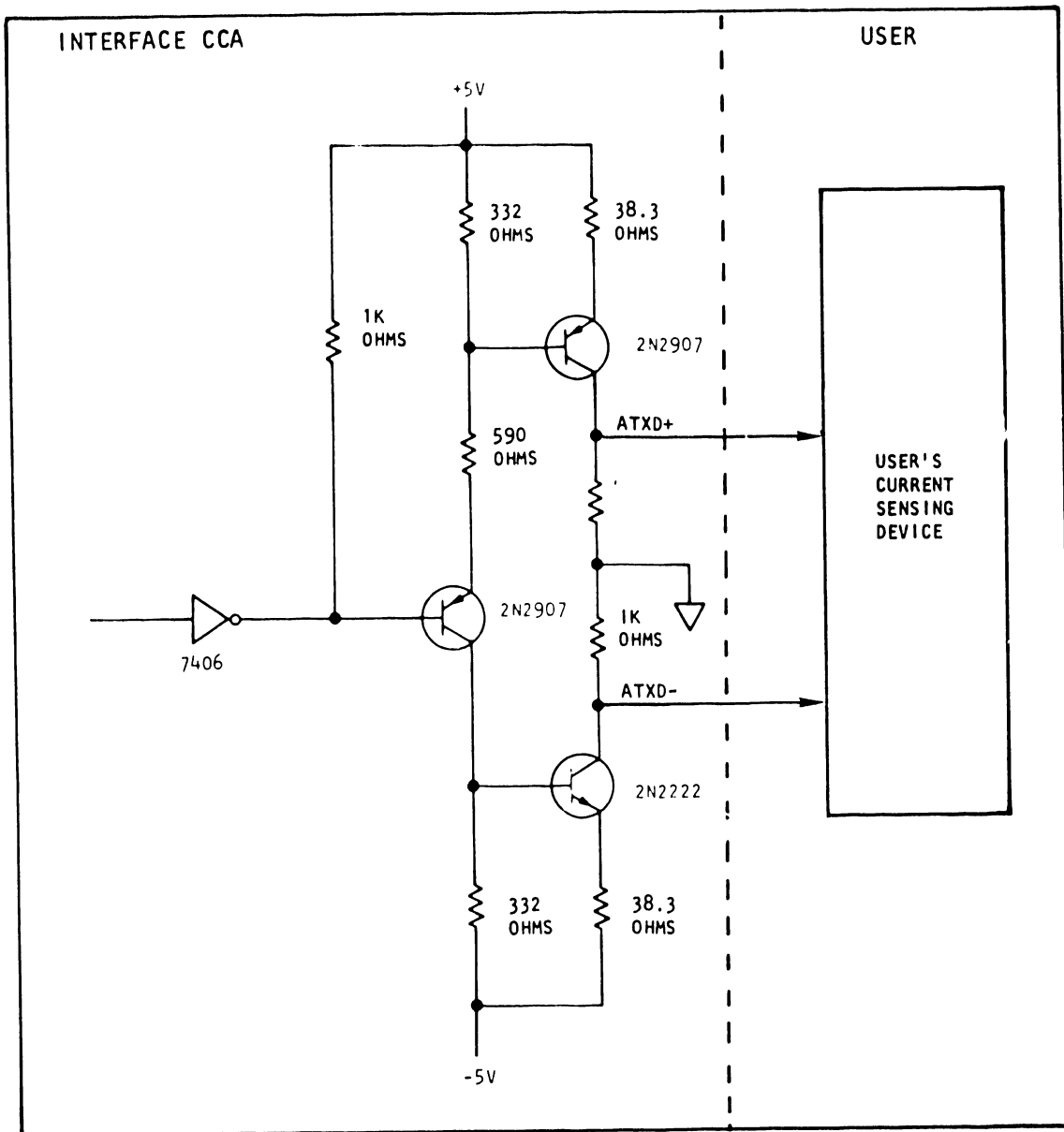


Figure 2-27. 20 mA Active Current Loop Transmitter Circuit

The passive transmit current loop is terminated in a current-sensing device located on the Serial Interface CCA (SH C4). The current source is supplied by the user. The presence of current in this loop indicates that the printer is able to receive data. The absence of current in either transmit loop indicates that the printer is busy or a fault exists. Figure 2-28 illustrates the 20 mA Passive Current Loop Transmitter Circuit.

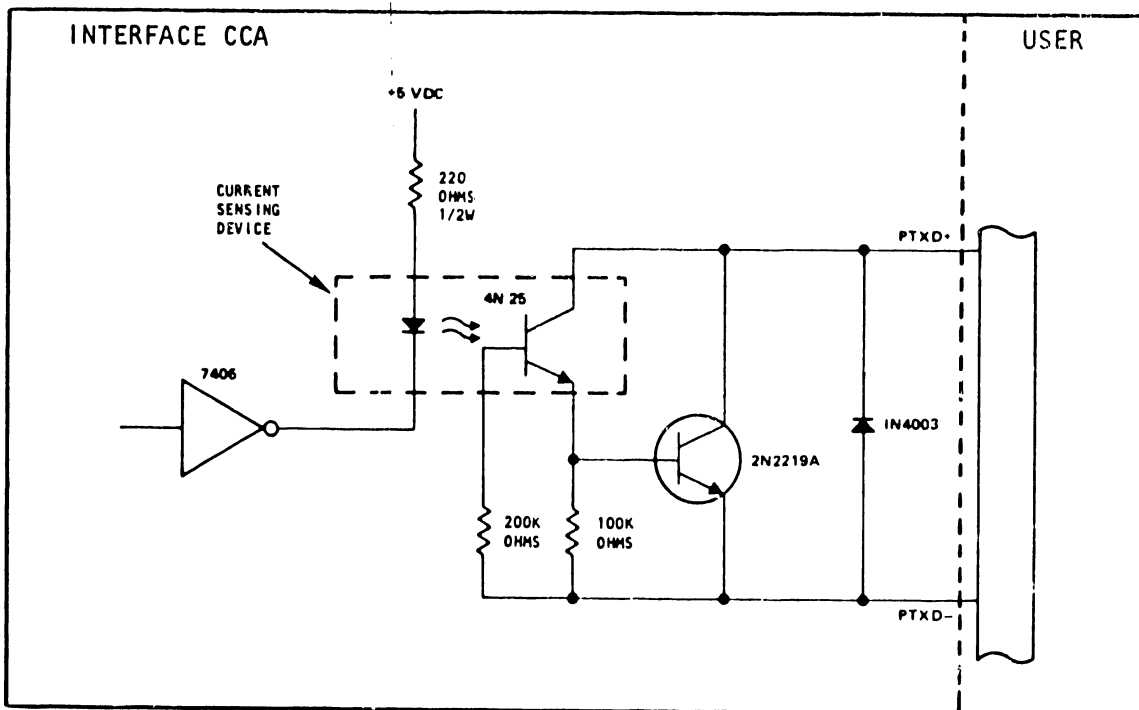


Figure 2-28. 20 mA Passive Current Loop Transmitter Circuit

(b) Configuration Switches - Three (3) sets of switches are mounted on the Serial Interface CCA. The setting of these switches defines the printer's mode of operation. Table 2-19A tabulates the signal conditions and format features provided by the three (3) Serial Interface CCA configuration switches.

TABLE 2-19A. SERIAL INTERFACE CCA CONFIGURATION SWITCH SETTINGS

Switch	Function	
	When ON	When OFF
S1-1	Data Strobe is high true (for use with Short Line Interface CCA without VFU)	Data Strobe is low true (for use with Centronics- Compatible Interface CCA)
S1-2	---	Not used

TABLE 2-19A. SERIAL INTERFACE CCA CONFIGURATION SWITCH SETTINGS
(Cont'd)

Switch	Function	
	When ON	When OFF
S1-3	BUSY* is low true	BUSY* is high true
S1-4	BUSY* is on SCA pins 11 and 20 of J2	BUSY* is ORed with DTR* and appears on SCA pins 11 and 20 of J2
S1-5	RS232C Voltage selected	20 mA Current Loop selected
S1-6	Clear to Send (CB) always enabled	Clear to Send (CB) under user control
S1-7	Data Carrier Detect (CF) always enabled	Data Carrier Detect (CF) under user control
S1-8	Data Set Ready (CC) always enabled	Data Set Ready (CC) under user control
S2-1	---	Not used
S2-2	---	Not Used
S2-3	---	Not used
S2-4	---	Not used
S2-5	---	Not used
S2-6	Parity bit is ignored	Parity bit is checked
S2-7	---	See table 2-19B
S2-8	---	See table 2-19B
S3-1	---	See table 2-19C
S3-2	---	See table 2-19C
S3-3	---	See table 2-19C
S3-4	---	See table 2-19C

TABLE 2-19A. SERIAL INTERFACE CCA CONFIGURATION SWITCH SETTINGS
(Cont'd)

Switch	Function	
	When ON	When OFF
S3-5	7 Data bits (without Parity bit)	8 Data bits (without Parity bit)
S3-6	1 Stop bit	2 Stop bits
S3-7	Accept data without Parity bit	Accept data with Parity bit
S3-8	Odd Parity with S3-7 OFF	Even Parity with S3-7 OFF

Table 2-19B defines the communication protocol switch settings available on the Serial Interface CCA.

TABLE 2-19B. SERIAL INTERFACE CCA PROTOCOL CONFIGURATION SWITCH SETTINGS

Switch S2-7	Switch S2-8	Protocol Selection
OFF	OFF	Simplex, with X-ON/X-OFF
OFF	ON	ACK-NAK by line (unblocked)
ON	OFF	Undefined
ON	ON	ACK-NAK by block

Table 2-19C outlines the configuration switch settings for the various baud rates available.

TABLE 2-19C. SERIAL INTERFACE CCA BAUD RATE CONFIGURATION SWITCH SETTINGS

Switch S3-1	Switch S3-2	Switch S3-3	Switch S3-4	Baud Rate
ON	ON	ON	ON	50
OFF	ON	ON	ON	75
ON	OFF	ON	ON	110
OFF	OFF	ON	ON	134.5
ON	ON	OFF	ON	150
OFF	ON	OFF	ON	300
ON	OFF	OFF	ON	600
OFF	OFF	OFF	ON	1200
ON	ON	ON	OFF	1800
OFF	ON	ON	OFF	2000
ON	OFF	ON	OFF	2400
OFF	OFF	ON	OFF	3600
ON	ON	OFF	OFF	4800
OFF	ON	OFF	OFF	7200
ON	OFF	OFF	OFF	9600
OFF	OFF	OFF	OFF	19200

NOTE: At 19.2K baud rate, 100% print density, the 1000 LPM will print a maximum of 832 LPM. As print density is reduced, speed will increase.

In addition to the switches located on the Serial Interface CCA, the configuration switches mounted on the parallel interface CCAs provide a variety of formatting and control options. **Table 2-20** lists and defines the switch settings available on the non-VFU Short Line Interface CCA when used in the serial configuration.

**TABLE 2-20. SHORT LINE INTERFACE* CCA SWITCH SETTINGS
FOR USE WITH THE SERIAL INTERFACE CCA
WITHOUT VFU**

Switch	Function	
	When ON	When OFF
S1-1	Not used	Not used
S1-2	Disable Paper Instruction (PI)	Not used
S1-3	Not used	Enable 8 Bit Interface
S1-4	Disable Buffer Clear	Not used
S1-5	Not used	High True Interface
S1-6	Enable 8th Data line to Odd/ Even Parity Generator	Not used
S1-7	Not used	Disable PI line to Odd/Even Parity Generator
CAUTION		
S1-6 and S1-7 should never be on at the same time.		
S1-8	Not used	Not used
S2-1	Paper Motion on Carriage Return	No Paper Motion on Carriage Return
S2-2	Defines Skipover as follows:	
	<u>S2-2</u>	<u>S2-3</u>
	OFF	OFF
	OFF	ON
	ON	OFF
	ON	ON
		<u>Number of Lines Skipped</u>
		3 Lines
		6 Lines
		0 Lines
		4 Lines
S2-4	No Print to BOF	Print to BOF
S2-5	Enable 140 CR Maximum	Enable 8 CR Maximum
S2-6	12 inch BOF	11 inch BOF
S2-7	Disable non-VFU Skipover	Enables non-VFU Skipover
S2-8	Not used	No Band Image PROM Sum Check

*Refer to tables 2-5A and 2-5B for a detailed description of the switch settings.

Table 2-21 provides similar information for the Centronics-Compatible Interface CCA switch selectable options when used with the Serial Interface CCA. Note that not all parallel interface CCA switch selectable options can be used with the serial configuration.

TABLE 2-21. CENTRONICS-COMPATIBLE INTERFACE CCA SWITCH SETTINGS FOR USE WITH THE SERIAL INTERFACE WITH VFU*

Switch	Function																
	When ON	When OFF															
S1-1		Spare															
S1-2		Spare															
S1-3	Not used	Enable 8 Bit Interface															
S1-4	Not used	Input Prime Disabled															
S1-5		Spare															
S1-6		Spare															
S1-7		Spare															
S1-8		Spare															
S2-1	Paper Motion on Carriage Return	No Paper Motion on Carriage Return															
S2-2	Defines number of lines skipover as follows:																
S2-3	<table border="0"> <tr> <td>S2-2</td> <td>S2-3</td> <td><u>Number of Lines Skipped</u></td> </tr> <tr> <td>OFF</td> <td>OFF</td> <td>3 Lines</td> </tr> <tr> <td>OFF</td> <td>ON</td> <td>6 Lines</td> </tr> <tr> <td>ON</td> <td>OFF</td> <td>0 Lines</td> </tr> <tr> <td>ON</td> <td>ON</td> <td>4 Lines</td> </tr> </table>	S2-2	S2-3	<u>Number of Lines Skipped</u>	OFF	OFF	3 Lines	OFF	ON	6 Lines	ON	OFF	0 Lines	ON	ON	4 Lines	
S2-2	S2-3	<u>Number of Lines Skipped</u>															
OFF	OFF	3 Lines															
OFF	ON	6 Lines															
ON	OFF	0 Lines															
ON	ON	4 Lines															
S2-4	No Print to BOF	Print to BOF															
S2-5	Line Feed on Buffer Full (132)	No Line Feed on Buffer Full (132)															
S2-6	12 inch BOF	11 inch BOF															
S2-7	Delete Code Enabled	Delete Code Disabled															
S2-8	Enable 140 CR Maximum	Enable 8 CR Maximum															
S3-1	Enable VFU Skipover	Disable VFU Skipover															
S3-2	Print on Paper Feed Command (LF, FF, VT)	No Print on Paper Feed Command (LF, FF, VT)															
S3-3	Enable Double Space on Line Feed or Step Switch	Disable Double Space on Line Feed or Step Switch															

*Refer to tables 2-11A through 2-11D for a detailed description of the switch settings.

TABLE 2-21. CENTRONICS-COMPATIBLE INTERFACE CCA SWITCH SETTINGS FOR USE WITH THE SERIAL INTERFACE WITH VFU* (Cont'd)

Switch	Function	
	When ON	When OFF
S3-4	Not used	Not used
S3-5	Tape Reader available	No Tape Reader available
S3-6		Spare
S3-7		Spare
S3-8		Spare
S4-1		Spare
S4-2		Spare
S4-3		Spare
S4-4		Spare
S4-5	Not used	Not used
S4-6		Spare
S4-7		Spare
S4-8		Spare

*Refer to tables 2-11A through 2-11D for a detailed description of the switch settings.

(c) Major Integrated Circuit Devices - There are six (6) major devices used by the Serial Interface CCA. The function of each device is discussed in the following paragraphs. **Figure 2-30**, at the end of this section, provides a block diagram to summarize the operation of the following devices:

- 8085A-2 Microprocessor (U16)
- 2651 Programmable Communications Interface (PCI) (U8)
- 8255A Programmable Peripheral Interface (PPI) (U15)
- RAM Data Buffers (U1, U2, U3, U4, U11, U12, U13, U14)
- 4-Line-to-16-Line Decoder/Demultiplexer Chip Select (U25)

(1) 8085A Microprocessor - The Serial Interface employs the Intel 8085A-2 microprocessor (SH C2, U16) to control the flow of serial input data to the rest of the printer system. Through outputs A8-A12, WR*/RD*, and IO/M*, the microprocessor accesses and enables the 2651 Programmable Communications Interface (PCI), the 8255A Programmable Peripheral Interface (PPI), MEM1, MEM2, and the data RAMs of the various RAM data buffer configurations.

Serial data is received on an interrupt basis from the PCI. When data is available at the PCI, an interrupt (RXRDY*) is sent to the RST 6.5 interrupt portion on the microprocessor. This causes the firmware to vector to an interrupt service routine to process the input data and inspect it for framing, overrun and parity errors. The data is then stored in the RAM data buffer.

After servicing the interrupt caused by the input data, the 8085A-2 microprocessor inspects the RAM data buffer to determine if it contains data. If data is found, it is transferred in an 8-bit parallel format to the parallel interface CCA via the PPI. Under a buffer almost-full condition, the microprocessor provides the user with a warning signal so that data transmission can be stopped to prevent loss of data.

The microprocessor also monitors, via Port C of the PPI, the status of the printer system by checking the ONLN, DEM and READY signals. If a change in these signals is detected, the appropriate control lines are enabled or disabled as required.

(2) 2651 Programmable Communications Interface (PCI) - The 2651 Programmable Communications Interface (SH C2, U8) is the device used to assembly the serial data stream into an 8-bit parallel data format. Three internal registers, under program control of the microprocessor, determine the handling of data.

The mode registers initialize the PCI to the proper data transmission format and baud rate as determined by the setting of configuration switches S3 and S2. The command register determines the condition of the RS232C status lines which indicate to the user whether the interface is able to receive and send data. The contents of the status register reflect the results of the parity and framing error check made on the input serial data. An overrun occurs when the microprocessor fails to service a data interrupt before another character is received by the PCI, and also is indicated in the PCI status register.

(3) 8255A Programmable Peripheral Interface (PPI) -The 8255A (SH C2, U25) is a multi-port device which interfaces the Parallel Interface CCA and configuration switch S3 with the microprocessor. Its 24 I/O pins are programmed as three 8-bit input or output ports (A, B, C). Port A, configured as an output port, is used to transfer the data word to the parallel interface CCA. Port B is configured as an input port for reading configuration switch S3.

Two (2) of the upper four bits of Port C are configured as outputs to send the STROBE signal to the parallel interface CCA and a busy condition signal to the user. Three (3) of the lower four bits of Port C are configured for input and used for monitoring the READY, ONLN, and DEM status indicators from the printer.

(4) RAM Data Buffer - The RAM data buffer acts as a first-in first-out (FIFO) buffer between the user and the printer system and as program stack and flag storage for the microprocessor. The standard 1K buffer

consists of two (2) four-bit static RAMs (SH C3, U1, U11). The optional 2K data buffer also uses U2 and U12 static RAMs in conjunction with U1 and U11. In the optional 4K buffer configuration, U3, U4, U13, and U14 are utilized in conjunction with all the other RAMs.

The upper 25 RAM locations are reserved for the program stack and flag storage. The remaining locations serve as the data buffer. **Figure 2-29** provides a complete memory map detailing the organization of the RAM memory and its relationship to the microprocessor program storage ROM.

ADDRESS (HEX)			
4K RAM	2K RAM	1K RAM	
13FF	BFF	7FF	FLAG (MICROPROCESSOR)
13FE	BFE	7FE	TEMP REG (MICROPROCESSOR)
13FD	BFD	7FD	FLAG 2 (MICROPROCESSOR)
13E8	BE8	7E8	MICROPROCESSOR PROGRAM STACK REGISTER 21 LOCATIONS
13E7	BE7	7E7	WRITE POINTER
13E6	BE6	7E6	WRITE POINTER
13E5	BE5	7E5	READ POINTER
13E4	BE4	7E4	READ POINTER
13E3	BE3	7E3	TOP OF RAM
			966 LOCATIONS FOR 1K RAM 2020 LOCATIONS FOR 2K RAM 4068 LOCATIONS FOR 4K RAM
400	400	400	BOTTOM OF RAM
3FF	3FF	3FF	TOP OF PROM
			1024 LOCATIONS
000	000	000	BOTTOM OF PROM

Figure 2-29. Serial Interface Memory Map

(5) 4-Line-to-16-Line Decoder/Demultiplexer - Internal chip select signals are produced by a 4-line-to-16-line decoder/demultiplexer (SH C5, U25) under the control of the microprocessor. High order address bits A10 through A12 and IO/M* perform the selection function when strobed by WR* ANDed with RD*. Chips are enabled only when the chip select signal is low. Table 2-22 lists the input signal conditions required to enable the program memory PROMs (MEM1, MEM2), the data buffer RAMs, the 2651 Programmable Communications Interface, the 8255A Programmable Peripheral Interface and line driver U22 which provides an output port (Port D) for configuration switch S2.

TABLE 2-22. DEVICE ENABLING AND ADDRESSING

G1 (RD*) (WR*)	Inputs				Enable Outputs
	A10	A11	A12	IO/M*	
L	L	L	L	L	PROMCS*
L	H	L	L	L	1K SEL*
L	L	H	L	L	2K SEL*
L	H	H	L	L	3K SEL*
L	L	L	H	L	4K SEL*
L	L	L	L	H	2651 SEL*
L	H	L	L	H	8255 SEL*
L	L	L	H	H	PORT D EN*

L = Logic Low
H = Logic High

(6) Programmed Instruction PROMs - The software used to program the microprocessor resides in MEM1 and MEM2 (SH C3) and is accessed by the PROM Address Latch (SH C2, U5) under control of the microprocessor signal ALE (Address Latch Enable). Address lines A0 through A7 from U5 and A8 and A9 from the microprocessor (U16) provide the required 10-bit PROM address.

2. Operational Description - This section contains a description of the printer-recognized control codes, the communications protocols, and three (3) major operational routines. The operation of the Short Line Interface CCA or the Centronics-Compatible Interface CCA remains basically the same with the Serial Interface CCA installed. See figure 2-30 for data flow information.

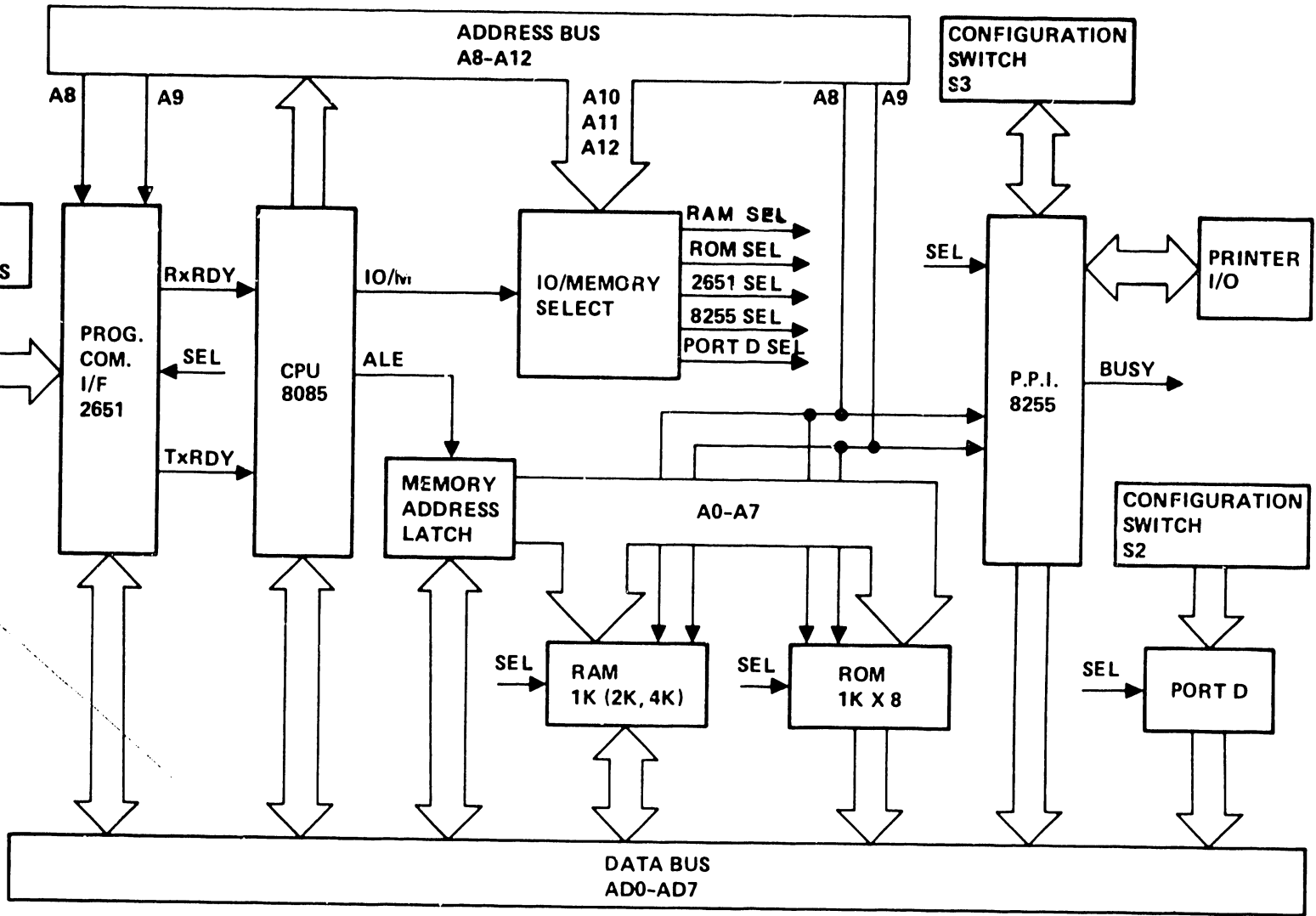


Figure 2-30. Serial Interface Block Diagram

(a) Printer Control Codes - The printer will accept for reception and transmission the user supplied ASCII control codes listed in **table 2-23**. The printer control codes are used to control print and/or VFU or DAVFU, ACK/NAK, and X-ON/X-OFF operations.

TABLE 2-23. PRINTER CONTROL CODES

ASCII Code	Hex Value	Octal Value
	<u>Received Codes</u>	
NULL (null character)	00	000
STX (start of text)	02	002
ETX (end of text)	03	003
LF (line feed)	0A	012
VT (vertical tab)*	0B	013
FF (form feed)	0C	014
CR (carriage return)	0D	015
DC1 (select)*	11	021
DC3 (deselect)*	13	023
GS (start DAVFU load)*	1D	035
RS (stop DAVFU load)*	1E	036
US (most significant byte of VFU command)*	1F	037
DEL (delete code)*+	7F	177
	<u>Transmitted Codes</u>	
ACK (acknowledge)	06	006
NAK (no acknowledge)	15	025
XON (clear to transmit)	11	021
XOFF (buffer overflow warning)	13	023
*Applicable only for VFU configuration. +Switch-selected option.		

(b) Communications Protocols - The Serial Interface CCA is capable of supporting three different communication protocols. Switches S2-7 and S2-8 (SH C5) determine whether the serial data transmission will be in simplex or duplex format. See **table 2-19B** for a definition of these switch settings. The following paragraphs will provide a more detailed description of these protocols.

(1) Simplex with X-ON, X-OFF Communications Protocol - By setting switches S2-7 and S2-8 to their off position, the printer will operate in the simplex mode. In this mode, when the power up cycle is completed and the printer is placed on line, Secondary Request to Send (SCA) will be set to its on condition to indicate that the printer is ready to receive data. If the optional signals Data Set Ready (DSR*) (CC) and Data Carrier Detect (DCD*) (CF) are implemented, the Serial interface must also wait until these signals are active before being able to receive data.

With SCA, DSR*, and DCD* on or active, the Serial interface will now respond to the valid start bit which indicates the beginning of character transmission. The character is then assembled and checked for parity, framing, and overrun errors.

If a transmission error is found, a question mark (?) will be substituted for the character in error. The character is then stored in the Serial Interface CCA RAM data buffer. Note that no provision is made for data error recovery in the simplex mode.

Data is loaded into the RAM data buffer in a continuous flow until a paper motion command or other control code is received. Refer to **table 2-23** for accepted control codes. However, in order to prevent loss of data, a control code must be received after not more than 132 printable characters. All printable characters in excess of 132 will be ignored until a control code is transmitted. At that time, data will be transferred to the printer parallel interface line buffer for a print operation.

The interface will continue to receive data while the printer is printing as long as the RAM data buffer is not full. The SCA signal will go inactive to warn the user of a possible buffer full condition at the following levels:

1K data RAM - 75%

2K data RAM - 85%

4K data RAM - 85%

Buffer full is possible when short line lengths or multiple paper motion commands are being transmitted at baud rates lower than 1200 baud. The SCA signal will remain inactive until the RAM data buffer has emptied to the following levels:

1K data RAM - 50%

2K data RAM - 40%

4K data RAM - 40%

In the buffer full condition, either the RS232C buffer overflow warning, or X-ON, X-OFF overflow warning procedure should be followed.

(a) RS232C (SCA) Buffer Overflow Warning -

When the SCA signal becomes inactive to indicate that the RAM data buffer is almost full, data transmission can continue. However, it is recommended that the user complete the transmission of the line in process and halt further transmission until after a paper motion command is sent.

Transmission may be stopped after the transmission of any data character, but an incomplete line may be stored in the RAM data buffer. If the optional DCD* is implemented, the user should cause the signal to become inactive after halting data transmission.

If the above procedure is not followed and the RAM data buffer is allowed to be fully loaded, Data Terminal Ready (DTR*) (CD), activated when the printer was ready to receive data, will become inactive to inhibit further data transmission. The printer will then print out the entire contents of the RAM data buffer. To allow for an incomplete line that may have been loaded when the buffer full condition occurred, an ASCII line feed (LF) will be inserted at the end of the printout to cause the incomplete line to be printed.

DTR*, inactive during the printing of the buffer contents, will remain inactive until the printer is manually taken off line and then placed on line again. At this point, the Serial interface is capable of receiving more data.

(b) X-ON, X-OFF Overflow Warning - The user has the option to monitor either the SCA signal or the Transmitted Data (TXD) (BA) signal for busy conditions. XON, ASCII code (Hex 11), is transmitted to the user along the BA line whenever SCA makes the transition from inactive to active. XOFF, ASCII code (Hex 13) is transmitted to the user when the SCA signal becomes inactive. An XOFF signal is sent to the user for every character received while in the buffer overflow warning area. In this condition, the user must follow the same procedure as detailed for the RS232C buffer overflow warning.

(2) Unblocked Full Duplex Communication Protocol

- In the unblocked full duplex mode, each line of print transmitted by the user must be followed by an ASCII carriage return (CR). Upon receiving a CR code, the user must wait for the Serial interface to respond with an ACK (Acknowledge) or NAK (No Acknowledge).

A NAK response indicates that a parity, framing, or overrun error has occurred and all data since the previous CR will be destroyed. When a NAK is received by the user, the line must be retransmitted.

(3) Blocked Full Duplex Communication Protocol -

In the blocked full duplex mode, an ASCII code STX (Start of Text) must precede the transmission of the data character block, and the user must limit the data block so that it does not exceed the size of the interface RAM data buffer. The following number of locations are available for the various size data buffers:

1K - 966 locations

2K - 2020 locations

4K - 4068 locations

After completion of the transmission of the data block, an ASCII code ETX (End of Text) must be sent. The interface will ignore all data not blocked by the STX and ETX codes. The user must then wait for the interface to respond with an ACK or NAK.

A NAK response indicates that a parity, framing, or overrun error has occurred and all data in the data block will be destroyed. When a NAK is received, the user must retransmit the entire data block.

(c) Power Up Routine/Switch Routine - During the power up routine, the RS232C signal SCA (Secondary Request to Send) is kept inactive to indicate to the user that the printer is unable to receive data. For current loop operation, the busy condition is indicated by the lack of current in the PTXD loop (SH C2).

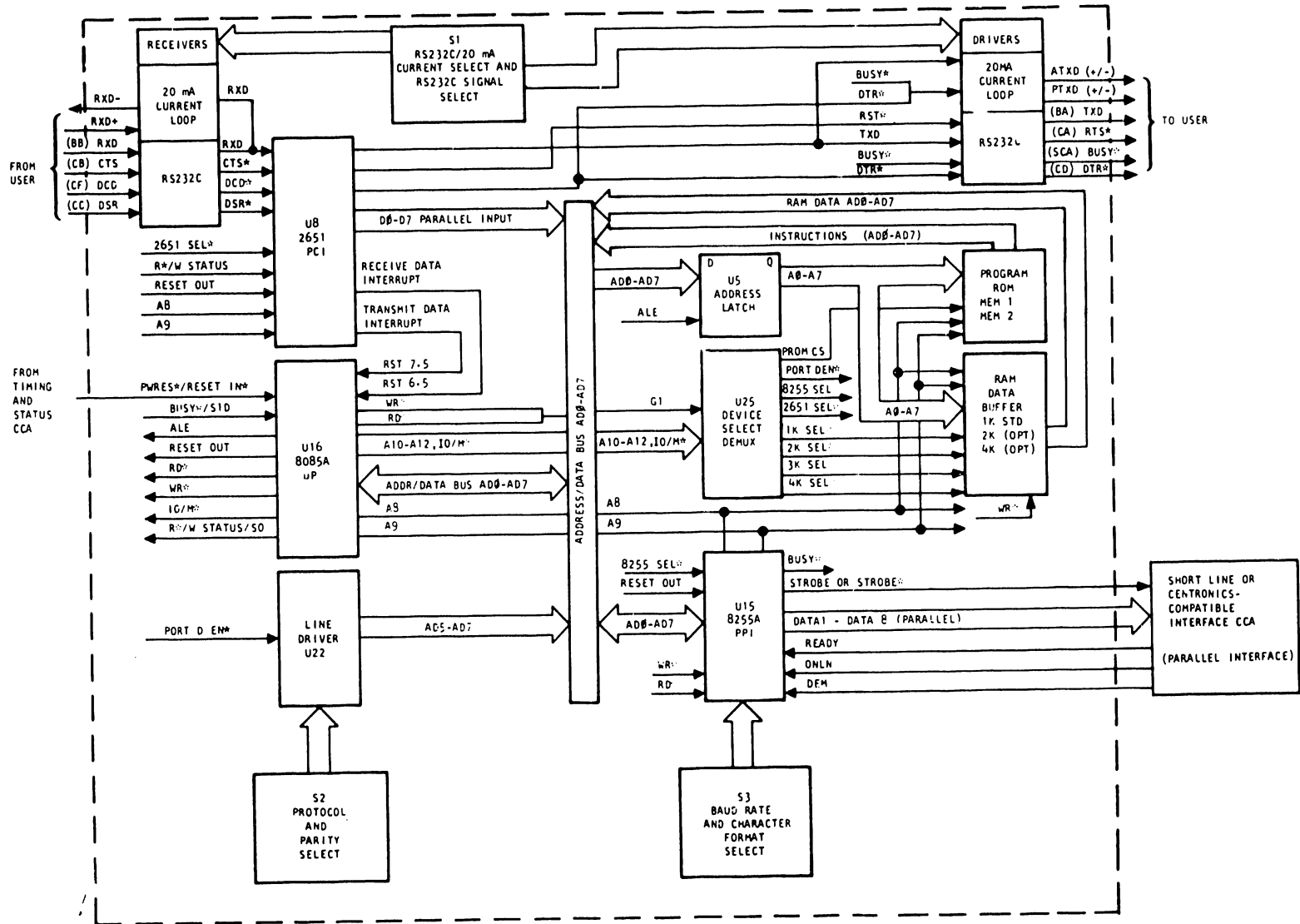
When power is applied to the printer, the system reset signal, PWRES*, from the Timing and Status CCA (SH 36) is sent to the Serial Interface CCA via the Mother Board CCA connector P2-20. See figure 2-31 for a block diagram of the Serial interface data flow.

PWRES* provides the microprocessor's RESET IN* signal (SH C2, U16) which sets the program counter to zero before proceeding through the routines needed to initialize the devices on the Serial Interface CCA. RESET IN* also sets the stack pointer to address Hex 7FD in the RAM data buffer, initializes all microprocessor flags and pointers, and unmask interrupt RST 6.5.

Meanwhile, RESET OUT resets the PPI and the PCI. Following the reset operation, the PPI must be programmed before it can receive command instructions from the microprocessor. This is done through the switch routine during which the contents of Port B of the PPI (SH C2, U15) and of Port D (SH C4, U22) are input to the 8085A microprocessor.

Character length, odd/even/off parity, and the number of stop bits are extracted from the input and loaded into the PCI mode register 1. The baud rate data is written into mode register 2. The type of communications protocol to be used is determined from Port D switches S-7 and S-8 and stored in flag bits D6 and D7 in the RAM data buffer address Hex 1FF.

Figure 2-31. Serial Interface CCA Functional Flow Diagram



Having completed the power up and switch routines, PPI Port C1 (U15-15) will be checked for the presence of a READY signal. When READY is high, the microprocessor interrupts are enabled. With READY high, a high ONLN signal at Port C3 (U15-17) will cause an enable transmitter command to be sent to the PCI command register. This command will enable the PCI transmitters and receivers, force DTR* and RTS* to low active, and reset the error flag.

At this point, the RAM data buffer is checked to determine if it contains data to be sent to the parallel interface CCA. Under power-up conditions, the RAM data buffer should be empty, and this is ascertained by loading (Hex 0FF) into the microprocessor H and L registers and adding this to the contents of the word count registers B and C. A carry indicates the presence of data.

A "no carry" condition will set the SCA mask and send this information to the PPI control register to inactivate the BUSY signal at PPI Port C6 (U15-11). The XON (Hex 11) character will then be loaded into the transmit data holding register of the PCI to be sent over the TXD (BA) line (**SH C4**) or ATXD+ (**SH C1**) as notice to the user that the printer is ready to receive data. If Data Set Ready (DSR*) and Data Carrier Detect (DCD*) options are implemented, the printer must also wait for these signals to be active before receiving data.

(d) User to Serial Interface Data Transfer - After the printer is ready to receive data, a low input to the PCI on the normally high RXD line constitutes a valid start bit. All data received by the PCI must be in the following format: start bit, 7 (optional 8) character bits with the LSB first, parity bit if used, and one (1) stop bit (optional 2 stop bits).

Input data is checked against the mode instructions which previously had been set in the PCI's mode registers by the CPU. A parity error will cause a parity error flag to be set in the status register. Failure to detect a valid stop bit will set a framing error flag. Note that the setting of an error flag does not stop the operation of the PCI.

The completed character is then loaded into the PCI's receive data holding register. RXRDY* is activated to notify the microprocessor that a character is ready to be fetched. If the microprocessor does not fetch the assembled character and complete a read operation before the next completed character is ready for the receive data holding register, an overrun error flag will be set and the character will be written over and lost.

Upon receiving a high signal at U16-8, the microprocessor will enter the RST 6.5 interrupt routine, which pushes the program status word and the contents of the registers onto the program stack and calls up the write routine. The first step in the write routine inputs the contents of the PCI status registers and checks for set error flags.

If no error flags are set, the character data is read from the PCI receiver and stored in a temporary register to be tested to determine if it is a US code, Null code, or a Select code (DC1). See **table 2-23** for the ASCII control codes. The US and DC1 codes are utilized by the Serial Interface CCA only when the Centronics-Compatible Interface CCA is installed. DC1 is recognized only

after the first time the printer is put On Line by pressing the ON LINE switch. If the test shows that the data is a US code, it will be stored in the next location of the RAM data buffer and the program will return from the RST 6.5 interrupt to await the next RXRDY* signal from the PCI.

The Null code (Hex 00) is used only to pad the data stream to prevent filling the data buffer at baud rates of 1200 and above (2400 baud for the 600 LPM). Since it is not printed, it is not loaded into the RAM data buffer. Therefore, the appearance of the Null code will cause the program to return immediately from the RST 6.5 interrupt to wait for the next RXRDY* signal from the PCI.

The Select code (DC1) (Hex 11) is not stored in the RAM data buffer, but is sent immediately to the PPI, Port A; and the PPI command register is notified to set PC7, which will furnish the STROBE* signal needed to transfer the Select code to the Centronics-Compatible Interface CCA. Note that the strobe polarity switch, S1-1, must be off to provide a low true strobe signal. After sending the Select code, the program will reset the STROBE* signal and return from the RST 6.5 interrupt.

If any error flags were set when the PCI status register was checked, Port D will be input to the microprocessor accumulator and the position of S-6 (SH C5) tested to determine whether parity should be ignored. If switch S2-6 is off, the program will check for framing and overrun errors and branch to the error routine. If the S2-6 switch is on, the routine branches immediately to the error routine.

In the error routine, the data is first read from the PCI receiver to prevent future overrun errors. The PCI receiver is enabled and the status error flags are reset. In the simplex mode, a question mark (?) is stored in the RAM data buffer in place of the questionable data. In the duplex mode, the microprocessor's error flag, D2 of flag, is set and later will cause a NAK to be sent to the user.

If the character read from the PCI receiver was neither a Null code nor a Select code, and the printer is configured for the simplex communications mode, the write pointer is loaded into the microprocessor's H and L registers, and the character data is moved into the RAM data buffer. The next write pointer value is calculated and the word counter is incremented.

In the duplex mode, line or full text duplex is first ascertained. In line duplex, the data is tested to determine if it is a Carriage Return (CR) which signifies the end of a line of transmission. Whether CR or character, the data is stored in the RAM data buffer and the word counter is incremented. However, after a CR, the error flag (flag bit D2) is checked and, if set, sets the NAK flag before returning from the RST 6.5 interrupt.

In the full duplex mode, no data will be stored in the RAM data buffer until a STX (Start of Text) code is received on the RXD input of the PCI (SH C2). Once transmitted, the STX code is not printed, but the program

sets the write-ok flag before returning from the RST 6.5 interrupt. If the data is not an STX code, and the write-ok flag had previously been set by the transmission of STX, the data is stored in the RAM data buffer.

An EXT (End of Text) code signifies the end of a block of transmission and sets the send-ok flag and resets the write-ok flag in the microprocessor. The error flag, flag bit D2, is then checked and, if set, sets the NAK flag before a return from the RST 6.5 interrupt.

(e) Serial Interface to Parallel Interface Data Transfer
- Once data has been loaded into the RAM data buffer, the PPI Port C inputs are tested to see if the parallel interface signals READY, ONLN, and DEM are active (SH C2, U15). When these conditions are met, the RAM data buffer is checked for empty and half-full conditions. If neither of these conditions occur, the protocol mode is tested.

In the simplex mode, transmission of data begins immediately. In the duplex mode, the send-ok flag must be set and a check of the NAK flag made before transmission of the data to the parallel interface CCA can be begun.

After monitoring the ONLN signal to assure that the printer is still on line, data is fetched from the RAM data buffer, moved to the microprocessor accumulator and from there sent to Port A of the PPI. A set strobe command is then sent to the PPI command register to provide the STROBE or STROBE* signal that notifies the parallel interface CCA that data is available on the DATA 1 through DATA 8 lines.

The function of the STROBE signal in the handshaking sequence and the manner in which data is handled by the printer after the STROBE signal is dependent on the type of parallel interface CCA installed. See **figure 2-3** for the standard Short Line Interface CCA data transfer timing and **figures 2-7 and 2-8** for the Centronics-Compatible Interface CCA data transfer timing.

After the data is transferred to the parallel interface CCA, the strobe is reset and the word counter is decremented. The program then returns to await another active DEM signal to signify that another byte of data can be transferred to the parallel interface CCA.

In the duplex mode, when READY, ONLN, and DEM are next active, an ACK signal will be sent to the user via the PCI transmit holding register and the TXD line. The ACK signal indicates that the data has been received without errors.

2.3.2 Processor CCA

The Processor CCA houses the printer master program and directs the execution of program instructions. It controls and stores data, monitors character band identity and position, generates all necessary enabling signals, and provides for system housekeeping functions.

Two (2) different Processor CCAs are used in B-Series printers. The 300 LPM and 600 LPM models use a 20-bit instruction word, while the 1000 LPM printer uses a 24-bit instruction word. The following paragraphs describe each of these Processor CCAs in terms of the types of instruction performed by each and the affected components.

a. 20-Bit Processor CCA (300 LPM and 600 LPM Printers)

The 20-bit Processor CCA is designed to accept five (5) program PROMs. The PROMs, MEM1 through MEM5 (SH 23), store the printer system program. The program is non-volatile when the printer is powered down and can be changed only by replacing the program PROMs.

Table 6-48 in section VI of volume II provides a list of the PROMs currently available for the 20-bit Processor CCA. Note that the Centronics-Compatible and serial interfacing systems use different PROMs with the same circuit card assembly.

Each PROM generates four (4) instruction signals that together make up the 20-bit micro-instruction word. Instruction registers, U15, U17, U18 (SH 24) and Address Bus Register U53 (SH 24) latch each instruction word that is output by the program PROMs. The registers are D-type flip-flops and output data on the positive-going edge of clock pulse C2* (SH 24). When C2* updates the instruction registers, it marks the beginning of a new micro-instruction cycle.

The Processor CCA executes four (4) types of micro-instructions. The format of each instruction word defines which one (1) of four (4) types is to be performed. **Figure 2-32** diagrams the micro-instruction format for each of the following types:

- ALU Functions
- Non-ALU Function/Conditional Address
- Non-ALU Function/Control Enable
- Non-ALU Function/Move Immediate Data

The following paragraphs describe each type of micro-instruction in terms of the devices or networks involved. **Figure 2-33** provides a block diagram of the major Processor CCA devices.

1. ALU Functions - As shown in **figure 2-32**, signal INST00, when equal to one (1), indicates that an ALU function is to be executed. The ALU, U32 and U51 (SH 25), is capable of performing 16 logical and 16 arithmetical operations for a total of 32 functions. INST01, the mode control, indicates a logical function when high and an arithmetical function when low.

Select signals INST02 through INST05 specify which of the 32 functions will be performed. **Table 2-24** lists the ALU function that results from each combination of INST02 through INST05 signal levels.

ALU FUNCTION INSTRUCTION DECODING CHART

INSTRUCTIONS																			
13	12	11	10	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
DEVICE ENABLE					REGISTER ENABLE					WORKING REGISTER WRITE	DEVICE LOAD			ALU FUNCTION					
DE4	DE3	DE2	DE1	DE0	R4	R3	R2	R1	R0	0 - NO WRITE TO WORKING REGISTER 1 - WRITE 0 PLUS TO WORKING REGISTER ADDRESS BY REGISTER ENABLE	DL2	DL1	DL0	S3	S2	S1	S0	M	I
REFERENCE DEVICE ENABLE CHART (TABLE 2-26) (FIGURE 2-35)					REFERENCE REGISTER ENABLE CHART (TABLE 2-25) (FIGURE 2-34)						REFERENCE DEVICE LOAD CHART (TABLE 2-27) (FIGURE 2-36)			REFERENCE ALU FUNCTION CHART (TABLE 2-24)					

NON ALU FUNCTION/PROGRAM ADDRESSING INSTRUCTION DECODING CHART																			
13	12	11	10	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
BRANCH OR CALL ADDRESS											CONDITION SELECTED			SEQUENCE FUNCTION					
A4	A3	A2	A1	A0		CONDITION ENABLE	C2	C1	C0	U1	U0	FL	PLP						
											REFERENCE CONDITION SELECTED CHART (TABLE 2-28) (FIGURE 2-37)			REFERENCE SEQUENCE FUNCTION CHART (TABLE 2-29) (FIGURE 2-38)					

NON ALU FUNCTION CONTROL ENABLE INSTRUCTION DECODING CHART																			
13	12	11	10	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
CONTROL ADDRESS				CONTROL GROUP NUMBER ENABLE				NOT USED											
CA3	CA2	CA1	CA0	CE3	CE2	CE1	CE0					1	0	0	1	0	0		
REFERENCE CONTROL GROUP CHART (TABLE 2-30)																			

NON ALU FUNCTION/MVI INSTRUCTION DECODING CHART																			
13	12	11	10	0F	0E	0D	0C	0B	0A	09	08	07	06	05	04	03	02	01	00
IMMEDIATE DATA										DEVICE LOAD									
I4	I3	I2	I1	I0	DL2	DL1	DL0												
										REFERENCE DEVICE LOAD CHART (TABLE 2-27) (FIGURE 2-36)									

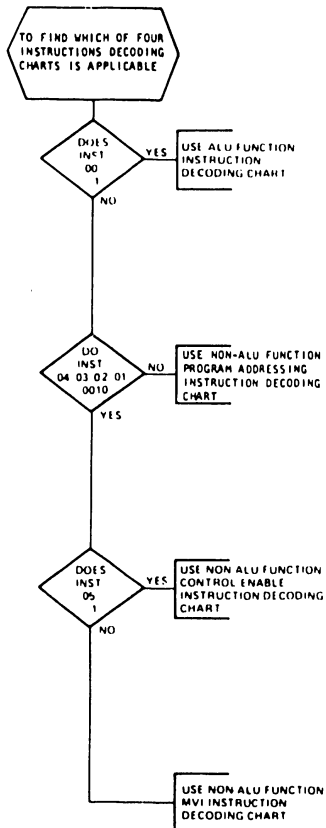


Figure 2-32. 20-Bit Processor CCA
 Micro-Instruction Types
 (300 LPM and 600 LPM Only)

TABLE 2-24. ALU FUNCTION CONTROL

Instruction Line					Function	Description
05 (S3)	04 (S2)	03 (S1)	02 (S0)	01 (M)		
0	0	0	0	0	A Plus 1	Increment A
0	0	0	1	0	(A + B) Plus 1	N/A
0	0	1	0	0	(A + B*) Plus 1	N/A
0	0	1	1	0	Zero	Clear
0	1	0	0	0	A Plus (A & B*) Plus 1	N/A
0	1	0	1	0	(A + B) Plus (A & B*) Plus 1	N/A
0	1	1	0	0	A Minus B	Subtract
0	1	1	1	0	A & B*	N/A
1	0	0	0	0	A Plus (A & B)	N/A
1	0	0	1	0	A Plus B	Add
1	0	1	0	0	(A + B*) Plus (A & B)	N/A
1	0	1	1	0	(A & B) Minus 1	N/A
1	1	0	0	0	A Plus A	Shift Left
1	1	0	1	0	(A + B) Plus A	N/A
1	1	1	0	0	(A + B*) Plus A	N/A
1	1	1	1	0	A Minus 1	Decrement
0	0	0	0	1	A*	Complement A
0	0	1	1	1	(A + B)*	NOR
0	0	1	0	1	A* + B	N/A
0	0	1	1	1	0	Clear
0	1	0	0	1	(A & B)*	NAND
0	1	0	1	1	B*	Complement B
0	1	1	0	1	A + B	Exclusive OR
0	1	1	1	1	A & B*	N/A
1	0	0	0	1	A* + B	N/A
1	0	0	1	1	(A + B)*	Exclusive NOR
1	0	1	0	1	B	B Out
1	0	1	1	1	A & B	AND
1	1	0	0	1	1	Preset
1	1	0	1	1	A + B*	N/A
1	1	1	0	1	A + B	OR
1	1	1	1	1	A	A Out

Notes: & = Logic AND Function
 + = Logical OR Function
 * = Logical NOT Function
 + = Logical EXCLUSIVE OR Function

Each instruction specifying an ALU function must also control ALU data input and output lines. Inputs to the ALU are controlled by the Register Enable (INST0A through INST0E) and Device Enable (INST0F through INST13) segments of the instruction word. See **figure 2-32**.

Output data from the ALU operations can be directed to any device determined by the Device Load (INST06 through INST08) portion of the instruction word or to one (1) of sixteen working registers at U42 and U43 (**SH 27**). INST09, the working register control bit, will, when high, store data on the OBUS in the working register determined by the Register Enable segment of the instruction word.

(a) Register Enable Network - The Register Enable Network (SH 27 and SH 29) controls the output of data from the various registers on to the RGBUS for processing by the ALU. The Register Enable Decoder U5 (SH 29) is a 3-to-8 line decoder/demultiplexer that decodes three (3) select inputs (INST0A, INST0B, INST0C) and three (3) enable inputs (INST0D, INST0E, INST00) to generate one (1) low active signal. This active signal enables the contents of the Accumulator 1, the Data Buffer, the User Data Latch, or the VFU Data Buffer to be output to the ALU.

The sixteen 8-bit working registers U42 and U43 (SH 27) are controlled by the Register Enable Network and by the working register write signal W* (INST09). These read/write RAMs provide scratch pad memory for controlling and moving data to and from the ALU. Instructions INST0A, INST0B, INST0C, and INST0D are the address signals for the registers.

Enable signal W* is the gated result of instructions INST00 (always high for ALU-Function operations), INST0E, INST09, and clock pulse C2. Instruction INST09 is the mode control and, when a logic "1", specifies a "Write OBUS to Addressed Register" operation. When it is a logic "0", it indicates a "No Write" operation. Register Latch U61 holds the data output from one (1) of the working registers for release onto the RGBUS.

The RGBUS Mask controls allow a single data bit of a register's contents to be selected and tested. In this way, the processor can determine the status of various program controls and flags.

Figure 2-34 diagrams the devices which make up the Register Enable Network. Table 2-25 lists the instruction word bits and their various combinations that control the choice of the register to be enabled or the RGBUS bit to be sampled.

TABLE 2-25. REGISTER ENABLE CONTROL

Instruction Word Bit					Register Enabled
0E (R4)	0D (R3)	0C (R2)	0B (R1)	0A (R0)	
0	0	0	0	0	No Operation
0	0	0	0	1	Accumulator One
0	0	0	1	0	Data Buffer
0	0	0	1	1	User Data Latch*
0	0	1	0	0	VFU Data Buffer*
0	0	1	0	1	N/A
0	0	1	1	0	N/A
0	0	1	1	1	N/A

*Actual registers resident on the Interface CCA.

TABLE 2-25. REGISTER ENABLE CONTROL (Cont'd)

Instruction Word Bit					Register Enabled
0E (R4)	0D (R3)	0C (R2)	0B (R1)	0A (R0)	
0	1	0	0	0	RGBUS Mask 0
0	1	0	0	1	RGBUS Mask 1
0	1	0	1	0	RGBUS Mask 2
0	1	0	1	1	RGBUS Mask 3
0	1	1	0	0	RGBUS Mask 4
0	1	1	0	1	RGBUS Mask 5
0	1	1	1	0	RGBUS Mask 6
0	1	1	1	1	RGBUS Mask 7
1	0	0	0	0	GP Register 0
1	0	0	0	1	GP Register 1
1	0	0	1	0	GP Register 2
1	0	0	1	1	GP Register 3
1	0	1	0	0	GP Register 4
1	0	1	0	1	GP Register 5
1	0	1	1	0	GP Register 6
1	0	1	1	1	GP Register 7
1	1	0	0	0	GP Register 8
1	1	0	0	1	GP Register 9
1	1	0	1	0	GP Register A
1	1	0	1	1	GP Register B
1	1	1	0	0	GP Register C
1	1	1	0	1	GP Register D
1	1	1	1	0	Flag Register
1	1	1	1	1	Mode Register

(b) Device Enable Network (SH 30) - The Device Enable Network allows data to be placed on the INBUS for processing by the ALU. Device Enable Decoder U47 (SH 30) is a 3-to-8-line decoder/demultiplexer with select inputs INST0F, INST10, and INST11, and enable inputs INST00, INST12, and INST13. Only one (1) output is active (low) at a time.

Signals from U47 control the character band-image/position-counter multiplexer U21/U22 (SH 26), Accumulator 2 at U55 (SH 26), Timing and Status CCA Ports 0 and 1 (SH 35), and the Information Port at U37 (SH 26). Table 2-26 lists the enable control signals for these and other affected devices. Figure 2-35 provides a block diagram of the major devices of the Device Enable Network.

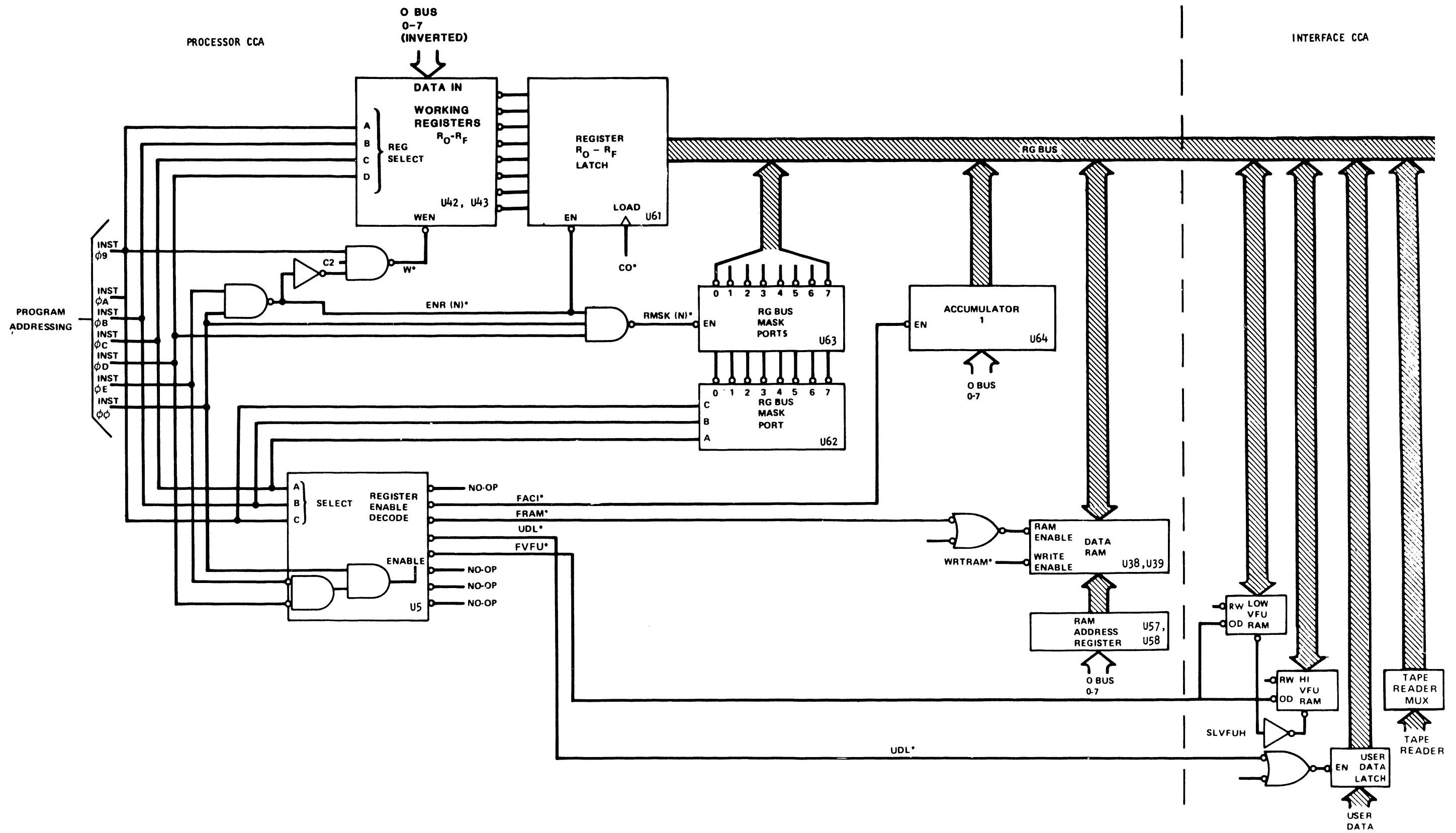


Figure 2-34. Register Enable Network

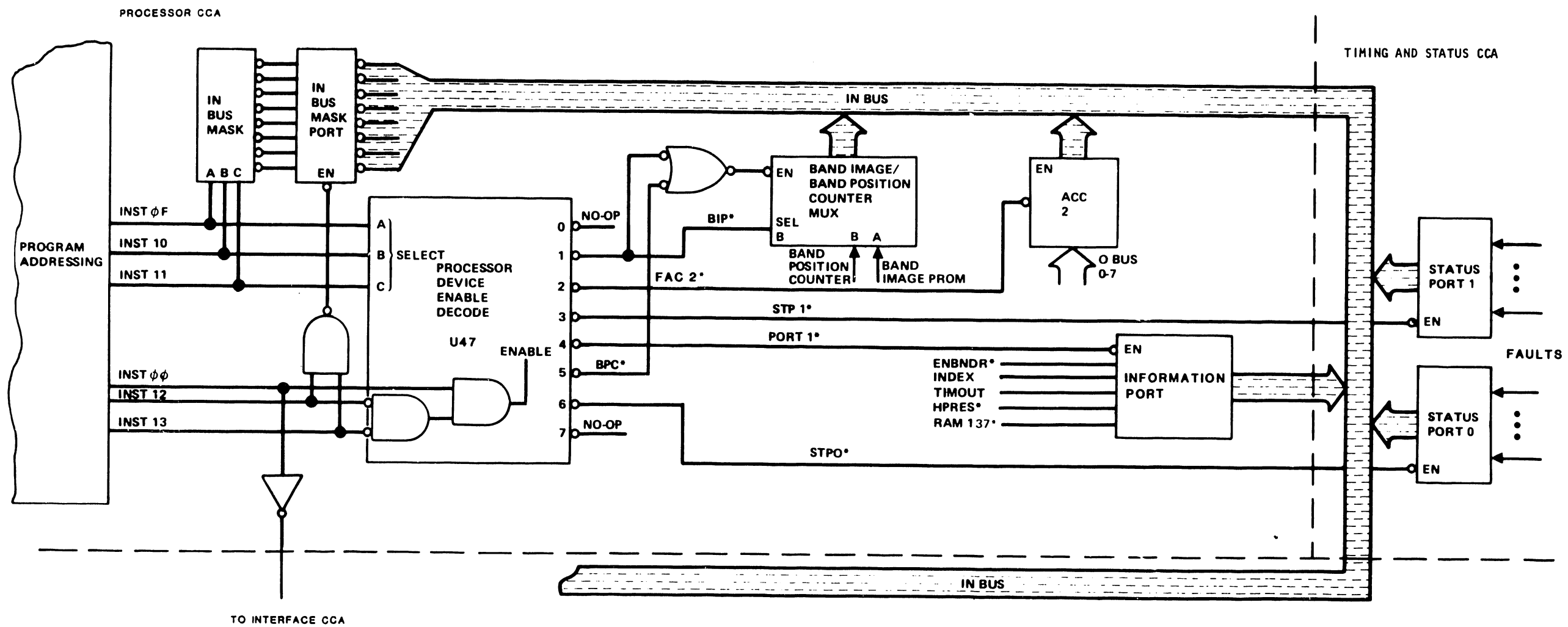


Figure 2-35. Device Enable Network

TABLE 2-26. DEVICE ENABLE CONTROL

Instruction Word Bit					Device Enabled	Signal Output Condition
13 (D4)	12 (D3)	11 (D2)	10 (D1)	0F (D0)		
0	0	0	0	0	No Operation	
0	0	0	0	1	Band Image PROM	BIP* active to U22-1 (SH 26)
0	0	0	1	0	Accumulator Two	FAC2* active to U55-1 (SH 26)
0	0	0	1	1	Timing and Status Port 1	STP1* active to P2-9 (SH 30)
0	0	1	0	0	Information Port 1	PORT1* active to U37-1 (SH 26)
0	0	1	0	1	Band Position Counter	BPC* active to U48-5 (SH 30)
0	0	1	1	0	Timing and Status Port 2	STP0* active to P1-55 (SH 30)
0	0	1	1	1	N/A	
0	1	0	0	0	N/A	
0	1	0	0	1	N/A	
0	1	0	1	0	N/A	
0	1	0	1	1	N/A	
0	1	1	0	0	N/A	
0	1	1	0	1	N/A	
0	1	1	1	0	N/A	
0	1	1	1	1	N/A	
1	0	0	0	0	Form Length PROM	FLSS* active from U29-15 (SH 7)
1	0	0	0	1	Configuration Group 4	CG4* active from U29-14 (SH 7)
1	0	0	1	0	Configuration Group 3	CG3* active from U29-13 (SH 7)
1	0	0	1	1	Control Panel Switches	CPS* active from U29-12 (SH 7)
1	0	1	0	0	Interlock Switches	INSW* active from U29-11 (SH 7)
1	0	1	0	1	N/A	
1	0	1	1	0	Configuration Group 2	CG2* active from U29-9 (SH 7)
1	0	1	1	1	Usr Control Data	UCL* active from U29-7 (SH 7)
1	1	0	0	0	INBUS Mask 0	INMSK0* active to U36-1 (SH 26)
1	1	0	0	1	INBUS Mask 1	INMSK1 active
1	1	0	1	0	INBUS Mask 2	INMSK2* active
1	1	0	1	1	INBUS Mask 3	INMSK3* active
1	1	1	0	0	INBUS Mask 4	INMSK4* active
1	1	1	0	1	INBUS Mask 5	INMSK5* active
1	1	1	1	0	INBUS Mask 6	INMSK6* active
1	1	1	1	1	INBUS Mask 7	INMSK7* active

(c) Device Load Network - The Device Load Network specifies the device into which data from an ALU operation should be stored. Table 2-27 lists the devices and their reference designations. Demultiplexer U29 (SH 29) decodes select inputs INST06, INST07, and INST08. The gating of instructions INST00, INST03, INST04, and INST05 provides one (1) enable input at pin 5. A second enable, C0*, is the first phase of the three-phase system clock generator U14. The third enable input at pin 4 is tied low. Figure 2-36 provides a block diagram of the Device Load Network.

TABLE 2-27. DEVICE LOAD CONTROL

Instruction Word Bit			Device Loaded	Device No.	Active Signal
08 DL 2	07 DL 1	06 DL 0			
0	0	0	No Operation	N/A	
0	0	0	Accumulator One	U64	TAC1*
0	1	0	Accumulator Two	U55	TAC2*
0	1	1	Buffer Address Reg.	U57, U58	TMAR*
1	0	0	Band Image Address Reg.	U24	TIAR*
1	0	1	VFU Data Buffer	U36, U38, U39, U40	TCFURM*
1	1	0	Data Buffer Write	U38, U39	TRAM*
1	1	1	Interval Timer	U26, U25, U45	TIME*

NOTE

For the non-ALU function, the Sequence Address Register is loaded instead of the VFU Data Buffer. TSQAR* is then active to U1, U2, and U20 (SH 24).

2. Non-ALU Function/Conditional Address Instructions - The conditional address function allows the program to branch to an instruction or subroutine other than the next one in program sequence. The processor samples one (1) of eight (8) possible system conditions (specified by the current instruction) to determine whether the program should branch to a subroutine address or continue with the next incremented address. **Table 2-28** lists these eight conditions.

TABLE 2-28. CONDITIONAL ADDRESS INPUTS

Instruction Word Bit				Conditional Operations
08 C3	07 C2	06 C1	05 C0	
0	0	0	0	Unconditional (Branch, Call, Return, Jump)
0	0	0	1	ALU: (A = B) Output = 1
0	0	1	0	ALU: (A = B) Output = 0
0	0	1	1	ALU: Carry Output
0	1	0	0	User Respond
0	1	0	1	System Status Change
0	1	1	0	Stop I/O Transfer
0	1	1	1	Sentinel Bit

Note: No conditional operations are currently defined for the remaining eight (8) possible combinations with the C3 bit at Logic "1". These eight additional combinations are provided for future expansion.

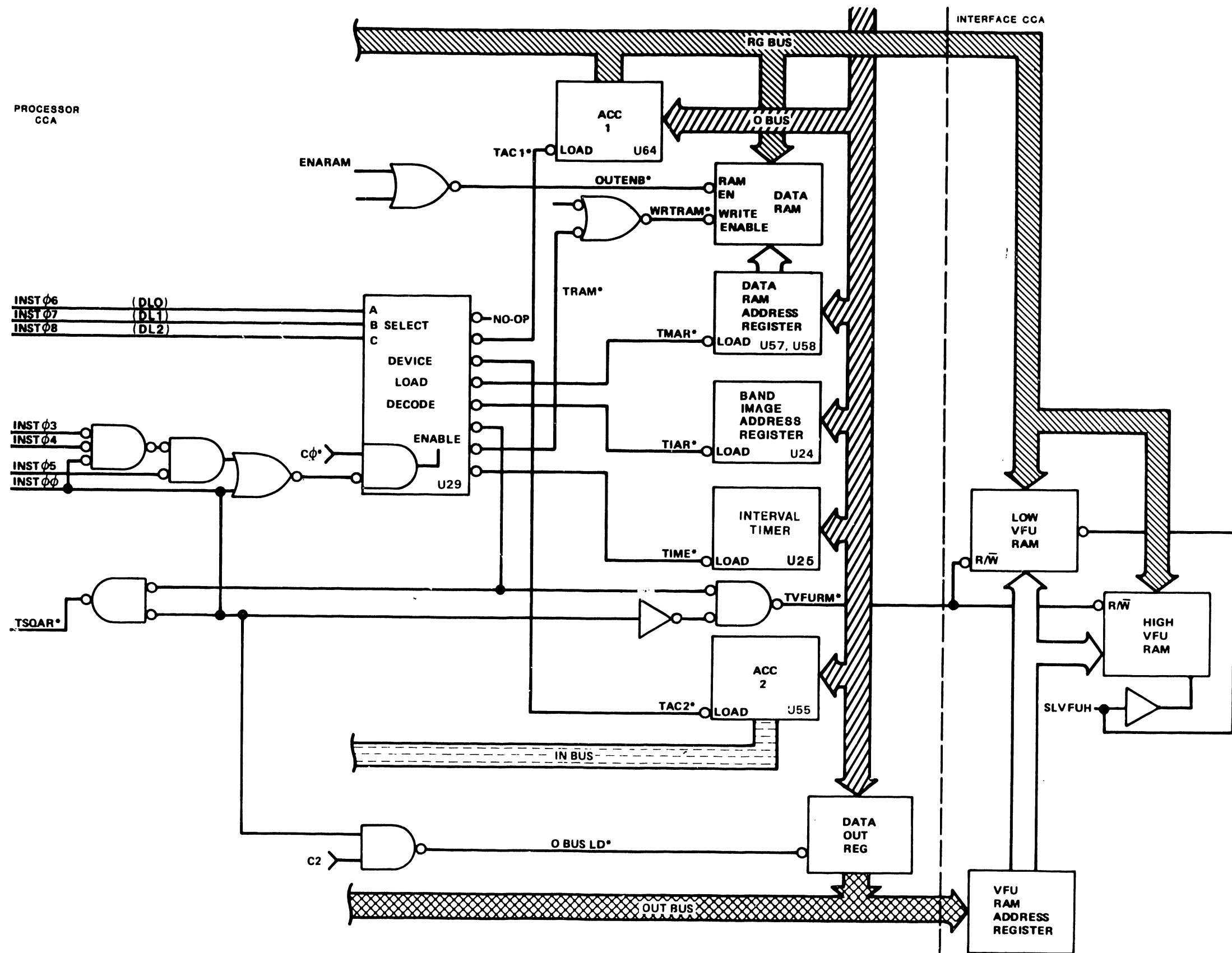


Figure 2-36. Device Loading Network

(a) Condition Monitor - The Condition Monitor consists of data latch U30 and data multiplexer U49 (SH 29). Latch U30 temporarily stores ALU output signals EQUAL and CARRY*, retaining the data when the enable input at pin 4 is low and transferring it when pin 4 is high. This enable signal is the gated result of INST00 (low for non-ALU operation) and C2* at U12.

Condition Monitor U49 is an 8-to-1-line multiplexer with two kinds of inputs: ALU output signals (EQUAL and CARRY*) via latch U30, and system status signals from the illegal decoder/multiplexer U40, Sentinel Monitor U59, and the Timing and Status CCA (RSPOND and SYSTCH*). The sentinel RAM is only installed on the circuit card assembly with part number 257315-001. The condition monitor samples one of these inputs according to the decoding of select lines INST05, INST06, and INST07. Instruction INST08 is the enable input.

If the sampled condition is inactive (status remains good), the monitor's single output is active low. It is gated at U13 with instructions INST00, INST03, and INST04 to generate the signal INCPC* (Increment Program Counter) that is the select input to the Microsequencer Function Selector U19. Figure 2-37 shows the Condition Monitor network.

(b) Microsequencer Function Selector - The Microsequencer Function Selector U19 (SH 24) is a 2-to-1-line multiplexer whose outputs control the Microsequencer Address Register U1, U21, and U20. Table 2-29 gives the function table for the control signals, Push/Pop (PUP), File Enable (FE*), S0, and S1.

The "A" inputs to the function selector are hard-wired to produce, when selected, the control code (001X) that increments the program counter.

TABLE 2-29. MICROSEQUENCER CONTROL

S1 (Q1)	S0 (Q0)	FE	PP	Function
0	0	0	0	Increment Program Counter, Pop Stack
0	0	0	1	Increment Program Counter, Push Stack
0	0	1	X	Increment Program Counter
0	1	0	0	Jump to Address Register, Pop Stack
0	1	0	1	Jump to Address Register, Push Stack
0	1	1	X	Jump to Address Register
1	0	0	0	Return, Pop Stack
1	0	0	1	Return, Push Stack
1	0	1	X	Return
1	1	0	0	Jump to Direct Data Input Signal, Pop Stack
1	1	0	1	Jump to Direct Data Input Signal, Push Stack
1	1	1	X	Jump to Direct Data Input Signal

Note: Push and Pop Stack commands are disabled when the "FE" signal is a logic "1". When "FE" is a logic "0", it enables the PP signal to increment or decrement the internal stack pointer within the microsequencer.

Incrementing the program counter moves the program to the next instruction address in sequence. The "B" inputs are instruction bits INST01-04. When the condition monitor output INCPC* is high, the "B" inputs are selected, forcing a conditional address and incrementing or decrementing the internal stack pointer according to the control logic detailed in **table 2-29**. **Figure 2-38** provides a block diagram of Microsequencer Function Selector and Sequencer.

(c) Microsequencer Address Register - The Microsequencer (U1, U2, U20, **SH 24**) generates the next address for each program instruction. It selects, as the source of the next address, either the Program Counter Register (for an incremental step), the direct address contained in bits 09 through 13 of the conditional address micro-instruction (for a program branch), or the internal Stack Register (for a jump or return). As detailed in **table 2-29**, inputs S0 and S1 select the microsequencer function; FE* and PUP control the internal Stack Register.

The Stack Register stores addresses to which the program can jump to begin a subroutine or to which it can return upon completion of a subroutine. Up to four micro-instruction addresses can be nested on a "First-in, Last-out" basis. An internal stack pointer always points to the last word written in the register.

Conditional address instructions thus may move the program to a branch address specified by the instruction itself if the condition is met, to the next address in normal sequence if the condition is not met, or to a jump or return address stored in the Stack Register (an unconditional branch).

3. Non-ALU Function/Control Enable Instructions - The control-enable decoding function allows the Processor CCA to generate various control signals needed for correct system operation. When control-enable instructions are executed, the INCPC* input to the Microsequencer Function Selector is inactive (high) and forces the microsequencer to output an incremented next address. The selected control function is performed according to program definition, and the program continues in its normal sequence.

(a) Control Enable Decoder - Control Group Enable Decoder U65 (**SH 29**) is a 3-to-8-line demultiplexer whose outputs select and enable eight (8) control group devices located on various printer CCAs. Only one (1) output is active low and one (1) control group is enabled at a time. Select inputs to U65 are instructions INST0C, INST0D, and INST0E. Enable inputs are INST05, the result of gating INST03, INST04, and INST00 at U34, and the output of U67 which NORs INST0F and clock signal C1*.

(b) Function Control Groups (**SH 29**) - Devices selected by the Control Enable Decoder generate two (2) kinds of output, set/reset flip-flop-signals and timing pulses. The eight (8) control groups, their location, and function are shown in **table 2-30**.

Figure 2-38. 20-Bit Processor CCA Microsequencer Function Selector and Sequencer

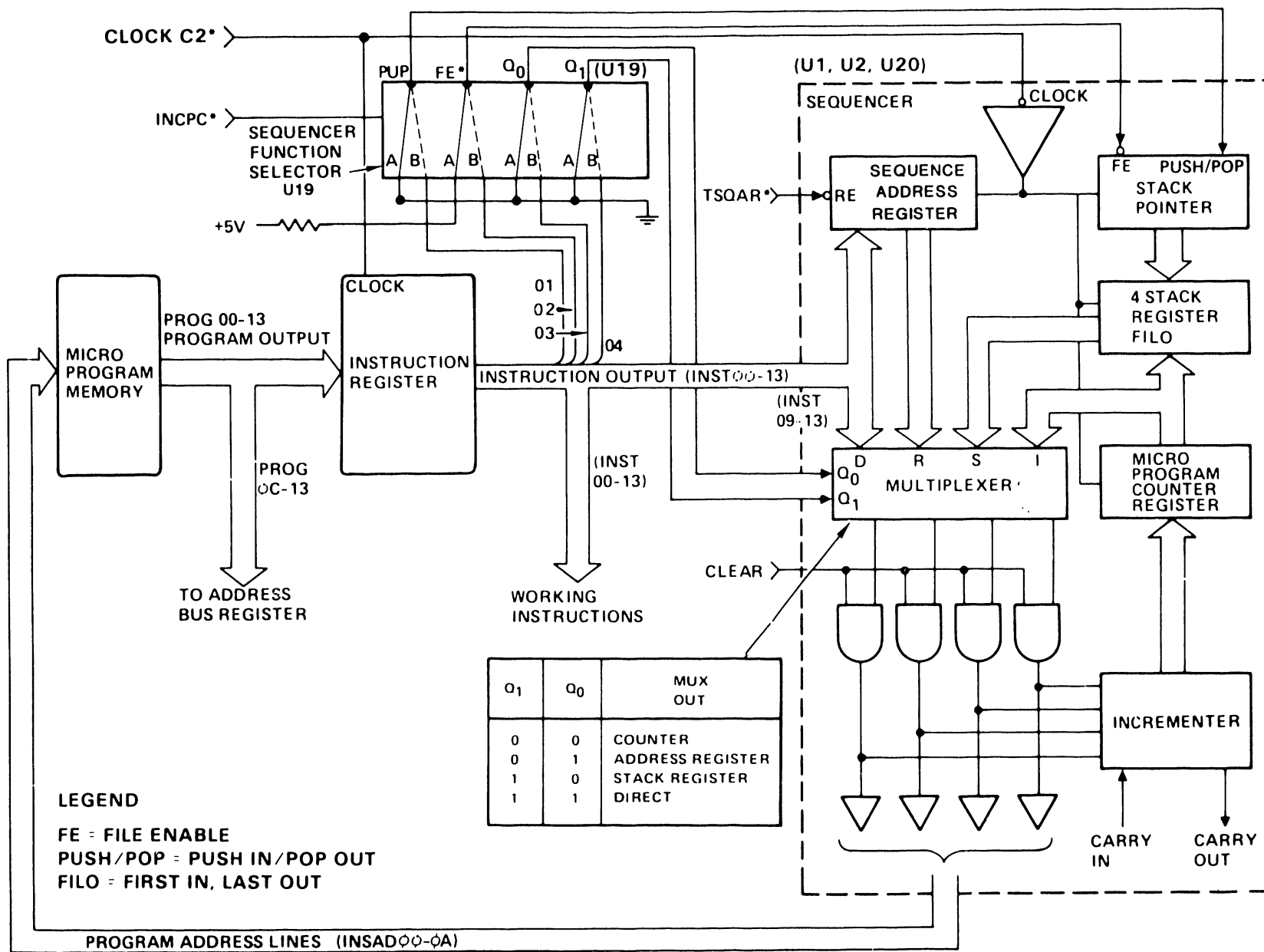


TABLE 2-30. FUNCTION CONTROL GROUPS

Control Group	Location	Circuit Reference	Control
0	Interface CCA	U47, SH 7	Set/Reset Flip-Flop
0	Centronics-Compatible Interface CCA	U27, SH B7	Set/Reset Flip-Flop
1	Processor CCA	U46, SH 30	Timing Pulse Generation
2	Centronics-Compatible Interface CCA	U24, SH B6	Timing Pulse Generation
3	Interface CCA	U28, SH 7	Timing Pulse Generation
3	Timing and Status CCA	U48, SH 36	Timing Pulse Generation
3	Centronics-Compatible Interface CCA	U43, SH B7	Timing Pulse Generation
4	Power Board CCA	U5, SH 39	Set/Reset Flip-Flop
5	Interface CCA	U14, SH 7	Set/Reset Flip-Flop
5	Centronics-Compatible Interface CCA	U25, SH B7	Set/Reset Flip-Flop
6	Interface CCA	U13, SH 6	Set/Reset Flip-Flop
6	Centronics-Compatible Interface CCA	U14, SH B6	Set/Reset Flip-Flop
7	Processor CCA	U28, SH 30	Set/Reset Flip-Flop

Tables 2-31 and 2-32 show the function assignments for Control Groups 1 and 7 located on the Processor CCA. Tables for the other control groups will be found in other sections that describe the respective CCAs.

(1) Control Group 1 Decoder - Control Group 1 Decoder U46 (SH 30) is a 3-to-8-line demultiplexer enabled by U65 output-signal ECG1* (Enable Control Group 1) and instruction INST13. This active-low device decodes select inputs INST10, INST11, and INST12 to generate one (1) of the output signals shown in table 2-31.

TABLE 2-31. CONTROL GROUP 1 DECODE AND FUNCTIONS

Instruction Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	Write Sentinel	WSENT* active to U48-1; WRSENT* low to U59-12 (SH 28)
0	0	0	1	Increment RAM Address	IMAR* active to U48-13; INCRAM* low to U57-5 (SH 28)
0	0	1	0	Decrement RAM Address	DMAR* active to U57-4 (SH 28)
0	0	1	1	Clear Band Timeout Counter	BTCLR* active to U9-1 to clear U8 (SH 30)
0	1	0	0	Load Even S Register	EVREG* active to P1-24
0	1	0	1	Load Even Hammer Data	EVHAMR* active to P1-36
0	1	1	0	Load Odd S Register	ODSREG* active to P1-23
0	1	1	1	Load Odd Hammer Data	ODHAMR* active to P1-35
1	0	0	0	N/A	
1	0	0	1	N/A	
1	0	1	0	N/A	
1	0	1	1	N/A	
1	1	0	0	N/A	
1	1	0	1	N/A	
1	1	1	0	N/A	
1	1	1	1	N/A	

(2) Control Group 7 Decoder - Control Group 7 Decoder U28 (SH 30) is an 8-bit addressable latch enabled by U65 output ECG7*. Instruction bits INST10, INST11, and INST12 are the select inputs. Instruction INST13 is the data-in bit that provides set/reset control for eight addressable latches. Control Group 7 sets the mode for the various Processor CCA functions. Table 2-32 lists the decoded set/reset signals.

TABLE 2-32. CONTROL GROUP 7 DECODE AND FUNCTIONS

Instruction Line				Function	Output Signal Condition
13	12	11	10		
0	0	0	0	Disable RAM Output	ENARAM inactive low
0	0	0	1	Reset Load Mode	LDMODE inactive low
0	0	1	0	Reset Format Mode	U28-6 low to U7-9
0	0	1	1	Set Sentinel Data Bit**	SENTIN* active low
0	1	0	0	Disable Band Drive	U28-9 low to U6-9
0	1	0	1	Enable Demand Increment	DISDEM inactive low to U67-12
0	1	1	0	Reset Image Address Bit 0	IMAD0 low to U27-14
0	1	1	1	Reset Image Address Bit 1	IMAD1 low to U27-13
1	0	0	0	Enable RAM Output	ENARAM active high
1	0	0	1	Set Load Mode	LDMODE active high
1	0	1	0	Set Format Mode	U28-6 high to U7-9
1	0	1	1	Reset Sentinel Data Bit**	SENTIN* inactive high
1	1	0	0	Enable Band Drive	U28-9 high to U6-9
1	1	0	1	Disable Demand Increment	DISDEM active high to U67-12
1	1	1	0	Set Image Address Bit 0	IMAD0 high to U27-14
1	1	1	1	Set Image Address Bit 1	IMAD1 high to U27-13

**The Sentinel Data Bit is used only on the dash -001 Processor CCA.

4. Non-ALU Function/Move-Immediate Data Instructions - Non-ALU Function/MVI Instructions allow the processor access to programmed constants stored in the program PROMs. This data value or address is moved directly to one of the devices listed in **table 2-27** as specified by device load bits INST06-08. When the selected device is the Sequencer Address Register, eleven instruction lines (INST09 - INST13) are used as the data input. For the other devices, eight instruction bits (INST09-INST10) are used.

This type of instruction can be used, for example, to load data into the Interval Timer for counting down a delay subroutine, or to load an address into one of the address registers. The INCPC* input to the Microsequencer Function Selector is inactive (high), causing instruction lines INST01-04 to be selected as input to the microsequencer. These bits are defined (001X) to cause the microsequencer to output an incremented next program address.

5. Processor CCA Devices - This paragraph describes the Processor CCA devices that transmit data onto the printer system INBUS. Each device's function, inputs, outputs, and enabling control are discussed in the following paragraphs.

(a) Band Image PROMs - The Band Image PROMs, MEM6, MEM7, and MEM8 (**SH 31**), store a digital-coded representation of the characters on the print band. Each PROM contains the coded likeness of one complete band. Thus, up to three (3) different bands can be used in the printer. To identify the band in use, the microprogram compares coded identification pulses read from the character band (via the transducer and Timing and Status CCA) with a code stored in a predefined location of each band image PROM. For this reason, all three (3) PROMs must have different dash numbers. When one of the three PROMs is found to match the band in use, the appropriate PROM select signal IMAG1*, IMAG2*, or IMAG3*, enables that device.

The Band Image PROM outputs are sent to the Band Image PROM/Band Position Counter Multiplexer U21 and U22 (**SH 26**) along with input from Band Position Counter U4 (**SH 30**). The select signal for the BIP/BPC multiplexer BIP*, an output of Device Enable decoder U47 (**SH 30**), is gated with another output of U47, BPC*, to produce enable input BPCBIP*. The states of these signals determine which data inputs will be output to the INBUS. If BIP* is logical "0", data inputs from the Band Image PROM are selected. If BIP* = 1, data signals from Band Position Counter U4 are selected.

(b) Band Position Counter - The Band Position Counter U4 (**SH 30**) is a cascaded, dual 4-bit binary counter clocked by the Hammer Pulse Reset Signal (HPRES*) from hammer timing circuitry on the Timing and Status CCA. U4 counts each time a character on the band lines up in front of hammer number 1. It is cleared after each band revolution (the maximum count range is 207) when signal INDEX* goes high. Output signals from U4, BPOST0 - BPOST8, are loaded on to the INBUS via the BIP/BPC U21/U22 and are used to determine a match between user data characters in the data RAM and band characters represented in the Band Image PROMs.

(c) Band Image PROM Addressing - The Band Image PROMs MEM6, MEM7, and MEM8 (**SH 31**) have two distinct sources for address

inputs as selected by the Band Image Address multiplexer U23 and U41. The multiplexer has as the "A" input signals, the output of the Image Address Register U24. The "B" input signals are derived from the data present on RGBUS 0 through 4 for the five (5) low order bits. The three (3) high order bits are hard-wired to force addressing the upper 32 locations of the Band Image PROMs.

The signal LDMODE from the Control Group 7 Decoder U28 provides the select input to the multiplexer. LDMODE at 0 selects image address "A" inputs; LDMODE at 1 selects the "B" inputs described above.

The Image Address Register U24 (SH 25) is used for addressing PROM locations 00 to BF hexadecimal. It receives input information from the OBUS that is loaded into its D-type flip-flops by the Device Load Decoder signal TIAR*. This addressing method selects all information in MEM6, MEM7, and MEM8 except the illegal look-up table in the 32 high order locations.

The "B" inputs from the RGBUS 0 through 4 access the illegal look-up table in the upper 32 locations of PROMs MEM6, MEM7, and MEM8 and provide the Processor CCA with a means of determining which user data received is legal and printable. The PROM outputs are presented to the Illegal (Detect) Decoder U40 in order that character legality may be defined. U40 is an 8-to-1 multiplexer with each input representing one of 256 possible 8-bit code combinations.

The output of U40, signal ILEGAL*, defines whether the 8-bit character on the RGBUS is legal and printable. When ILEGAL* is 1, the character is legal; when ILEGAL* is 0, the character is not legal. This output information is gated at U56 and used to generate the STOPIO signal for input to the Condition Monitor U49.

(d) Accumulator 2 - Accumulator 2 (U55, SH 26) is a 1x8 latch that stores data from the OBUS for transmission to the INBUS. Accumulator 2, a group of D-type flip-flops, clocks in data when TAC2* (To Accumulator 2) is low and transfers the input data to output data on the positive-going transition of TAC2*. The Q outputs remain at the logic states that were set up at the D inputs. Output control for Accumulator 2 is signal FAC2* (From Accumulator 2) generated by Device Enable Decoder U47 (SH 30).

Accumulator 2 typically is used to hold data for manipulation by the ALU. An instruction might direct the ALU (U32, U51) to add the contents of a register, which has been enabled onto the RGBUS, to the operand stored in Accumulator 2 and to hold the result in Accumulator 2.

(e) Information Port 1 - Information Port 1 (U37, SH 26), a tri-state driver, receives input signal information from the following:

- Interval timer U26 for TIMOUT*.
- RAM Address Registers U57, U58 for RAM137*.

- Enable band drive signal generated by Control Group 7 for ENBNDR*.
- Timing and Status CCA via P2 for INDEX.
- Timing and Status CCA via P1 for HPRES*.

Signal PORT1*, generated by the Device Enable Decoder U47, enables data from Information Port 1 on to the INBUS. A typical program instruction might direct the ALU (U32, U51) to test the Internal Timer signal TIMOUT* to see if a delay period has elapsed.

(f) INBUS Mask and Mask Port (INMSK) - The INBUS Mask (U35, SH 26) is a 3-to-8 line decoder. The select inputs are INST0F, INST10, and INST11 from the instruction register. The three enable inputs are hard-wired to force permanent enabling of the decoder. The eight output signals provide the inputs for the INBUS Mask Port U36. Only one output of the decoder is active low at any one time.

The INBUS Mask Port U36 is a tri-state buffer/driver that interfaces the INBUS Mask with the INBUS. The enable signal IMSK(N)* for the INBUS Mask Port is generated by the gating of INST12-13 from the instruction register.

A typical use of the INBUS Mask and Port is to select a specific bit in a register that has been enabled on the RGBUS and to test the logic state of that bit.

(g) Processor CCA Registers - These paragraphs detail the various Processor CCA registers.

(1) Accumulator 1 - Accumulator 1 (U64) is a 1x8 line latch used to store data from the OBUS to drive the RGBUS. The clocking signal TAC1*, generated by Device Load Decoder U29, stores data in the latch. Accumulator 1 is a group of D-type flip-flops that toggle on the positive transition of signal TAC1*. Hence, the Q outputs will be set to the logic states that were set up at the D inputs.

Signal FAC1*, the Accumulator 1 output control enable, is generated by the Processor CCA Register Enable Decoder U5. Accumulator 1 (U64) may be used to store data to be manipulated by the ALU. A typical instruction might direct the ALU (U32, U51) to add the contents of a device, which has been enabled onto the INBUS, to Accumulator 1 and to store the results in Accumulator 1.

(2) Data RAMs and RAM Address Register - The Data RAMS (U38 and U39, SH 28) are 256 x 8 RAMs used to store user data and as temporary storage registers. The data input/output signal lines are bi-directional lines which interface the data RAMs (U38, U39) with the RGBUS. The direction of the data is controlled by the Output Enable Signal (OUTENB*) derived from gating the Control Group 7 output signal, ENARAM, and the Register Enable Decoder output signal FRAM* at U10.

When OUTENB* is 0, data stored in the data RAM is output onto the RGBUS. When OUTENB* is 1, data on the RGBUS is available for input and storage in the data RAMs. Data will be stored only when OUTENB* equals 1 and WRTRAM* equals 0. The signal WRTRAM* (Write Control) is derived from gating the Device Load Decoder U29 output signal TRAM* with DIKFIX at U48-8 (SH 29). Signals DEMAND* and DISDEM, gated at U67 (SH 30), produce DIKFIX.

Input addressing control for the data RAMs is received from the RAM Address Register U57, U58. The RAM Address Register can be cleared, loaded, incremented, and decremented as follows:

(a) Clearing of the address register occurs automatically on power-up or when the operator presses the ALARM/CLEAR switch.

(b) Loading an address is accomplished by the Device Load Decoder U29 output signal TMAR*. The data loaded is the data present on the OBUS at the time the TMAR* signal is active low. This allows the Processor CCA to control the next address if the next address must be other than an incremented or decremented value, and to randomly access all data RAM locations.

(c) Incrementing the RAM Address Register U57, U58 is accomplished in two (2) ways. The signal INCRAM* is derived through gating at U48. One input is the Control Group 1 (U46) output signal IMAR*. The second input is derived from gating at U67 and allows automatic incrementing to occur during data transfer from the user system. The second term is the DEMAND* signal received via P2-18 from the Interface CCA and gated with the DISDEM output signal from Control Group 7 Decoder U28. Signal DEMAND* will cause an increment on its positive going edge if the DISDEM signal is low.

(d) Decrementing the RAM Address Register is accomplished by the Control Group 1 Decoder U46 output signal DMAR*.

(3) Working Registers - The sixteen working registers U42 and U43 (SH 27) in the Processor CCA are used for temporary storage of data while the program routines are being executed. The register configuration, 16 x 8, is addressed by the Instruction Register U17 (SH 24). Input data for the registers is received from the OBUS.

Output from the working registers U42 and U43 is provided as input to the Working Register Latch U61 for output onto the RGBUS. Data present at the latch input is stored on the positive going edge of clock phase signal C0*.

Stored data is enabled onto the RGBUS by the signal ENR(N)*, which is derived by gating the INST00 and INST0E signals at U13 (SH 29). Data on the RGBUS is available for processing by the ALU (U32, U51) and the resultant output of the ALU can be stored in the 16 x 8 working register at the same address as the original processed data. In this manner a "Read Register/Modify Information/Write Register" type operation can be executed by the Processor CCA.

(4) Data Out Register - The Data Out Register U54 (SH 25) is a group of D-type flip-flops which receive data from the ALU/instruction multiplexers U16 and U33. The data is transferred to the OUTBUS when the OBUSLD* signal is received. The low active OBUSLD* signal is generated by the gating of Phase 2 Clock (C2) and INST00 at U13 (SH 29). The Data Out Register is loaded for every ALU-type instruction. Data is transferred at the positive going edge of the OBUSLD* signal.

This register is used by the Processor CCA for outputting processed data to the rest of the printer system via connector P2 and the OUTBS(N) signal lines. An example is the transmission of hammer driver data to the Hammer Driver CCA to signify which hammers are to be activated.

(h) RGBUS Mask and Mask Port - The RGBUS Mask Port U62 (SH 27) is a 3-to-8 line decoder. The select inputs are INST0A, INST0B, INST0C from the Instruction Register. Three enable inputs are hard-wired to force permanent enabling of the decoder. The eight output signals provide the inputs for the RGBUS Mask Port U63. Only one output of the decoder is active low at any one time.

The RGBUS Mask Port U63 is a tri-state buffer/driver that interfaces the RGBUS mask with the RGBUS. The enable signal RMSK(N)* for the RGBUS Mask Port is generated by the gating of INST0D with ENR(N) which is INST00 and INST0E gated at U13.

A typical use of the RGBUS mask and port is to select a specific bit in a register that has been enabled on the INBUS and to test the logic state of that bit.

(i) Sentinel Monitor - The Sentinel Monitor RAM U59 (SH 28) is a 256 x 1 bit RAM used in conjunction with the data RAMs to define which locations contain legal, printable characters. The address inputs to the Sentinel Monitor are the same as those for the data RAMs. The single data bit out of the Sentinel Monitor, SENOUT, is sent to the Condition Monitor U49 (SH 29).

The Sentinel Monitor write control pulse (WRSENT*) is generated by gating signal IMAR* (U48) (SH 30) with the WSENT* signal of Control Group 1 Decoder U46. The data input signal to the Sentinel Monitor is the Control Group 7 Decoder U28 output signal SENTIN*.

Data is inverted through the Sentinel Monitor, and, as such, a high on the data-in is seen as a no-sentinel present when the SENOUT signal is monitored. **Note that the Sentinel Monitor is used only on the Processor CCA with the part number 257315-001.**

(j) Interval Timer - The Interval Timer (U45, U25, U26) (SH 25) is used for delay functions to permit high speed processing to overlap slower functions. U45, a dual cascaded binary counter, is used to generate a 55.5 microsecond clock for clocking U25, U26. U45 is clocked by the Processor CCA 868 Clock when the U25, U26 output signal TIMOUT* is inactive high. An active low TIMOUT* will inhibit the 868 Clock disabling the 55.5 microsecond clock to U25, U26, and will return U45 to its beginning count state.

U25 and U26 are cascaded 4-bit binary pre-loadable counters. These counters are loaded with data on the OBUS when the Device Load Decoder U29 output signal TIME* is active low. When U25 and U26 are loaded, the TIMEOUT* signal will go inactive high, enabling the 868 Clock to generate the 55.5 microsecond clock. As a result, U25 and U26 will be decremented once every 55.5 microseconds until a terminal count of zero is reached. The output signal TIMEOUT* is provided as an input to Information Port 1 (U37, SH 26).

(k) Band Time Out Counter (SH 30) - The function of the band time out counter U8 (SH 30) is to asynchronously disable the band drive system if no user data is received before the terminal count is reached. The clock input signal to U8 is INDEX, the inverted form of INDEX* from the Timing and Status CCA. The clear input signal to U8 is BTCLR, the inverted form of the BTCLR* signal from Control Group 1 Decoder U46.

As long as user data is received before the terminal count is reached, the Processor CCA will execute the BTCLR instruction once for each line printed, and the band system will continue to run. When the terminal count is reached, the output signal from U8 is gated at U6 with the ENBNDR signal from Control Group 7 Decoder U29. This disables signal ENBNDR*, which is transmitted to the Timing and Status CCA via connector P2-6. This condition, in turn, shuts off the band drive motor.

Receiving legal printable data will cause the Processor CCA to execute the BTCLR instruction and restart the band drive motor. When the band drive motor has reached its normal speed and the band has been identified, print can occur.

The period of time the band will run before time-out is selectable by switch S1 on the Processor CCA. One switch must be on at all times or the band will not turn, the status display will show 40, and the ALARM/CLEAR indicator will be lit. If any two switches are both on, the band will not time out. See **table 2-33** for available time intervals.

TABLE 2-33. SWITCH CONFIGURATION FOR BAND TIME OUT

Configuration	Processor CCA Switch					Band Time Out	
	S1-1	S2-2	S3-3	S1-4	S1-5	B300* 184.0 IPS	B600* 106.7 IPS
8 COUNT	ON	OFF	OFF	OFF	OFF	2.0 SEC.	1.8 SEC.
16 COUNT	OFF	ON	OFF	OFF	OFF	4.1 SEC.	3.5 SEC.
32 COUNT	OFF	OFF	ON	OFF	OFF	8.1 SEC.	7.0 SEC.
64 COUNT	OFF	OFF	OFF	ON	OFF	16.3 SEC.	14.0 SEC.
128 COUNT	OFF	OFF	OFF	OFF	ON	32.6 SEC.	28.1 SEC.

*Time out varies for 300 LPM 165.5 IPS and for 600 LPM 126.6 IPS.

(I) System Clocks - An 18.432 MHz oscillator V6 (SH 29) is the base for generation of the various clock signals required for correct system operation. Clocks provided include:

- 3-phase instruction cycle (C0, C1, C2)
- Interval time base clock (868CLK)
- Timing and Status CCA band speed control (434CLK)

Each clock is described in the following paragraphs.

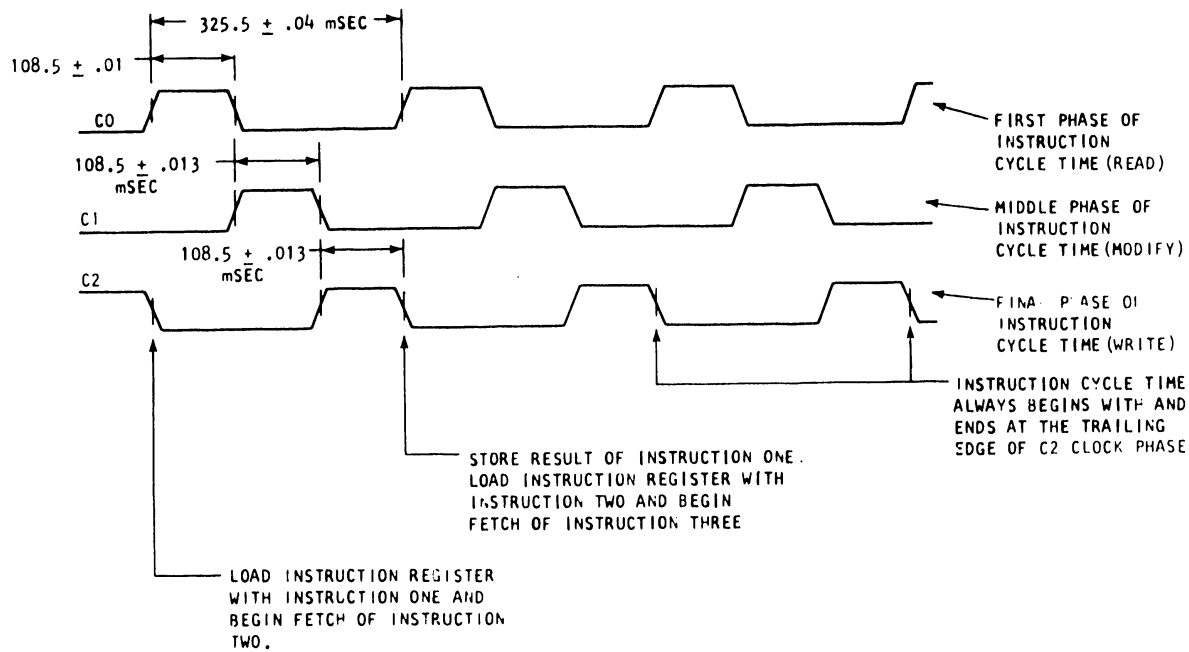
Oscillator Y1 outputs via U31 to one half of dual 4-bit binary counter U11, as its clock input. The output of gate U6 provides the clock input signal to the second half of dual 4-bit binary counter U11.

The part of U11, whose input clock is gated at U6, is used as a divider that divides the frequency of Y1 in half. The output of this half of U11, a 108.5 nanosecond clock, is used as an input to clock the three-phase generator U14. The outputs of U14 are the three clock phases C0, C1, and C2, which are necessary for correct Processor CCA instruction execution.

The three phases are gated and enabled to cause the various decoders to be active at the correct time during the total 325.5 nanosecond instruction execute cycle. The outputs of U14 feed the appropriate next input to cause the phase generator U14 to cycle through its phases like a shift register. Gating on the inputs is such as to cause the generator to be self-initializing upon printer system power-up.

All clock phases will be in their correct states in a maximum of 325.5 nanoseconds after the +5 volt DC supply has reached its nominal operating value. **Figure 2-39** is a timing diagram of the three-phase clock system.

The second half of the dual 4-bit binary counter U11 is used for generation of both the 434CLK and 868CLK signals. The counter is used to divide both by eight and sixteen for generation of these two clock signals. The 434CLK, as noted above, is used by the Timing and Status CCA for character band speed control. The 868 Clock provides the base clock frequency for the interval timers U45, U25, and U26 (SH 25).



NOTE: ONLY THE POSITIVE TIMING IS ILLUSTRATED HERE, ALTHOUGH THE PRINTER USES BOTH POSITIVE SIGNALS AND THEIR COMPLEMENTS.

Figure 2-39. Instruction Cycle Timing

b. 24-Bit Processor CCA (1000 LPM Printers)

The 24-bit Processor CCA is designed to accept up to twelve (12) program PROMs. Normally, six (6) PROMs are installed in locations MEM1 through MEM6 (SH A24 and SH A25) on the circuit card. The other six (6) locations, MEM7 to MEM12, are reserved for possible program expansion to 4K (4096x24) instructions.

The PROMs store the printer system program. The program is not volatile when the printer is powered down and can be changed only by replacing the PROMs. **Table 6-49** in **section VI** of volume II provides a list of the PROMs currently available for the 24-bit Processor CCA.

The PROMs function in groups of six (6). MEM1 through MEM6 are enabled by the LOMEM* (Low Memory) signal, while HIMEM* (High Memory) enables MEM7 through MEM12. Since LOMEM* is the inverted form of HIMEM*, only one (1) group of PROMs can be active at a time. Each PROM in the group generates four (4) instruction bits that together make up the 24-bit instruction word.

The Processor CCA executes five (5) types of instructions. The format of each instruction word defines which one (1) of the five (5) types is to be performed. **Figure 2-40** diagrams the format for each of the following instruction types:

- ALU Functions
- ALU Function/Immediate Address
- Non-ALU Function/Conditional Address
- Non-ALU Function/Conditional Load Sequencer
- Non-ALU Function/Conditional Control Enable

The discussion in the following paragraphs describes each of the micro-instruction types in terms of the devices and networks used for execution. **Figure 2-41** provides a block diagram of the major Processor CCA devices.

1. ALU Function Instructions - As shown in **figure 2-40**, the three (3) most significant bits of the micro-instruction word define ALU function operations. Bit 17 is always logic 1 for ALU functions. Bit 16 is logic 1 for ALU operations using immediate data constants, and logic 0 for other ALU functions. Bit 15 is the stack register write control. Logic 1 causes a "Write OBUS to Register" operation, and logic 0 means "No Write."

The ALU consists of U14-U15 (**SH A27**) and is capable of performing thirty-two different operations, sixteen logical and sixteen arithmetic. Select signals INST01-04 specify which of these operations will be performed. INST00 is the mode control, defining logic functions when high and arithmetic when low. **Table 2-34** lists the ALU functions and control codes.

Each micro-instruction specifying an ALU function also must control the ALU data input and output lines. Operands input to the ALU are controlled by the RGBUS Enable (INST10-14) and INBUS Enable (INST0B-0F) segments of the instruction word (refer to **figure 2-40**). Output data from ALU operations can be directed to any device specified by the Device Load portions (INST05-07) or to one (1) of sixteen (16) working registers at U16-A/U17-A (**SH A29**) as specified by the register control bit, INST15.

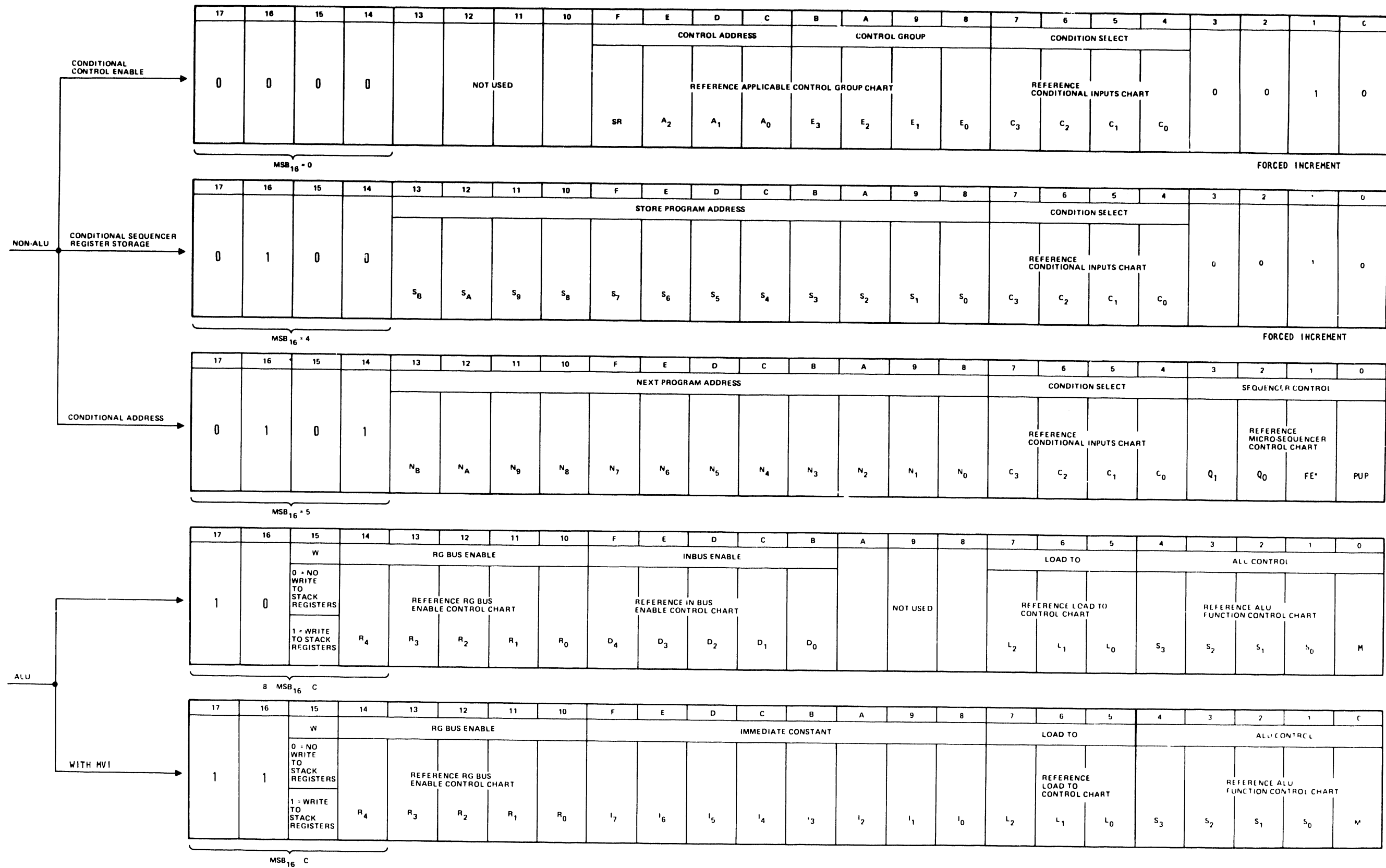


Figure 2-40. 24-Bit Processor CCA Micro-Instruction Types [1000 LPM Printers]

Figure 2-41. 24-Bit Processor CCA Block Diagram

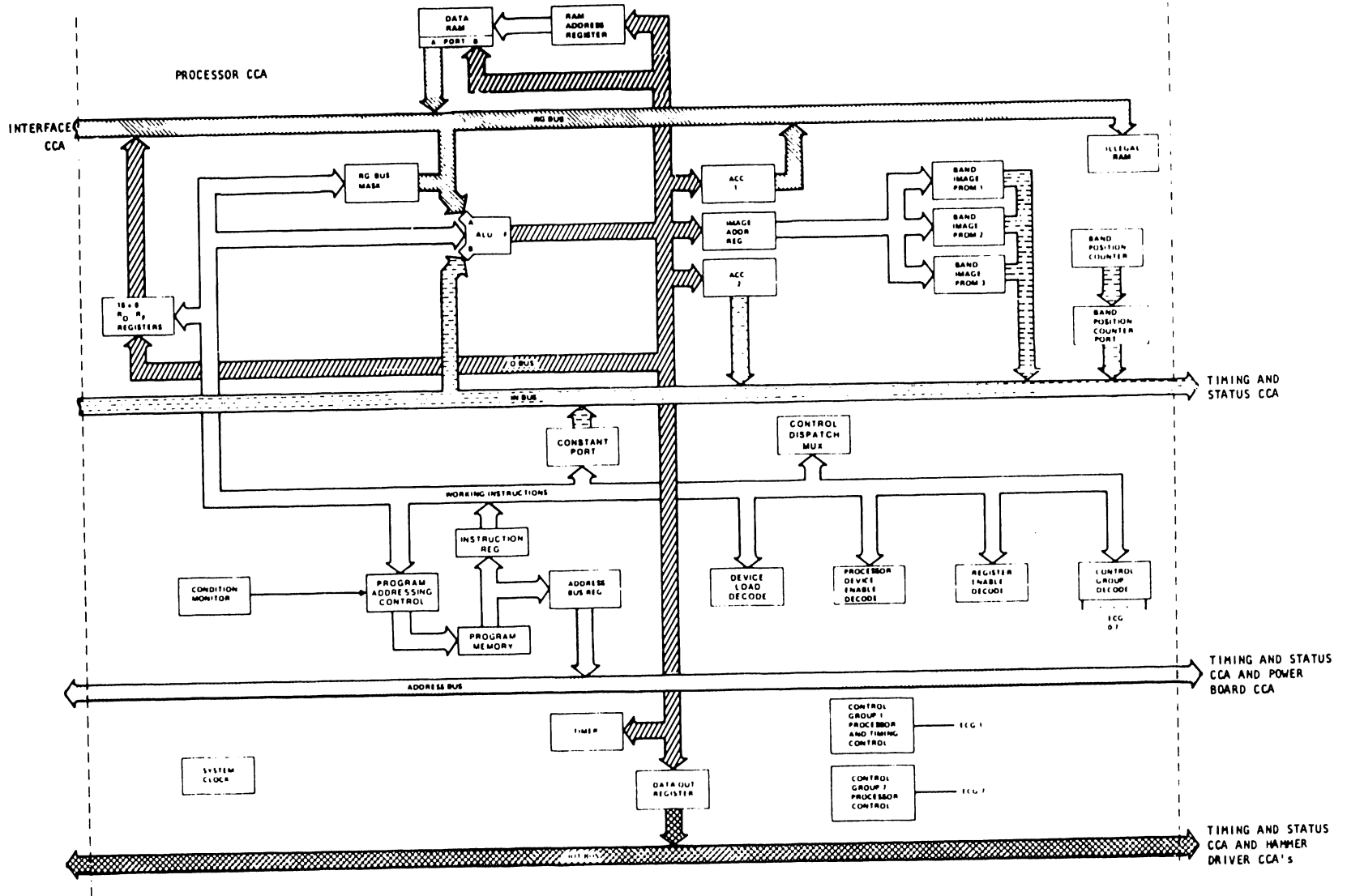


TABLE 2-34. ALU FUNCTION CONTROL
(24-BIT PROCESSOR)

Instruction Bits					Function	Description
04	03	02	01	00		
0	0	0	0	0	A Plus 1	Increment A
0	0	0	1	0	(A + B) Plus 1	
0	0	1	0	0	(A + B*) Plus 1	
0	0	1	1	0	Zero	Clear
0	1	0	0	0	A Plus (A & B*) Plus 1	
0	1	0	1	0	(A + B) Plus (A & B*) Plus 1	Subtract
0	1	1	0	0	A Minus B	
0	1	1	1	0	A & B*	
1	0	0	0	0	A Plus (A & B)	Add
1	0	0	1	0	A Plus B	
1	0	1	0	0	(A + B*) Plus (A & B)	
1	0	1	1	0	(A + B) Minus 1	Decrement B
1	1	0	0	0	A Plus A	Shift Left
1	1	0	1	0	(A + B) Plus A	
1	1	1	0	0	(A + B*) Plus A	Decrement Complement A
1	1	1	1	0	A Minus 1	
0	0	0	0	1	A*	
0	0	0	1	1	(A + B)*	Nor
0	0	1	0	1	A* & B	
0	0	1	1	1	0	Nand Complement B
0	1	0	0	1	(A & B)*	
0	1	0	1	1	B*	
0	1	1	0	1	A + B	Exclusive OR
0	1	1	1	1	A & B*	
1	0	0	0	1	A* + B	Exclusive NOR
1	0	0	1	1	(A + B)*	
1	0	1	0	1	B	
1	0	1	1	1	A & B	B Out
1	1	0	0	1	1	And
1	1	0	1	1	A + B*	Preset
1	1	1	0	1	A + B	
1	1	1	1	1	A	OR A Out

NOTES: & = Logical AND Function
+ = Logical OR Function
* = Logical NOT Function
+ = Logical Exclusive OR Function

(a) Register Enable Network - The Register Enable Network (SH A32) selects which registers will output data into the RGBUS for processing by the ALU. Register Enable Decoder U34 (SH A32) is a 3-line-to-8-line demultiplexer that decodes three (3) select inputs (INST10, INST11, INST12) and three (3) enable inputs (INST13, INST14, INST17) to generate one active-low output signal. This active output line (all other outputs are inactive) enables one register to output its data. Table 2-35 lists the Register Enable control functions and signals.

TABLE 2-35. RGBUS ENABLE CONTROL

Instruction Word Bits					Register Enabled
14	13	12	11	10	
0	0	0	0	0	No Operation
0	0	0	0	1	Accumulator One
0	0	0	1	0	Data Buffer
0	0	0	1	1	User Data Latch
0	0	1	0	0	Not Used
0	0	1	0	1	Not Used
0	0	1	1	0	Not Used
0	0	1	1	1	Not Used
0	1	0	0	0	RGBUS Mask 0
0	1	0	0	1	RGBUS Mask 1
0	1	0	1	0	RGBUS Mask 2
0	1	0	1	1	RGBUS Mask 3
0	1	1	0	0	RGBUS Mask 4
0	1	1	0	1	RGBUS Mask 5
0	1	1	1	0	RGBUS Mask 6
0	1	1	1	1	RGBUS Mask 7
1	0	0	0	0	GP Register 0
1	0	0	0	1	GP Register 1
1	0	0	1	0	GP Register 2
1	0	0	1	1	GP Register 3
1	0	1	0	0	GP Register 4
1	0	1	0	1	GP Register 5
1	0	1	1	0	GP Register 6
1	0	1	1	1	GP Register 7
1	1	0	0	0	GP Register 8
1	1	0	0	1	GP Register 9
1	1	0	1	0	GP Register A
1	1	0	1	1	GP Register B
1	1	1	0	0	GP Register C
1	1	1	0	1	GP Register D
1	1	1	1	0	Flag Register
1	1	1	1	1	Flag Register

*RMSK(N) is the low-active output of a 3-line-to-8-line decoder. Bit masking must compensate for this low-active signal.

(b) INBUS Enable Network - The INBUS Enable Network (SH A32) allows data to be placed on the INBUS for processing by the ALU. Device Enable Decoder U32 (SH A32) is a 3-line-to-8-line demultiplexer with select inputs INST0B, INST0C, and INST0D, and enable inputs INST0E, INST0F, and INST17 (transmitted via U50-4). Only one (1) output is active low at a time.

Signals from U32 control the outputs of the band image PROMs (MEM13-MEM15), Accumulator 2 at U1 (SH A29), Timing and Status CCA Ports 0 and 1, and the Band Position Counter Buffer U8 (SH A30). Table 2-36 lists the Enable Control signals for these and other affected devices.

TABLE 2-36. INBUS ENABLE CONTROL

Instruction Word Bits					Device Enabled	Signal Output Condition
0F	0E	0D	0C	0B		
0	0	0	0	0	No Operation	
0	0	0	0	1	Band Image PROM	BIP* active to MEM13-15 (SH A30)
0	0	0	1	0	Accumulator Two	FAC2* active to U1 (SH A20)
0	0	0	1	1	T & S Port 1	STP1* active to P2-9
0	0	1	0	0	N/A	
0	0	1	0	1	Band Position Counter	BPC* active to U8-1 (SH A30)
0	0	1	1	0	T & S Port 0	STP0* active to P1-55
0	0	1	1	1		
0	1	0	0	0		
0	1	0	0	1		
0	1	0	1	0		
0	1	0	1	1		
0	1	1	0	0		
0	1	1	0	1		
0	1	1	1	0		
0	1	1	1	1		
1	0	0	0	0	Form Length PROM	FLSS* active from U29-15 (SH 7)
1	0	0	0	1	Configuration Group 4	CG4* active from U29-14
1	0	0	1	0	Configuration Group 3	CG3* active from U29-13
1	0	0	1	1	Control Panel Switches	CPS* active from U29-12
1	0	1	0	0	Interlock Switches	INSW* active from U29-11
1	0	1	0	1	N/A	
1	0	1	1	0	Configuration Group 2	CG2* active from U29-9
1	0	1	1	1	User Control Data	UCL* active from U29-7
1	1	0	0	0		
1	1	0	0	1		
1	1	0	1	0		
1	1	0	1	1		
1	1	1	0	0		
1	1	1	0	1		
1	1	1	1	0		
1	1	1	1	1		

(c) Device Load Network - The Device Load Network (SH A32) specifies the device in which data from an ALU operation should be stored. Table 2-37 lists the devices. Demultiplexer U35 decodes select inputs INST05, INST06, and INST07, and is enabled by INST17 and C0, to generate one active-low output.

TABLE 2-37. LOAD TO CONTROL

Instruction Word Bits			Device Loaded	Device Number	Active Signal
07	06	05			
0	0	0	No Operation	N/A	-
0	0	1	Accumulator One	U2	TAC1*
0	1	0	Accumulator Two	U1	TAC2*
0	1	1	Buffer Address Reg.	U40	TMAR*
1	0	0	Band Image Address Reg.	U4	TIAR*
1	0	1	Illegal Code Memory	U37	TILL*
1	1	0	Data Buffer Write	U57,U58	TRAM*
1	1	1	Interval Timer	U19,U18	TIME*

(d) Working Register Write - The sixteen working registers, U16A/U17A (SH A29) are controlled by the register enable segment of the micro-instruction word and by signal ENWRT*. These read/write RAMs provide scratch-pad memory for controlling and moving data to and from the ALU. Instructions INST10-13 address one (1) of the registers. Enable signal ENWRT* is the gated result of INST14 (always "1" for register read/write), INST15 (Mode Control), INST17 (ALU Function), and clock pulse C2CLK. INST15, when logic "1," specifies "Write OBUS" to the addressed register, and, when logic "0," indicates "No Write."

2. ALU Function/Immediate Data Instructions - For ALU operations using immediate data constants, bit 16 of the micro-instruction word is logic "1." This kind of instruction allows the processor access to programmed constants stored in the program PROMs; the operand normally input to the ALU from an INBUS device is instead contained in the micro-instruction word itself in bits 09 through 0F (see micro-instruction format **figure 2-40**). This type of instruction is used, for example, to load a data value into the system Interval Timer for counting down a delay subroutine, or into the STATUS indicator for display.

Immediate data instructions specify RGBUS input and device-load output in the same way as do ALU function instructions without immediate constants. Refer to **tables 2-35 and 2-37** for instruction bit assignment and decoding.

3. Non-ALU Function/Conditional Address Instructions - As shown in **figure 2-40**, the four most significant bits of the micro-instruction word define non-ALU function instructions. Bit 17 is always logic 0 for non-ALU operations. Conditional address functions are indicated when bits 16 and 14 are logical 1.

The conditional address function allows the program to branch to some address other than the next address in program sequence. The processor samples one of sixteen possible system conditions specified by the instruction to determine whether the program should branch to a subroutine address or continue with the next incremented address. **Table 2-38** lists these sixteen (16) conditions.

TABLE 2-38. CONDITIONAL INPUT INSTRUCTIONS

Instruction Word Bits				Conditional Operations
07 C3	06 C2	05 C1	04 C0	
0	0	0	0	Unconditional
0	0	0	1	ALU: (A=B) Output = 1
0	0	1	0	ALU: (A=B) Output = 0
0	0	1	1	No ALU Carry Out
0	1	0	0	ALU Carry Out
0	1	0	1	Parity Error
0	1	1	0	Stop I/O Transfer

TABLE 2-38. CONDITIONAL INPUT INSTRUCTIONS (Cont'd)

Instruction Word Bits				Conditional Operations
07	06	05	04	
C3	C2	C1	C0	
0	1	1	1	User Respond
1	0	0	0	No Timeout
1	0	0	1	System Status Change
1	0	1	0	Undefined External Input
1	0	1	1	"HPRES" Not Present
1	1	0	0	"INDEX" Present
1	1	0	1	Band On Interval Timeout
1	1	1	0	Enable Band Drive Off
1	1	1	1	Not Used

(a) Condition Monitor - The Condition Monitor (SH A31) consists of data latches U21 and U23 and data multiplexer U22. Latches U21 - U23 temporarily store ALU output signals and status signals from the illegal code memory U37 (SH A28), Control Group 7 Decoder U33 (SH A28), Band Time-Out Counter U42 (SH A30), and the Timing and Status and Interface CCAs. Condition Monitor Multiplexer U22 samples one (1) of these inputs according to its decoding of select lines INST04-07. If the sampled signal is active (the specified condition is met), U22 generates Condition Met (CONMET*). CONMET* is gated at U51 with the product of INST14 and INST16 -- the instruction bits that define a conditional address function -- to produce the select input to the Microsequencer Function Selector U46 (SH A26).

(b) Microsequencer Function Selector - The Microsequencer Function Selector, U46 (SH A26), is a 2-to-1-line data multiplexer whose outputs control the Microsequencer Address Register, U45/U44, U43 (SH A27). Table 2-39 gives the function table for these control signals, Push/Pop (PUP), File Enable (FE*), S0, and S1. The "A" inputs to the function selector are hard-wired to produce, when selected, the control code (001X) that increments the program counter -- that is, moves the program to the next address in normal sequence.

The "B" inputs are micro-instruction bits INST00-03. When the condition monitor output CONMET* is active low, the "B" inputs are selected, forcing a conditional address and incrementing or decrementing the internal stack pointer according to the control logic detailed in table 2-39.

(c) Microsequencer Address Register - The microsequencer U45/U44/U43 (SH A27) generates each micro-instruction address. It selects, as the source of the next address, either the program counter register (for an incremental step), the direct address contained in bits 08 to 13 of the conditional address micro-instruction (for a program branch), or the internal stack register (for a jump or return). As detailed in table 2-39, inputs S0 and S1 select the microsequencer function, and FE* and PUP control the internal stack register.

The Stack Register stores addresses to which the program can jump to begin a subroutine or to which it can return upon completion of a subroutine. Up to four micro-instruction addresses can be nested on a "First-in, Last-out" basis. An internal stack pointer always points to the last word written in the register.

Conditional address instructions thus may move the program to a branch address specified by the instruction itself (if the condition is met), to the next address in normal sequence (if the condition is not met), or to a jump or return address stored in the stack register (an unconditional branch).

TABLE 2-39. MICROSEQUENCER CONTROL

Instruction Word Bit				Function
03	02	01	00	
S1 (Q1)	S0 (Q0)	FE	PUP	
0	0	0	0	Increment Program Counter Register, Pop Stack
0	0	0	1	Increment Program Counter Register, Push Stack
0	0	1	X	Increment Program Counter Register
0	1	0	0	Jump to Address Register, Pop Stack
0	1	0	1	Jump to Address Register, Push Stack
0	1	1	X	Jump to Address Register
1	0	0	0	Return, Pop Stack
1	0	0	1	Return, Push Stack
1	0	1	X	Return
1	1	0	0	Jump to Direct Data Input, Pop Stack
1	1	0	1	Jump to Direct Data Input, Push Stack
1	1	1	X	Jump to Direct Data Input

Note: Push and Pop Stack commands are disabled when the "FE" signal is at logic "1." When "FE" is at logic "0," it enables the "PUP" signal to increment or decrement the internal stack pointer within the microsequencer.

4. Non-ALU Function/Conditional Load-Sequencer Instructions - Conditional load-sequencer instructions are specified when micro-word bit 16 is logic "1" and bit 14 is logic "0." This instruction loads the internal Stack Register with a subroutine address to which the program later can move on the "JUMP" command. As with the conditional address instruction, the branch address is specified in instruction bits 08 through 13. As used in this program, however, the load-sequencer instruction is unconditional; it is used only to store the branch address for a call at some later point in the program.

5. Non-ALU Function/Conditional Control-Enable Instructions - The control-enable decoding function allows the Processor CCA to generate various control signals needed for correct system operation. When control-enable instructions are executed, the CONMET* input to the Microsequencer Function Selector is inactive (high), forcing the microsequencer to output an incremented next address. The selected control function is performed according to program definition, and the program continues in its normal sequence.

(a) Control Enable Decoder - Control Enable Decoder U53 (SH A32) is a 3-to-8-line demultiplexer whose outputs select and enable eight (8) control-group devices located on the printer CCAs. Select inputs are INST08, INST09, and INST0A. Enable signals are INST0B, Clock Pulse C2*, and CONMET (the inverted form of condition monitor output CONMET*) via U50, pin 9. One output is active low and one control group enabled at a time.

(b) Function Control Groups - Each output signal from Control Enable Decoder U53 (SH A32) enables one of the eight (8) control group decoders (numbered 0 to 7). These devices generate two kinds of outputs: set/reset flip-flop signals, and control for timing pulses. Their circuit card locations and functions are shown in table 2-40.

TABLE 2-40. FUNCTION CONTROL GROUPS

Control Group	Location	Circuit Reference	Control
0	Interface CCA	U47, SH 7	Set/Reset Flip-Flop
0	Centronics-Compatible Interface CCA	U27, SH B7	Set/Reset Flip-Flop
1	Processor CA	U54, SH A30	Timing Pulse Generation
2	Centronics-Compatible Interface CCA	U26, SH B6	Timing Pulse Generation
3	Interface CCA	U28, SH 7	Timing Pulse Generation
3	Timing and Status CCA	U48, SH 36	Timing Pulse Generation
3	Centronics-Compatible Interface CCA	U43, SH B7	Timing Pulse Generation
4	Power Board CCA	U5, SH 39	Set/Reset Flip-Flop
5	Interface CCA	U14, SH 7	Set/Reset Flip-Flop
5	Centronics-Compatible Interface CCA	U25, SH B7	Set/Reset Flip-Flop

TABLE 2-40. FUNCTION CONTROL GROUPS (Cont'd)

Control Group	Location	Circuit Reference	Control
6	Interface CCA	U13, SH 6	Set/Reset Flip-Flop
6	Centronics-Compatible Interface CCA	U14, SH B6	Set/Reset Flip-Flop
7	Processor CCA	U33, SH A32	Set/Reset Flip-Flop

Tables 2-41 and 2-42 give the decoding for Control Group Decoders 1 and 7 located on the Processor CCA. For information on the other decoders, see the description of their respective CCAs elsewhere in this section.

(1) Control Group 1 Decoder - Control Group 1 Decoder U54 (SH A30) is a 3-to-8-line demultiplexer enabled by signal ECG1* (Enable Control Group 1) and INST0F. U54 decodes INST0C, INST0D, and INST0E to generate one of the output signals shown in table 2-41.

TABLE 2-41. CONTROL GROUP 1 DECODE AND FUNCTIONS

Instruction Word Bits				Function	Signal Condition
0F	0E	0D	0C		
0	0	0	0	N/A	
0	0	0	1	N/A	
0	0	1	0	N/A	
0	0	1	1	Clear Band Timeout Counter	U54-12 low; BTCLR active
0	1	0	0	Load Even "S" Register	EVSREG* active to P1-24
0	1	0	1	Load Even Hammer Dat	EVHAMR* active to P1-36
0	1	1	0	Load Odd "S" Register	ODSREG* active to P1-23
0	1	1	1	Load Odd Hammer Data	ODHAMR* active to P1-35
1	0	0	0	N/A	
1	0	0	1	N/A	
1	0	1	0	N/A	
1	0	1	1	N/A	
1	1	0	0	N/A	
1	1	0	1	N/A	
1	1	1	0	N/A	
1	1	1	1	N/A	

(2) Control Group 7 Decoder - Control Group 7 Decoder U33 (**SH A32**) is an 8-bit addressable latch enabled by the Control Enable Decoder (U53) output at pin 7. Micro-instruction bits INST0C, INST0D, and INST0E are the address select inputs. INST0F (pin 13) is the data-in bit that provides set/reset flip-flop control. **Table 2-42** lists the control functions for Control Group 7.

TABLE 2-42. CONTROL GROUP 7 DECODE AND FUNCTIONS

Instruction Word Bits				Function	Output Signal Condition
0F	0E	0D	0C		
0	0	0	0	Disable Band Drive	ENBNDR* high inactive
0	0	0	1	Reset RAM Address Bit 8	RAMAD8 low
0	0	1	0	Reset RAM Address Bit 9	RAMAD9 low
0	0	1	1	Reset Legal Data Bit	LEGAL low inactive
0	1	0	0	Enable Band Image PROM #1	ENBIP1* low active
0	1	0	1	Enable Band Image PROM #2	ENBIP2* low active
0	1	1	0	Enable Band Image PROM #3	ENBIP3* low active
0	1	1	1	Reset Inhibit Master Clear	INHMC low inactive
1	0	0	0	Enable Band Drive	ENBNDR* low active
1	0	0	1	Set RAM Address Bit 8	RAMAD8 high
1	0	1	0	Set RAM Address Bit 9	RAMAD9 high
1	0	1	1	Set Legal Data Bit	LEGAL high active
1	1	0	0	Disable Band Image PROM #1	ENBIP1* high inactive
1	1	0	1	Disable Band Image PROM #2	ENBIP2* high inactive
1	1	1	0	Disable Band Image PROM #3	ENBIP3* high inactive
1	1	1	1	Set Inhibit Master Clear	INHMC high active

(c) Control Dispatch Multiplexer - The Control Dispatch Multiplexer U50 (**SH A32**), is a 2-to-1-line device that directs control signals for ALU Function/Immediate Data Constant instructions and Non-ALU Function/Conditional Control Enable Instructions.

Micro-instruction bits INST17 and INST16 control the dispatch multiplexer. INST17 provides the four (4) variable inputs, direct at pins 2 and 13, inverted at pin 6, and via signal CONMET at pin 11 (CONMET is the inverted form of CONMET* from Condition Monitor U22, **SH A31**). All remaining inputs are hard-wired. INST16 is the select line. It transfers the "A" inputs (pins 2, 5, 11, 13) to output when it is low, the "B" inputs to output (pins 3, 6, 10, 14) when high.

For ALU Function/Immediate Data Constant instructions, INST17 and INST16 are both logic "1." The "B" inputs are selected, and output signal Enable Direct Constant (ENDRCN*) becomes active low, enabling data buffer U30 (**SH A26**) to transmit the immediate data segment of the micro-instruction word via INBUS lines 0 - 7. The remaining output signals (all low) disable the Device Enable Decoder U32 and Control Group Decoder U53 (both **SH A32**) and the Address Bus Latch Clear (ADCL*) signal.

For non-ALU Function/Conditional Control Enable instructions, INST17 and INST16 are both logic "0." The "A" inputs are selected (all are high) to disable Direct Constant Buffer U30, enable Control Group Decoder U53 and Device Enable Decoder U32, and activate signal ADCL* to update the Address Bus Latch U27 (SH A26).

6. Processor CCA Devices - This paragraph describes the major Processor CCA devices.

(a) Band Image PROMs - The Band Image PROMs (SH A30) MEM13-MEM15 store a digital-coded representation of the characters on the print band. Each PROM contains the coded likeness of one complete band. Thus, up to three different bands can be used in the printer. To identify the band in use, the microprogram compares coded identification pulses read from the character band (via the transducer and Timing and Status CCA) with a code stored in a predefined location of each band image PROM. When one of the three PROMs is found to match the band in use, the appropriate PROM select signal, Enable Band Image PROM (ENBIP1*, ENBIP2*, or ENBIP3*) enables that device. Because of this, none of the bands can have the same dash number.

PROM output is transmitted to the ALU via INBUS0 - INBUS7 on receipt of signal Band Image PROM Enable (BIP*).

(b) Band Position Counter - Band Position Counter U9 (SH A30) is a dual 4-binary counter clocked by signal HPRES* from the hammer timing circuitry on the Timing and Status CCA. U9 counts each time a new character centers in front of hammer number 1, and it is cleared after each band revolution by signal INDEX*. Its output is loaded to the INBUS and used in determining a match between user output characters in the Data RAM and band characters represented in the Band Image PROMs.

(c) Accumulator 2 - Accumulator 2 (U1) (SH A29) is a 1 x 8 latch that stores data from the OBUS for transmission to the INBUS. It clocks in data when Accumulator 2 (TAC2*) is active (low) and transfers input data to output on the positive-going transition of TAC2*. The output control for Accumulator 2 is signal FAC2* (From Accumulator 2).

(d) Processor CCA Registers - This section describes the various registers and related devices used by the Processor CCA.

(1) Accumulator 1 - Accumulator 1 (U2, SH A29) is a 1 x 8 latch that stores data from the OBUS for transmission to the RGBUS. U2 inputs data when signal TAC1* is active (low) and transfers input data to output on the positive-going transition of TAC1*. Signal FAC1* is the output control.

(2) Data RAMs - Data RAMs U54-U58 (SH A28) provide 1024 x 8 memory for storing user input data and for temporary storage of processor operands. The RAMs are addressed through Memory Address Register U40. Data input/output signals (pins 11 - 14) are bi-directional: inputs are written into RAM memory via data-write buffer U39, and outputs enter the RGBUS by way of Data Buffer U38. This output buffer, U38, is enabled by FRAM*, generated by

register-enable decoder U34 (SH A32). Signal TRAM*, originating at Device Load Decoder U35 (SH A32), enables the data-write buffer and also provides input control for the data RAMs themselves.

The 1024 memory locations of the data RAMs are divided into four pages of 256 locations each. Signals RAMAD8 and RAMAD9 select one page of memory for data input and output as shown in table 2-43. Only page 1 of memory is used for user data and processor storage. Pages 3 and 4 store VFU data. Page 2 is not used.

TABLE 2-43. DATA RAM PAGE SELECTION

RAMAD 9	RAMAD 8	Memory Page Selected
0	0	1
0	1	2
1	0	3
1	1	4

(3) Register Mask - The RGBUS Mask (U3) (SH A29) is used to test the logical state of printer status signals on the INBUS. U3 functions as a 3-to-8-line demultiplexer, generating one selected active-low output to the RGBUS. All other lines are inactive (high). This RGBUS data is compared (ORed) with INBUS data at the ALU to determine whether the INBUS status line corresponding to the selected RGBUS mask bit is active (low) or inactive (high). Select lines to U3 are INST10, INST11, and INST12. The enable input is signal ENRMSK* (Enable RGBUS Mask).

(4) Working Registers - The sixteen 8-bit working registers, U16-A and U17-A (SH A29) provide temporary storage for data while program routines are executed. Registers are addressed by instruction signals INST10-INST13. OBUS data present at the latch inputs are stored on the positive-going edge of clock-phase signal C0*. Data is enabled onto the RGBUS by signal ENWRT*. Information on the RGBUS is available for processing by the ALU, and the result of the ALU operation frequently is returned to the original register address. In this manner the Processor CCA executes a "Read Register/Modify Information/Write Register" operation.

(5) Data Out Register - The Data Out Register U47 (SH A27) receives information from the ALU, U14-U15, for transmission, via connector P2, from the Processor CCA to other system CCAs. Data transfers to the OUTBUS when clock signal OBUSLD* is active low. Because this signal is generated by gating of INST17 and the system clock pulse at U10-3 (SH A31), the Data Out Register is loaded for every ALU-type instruction. Information is transmitted at the positive-going edge of the signal.

(e) Internal Timer - The Internal Timer U11, U18, U19 (SH A31) provides delays to permit high-speed processing to overlap slower functions. Oscillator Y1 (10 mHz) generates the base pulses for the interval timer (and for other system clocks as well). The output of Y1, gated through U13 and divided to one-half original frequency by flip-flop U12, becomes the input to U11 at pin 1. U11, a dual cascaded binary counter, generates the clock pulse to U19-U18 every 51.2 microseconds.

Counters U19-U18 are cascaded, four-bit binary pre-loadable devices. They input a count value from the OBUS when signal TIME*, from Device Load Decoder U35 (SH A32), is active low. (The count value is the immediate constant in an ALU-Function/Immediate Data Instruction.) This pre-loaded value, a multiple of the base interval, is decremented each time U11 generates its clock pulse - that is, every 51.2 microseconds. U19-U18 continues to decrement until it reaches a count of zero. Then signal TMOUT* (U18-13) goes active low, clearing counter U11 to its beginning count state. (TMOUT* is inactive high when U19-U18 is loaded with a count value.) TMOUT* becomes one input to Condition Select Monitor U22 through D-type flip-flop U23 (pin 19).

(f) Illegal Code Memory - Illegal code RAM U37 (SH A28) tests whether user input data corresponds to printable characters on the band and in the selected band image PROM. It is a 256 x 1 device with inputs from the RGBUS and a single output, STOPI0*, to Condition Monitor U22 (SH A31) via latch U21. The data input signal, LEGAL (pin 13), originates at Control Group 7 decoder U33 (SH A32). Write-enable signal TILL* (pin 12) is generated by U35 (SH A32).

The illegal RAM is loaded each time the band motor starts and a band image PROM is selected. The code for each band character addresses the RAM, and memory locations, whose address corresponds to code for a specific character, are loaded with a "legal" bit. All other RAM locations store "0," signifying that any user-sent character whose code addresses that location is unprintable.

During the user data-load routine, each transmitted character is tested at the illegal RAM. If any character code addresses a RAM location marked "illegal," signal STOPI0* is generated to U22 (SH A31).

(g) Band Time-Out Counter The band-drive system is enabled and disabled under firmware control. The Band Time-Out Counter, U42 (SH A30), determines when the band should be stopped. The clock input signal to U42 is INDEX, the inverted form of INDEX*, received from the Timing and Status CCA via connector P2-14. The clear input signal is BTCLR, the inverted form of signal BTCLR*, generated by Control Group 1 Decoder U54 (SH A30). If, during the data load routine the band completes 16 revolutions before printable user data is received, U42 generates signal STPBND to Condition Monitor U22 (SH A31). The processor samples this condition bit when DTS* (Data Transfer Strobe) is active, and if the band has timed out (STPBND is high), the ENBND* (Enable Band Drive) signal to the Timing and Status CCA is removed, stopping the band motor. As long as user data is received before the terminal count occurs, the processor executes the BTCLR (Band Timer Clear) instruction once for each line printer, and the band continues to run.

The standard time-out interval of 16 revolutions can be changed to other values using an optional switch (S1) mounted on the Processor CCA. The standard value is the equivalent of S1-2 ON and is hard-wired. Other values are shown in **table 2-44**.

TABLE 2-44. OPTIONAL SWITCH CONFIGURATION FOR BAND TIME-OUT

Configuration	Processor CCA Switch					Band Time Out 1000 LPM - 199.8 IPS	
	S1-1	S1-2	S1-3	S1-4	S1-5	Count	Seconds
	8 COUNT	ON	OFF	OFF	OFF	OFF	8
16 COUNT	OFF	ON	OFF	OFF	OFF	16	1.87
32 COUNT	OFF	OFF	ON	OFF	OFF	32	3.75
64 COUNT	OFF	OFF	ON	ON	OFF	64	7.49
128 COUNT	OFF	OFF	OFF	OFF	ON	128	15.00

If optional switch settings are used, one switch must be ON or the band will not turn, the status indicator displays 40, and the ALARM/CLEAR indicator lights. If any two switches are set ON, the band will not time-out.

(h) System Clocks - A 10 mHz oscillator, Y1 (SH A31), generates the base pulses that are developed into system clock signals. These include:

- Two-phase or three-phase instruction cycle (C0, C1, C2*);
- Timing and Status CCA Band speed control (400 CLK);
- Interval time clock input;
- Interface Timing signals (C2CLK and C0CLK).

Clock-phase Generator U20/U10 outputs two-phase or three-phase timing signals depending on the type of instruction being executed: two-phase for non-ALU-operation instructions, three-phase for ALU-operation instructions. OSCCLK, the base pulse of oscillator Y1, is the clock input. Outputs are C0, C1, C2*, C0CLK, and C2CLK. These pulses are gated to actuate system registers and decoders at the correct time during the complete instruction cycle. With selected outputs and inputs connected in a feedback path, U10 cycles through its phases like a shift register. Gating on the inputs initializes U10 on printer-system power-up.

Clock signal C0 activates master-clear flip-flop U12 (SH A26), enables inputs to working registers U16A-U17A (SH A29), and enables working registers U16B-U17B (SH A29).

Signal C2* clocks Address Bus Latch U27 (SH A26), Instruction Registers U29, U26, and U25 (SH A26), and Sequencer Address Register U43, U44, U45 (SH A27), and enables Control Group Decoder U53 (SH A32). C2CLK, the inverted form of C2*, gates with INST14, INST15, and INST17 to produce the write enable input to working register U16A-U17A.

C0CLK is transmitted via connector P2-5 to the Interface CCA and RSPOND flip-flop U16.

The base output of Y1, OSCLK, also is gated with C0 and INST17 (via the Control Dispatch Multiplexer, U50 - pin 12) to form ADCL*, the clear signal to Address Bus Latch U27 (SH A26).

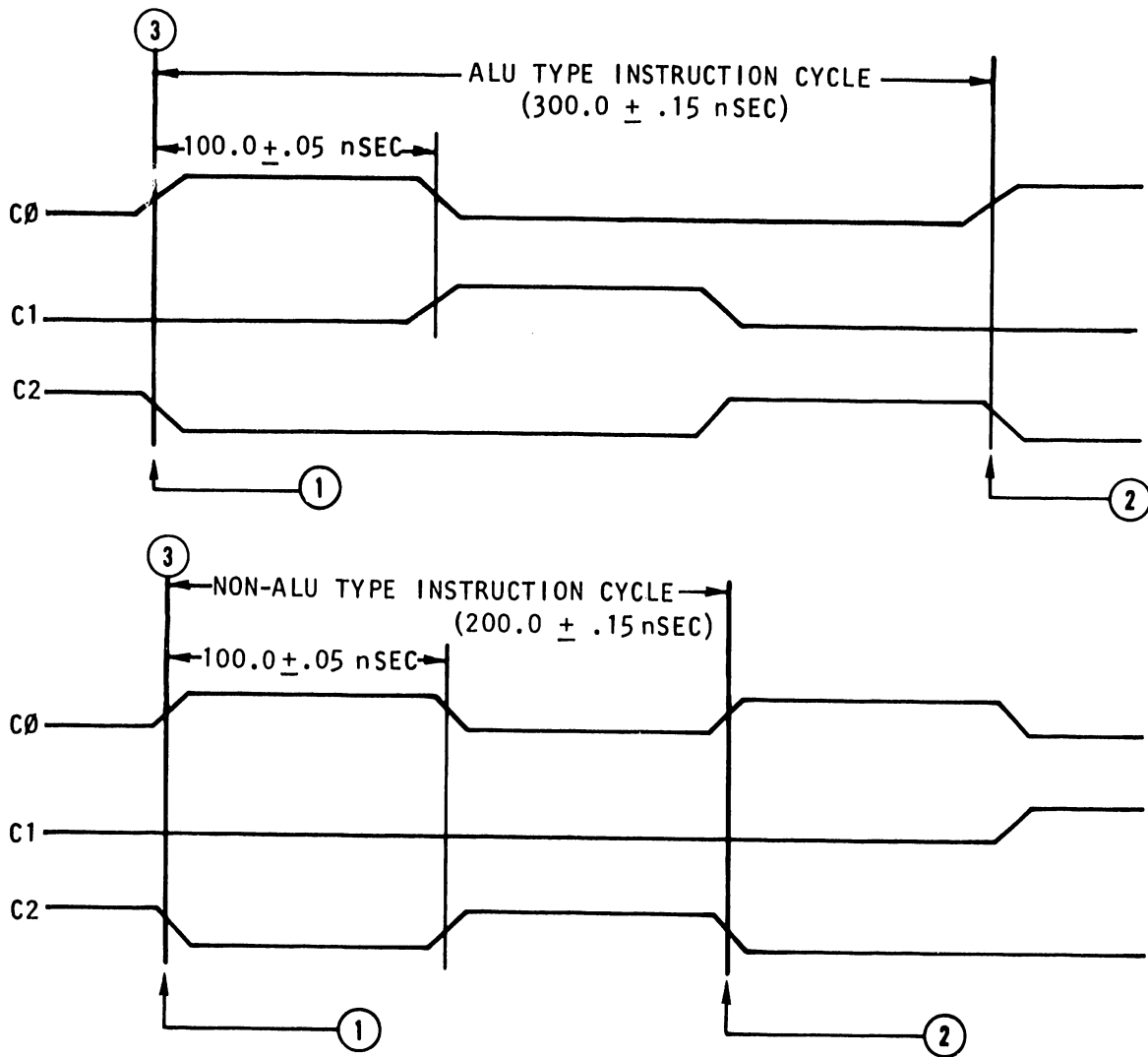
Counter U11 develops the Interval Timer Clock signal described in paragraph 1 of this section. In addition, it generates the 400 CLK pulse sent via connector P2-7 to the Timing and Status CCA for band speed control.

Figure 2-42 shows two-phase and three-phase instruction-cycle timing for the 24-bit Processor CCA.

2.3.3 Timing and Status CCA

The Timing and Status CCA enables the Processor CCA to monitor the current status of the printer. It communicates with the Processor CCA on the Address Bus (ADRBS), the INBUS, and on discrete control lines. The logical functions that are performed by the Timing and Status CCA include the following:

1. Generation of the power up and power down reset sequence.
2. Identification, amplification and digitizing of the character band timing marks to provide the time base needed to control hammer fire.
3. Synchronizing the band timing clock with the Processor CCA system clock to monitor and control band speed.
4. Providing the character phasing and copies compensation for optimum print output.
5. Defining the hammer driver waveform for the Processor CCA to determine hammer fire conditions.
6. Providing correct column spacing control for the 300 LPM model printers.
7. Monitoring all power supply voltages, the transducer, the band drive, and the paper feed drive status in order to tell the Processor CCA of a status change.



① LOAD INSTRUCTION REGISTER WITH INSTRUCTION ONE AND BEGIN FETCH OF INSTRUCTION TWO.

② STORE RESULT OF INSTRUCTION ONE. LOAD INSTRUCTION REGISTER WITH INSTRUCTION TWO AND BEGIN FETCH OF INSTRUCTION THREE.

③ INSTRUCTION CYCLE TIME ALWAYS BEGINS WITH AND ENDS AT THE TRAILING EDGE OF C2 CLOCK PHASE

NOTE: ONLY THE POSITIVE TIMING IS ILLUSTRATED HERE, ALTHOUGH THE PRINTER USES BOTH POSITIVE SIGNALS AND THEIR COMPLEMENTS.

Figure 2-42. 24-Bit Processor Instruction Cycle Timing

8. Monitoring the over-temperature, hammer fire condition signals, +5 volts, and the system clock fault conditions in order to immediately shut down the printer system when a fault occurs.
9. Providing a print inhibit switch to disable the hammer driver(s) and prevent printing of data for troubleshooting purposes.

Figure 2-43 shows, in a block diagram format, the signals and devices necessary for the Timing and Status CCA functions. The following paragraphs discuss the devices shown in the block diagram as they relate to the operation of the Timing and Status CCA.

a. Timing and Status CCA Headers

The Timing and Status CCA is programmed for different model levels of operation by the installation of a Band Speed Header (J2, SH 33) and a Programmable Header (J4, SH 37). Each printer model uses a different set of headers to accommodate various band speeds.

Table 6-52 in section VI of volume II lists the Timing and Status Header Kits currently available for the 300 LPM, 600 LPM and 1000 LPM printers. The wiring for the Band Speed and Programmable Headers is shown in Logic Diagram Sheet 4 in section V of volume II.

b. Timing Characteristics

Timing characteristics vary with the printer model. **Table 2-45** lists the timing essential for proper operation of each model.

TABLE 2-45. TIMING AND STATUS CCA TIMING CHARACTERISTICS

Function	300 LPM	600 LPM	1000 LPM
Index Period	254 mSec	185 mSec	118 mSec
Raw Clock Period	611.4 \pm 7 μ Sec	889 \pm 20 μ Sec	563 \pm 20 μ Sec
Character Period	1.22 mSec \pm 15 μ Sec	889 \pm 20 μ Sec	563 \pm 20 μ Sec
Band Speed	184 IPS	126.6 IPS	199.75 IPS
Copies Delay at 1V to 6V range	45-250 μ Sec	35-230 μ Sec	35-200 μ Sec
Phasing Delay at 0.5V -8.5V range	21-390 μ Sec	30-410 μ Sec	30-180 μ Sec

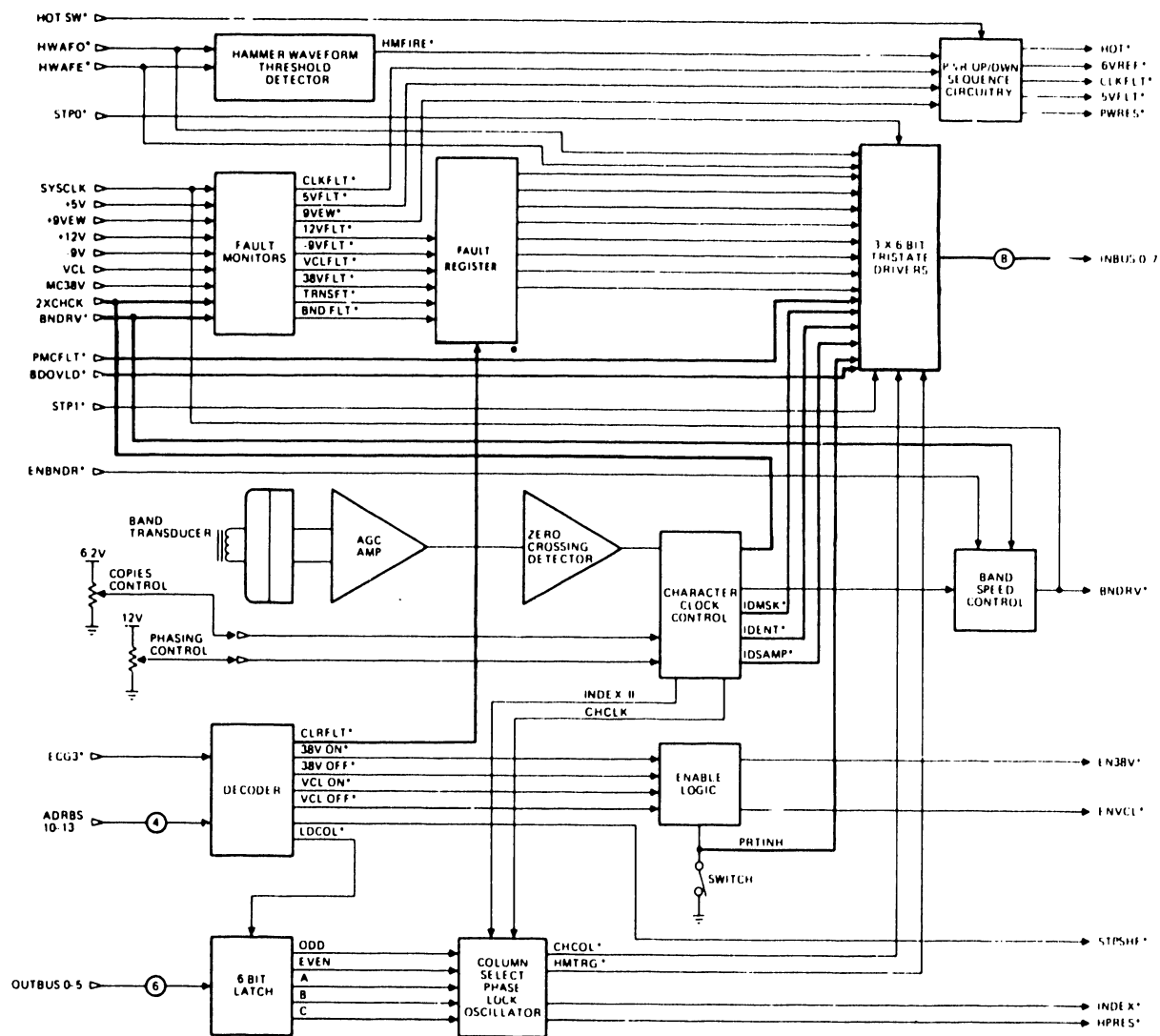


Figure 2-43. Timing and Status CCA Block Diagram

c. Power Up/Power Down Sequence Control

When the AC Power switch is pressed to the on position, voltage comparator U53-2 is at first off and slowly charges capacitor C54. Since U53-1 stays low, a Power Reset (PWRES*) signal is generated for about 0.5 seconds until C54 reaches 4.5 volts. PWRES* is sent to the Processor, Interface and Power Board CCAs via the Mother Board CCA connector P2-20.

When power is turned off in the printer, the 9VEW (9 Volt Early Warning) input to U53-5 goes low. U53-2 then goes low and capacitor C54 is discharged. This causes U53-1 to activate the PWRES* signal to the Processor, Interface, and Power Board CCAs as an indication that there is a loss of primary power to the printer system.

d. Band Timing Circuitry

The Timing and Status CCA monitors the character band marks through the transducer input (**SH 4**). In 300 LPM printers, there are ordinarily two (2) timing marks per character. At a band speed of 184 IPS, they occur every 611 microseconds. For 600 LPM and 1000 LPM printers, there is one (1) timing mark per character. At the typical 600 LPM band speed of 126.6 IPS, they occur every 889 microseconds. The 1000 LPM band speed of 199.75 IPS creates a character period time of 563 microseconds.

Additional character band marks generate index pulses to sense the beginning of a character set. Other marks, inserted after the index mark, are used as code identifiers for the various band character sets.

The transducer signals are amplified, and digitized, and separated into valid character clocks, an index clock, and band identifier clocks. The band index clocks and the index clock are sent to the Processor CCA. The character clock is used by the Timing and Status CCA as a reference to create hammer trigger and hammer reset pulses. The trigger and reset pulses are sent to the Processor CCA as synchronizing references when the printer is in the print mode.

The following paragraphs describe the various devices used by the Timing and Status CCA to generate the character clock and other signals used in the Band Timing circuitry.

1. AGC Amplifier - The operational amplifier U13 (**SH 32**) accepts the transducer input signals and provides an amplified output of 15 volts peak-to-peak for a 300 LPM input of 600 millivolt. The input voltage amplitude is determined by setting the gap between the transducer and the character band. Typically the gap is 0.005 inches. Input voltage amplitude for 600 LPM and 1000 LPM printers should be 800 millivolts.

The amplified transducer signal is then referenced to between 4 and 5 volts before being squared by voltage comparator U14. The "squared" output of U14 is inverted and becomes the BNDCLK (Band Clock) input to the set/reset flip-flop U2.

2. Character Clock Control - Character Clock control is derived from U2 and U1 (SH 32). BNDCLK is input to U2 and clocked by the Systems Clock (SYSCLK) signal developed from the basic timing circuit on the Processor CCA (SH 29 or SH A31). U2 then produces a system-synchronized signal Raw Clock Pulse (RAWCLK PULSE).

The trailing edge of RAWCLK PULSE sets the 2XCHCK flip-flop U1. The positive going edge of 2XCHCK generates an 800 nanosecond pulse from the sync flip-flops U6 (SH 33) that resets the band speed counters U12, U24, and U25. When the counters, which are clocked by SYSCLK, reach a final count of 1216 (528 microseconds) for the 300 LPM or 1088 (472 microseconds) for the 600 LPM, or 832 (333 microseconds) for the 1000 LPM, the 2XCHCK flip-flop is cleared. 2XCHCK is set twice per character for the 300 LPM and once per character for the 600 LPM and 1000 LPM printers.

3. Band Speed Control - The character band speed is controlled by a Band Speed Header installed on the Timing and Status CCA. Logic Diagram Sheet 4 in section V of volume II shows the wiring for the various Band Speed Headers used in the B-Series printers.

The band speed operates with a simple speed up or slow down ("bang-bang") servo system controlled by signal BNDRV* (SH 33). If the counter U12, U24, U25 reaches a final count before 2XCHCK sets, the band is moving too slowly, and U7-9 will go low. BNDRV* also goes low to the Power Board CCA to signal for an increase in band speed. If the final count is not reached and 2XCHCK sets, the band is moving too fast. U7-9 forces BNDRV* high to cause the band to slow down. See table 2-45 for the correct band speed for the various printer models.

e. Band Identification

Band identification is made through the identification and index pulses picked up by the transducer from the character band. All extra or non-character pulses appear as signal Index Pulse (IDPLS*) from U9-3 (SH 32). The first such pulse is masked off by the IDENT Mask flip-flop U26 and by gate U8-6 (SH 37). The signal becomes Raw Index (RAWINDX*) which sets the initializing flip-flop U32 (SH 33) and Index I flip-flop U5.

The initializing flip-flop is used to synchronize the 300 LPM model's divide-by-two flip-flop output at U32-9 (SH 33) when the band first starts. The output of Index I flip-flop generates the INDEX II and INDX* signals used in character clock timing.

f. Copies Control and Phase Compensation

Copies control and phase compensation are achieved by the interaction of the COPIES and PHASE potentiometers on the operator control panel and the character clock signal 2XCHCK (SH 33 and SH 37).

1. Copies Potentiometer - The COPIES potentiometer (COPOT) controls the input voltage to comparator U14-11. It is used to vary the hammer current to compensate for the number of copies being printed. The second input to voltage comparator U14-10 is the character clock (2XCHCK*) derived from the band drive system via the programmable header.

A COPOT variation of from one (1) to six (6) volts at U14-11 changes the timing of the output of U14-13. The result is a delay in the hammer trigger that keeps the phasing of the print output constant as the hammer current is increased or decreased with variations in COPOT.

In the 300 LPM printer, the output of the copies delay, which cycles two (2) times per band character, is divided by a divide-by-two flip-flop U32 and passed to the phasing delay circuitry. Because the 600 LPM and 1000 LPM printer does not need the divide-by-two flip-flop, an extra signal CHRCLK must be generated. It is the output of flip-flop U1 (SH 37) that is clocked by 2XCHCK* and cleared approximately 100 microseconds later. This compensates for the timing differences between the 300 LPM and 600 LPM and 1000 LPM models.

For the 300 LPM printer, the copies delay is a leading edge delay determined by the time constant of C33, R33 (SH 33) and R93 (SH 37) and the COPOT threshold voltage of 1-6 volts on the positive input of U14. Time constant for the 600 LPM and 1000 LPM printers is determined by C33, R33 and a resistor provided on the programmable header J4.

2. Phasing Compensation - The PHASE potentiometer, located on the operator control panel, is the control that varies the input voltage to comparator U14-5 (SH 33) to signal a change in the hammer trigger timing. The second input to the comparator is a combination of COPOT and the character pulse derived from U20 and the programmable header J4 (SH 37).

The phasing delay, a leading edge delay, is determined by the time constant of C35, R41, and R89 (for 300 LPM), or C35, C41, and a resistor on the programmable header (for 600 LPM and 1000 LPM) and the input threshold voltage of 0.5 to 8.5 volts from the PHASE potentiometer. A PHPOT voltage variation will also result in a phase delay of signal BDCK÷2.

g. Hammer Waveform Monitor

The Timing and Status CCA monitors the hammer waveforms and notifies the Processor CCA through the INBUS. The waveform HWAFO* is an analog signal derived from the Hammer Driver CCA (A6) circuitry. The voltage level of HWAFO* is 7.38 volts when all drivers are off and a maximum of 5.5 volts when any driver is on. This waveform is detected at a threshold of 6.2 volts by voltage comparator U42-1 (SH 36) and is sent to INBUS 2 as ODDHMR* (SH 35). INBUS 2 will be high when a hammer driver is on and low when the hammer drivers are off. HWAFO* is used by all three (3) printer models.

In 600 LPM and 1000 LPM printers, HWAFF* from the second Hammer Driver CCA A26 is also used. Its function is the same as that of HWAFO*. It is sent to INBUS 0 as EVNHMR* (SH 35). In 300 LPM printers, the HWAFF* is disabled because there is no input on P1-22 and therefore U42-5 is pulled up to about +9 volts.

The three (3) signals, ODDHMR*, EVNHMR*, AND HMFIRE*, derived from the hammer waveform detection circuitry, are used by the Processor CCA to assess hammer fire conditions. If a hammer fires while the printer is not in the print mode, the +38 volts is disabled and a fault status is shown on the control panel STATUS display.

h. 300 LPM Print Column Select Circuitry

The 300 LPM printer requires various hammer firing times because of the use of double spanning hammers and the possible multiple print column positions that result from the 10CPI/15CPI option. The ECG3* (Enable Control Group 3) signal from the Processor CCA enables decoder U45 (SH 36) and allows LDCOL* (Load Column) to load latch U46 (SH 34). Latch U46 then decodes the OUTBUS lines that select the print column (ODD, EVEN, A, B, or C) and sends the selection to gates U47 and U38. Table 2-46 shows the print column selection decoding of the OUTBUS lines.

TABLE 2-46. PRINT COLUMN SELECTION DECODE

OUTBUS Bit						Column Selected
5	4	3	2	1	0	
X	1	1	1	1	0	Odd
X	1	1	1	0	1	Even
X	1	1	0	1	1	A
X	1	0	1	1	1	B
X	0	1	1	1	1	C

The gated output of U38 and U39 is then used to develop the HPRES* (Hammer Pulse Reset) signal. HPRES* initiates the hammer trigger pulse by resetting hammer trigger generator U37 (SH 26) or U9 (SH A30). U37 or U9 generates nine hammer trigger pulses for every character clock. The output is fed into U35 (SH 34) to develop the signal Hammer Trigger (HMTRG*) that is then placed under Processor CCA control.

Using the SYSCLK signal, counter U31 (SH 34) and gate U30-8 generate a pulse which is 54-times the CHRCLK frequency. This pulse is sent through a divide-by-two flip-flop U17-5 and is used as the clock for counters U16 and U17-9. These counters provide the necessary pulses for the select circuitry. The counters U31 and U16 and the flip-flops U17-5 and U17-9 are cleared by the leading edge of the CHRCLK signal from U18-9 and 8. This keeps the digital circuitry in synchronization with the character band speed.

i. Fault and Status Detection

The Timing and Status CCA fault and status detection logic consists of the circuitry to monitor nine (9) different faults, a 4-bit fault register, and three (3) 6-bit tri-state drivers. The fault register is cleared by enabling the CLRFLT* line from the Control Group 3 Decoder U45 (SH 36). When any one (1) fault occurs, the SYSTCH* signal line goes low, and the INBUS drivers U40, U48, or U47 place the fault on the INBUS. Status data does not activate the SYSTCH* signal.

The INBUS drivers are enabled by the Status Port 1 (STP1*) and Status Port 0 (STP0*) signals. Table 2-47 lists the INBUS bit signals for the STP0* and STP1* signal combination.

TABLE 2-47. FAULT AND STATUS ENABLE

<u>INBUS Bit</u>	<u>STP0*</u>	<u>STP1*</u>	<u>Signal on INBUS</u>	<u>SYSTCH* Level</u>
0	1	0	PMCFLT* (U48-11 active)	Low
1	1	0	BNDSPDFLT* (U48-13 active)	Low
2	1	0	TRNSFT* (U40-13 active)	Low
3	1	0	+38VFT* (U40-3 active)	Low
4	1	0	VCLFT* (U40-11 active)	Low
5	1	0	-9VFLT* (U40-7 active)	Low
6	1	0	+12VFLT* (U40-5 active)	Low
7	1	0	BNDCUR* (U40-9 active)	Low
0	0	1	EVNHMR* (U48-9 active)	High
1	0	1	IDENT* (U48-7 active)	High
2	0	1	ODDHMR* (U48-5 active)	High
3	0	1	PRTINH (U48-3 active)	Low
4	0	1	IDMSK* (U47-9 active)	High
5	0	1	IDSAMP* (U47-3 active)	High
6	0	1	CHCOL* (U47-5 active)	High
7	0	1	HMTRG* (U47-7 active)	High

Figure 2-44 illustrates, in block diagram format, the fault detection system used by the B-Series printer. The following faults or status conditions are monitored by the Timing and Status CCA.

1. Band Speed Fault (BNDSPDFLT*) - When the band and transducer are operating normally, the BNDRV* signal is toggling. If BNDRV* stops toggling, the RC circuit C42/R56 (SH 35) will discharge to less than 1.0 volt and the output of voltage comparator U14-14 will go low to signify a fault. The Processor CCA is notified by signal SYSTCH* (SH 35) and INBUS driver U48.

2. Transducer Fault (TRNSFLT*) - When the band and transducer system are operating normally, the 2XCHCK signal is toggling. This signal is monitored by a retriggerable one-shot U33, C43, CR3, and R62 (SH 35). If the signal stops toggling, the one-shot will time out and U33-13 will go low. The Processor CCA is notified by signal SYSTCH* and INBUS driver U40.

3. Paper Motor or Clamp Fault (PMCFLT*) - An over current (more than 6.8 amps) in the paper feed motor, or a current over 2.9 amps in the paper clamps, or no clamp current signalled by an active input from the Power Board CCA will cause an active SYSTCH* signal to be sent to the Processor CCA and a PMCFLT* output from INBUS driver U48.

4. Band Current Fault (BNDCUR*) - When band current exceeds 3.8 amps, the BDOVLD* (Band Overload) signal from the Power Board CCA is input to latch U50 (SH 35). When the output of U50 goes low, the SYSTCH* signal to the Processor CCA is activated and INBUS driver U40 activates the INBUS 7 line.

5. +38 Volt Fault (+38VFLT*) - Comparators U41 (SH 35) are configured to check for over-voltage and under-voltage levels. An over-voltage of over +42.79 volts will switch U41-2 low, and an under-voltage of less than +31.06 volts will switch U41-1 low. These outputs indicate that a +38 volt fault has occurred and SYSTCH* is activated. INBUS driver U40-3 will activate the INBUS 3 bit.

6. +12 Volt Fault (+12VFLT*) - Comparator U41 is configured to detect levels below +10.8 volts and above +13.2 volts. An under-voltage will switch U41-13 low, and an over-voltage will switch U41-14 low. This causes the +12VFLT* signal to be placed on INBUS 6 and activates the SYSTCH* line to the Processor CCA.

7. -9 Volt Fault (-9VFLT*) - A -9 volt fault is sensed when the voltage level drops to -5.085 volts. U42-14 will then switch low. -9VFLT* is sent to INBUS 5 by driver U40-6 and SYSTCH* is sent to the Processor CCA.

8. Voltage Clamp Fault (VCLFLT*) - The hammer driver VCL level is monitored by U42 (SH 35). A level of less than +1.0 volts will set U42-13 low and is output by INBUS Driver U40. The SYSTCH* signal to the Processor CCA notifies the Processor CCA of the status change.

9. Unconditional Faults - The unconditional faults are not controlled by the Processor CCA and will cause an immediate shut down of the printer system. **Table 2-48** summarizes all unconditional logic conditions and the signal levels affected. The +5 volt fault, the over-temperature fault and the clock fault are discussed in the following paragraphs.

TABLE 2-48. UNCONDITIONAL FAULT SIGNAL LEVELS

Input Condition	HOT*	+6VREF	5VFLT*	PWRES*	ENVCL*	EN38V*
HOTSW* is low	Low	0V	High	Low	X	High
5VFLT* is low	X	0V	Low	Low	X	High
HWAFO* is low	X	0V	High	Low	X	High
HWAFF* is low	X	0V	High	Low	X	High
9VEW is low (power up or power down)	High	6.2V	High	Low	X	High
Normal Printing Operation	High	6.2V	High	High	Low	Low
Normal with Print Inhibit switch on	High	6.2V	High	High	High	Low

Note: The VCL fault is disabled by gate U8-3 when the print inhibit switch is on.

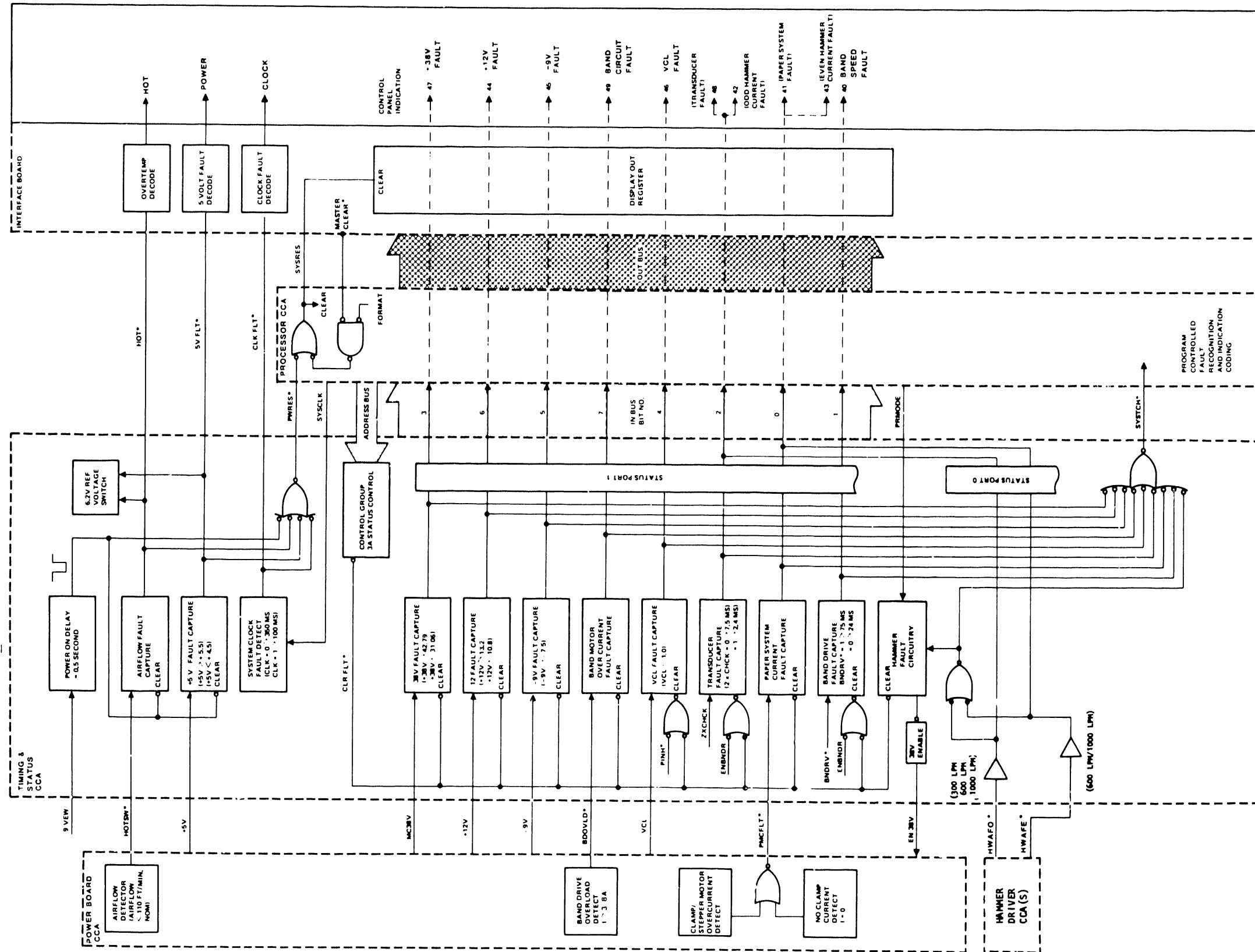


Figure 2-44. Fault Detection System

(a) Over-temperature Condition - If an over-temperature condition occurs, the HOTSW* (Hot Switch) signal goes low and sets the flip-flop U54-7 (SH 36) output to produce a high at inverter U54-4. This causes a HOT* fault to appear at U21-3. The HOT* fault disables the 5VFLT* at U22-1, disables the 6VREF at U43-2, and enables PWRES* at U43-5.

(b) Clock Fault (CLKFLT*) - CLKFLT* is monitored at U33 (SH 36), a retriggerable one-shot. The SYSCLK signal keeps U33 retriggered. If SYSCLK stops, the signal at U33-12 goes high enabling PWRES* and generating the CLKFLT* signal at U22-5.

(c) +5 Volt Fault (5VFLT*) - The comparator U53 (SH 36) monitors the 5 volts for an over- or under-voltage. If the voltage is greater than +5.5 volts or less than +4.5 volts, the fault latch U54-13 goes low. This will shut the printer down by driving the 6.2 volt reference voltage to ground.

j. Control Group Enable

Control Group 3 is used by both the Interface CCA and the Timing and Status CCA. When enabled by signal ECG3*, decoder U45 (SH 36) will output one (1) of the following signals: CLRFLT*, 38VOFF*, 38VON*, VCLON*, VCLOFF*, LDCOL*, or STPSHF*. See table 2-8 or table 2-14 for the Centronics-Compatible Interface CCA, for complete decode and output signal conditions.

k. Print Inhibit Switch - Switch S1 (SH 35) is used to manually disable the Hammer Driver CCAs during maintenance or troubleshooting. S1 to ground will cause a high output from U8-3. This disables the ENVCL* (Enable VCL) signal to the Power Board CCA.

2.3.4 Hammer Driver CCA

The Hammer Driver CCA contains the circuitry for firing the hammers and detecting misfire. It receives print data from the Processor CCA via the OUTBUS and latches and decodes the information to enable the selected hammers to fire.

Figure 2-45 is the block diagram of the Hammer Driver CCA which can be used in support of logic diagram sheets 41-44 (section V, volume II).

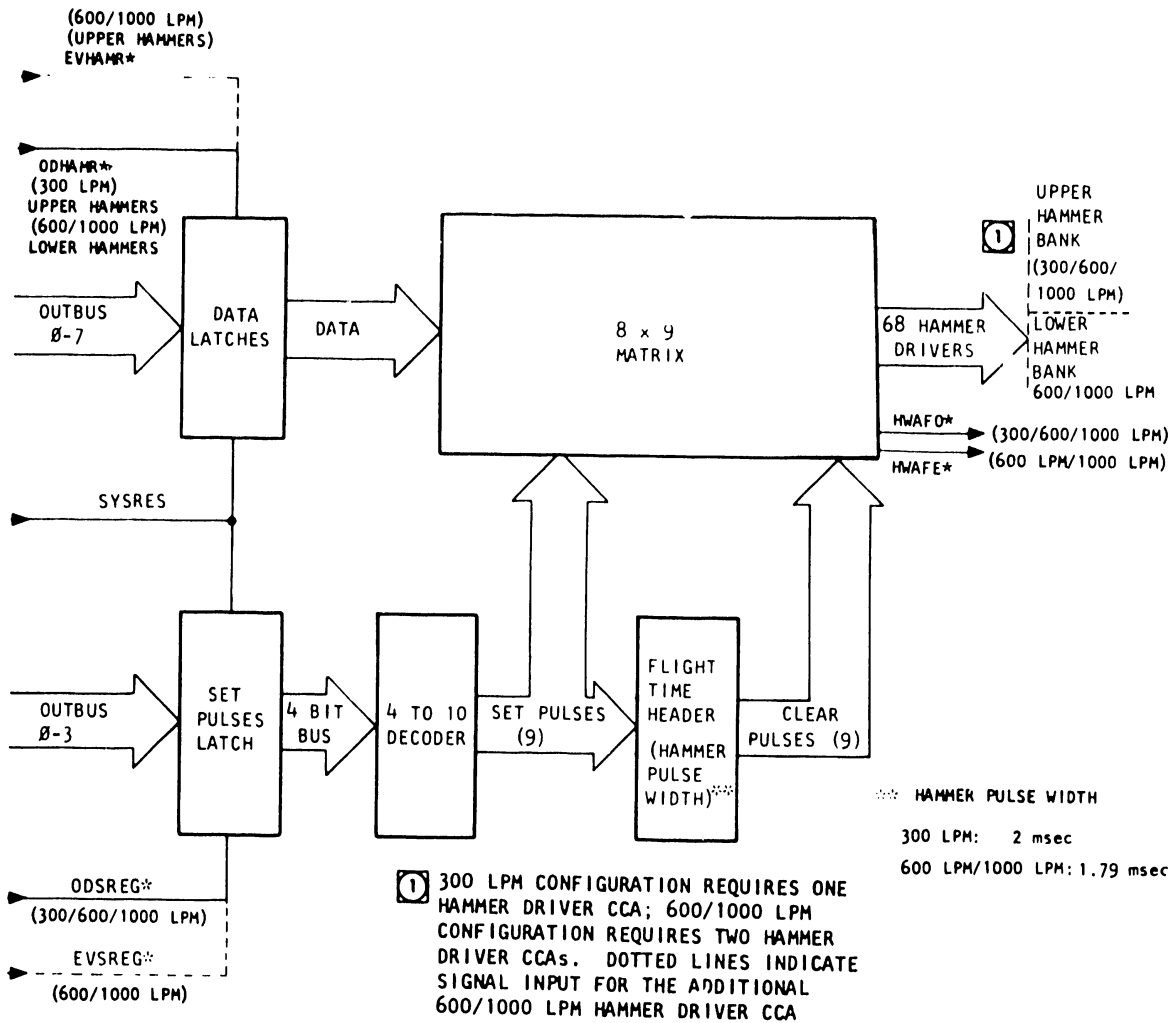


Figure 2-45. Hammer Driver CCA Block Diagram

The Hammer Driver CCA can perform the following functions:

1. Load and decode incoming data, under control of the Processor CCA, through a decoding matrix to enable a specific hammer to fire so that a specific character can be printed.
2. Perform system reset (SYSRES*) of hammer circuitry.
3. Fire hammers.
4. Detect hammer overheating.

a. Data Loading

Compare data from the Processor CCA data out register U54 (SH 25) or U47 (SH A27) is loaded into the Hammer Data Register U40 and U41 (SH 42) via the OUTBUS lines 0-7. The outputs of the hammer data register form one side of the hammer driver matrix, comprised of latches, which are internal components of hammer driver ICs U1 through U33 and U42.

S register U39 (SH 43), clocked by ODSREG* or EVSREG*, is loaded with data bits from OUTBUS0-3. The S register outputs, through decoder U38, for the set and clear signals for the hammer driver matrix.

b. System Reset

Signal SYSRES, generated manually by pressing the ALARM/CLEAR switch or under Processor CCA control, will clear the data register, set register, and the hammer driver matrix (SH 43).

c. Hammer Fire Detection

Hammer HWAFO* or HWAFF* (SH 44) is monitored by the Timing and Status CCA (SH 36) and sent as ODHAMR*, EVHAMR* and HMFIRE* to the Processor CCA.

d. Hammer Overheating Protection

Hammer overheating protection (SH 44) is provided in each of the hammer driver matrix latches. An overheated condition is transmitted by signal HWAFO*, at a 0.5 volt level, to the Timing and Status CCA.

e. Hammer Flight Time Header

Each B-Series printer requires a different flight time header J1 (SH 43) to establish the proper hammer driver current pulse width. The 300 LPM requires a pulse width of 2 mS and the 600 LPM and 1000 LPM require a pulse width of 1.79 mS. See logic diagram sheet No. 4 in section V of volume II for the flight time header wiring.

f. Circuit Description

The following circuit description is applicable to all configured hammer drivers with signal applicability as noted:

1. HWAFO* - Hammer fire detection signal used for all hammers on the 300 LPM and odd hammers for 600 LPM and 1000 LPM printers.

2. HWAFF* - Hammer fire detection signal used for the 600 LPM and 1000 LPM even hammers.

3. ODHAMR* - Enable Odd Hammers from the Processor CCA. Used for all hammers on the 300 LPM and the lower hammer bank on 600 LPM and 1000 LPM printers.

4. EVHAMR* - Enable Even Hammers from the Processor CCA. Used for 600 LPM and 1000 LPM upper hammer bank.

5. ODSREG* - Load Odd S Register signal from the Processor CCA. Used for odd/even columns with the 300 LPM; used for odd columns only (lower hammer bank) with the 600 LPM and 1000 LPM printers.

6. EVSREG* - Load Even S Register signal from the Processor CCA. Used for the 600 LPM and 1000 LPM for even columns (upper hammer bank).

A total of 66 or 68 hammer drivers can be selected and driven via the incoming data on the OUTBUS (SH 42). The drive voltage to the hammer drivers, termed HD38V (SH 44), is supplied via connectors P1 and P2 for use by the matrix logic. The hammer protect signal HPROT (SH 44) is from pin 1 of each hammer driver located in the matrix. This signal is derived from the thermal shutdown circuitry contained in each circuit and is transmitted to transistor Q1 from diodes CR1, CR2, or CR3.

The hammer driver collectors are ORed to turn on transistor Q1 for any hammer that is active to generate the hammer waveform (HWAFO* or HWAFF*) signal (see figure 2-46 for the hammer timing diagram). The voltage level when all drivers are off is approximately 7.5V; 4.0V when any driver is on; and 0.5V if a logic fault causes the hammer to overheat and go into thermal shutdown. The HWAFO* or HWAFF* signal is monitored by the Timing and Status and the Processor CCAs for a fault condition. HD28V (hammer driver voltage) is disabled if a fault occurs.

The VCL (reference voltage) signal from the Power Board CCA via connector P1-40 (SH 42) provides a reference voltage of approximately 1.4 volts that controls the output current load of the hammer drivers at the matrix logic. This voltage is varied by the COPIES control potentiometer on the operator control panel.

The ODHAMR* or EVHAMR* signal from the Processor CCA via connector P1-35 enables the U40 and U41 data latches to accept information from OUTBUS bits 0-7. Latches U40 and U41 are D-type flip-flops that are edge-triggered. Data on the D input is transferred to the Q outputs on the positive going edge of the ODHAMR* or EVHAMR* signal. The data latches (U40 and U41) output four lines each to the matrix logic D input.

The hammer driver matrix logic consists of eight (8) data inputs driving the rows and nine (9) pairs of timing inputs driving the columns. The duration of the hammer pulse is controlled by the geometry and inductance of the hammer, by the frequency of the timing inputs, and by the configuration of timing header J18. The hammer driver voltage normally will remain at +38 volts when the hammer is off.

The ODSREG* or EVSREG* pulse from the Processor CCA via connector P1-23 (SH 43) enables the set latch U39 (at the rate of once per subscan) to accept information from OUTBUS bits 0-3. OUTBUS bits 0-3 control the set-clear pulses.

The output of set pulse latch U39 goes to the 4-to-10-line decode U38 for generation of the set and the clear pulses to the hammer driver matrix logic. U39 outputs to the hammer flight time header J18 for configuring the inputs to the decoders U35, U36, and U37. See the hammer timing diagram, figure 2-46.

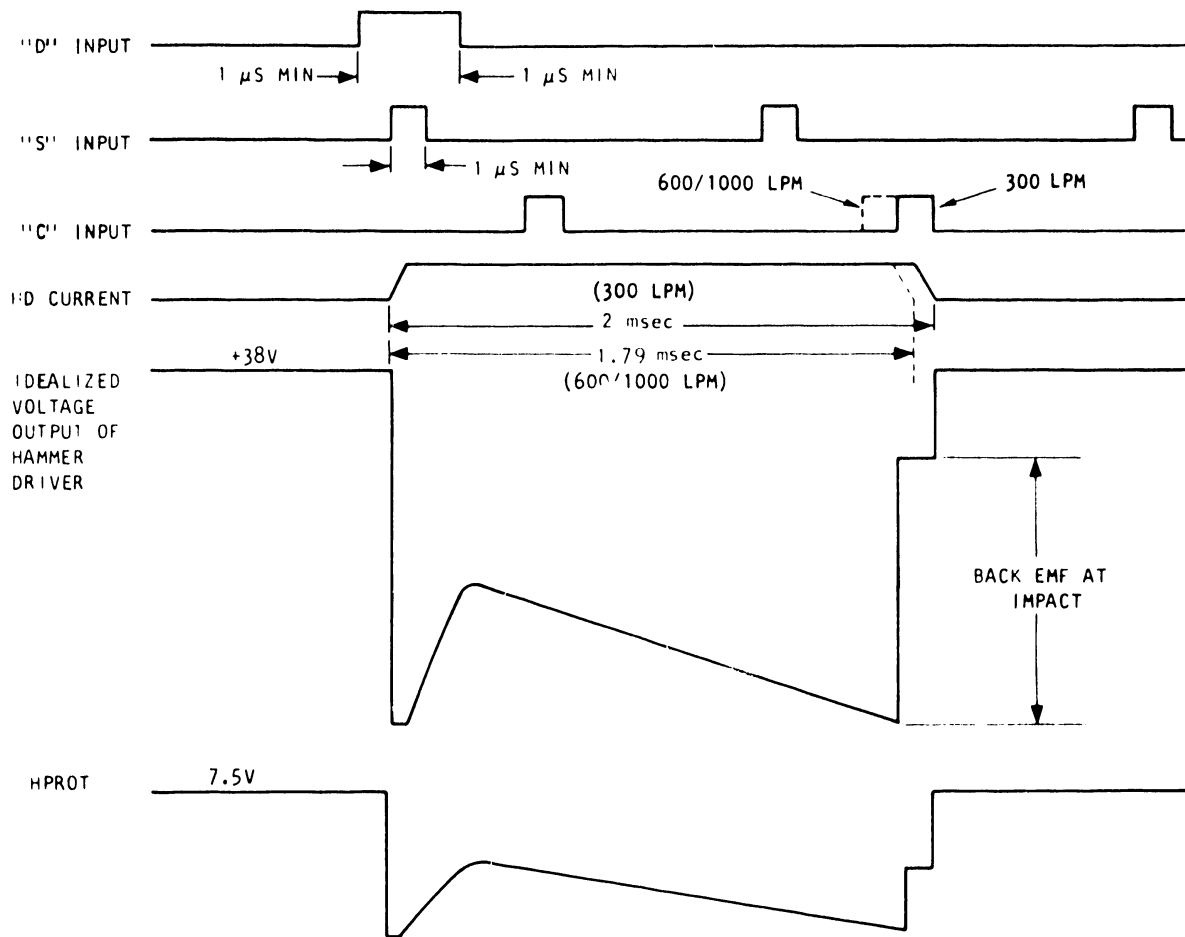


Figure 2-46. Hammer Timing Diagram (Ideal)

The 300 LPM print system uses one Hammer Driver CCA to fire the selected double column spanning hammers, all located in the upper hammer bank. It will scan the odd print columns first and sequence firing for required characters in those columns; then it will switch to scan the even print columns and sequence firing for required characters in the even columns.

The 600 LPM and 1000 LPM print system uses two Hammer Driver CCAs for its upper and lower hammer bank configuration. It matches up a single column spanning hammer and hammer driver with one print column. It scans for every ninth hammer, odd and even, and selects hammer drivers from each CCA to initiate hammer fire.

g. 300 LPM Hammer Firing

Hammer firing occurs with the coincidence of a character compare between the Processor CCA data RAM and band image PROM and the timing of a hammer trigger (HMRTRG*) set pulse S1 through S9 (see figure 2-46). The set pulses S1 through S9 are a continuous set of pulses with a minimum width of one microsecond, a period of 1.36 milliseconds (165 IPS) or 1.22 milliseconds (184 IPS), and a delay of 151 microseconds (165 IPS) or 136 microseconds (184 IPS) between two successive pulses (see figure 2-47).

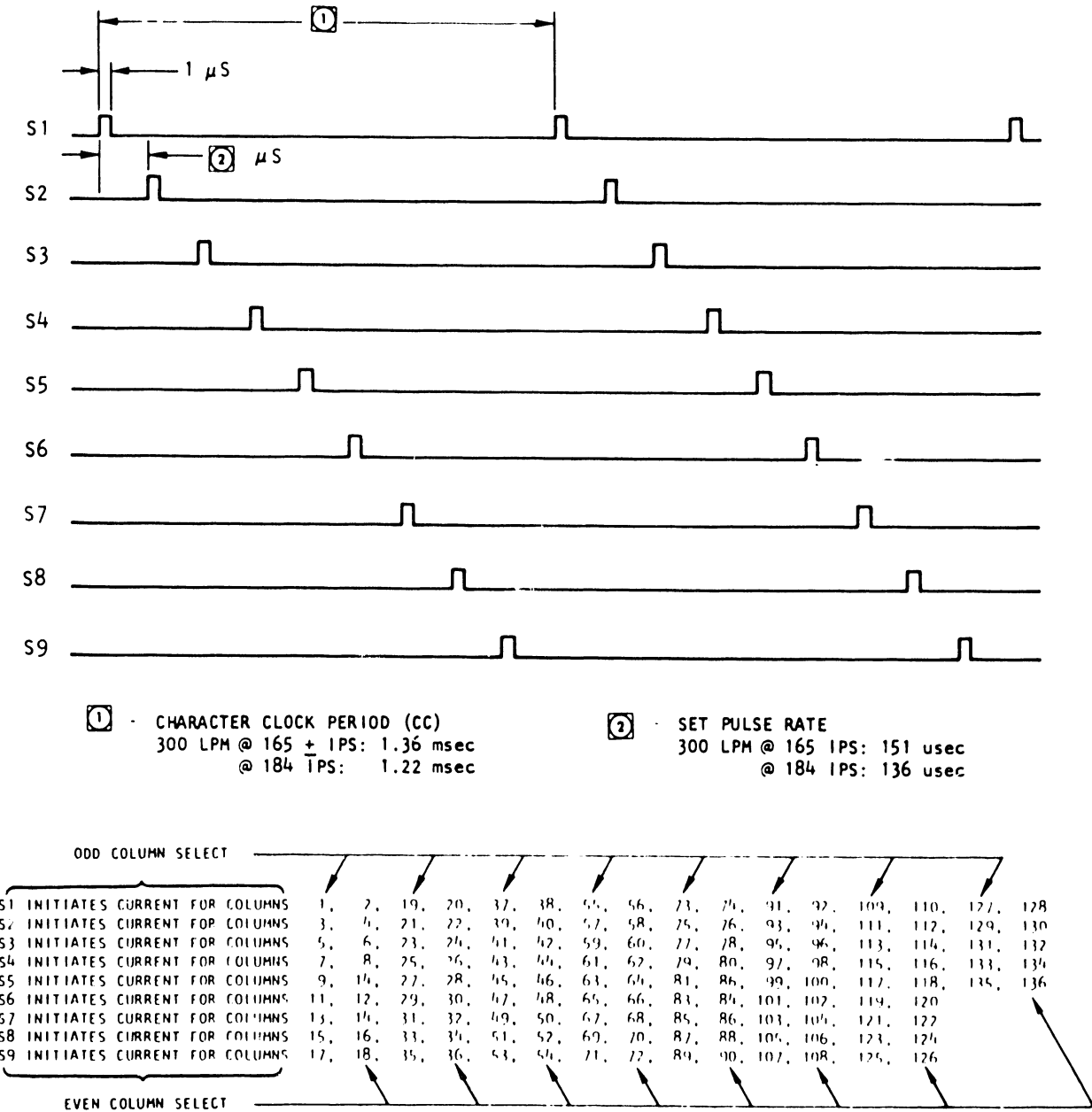


Figure 2-47. 300 LPM Set Pulse Timing Diagram

To fire a hammer, the desired hammer drivers data (D) input (a compare of data RAM character and band image PROM character) is enabled high for a minimum of one microsecond before its "S" pulse and dropped to a minimum of one microsecond after the end of the "S" pulse. The hammer driver is turned off on the leading edge of the second "C" pulse. Set pulses S1 through S9 will initiate current to print in the columns as shown in **figure 2-47**.

h. 600 LPM and 1000 LPM Hammer Firing

The hammer firing sequence is effected by a series of mini "subscans" of print columns to determine a compare of the character and the proper timing for hammer fire. The Processor CCA will switch between the two Hammer Driver CCA data registers (A and B) to fire the odd and even hammers properly matched up in a subscan (see **figure 2-49**). In subscan one, hammers for print columns 1, 10, 19, 28, etc., would be fired by set pulse S1 in the "A" register for the odd columns and set pulse S5 in the "B" register for the even columns. In subscan two, hammers for the even hammers 2, 20, 38, etc., would be fired from the "A" register by set pulse S1 and for the odd columns from the "B" register by set pulse S6. This method is used through the nine subscans needed to determine hammer firing for 136 columns of print data.

2.3.5 Power Board CCA

The Power Board CCA interfaces the Processor CCA to the paper feed drive system and the Timing and Status CCA to the band drive system. The Power Board CCA provides regulated voltages to the printer's analog and digital circuits. **Figure 2-48** is a block diagram of the Power Board CCA.

The Power Board CCA performs the following functions:

1. Supplies the regulated DC voltages.
2. Translates the band drive enable signals into a specific voltage and current level.
3. Detects the loss of air flow for complete printer system shutdown.
4. Controls the hammer drive current for penetration control.
5. Converts the Processor CCA paper feed digital signals into usable voltage levels for the paper feed system.
6. Amplifies and controls the application of 9 volt and 38 volt supplies to the stepper motor and paper clamp solenoid.
7. Protects the stepper motor and paper clamp circuits from overcurrent.
8. Monitors all voltage for over-voltage or over-current conditions.

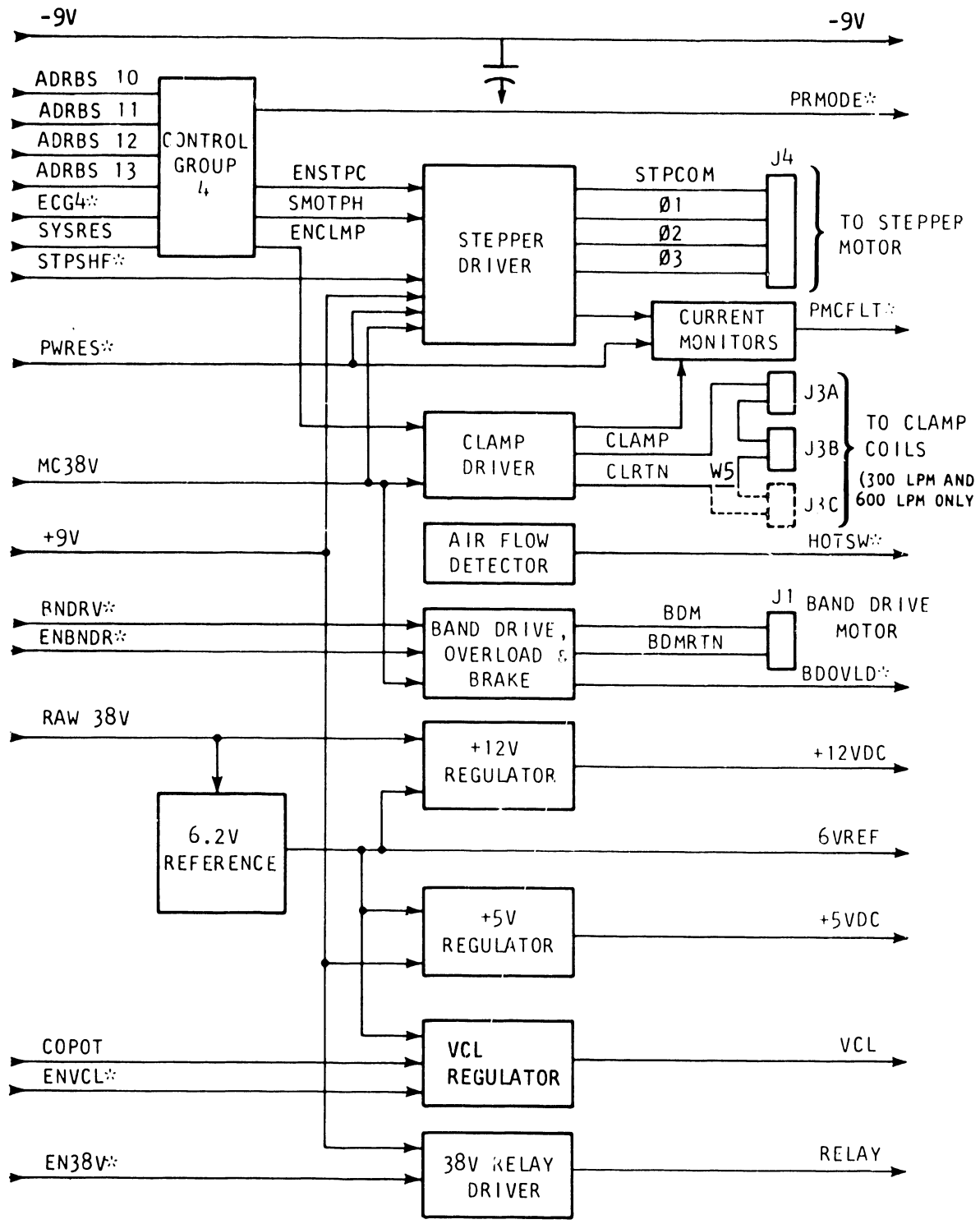
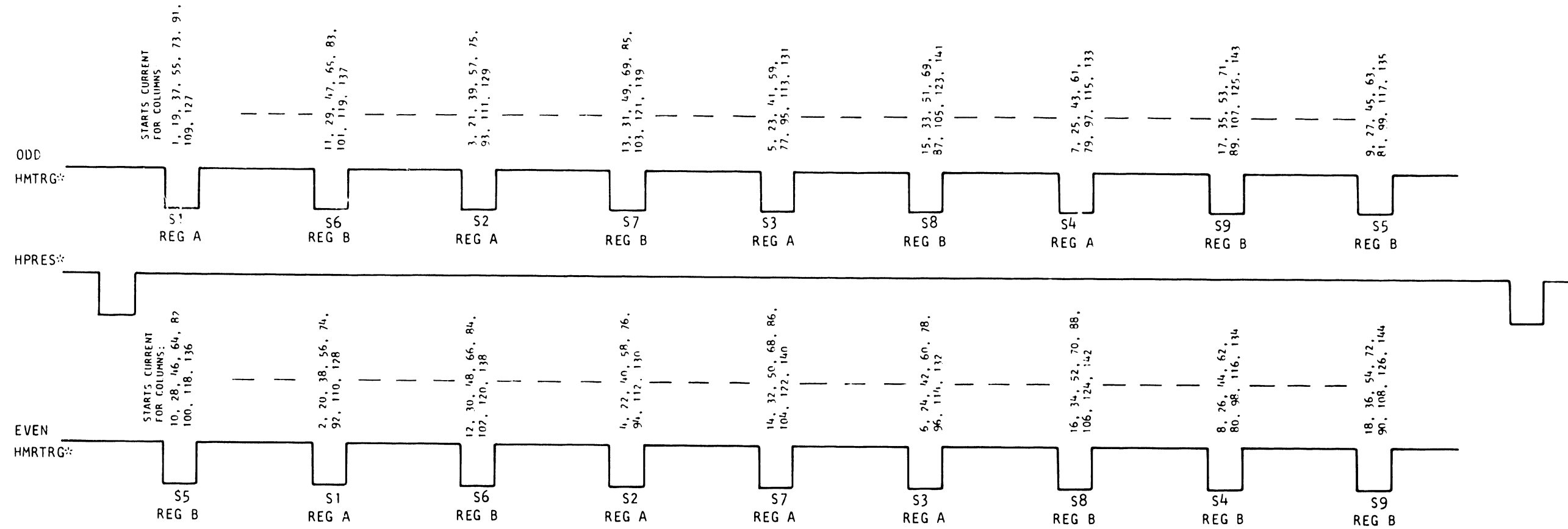


Figure 2-48. Power Board CCA Block Diagram



		PRINT COLUMN															
		⊗	⊕	⊗	⊕	⊗	⊕	⊗	⊕	⊗	⊕	⊗	⊕	⊗	⊕	⊗	⊕
SUB SCAN	FIRST	1	10	19	28	37	46	55	64	73	82	91	100	109	118	127	136
	SECOND	2	11	20	29	38	47	56	65	74	83	92	101	110	119	128	-
	THIRD	3	12	21	30	39	48	57	66	75	84	93	102	111	120	129	-
	FOURTH	4	13	22	31	40	49	58	67	76	85	94	103	112	121	130	-
	FIFTH	5	14	23	32	41	50	59	68	77	86	95	104	113	122	131	-
	SIXTH	6	15	24	33	42	51	60	69	78	87	96	105	114	123	132	-
	SEVENTH	7	16	25	34	43	52	61	70	79	88	97	106	115	124	133	-
	EIGHTH	8	17	26	35	44	53	62	71	80	89	98	107	116	125	134	-
	NINTH	9	18	27	36	45	54	63	72	81	90	99	108	117	126	135	-

- After HPRES*, ODD/EVEN HMTRG*, will successively set A and B Hammer Driver CCA hammer drivers. S1 will set the Set 1 driver in Hammer Driver Matrix A; S5 will simultaneously set the Set 5 drivers in Hammer Driver Matrix B. If a compare exists for a print column from the data register, hammer fire will occur.
- ⊗ Compare info sets up the "A" Hammer Driver CCA S-Register and Matrix;
⊕ Compare info sets up the "B" Hammer Driver CCA S-Register and Matrix.

NOTES:

Figure 2-49. 600 LPM/1000 LPM Hammer Firing Sequence

a. DC Regulated Voltages

The Power Board CCA supplies the following regulated voltages for use by the printer system: +12V, 6.2VREF, +5V reference, and VCL voltages. The following paragraphs describe the voltage regulators.

1. +12 Volt Regulator - The +12 volts is developed from RAW38V input (SH 38). Power is applied to the operational amplifier U3 from resistor R16 and zener diode VR1. The regulator output is divided down to 6.2 volts by resistors R14, R15, and R18 and compared to the 6 Volt Reference (6VREF) at pins 5 and 6 of U3. Control is furnished at pin 7 of U3 by the drive transistor Q2.

Output current limiting is provided by the current sensing circuit made up of R21, R23, R26 and Q1. If the output current exceeds about 100 mA, the voltage across R21 becomes large enough to turn on Q1. Turning Q1 on turns off the output of Q2. Zener diode VR1 and resistor R25 limit the output voltage to 19 volts should the regulator fail.

2. VCL Regulator - The VCL regulator must provide a variable voltage of 1.03 to 1.58 volts, to the hammer drivers, that can be turned on and off by the ENVCL* signal. A reference voltage is provided by R10, R13, W3, R20, and COPOT and is regulated by operational amplifier U3 (SH 38). Inverter U5 is used to turn the VCL regulator on and off via the ENVCL* signal.

Output voltage is limited to approximately +4.4 volts by CR4, and to -0.6 volts by CR5 if a malfunction occurs. R11, R12, W4, and R20 provide a voltage divider to give a slightly higher VCL voltage range than the W3 position.

3. +5 Volt Regulator - The +5 volt regulator reduces a semi-regulated +9 volts to +5 volts. A 2.5 volt (SH 38) reference is supplied to regulator U14 by the 6VREF and R19 and R22. The U14-10 (SH 40) output, Q13, Q14, and Q15 maintain the output voltage at +5 volts. When the Timing and Status CCA senses an over or under voltage condition, the loss of airflow, or the loss of the 434CLK, and clamps the 6VREF to ground, the 2.5 volt reference is also reduced to near zero volts.

Resistors R95 through R100 and operational amplifier U13 form a fold back current limiter that limits the output current to approximately 14 amps at +5 volts and 4.5 amps at 0 volts. Zener diode VR5, Q18, and Q19 form the over voltage circuit that shorts the output to ground if the regulator output ever exceeds about 6.3 volts. The results will be a power fault display of "P" on the control panel STATUS display.

b. Band Motor Drive/Brake System

The band drive system is a velocity servo of the "Bang-Bang" type (either full on or full off). The Timing and Status CCA monitors the band velocity by the band timing marks and the transducer pickup. It controls band speed by controlling the logic level of the BNDRV* signal.

When the band is off, BNDRV* and ENBNDR* are high. The band drive is disabled by inverter U5-11 and comparator U2-6 (SH 40). Brake transistor Q12 is on because the comparator circuitry of U2-5 senses that the motor terminal voltage is less than 22.8V.

When the band is to be turned on, BNDRV* and ENBNDR* go low. U11-6 (SH 40) immediately goes low, but U11-5 can not go high until the voltage on comparator U2-6 becomes less than U2-7. This takes about 150 microseconds, and assures that the brake transistor Q12 will be turned off before the drive transistor Q17 turns on.

When Q17 does turn on, it connects the band drive motor to the FUSD38V. If the motor current builds to a level of about 8.5 amps, the voltage across R106 and at U2-6 becomes more positive than the reference voltage on U2-7. This causes the comparator output to go low and turns off Q16 and Q17. The collector of Q17 immediately goes negative and is clamped to ground by the high speed catch diode CR17.

When the motor current decreases to about 8 amps, the voltage across R106 and at comparator U2-6 becomes negative with respect to U2-7, and the U2-1 output goes high. This turns Q16 and Q17 on again. This process is repeated until the band drive is turned off.

When the band drive is turned off, both BNDRV* and ENBNDR* go high. Drive transistor Q17 is turned off by BNDRV* at U5-11. U11-6 goes high as a result of a high ENBNDR* signal. However, brake transistor Q12 can not turn on until the motor terminal voltage is less than 22.8 volts at U2-5. This assures that the brake transistor will not turn on until Q17 has turned completely off.

During normal servo operation, the motor is connected to the +38 volts source for less than 10 milliseconds at a time. The currents are usually spikes of less than 8.5 amps. (The average current is usually about 2.5 amps.)

However, during initial start up or during excessive band loads, current limiting is needed to protect the circuit and motor from over load. Therefore, the motor current is filtered and monitored by comparator U2-10 (SH 40). If the average current exceeds 3.8 amps, pin 10 of U2 becomes more positive than pin 11 and causes BDOVLD* to go low to signal the Processor CCA that a fault has occurred.

c. Stepper Motor and Clamp Drive System

The stepper motor and clamp drivers are enabled by the Processor CCA through the Enable Control Group 4 circuitry and the Stepper Phase Shift Clock (STPSHF*) signal from the Timing and Status CCA. ADRBS10 through ADRBS12 and ECG4* control the output of addressable latch U10 (SH 39). ADRBS13 determines the logic level of the output.

Table 2-49 lists the Address Bus line signal levels, their functions, and the output signal conditions that are controlled by Control Group 4. See figure 2-16 for a function table and loading diagram for the U10 latch.

TABLE 2-49. CONTROL GROUP 4 DECODE AND FUNCTIONS

Address Bus Lines				Function	Output Signal Conditions
13	12	11	10		
0	0	0	0	Reset Print Mode	U10-4 low; PRMODE* high to P2-47
0	0	0	1	N/A	
0	0	1	0	Disable Paper Clamp	U10-6 low; ENCLMP low to U5-3
0	0	1	1	Disable Stepper Current	U10-7 low; ENSTPC low to U6-2
0	1	0	0	N/A	
0	1	0	1	Reset Motor Phase Initialize	U10-10 low; SMOTPH low to U7-1
0	1	1	0	N/A	
1	1	1	1	N/A	
1	0	0	0	Set Print Mode	U10-4 high; PRMODE* low at P2-47
1	0	0	1	N/A	
1	0	1	0	Enable Paper Clamp	U10-6 high; ENCLMP high to U5-3
1	0	1	1	Enable Stepper Current	U10-7 high; ENSTPC high to U6-2
1	1	0	0	N/A	
1	1	0	1	Set Motor Phase Initialize	U10-10 high; SMOTPH high to U7-1
1	1	1	0	N/A	
1	1	1	1	N/A	

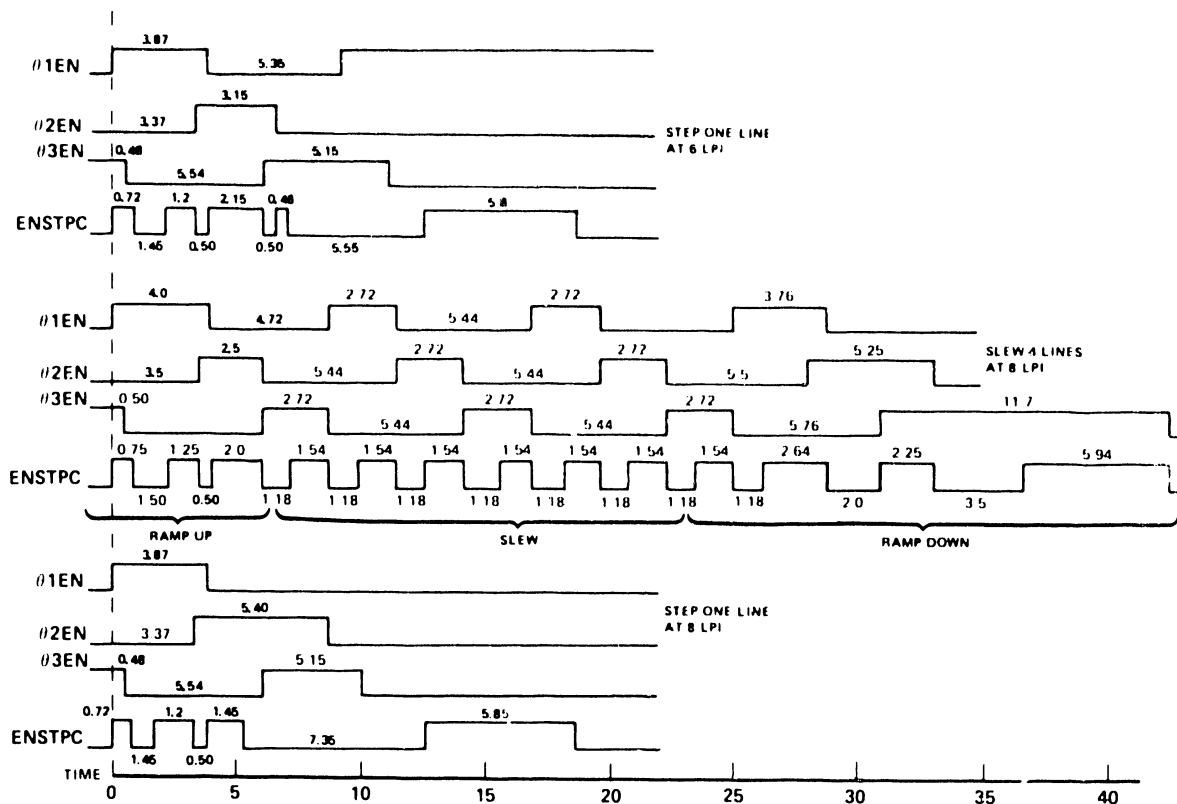
1. Stepper Motor Drive System - The motor used to move paper is a three (3) phase 15 degree stepper motor that must step through three (3) steps for each line printed at eight (8) lines per inch or four (4) steps for each line printed at six (6) lines per inch. Basically one (1) phase winding at a time is energized for each step of motion.

When the stepper system is at rest, one (1) phase is always energized by a 3.2 amp current flowing from the +9 volt power supply through diode CR15 (SH 39), the stepper motor common lead, back through the appropriate phase winding (01, 02, or 03), and through a sink transistor (Q8-Q10) to ground.

The energizing of the stepper phases is controlled by the 6-bit Stepper Phase Shift Register U9 (SH 39) and signals STPSHF* and SMOTPH (Set Motor Phase). During power up, a PWRES* clears all bits of the register. During printer initialization, the first two (2) bits of the register are set by STPSHF* and SMOTPH. This energizes the first phase and sets up the timing for subsequent phases.

A maximum high current pulse of 7 milliseconds duration is enabled by an active high ENSTPC command from the stepper/clamp control latch U10 (SH 39). Gate U6-2 is enabled and turns on Q5 and drive transistor Q11. The voltage on STPCOM goes to about 36 volts and increases the current through the enabled phase winding.

As the current rises, the voltage across current-sensing resistor R63 and U4-8 also increases. When this voltage becomes more positive than U4-9, the comparator output U4-14 goes low, causing a low at U6-3, and turning Q5 and Q11 off. As long as ENSTPC remains high for 7 milliseconds or less, this signal will control the time that high current is provided to the stepper motor. Figure 2-50 illustrates the typical stepper motor timing.



NOTE:

2. ALL TIMES SHOWN IN MILLESECONDS.
1. ACTUAL TIMING DEPENDS ON THE STEPPER MOTOR, THE SPROCKET SYSTEM AND PERFORMANCE REQUIREMENTS.

Figure 2-50. Typical Stepper Motor Timing Diagram

By limiting the high current pulse to a maximum of seven (7) milliseconds, damage from a logic failure is prevented. When Enable Stepper Current (ENSTPC) is high, C23 is charged by R38 (SH 39). The capacitor voltage is divided down by R39, R42 and applied to comparator input U4-8 through diode CR6.

After approximately seven (7) milliseconds, this voltage will become high enough for comparator input U4-8 to be pulled higher than pin 9. This unconditionally stops the current source from switching by shutting it off. U11 and R33 provide the discharge path for C23 when ENSTPC goes low. This allows the time out process to begin each time ENSTPC goes high.

A gross over-current condition can occur if the high current transistor Q11 fails to turn off. The circuit is protected by an over-current detector comprised of comparator U4-13 and flip-flop U12.

If the motor current exceeds seven (7) amps for about 50 milliseconds, comparator U4-10 will become more positive than pin 11 and will set the Paper Motor Current flip-flop U12 (SH 39). The stepper driver will be disabled by CR9 pulling U4-8 high. In addition, the Processor CCA will disable the printer and turn off the +38 volt power supply.

A no-current detector is made up of U4-4 and U4-5, R70, R71, R73, and C29 and C31 (SH 39). This detector can be disabled by placing a jumper in the W7 position.

2. Clamp Drive System (300 LPM and 600 LPM printers only) - The paper clamp system is comprised of two (2) separate clamp solenoid assemblies that are mounted beneath the Hammer Bank Assembly on the back side of the paper path. Two (2) armature assemblies are mounted beneath the platen on the front side of the paper path. The solenoid assemblies are series-connected to the Power Board CCA. When the solenoids are energized, the armatures are pulled toward the solenoids and clamp the paper in place during the printing operation.

When paper has stopped moving, clamp current is initiated by Enable Clamp (ENCLMP) going high. This turns Q3 on and pulls its collector to +5 volts. This turns Q7, Q4, and clamp drive transistor Q6 on and starts establishing the current reference voltage at C22 and U4-7.

The clamp current will increase until it reaches about 2.4 amps and the voltage across current-sensing resistor R66 reaches 1.2 volts. U4-6 will be more positive than U4-7. The comparator output then goes low and turns Q4 and Q6 off. The collector of Q6 goes immediately negative and is clamped to ground by high speed diode CR11. The clamp coil current decreases until the voltage at comparator U4-6 becomes more negative than U4-7.

At this time, the comparator output becomes high and turns Q4 and Q6 on. When printing is complete, ENCLMP goes low and turns off Q3. This turns off all driving transistors and allows the solenoid coils to quickly dissipate their energy by forward biasing CR10 and CR11 until the coil current drops to zero.

Clamp circuit operation is protected from open coils or connections by the no-current detector made up of U4-2 and discrete components. When the clamp is turned off, comparator U4-5 is biased at +0.63 volts by R70 and R73. Since U4-4 is at zero volts, it leaves the comparator output high and indicates no fault.

When the clamp is turned on, the voltage on comparator U4-5 goes to about 1.8 volts and U4-4 goes to about +1 volt. If no clamp current occurs, the voltage on U4-4 will become more positive than U4-5 and the output will go low. This sets the PMCFLT flip-flop U12 (SH 39) that flags the Processor CCA of the fault. The PMCFLT will also occur if drive transistor Q6 fails to turn off and causes the clamp current to exceed 5 amps.

d. Airflow Detector

The airflow detector uses two (2) thermistors biased in a bridge configuration and monitored by comparator U2 (SH 40). Thermistor RT2 monitors the ambient temperature and, at 25 degrees C, applies approximately 2 volts to U2-9.

Thermistor RT1 is self-heated by its low resistance and is ordinarily cooled by a 340 FPM airflow to produce 1.8 volts at U2-8. If the airflow drops below 110 FPM, the thermistor becomes hotter and its resistance decreases.

This causes U2-8 to become more positive than U2-9. HOTSW* then goes low and causes the timing and status circuitry to shut down the 6VREF and regulated voltages and display an "H" on the control panel STATUS indicator.

2.3.6 Mother Board CCA

The Mother Board CCA functions as a common bus for the transmission of required voltages and signals to and between the circuit card assemblies. Two (2) different CCAs are used in B-Series printers.

The 300 LPM Mother Board CCA (**SH 45 and SH 46**) has six (6) pairs of 60-pin card edge connectors into which the previously described CCAs are plugged. The connectors are designated XA1P1-XA6P1 and XA1P2-XA6P2.

The 600 LPM and 1000 LPM Mother Board CCA (**SH A45 and SH A46**) has seven (7) pairs of card edge connectors. The connectors are designated XA1P1-XA6P1, XA1P2-XA6P2, and XA23P1 and XA23P2.

The XA1 slot is a spare reserved for the Serial Interface CCA or for other special customer configurations. The XA23 slot is used by the 600 LPM and 1000 LPM models for a second Hammer Driver CCA. Connectors are provided for plugging in the Capacitor Bank Harness Assembly and for the optional Elapsed Time Meter Assembly. **Logic Diagram Sheet 47** provides a signal list for both circuit card assemblies.

A three (3) pole relay is used to connect the +38 volt power supply to the Hammer Driver CCA and to the drive circuits on the Power Board CCA. The relay has a 6 volt, 32 ohm winding and is driven from the +9 volts. The relay is energized when EN38V* to the Power Board CCA (**SH 38**) goes low and turns on U6. Resistor R28 drops the +9 volts to +6 volts before the signal is sent to the Mother Board CCA as the RELAY input.

2.4 PRINTER SUBSYSTEMS

Four (4) major printer subsystems are described in the following paragraphs. Each description deals primarily with the mechanical components of the subsystem and treats the functions of the various circuit card assemblies in general terms. The circuit card assembly descriptions in **paragraph 2.3** should also be consulted when needed.

The discussion of the following subsystems are also keyed to the logic diagram sheets in **section V** of volume II:

- Character/Band Ribbon Drive
- Paper Feed/Paper Clamp
- Print
- Power Supply

2.4.1 Character Band Drive and Ribbon Drive Subsystem

The character band/ribbon drive subsystem involves the components and circuitry used to drive the character band, track the band's markings during motion, and to drive the ribbon. It is activated by the program Start Motor subroutine described in **paragraph 2.6**. **Figure 2-51** provides a block diagram of the Character Band/Ribbon Drive Subsystem.

The character band is a steel horizontal font carrier containing 208 (300 LPM) or 416 (600 LPM and 1000 LPM) etched characters. Character clocks, index, identifier codes, and the 15 CPI (300 LPM only) code are derived from the band markings. The printer can accept different character bands without a change in the electronics when three (3) different Band Image PROMs are installed on the Timing and Status CCA. All bands are operator-changeable.

Ribbon movement past the hammer bank is controlled by the band drive. The ribbon drive roller is coupled to the band drive pulley. The capstan pinch wheel assembly then moves the ribbon in a continuous loop through the cartridge and across the print path in the paper throat.

a. Character Band Drive

The character band motor provides the mechanical energy to turn the character band. It is plugged into the J1 connector on the Power Board CCA and receives power and control instructions from the Processor CCA and Timing and Status CCA.

By means of program control, the Processor CCA issues ENBNDR* (Enable Band Drive). This signal is sent to the Timing and Status CCA band speed counter circuitry (**SH 33**) and then to the Power Board CCA (**SH 40**) which provides power to enable the band motor and control band speed. On the Timing and Status CCA, the band speed is sensed and compared to an ideal speed, and signal BNDRV* (**SH 33**) is generated.

At start up time, the band transducer senses the character band markings in order to establish the beginning index to provide the Processor CCA with the band identification. The Processor CCA can then compare the band I.D. data with the data in the image address PROMs to determine the validity of the band. After the band reaches proper speed, the subsystem functions to maintain the band at that speed and tracks the individual characters on the band.

Overload protection is provided to protect the band motor from problems such as mechanical overload. Band brake circuitry is used as an aid in stopping the band drive motor after it has been turned off.

b. Ribbon Drive

Ribbon drive operates whenever the band motor is operating and the ribbon rollers are engaged. The ribbon drive roller operates by means of a drive belt from the pulley on the band motor shaft. When the spring loaded pivot arm roller is closed, it engages with the ribbon drive roller and begins turning. The

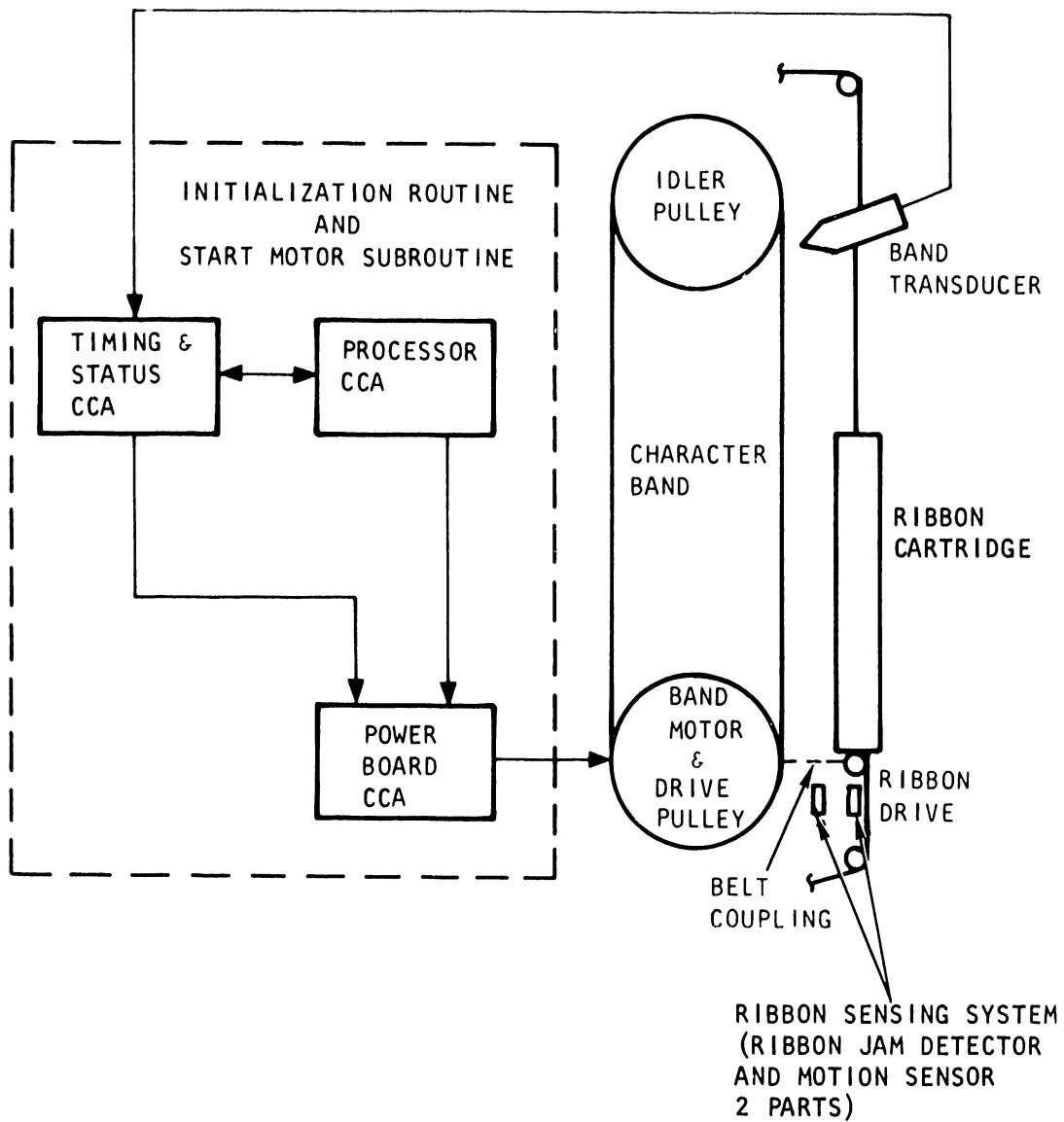


Figure 2-51. Character Band/Ribbon Drive Subsystem Block Diagram

ribbon is pulled from the ribbon cartridge, past the print station, and through the drive rollers in such a way that even folds are formed. The folds are forced back into the cartridge at the ribbon drive roller end.

The ribbon cartridge is comprised of a one-inch wide inked ribbon, whose entire length, except for that portion running through the print area and around the ribbon guides, is stored internally within the ribbon cartridge. The ribbon cartridge is placed on the band deck base and then locked into position by engaging it with the two (2) locating buttons provided on the band deck base. The ribbon is then threaded around the ribbon guides and between the band and the ribbon mask.

The ribbon mask is designed to serve a twofold purpose. First, it separates the ribbon from the paper in areas where no printing occurs to prevent paper smear. It also provides a smooth surface to assist the paper in passing through the paper throat area.

The ribbon is skewed as it goes through the print area. Skewing assures that most of the ribbon area is used, thus providing longer ribbon life. The ribbon guide attached to the platen aids in maintaining proper ribbon position to prevent ribbon smear.

In the Posidrive system, a two (2) part Ribbon Sensing Assembly monitors ribbon motion. A ribbon motion sensor is installed in the pivot arm, and its output is sent to the Interface CCA (Sh 2 and SH 9). This allows the Processor CCA to verify actual ribbon motion.

A ribbon jam detector, mounted near the pivot arm, is activated if the pivot arm is opened by a ribbon jam. The output of the jam detector microswitch is also sent to the Interface CCA. If ribbon motion stops or if a ribbon jam is detected, the same fault condition will be displayed on the control panel STATUS indicators.

2.4.2 Paper Clamp and Paper Feed Subsystem

The paper clamp and paper feed subsystem involves those components that hold the paper rigid during the print routine and move the paper during the move paper routine. The major components and functions of the paper clamp and paper feed subsystem consist of the following:

- Clamp Coils - Used to clamp the paper firmly during print routine in 300 LPM and 600 LPM printers.
- Clamp Driver - Supplies +38V to energize the clamp coils.
- Stepper Motor - A three phase stepper motor used to operate the paper feed system.
- Stepper Motor Driver - Supplies 38V to the stepper motor coils and allows a path to ground through the stepper motor phase register.

During the print routine, the paper is held rigid by two (2) solenoid-actuated paper clamps located below the print station. During the move paper routine, the three-phase stepper motor, also referred to as the paper feed motor, moves through its step phases to move the paper. Smooth paper motion is ensured by the Power Board CCA stepper-phase-control, which activates the next phase before deactivating the last phase.

The stepper motor is belt-coupled to the sprocket shaft clutch mechanism which engages the sprocket shaft. The two sprockets mounted on the sprocket shaft pull the paper through the paper throat area and past the print station to feed the paper out of the rear of the printer. **Figure 2-52** provides a block diagram of the Paper Clamp/Paper Feed Subsystem components.

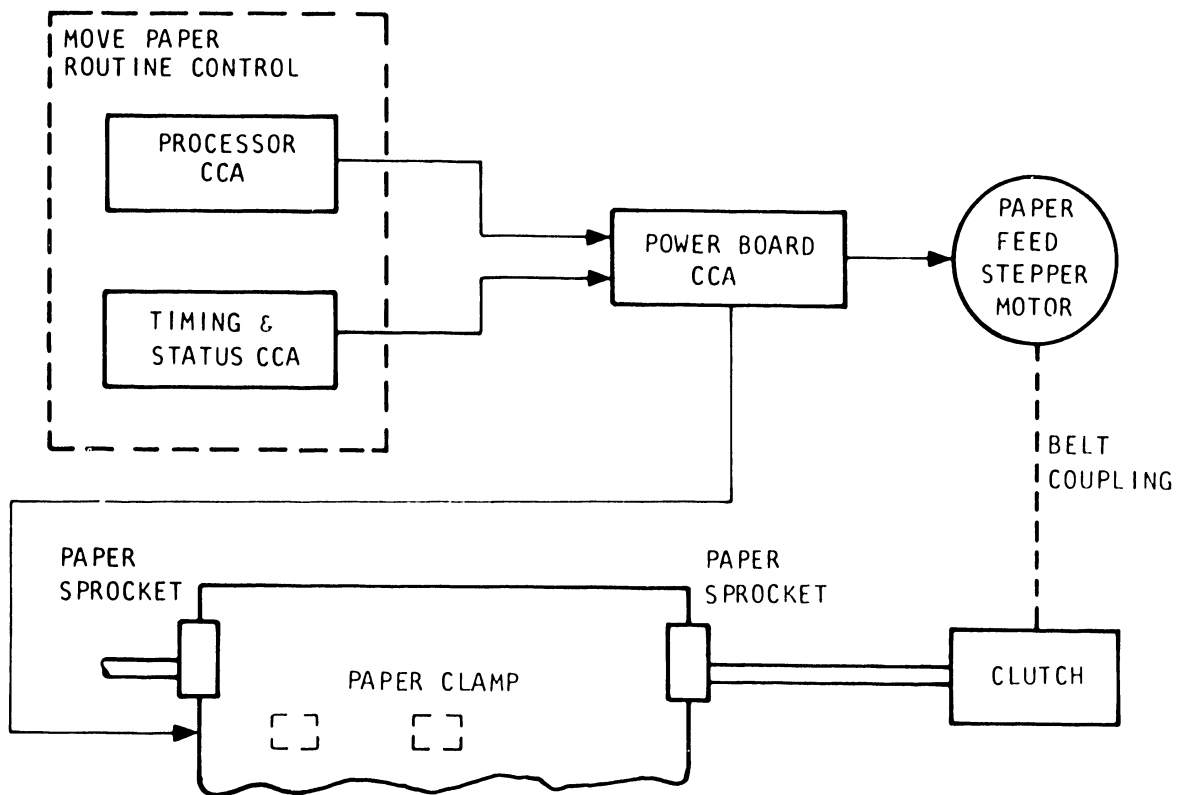


Figure 2-52. Paper Clamp/Paper Feed Subsystem Block Diagram

a. Clamp Coils (300 LPM and 600 LPM Printers Only)

The paper clamps are designed to hold paper in position during the print cycle. The paper clamp system is comprised of two (2) separate clamp solenoid assemblies mounted on the front side of the paper path. When the solenoids are energized by ENCLMP (SH 39), the armatures are pulled toward the solenoids, clamping the paper in place during the print operation. A slight drag is kept on the paper by the spring-loaded armature to keep it taut during the paper move operation.

b. Clamp Driver

The clamp driver is a switching mode constant current source that supplies about 2.2 amps of current to the series-connected solenoid coils. See the Power Board CCA description for a discussion of the clamp driver enable process.

c. Stepper Motor

Upon completion of the print routine, the Processor CCA determines the type of paper motion desired by the format command and causes the appropriate stepper motor control signals to be transmitted to the Power Board CCA to move the paper accordingly.

The 6LPI/8LPI switch on the operator control panel generates a signal which is sampled by the Processor CCA in the off line mode. The Processor CCA generates stepper motor control signals for the Power Board CCA to step paper at 6 or 8 lines per inch. When the printer is on line, any change in switch position is ignored to ensure that forms control is not lost by accidental switch operation.

In the off line mode, the control panel STEP switch, when activated, is detected by the Processor CCA, which interprets the desired function, and generates the stepper motor control pulses for the Power Board CCA to step the paper one line.

The control panel TOP OF FORM switch, when activated in the off line mode, is also detected by the Processor CCA, which generates stepper motor control pulses for the Power Board CCA to slew paper until the next top of form position is reached.

The motor used to move paper is a three-phase stepper motor (SH 4) that moves paper 1/24 inch for each phase advance. Thus to move paper one line at 6 LPI, the motor must be advanced through four phases, or 1/6 inch. To move paper one line at 8 lines per inch, the motor must be advanced through three phases, or 1/8 inch.

Stepper Motor Timing is shown in **figure 2-50**. Note that the following phase is activated before the previous phase is deactivated. This procedure allows smoother paper motion.

Actual timing of the stepper phases and ENSTPC depends upon the stepper motor and sprocket system and the performance required. At the end of a paper advance, a high current pulse of approximately 5.8 milliseconds helps to settle any paper vibration. The high current pulse-generating circuitry is basically a switching mode constant current source. See **figure 2-53** for a detailed Paper Clamp/Paper Feed Drive Subsystem diagram.

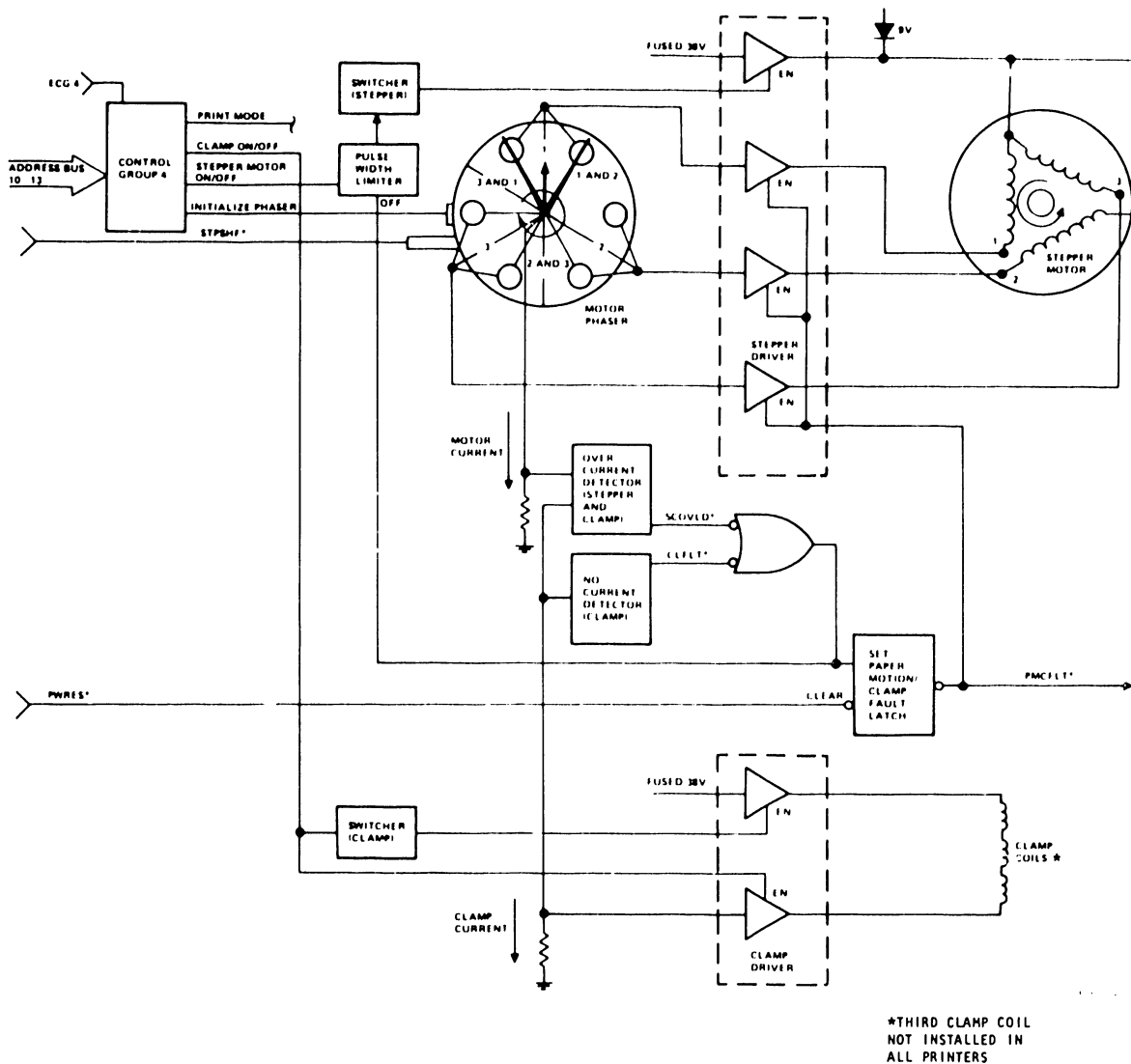


Figure 2-53. Paper Clamp/Paper Feed Drive Subsystem Diagram

d. Paper Feed Motor Over-Current Detection

A failure in the stepper motor driver system could cause an over-current condition to occur. If an over-current condition should occur, protection circuitry on the Power Board CCA (SH 39) has been designed to prevent any catastrophic failures or damage.

2.4.3 Print Subsystem

On completion of the loading and editing of data, a print function will occur. For correct printing to occur, two conditions must be met. First, hammer triggering must be timed so that at impact the hammer and band characters are precisely aligned. Next, the band character aligned with the hammer must compare with the respective column in memory. Figure 2-54 shows, in block diagram format, the major components of the print subsystem involved in the print operation.

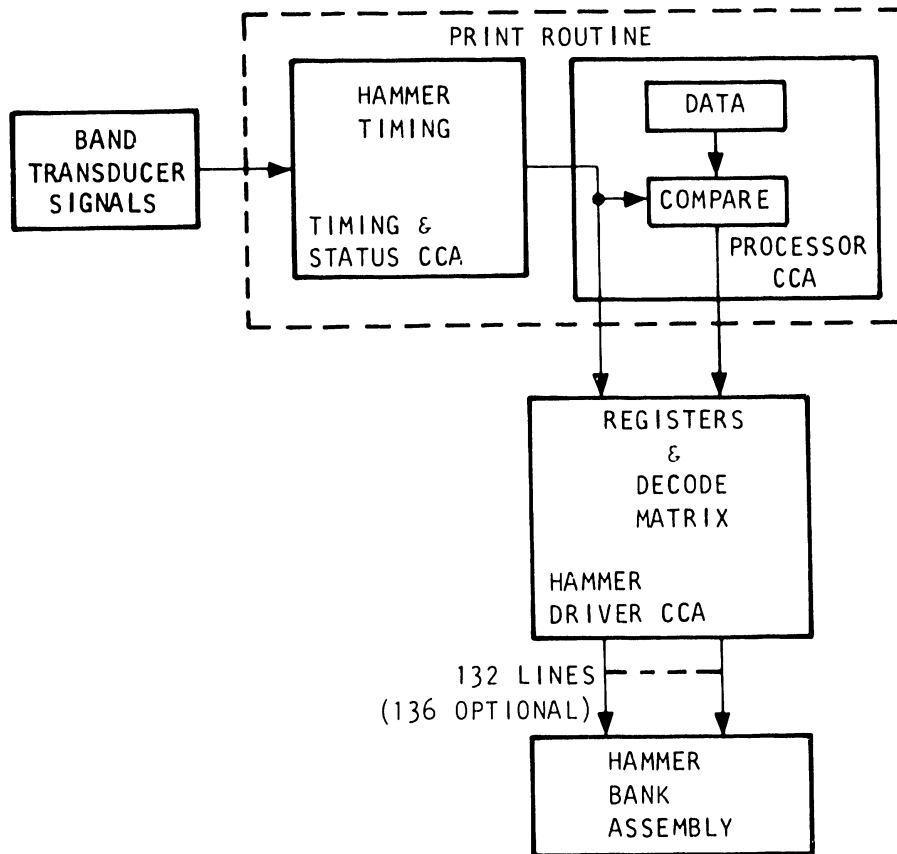


Figure 2-54. Print Subsystem Block Diagram

Two (2) different Hammer Bank Assemblies are used in B-Series printers. The following paragraphs discuss the hammer timing, the compare process, and the hammer fire operation for each type.

a. 300 LPM Print Subsystem

The 300 LPM printer uses a single Hammer Bank Assembly with 66 double-spanning hammers to print 132 columns, or 68 double-spanning hammers to print the optional 136 columns. Each hammer covers a distance equal to two (2) column widths. Because of the double-spanning hammers, and the use of one (1) Hammer Driver CCA, 300 LPM model print operation differs from that of the 600 LPM or 1000 LPM printers.

1. Hammer Timing - The hammer timing circuit divides one (1) character clock time, which is the time needed to move between characters on the band, into ninths. At each 1/9th of a character clock, a hammer will have a character aligned with it, and a hammer trigger pulse can be sent.

Due to the physical relationship of the hammer width and the separation of characters on the band, every eighth character on the band will be precisely aligned with every ninth hammer. **Figure 2-55** provides a diagram of the physical relationship of the band column to the hammers.

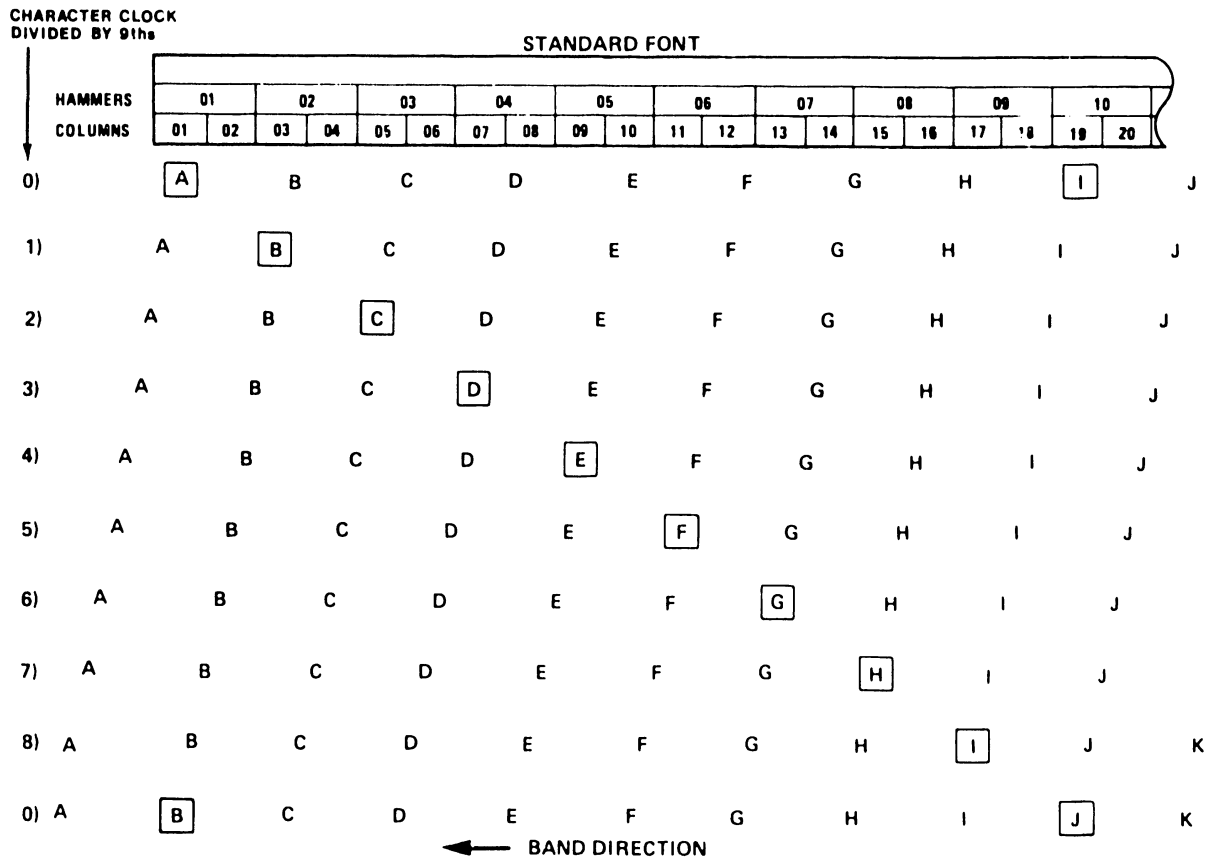


Figure 2-55. 300 LPM Physical Relationship of the Band Column and Hammers

Note that eight (8) characters after the letter "A" is at hammer 1, column 01 on the band, the letter "I" is also aligned at hammer 10, column 19. In one (1) character clock time, the letter "B" will be lined up with hammer number 1 and the letter "J" will be aligned at hammer 10, column 19.

In order to fire the hammers at the proper intervals, nine equally spaced pulses must be generated per character. A counter on the Timing and Status CCA (SH 39), using signal SYCLK and operating as a frequency multiplier, provides this function in the digital timing system. Timing marks on the band provide the information to the hammer timing circuit so that the hammers can be triggered at precisely the right time. A magnetic reluctance pick-up, the transducer, senses the band timing marks and produces an analog signal for use by the Timing and Status CCA. An extra timing mark on the character band creates an index pulse which signifies the first character of a character set.

The printer is available with an optional compressed font band, which prints three columns in front of each hammer on the hammer bank. In order to fire the hammers so that the characters are printed in the various possible column positions, a means of delaying the hammer trigger signal a different amount of time for each column position is necessary. Signal HPRES* (SH 34) creates the column offset and signifies the beginning of each set of nine (9) hammer trigger pulses. Note that the actual width of the print-out is reduced with the 15 CPI option.

Paper thickness affects the hammer flight time. A COPIES control on the control panel is necessary for varying the hammer current and at the same time compensating for the character phasing. The Timing and Status CCA uses the COPIES and PHASE control signals, COPOT (SH 33) and PHPOT (SH 33), to generate the needed variations in hammer current and timing.

2. Compare - Hammer timing circuitry enables the printer to time the hammer fire with respect to the band. A comparison of the character loaded in memory and the band character presently in front of a hammer is necessary to ensure printing of correct data.

After synchronizing with the character band, the compare section of the Processor CCA uses the hammer timing information to decide which band character is in front of which hammer at what time. On the Processor CCA, HPRES* from the hammer timing circuitry of the Timing and Status CCA, clocks the band position counter U4 (SH 30). U4 counts each time a new character is in front of hammer number 1, and is cleared after each band revolution by signal INDEX*. The information is stored in a working register when the print function is being executed. See figure 2-56 for a pictorial description of the compare process.

The data RAM circuitry U38 and U39 (SH 28) on the Processor CCA is comprised of the storage locations which correspond to the print columns. By means of the RAM address pointer circuitry U57 and U58, the correct location in the data RAM will output its stored data character to the ALU circuitry U32 and U51 (SH 25) for comparison with the band image PROM.

The band image PROMs, MEM6, MEM7, and MEM8 (SH 31), contain the characters that correspond to the 208 characters on the character band. Only one of the band image PROMs is enabled at any time. The result of this data comparison of the band image PROM (SH 31) and the data RAM (SH 28) is stored in the Processor CCA hammer data register and is then transferred to the hammer data register on the Hammer Driver CCA.

This data comparison occurs once each time HMTRG* occurs. Therefore, once during each HMTRG* time period, a byte of data will be transmitted to the Hammer Driver CCA.

The "S" clock keeps track of which set of hammers is able to fire by synchronizing the first hammer trigger pulse occurring after the hammer pulse reset, and by counting the hammer trigger pulses occurring thereafter.

In printers with the sentinel configured Processor CCA (257315-001), the scan flag determines if all characters in the data RAM that have a sentinel bit have been compared after a complete column phase has occurred.

The column phase register keeps track of ODD, EVEN, A, B, or C column positions, and, when all phases are complete and all legitimate data has been compared, allows the print mode to end.

This compare operation continues until odd column positions have been printed. Then, after a delay to allow the hammers to recover, the same procedure occurs with the even columns. When this procedure is complete, the Processor CCA ensures that all the hammers are turned off, terminates the print cycle, and enters the format routine to execute the paper motion specified by the format commands.

3. Hammer Fire - The Hammer Driver is the interface between the Processor CCA and the hammer bank of the printer system. The Hammer Driver CCA, by means of a decoding matrix, enables hammer fire, and, whenever a hammer is activated, sends a signal, HWAFO*, to the printer system signifying that a hammer is activated.

The Hammer Driver CCA (SH 42) has a total of 33 hammer driver ICs capable of driving a total of 66 hammers. These drivers are arranged in an 8 x 9 matrix. The Hammer Driver CCA for the optional 136 print column has a total of 34 hammer driver ICs to drive a total of 68 hammers. See **figure 2-57** for the hammer fire operation.

The signal ODHAMR* loads the data present on the OUTBUS lines 0-7 into the hammer data register. The outputs of the hammer data register form one side of the hammer driver matrix.

The "S" register U39 (SH 43), by means of the signal ODSREG*, is loaded with data bits on the OUTBUS 0 through 3 lines and, through the decoder U38, forms the output for the other side of the hammer driver matrix. The "S" outputs determine which set of hammers can fire.

The Hammer Driver CCA is turned off by the "C" (clear) pulses. The duration of the hammer pulse width is controlled by the flight time header J18 (SH 43).

The signal HD goes to the hammer coil and the other side of the hammer coil goes to +38 volts. The XR1 and XR2 lines attach to ground through a 2 ohm resistor, which together with VCL, controls the current level of the hammer driver.

Upon receipt of the D (data) pulse and the S (set) pulse, the transistor is forward biased and the hammer is activated. The leading edge of the second "C" pulse will turn off the hammer driver.

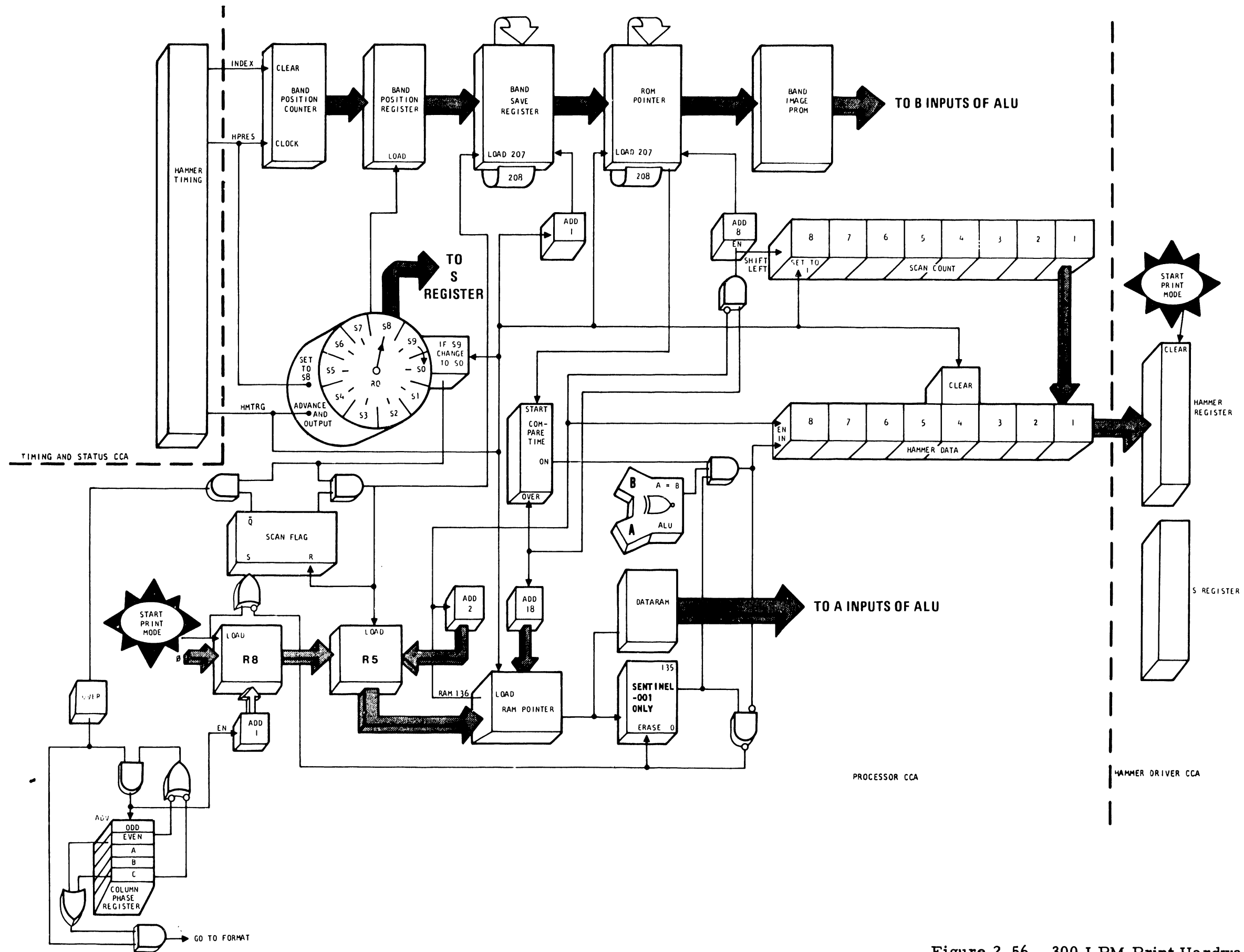
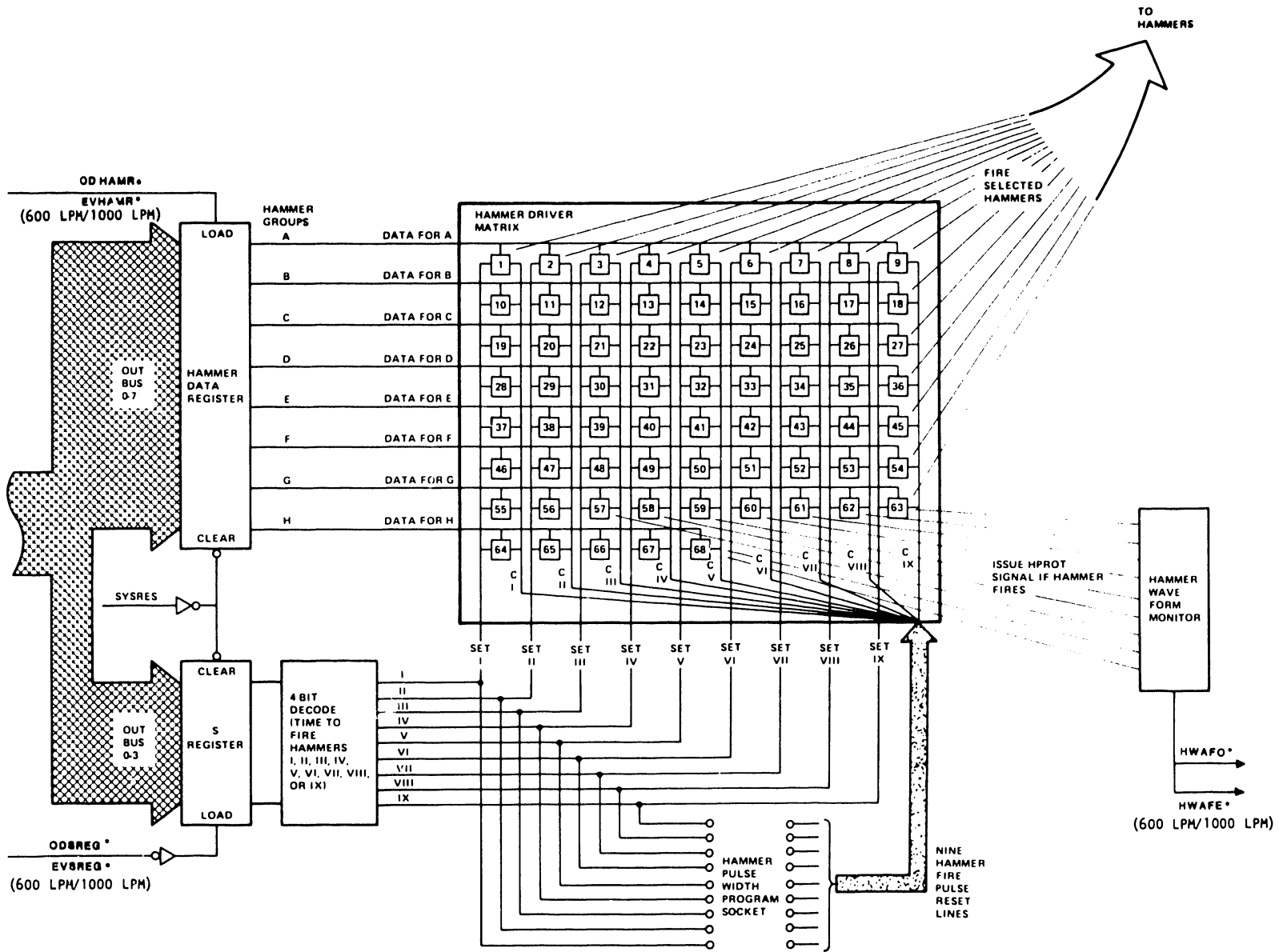


Figure 2-56. 300 LPM Print Hardware Analogy

Figure 2-57. Hammer Fire Operation



NOTE: TWO HAMMER DRIVER BOARDS USED FOR 8600 OPERATION

245059 279

The signal HWAFO* (SH 44) is an analog signal that is an ORed and attenuated combination of all the hammer driver protect circuitry. If a fault condition causes a hammer driver to overheat and go into thermal shutdown, the level of HWAFO* will drop to 0.5 volts. This fault condition is monitored by the Timing and Status CCA and the Processor CCA, and the +38 volts is turned off.

b. 600 LPM and 1000 LPM Print Subsystem

The 600 LPM and 1000 LPM printer has a hammer bank consisting of 136 hammers which can be wired for 132 or 136 print capability. Each hammer is single column-spanning; that is, each hammer prints in one column only as compared to the 300 LPM printer double column-spanning hammer.

NOTE

Compressed font is not available on the 600 LPM or 1000 LPM printers.

There is no column phase advancement necessary. Hammer timing is set to one phase, odd, and supplies a hammer trigger every one-ninth of a character clock. Therefore, there is no need for odd and even phase print sub-steps.

600 LPM and 1000 LPM hammers are narrower than the 300 LPM hammers and allow the band characters to be spaced closer together. Therefore, every ninth hammer still aligns with every eighth band character.

There are two Hammer Driver CCAs in the 600 LPM and 1000 LPM printers. The odd Hammer Driver CCA is nearest to the front of the printer and drives all the odd numbered hammers. The even Hammer Driver CCA is closest to the rear of the printer and drives all the even numbered hammers.

1. Hammer Timing - Timing marks on the character band provide the information to the hammer timing circuitry so that the hammers can be triggered at precisely the right time. There is one (1) mark per character on the character band. An extra mark, called an index mark is used to identify the beginning of a character set. Additional marks are inserted after the index mark as identifiers for the various character sets.

A magnetic reluctance pickup (transducer) senses the character band timing marks and produces an output that is amplified and squared by the Timing and Status CCA (SH 32). This digitized output becomes the base for the character clock circuitry and determines hammer timing and firing. The COPIES and PHASE controls on the control panel are used to vary the hammer driver current and timing when multi-part paper is used.

2. Compare - With a one-to-one hammer to print column relationship, the odd and even columns that align can both be printed. Two clocks located in the Processor CCA working registers are used to keep track of the odd and even Hammer Driver CCAs and the set number for the first and second aligning columns respectively. **Figure 2-58** illustrates the physical relationship of the band columns and hammers.

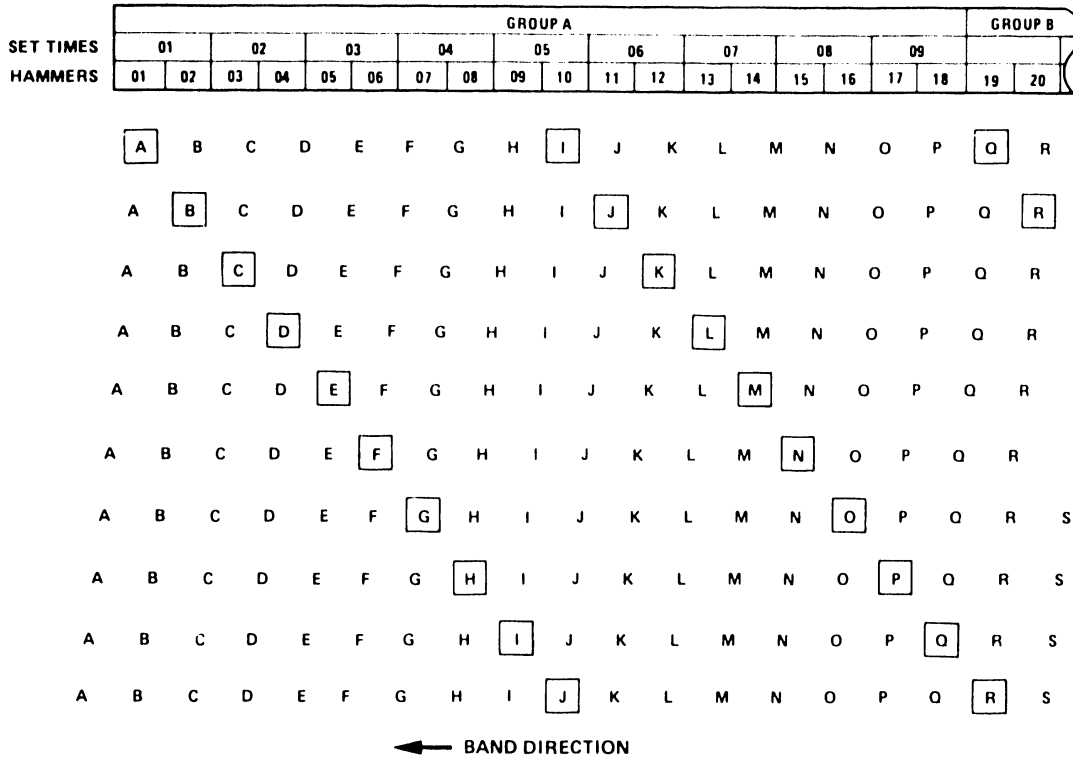


Figure 2-58. 600 LPM and 1000 LPM Physical Relationship of the Band Column and Hammer

The band image PROMs, MEM6, MEM7, and MEM8 (**SH 31**) or MEM13, MEM14, and MEM15 (**SH A30**), contain the characters that correspond to the characters on the band. The data RAM circuitry on the Processor CCA (**SH 28 or SH A28**) stores print column data.

The comparison from the ALU, of the band image PROM and the data RAM is stored in Processor CCA working registers. One data register receives the compare of the first aligning print column, and a second data register receives the compare of the second aligning print column. They will alternately receive compares for the maximum number of print columns allowed. The average number of compares is limited to ten (10) so as to prevent band drag due to hammer impact and to optimize print quality.

3. Hammer Fire - The contents of the Processor CCA working registers that received the compare data are transferred to the Hammer Data Registers U40 and U41 (SH 42). The Hammer Driver CCA, by means of a decoding matrix, enables hammer fire. Whenever a hammer is activated, the signal HWAFO* is sent if from the odd Hammer Driver CCA. HWAFF* is sent if the even Hammer Driver CCA activated the hammer.

Figure 2-60 illustrates the 600 LPM and 1000 LPM print operation and hardware. Note that a thermal shut-down of a hammer driver will cause a HPROT signal and also activate the HWAFO* and HWAFF* signals.

2.4.4 Power Subsystem

The 300 LPM and 600 LPM printer power subsystem can function with either the standard 115 VAC, 60 Hz power supply or the optional universal power supply. The 1000 LPM uses only the universal power supply.

Either power supply combined with the Power Board CCA can provide the system voltages and current necessary for operating the circuit card assemblies, the character band/ribbon drive subsystem, the paper clamp/paper feed subsystem and the print subsystem.

The universal power supply is configured to operate with nominal inputs of 115/230 VAC and 50/60 Hz. Both the standard and the universal power supplies utilize a constant voltage transformer which allows for a wide range of AC input voltages without the necessity of intermediate voltage primary taps. **Figure 2-59** provides a block diagram of the major components involved in the power subsystem.

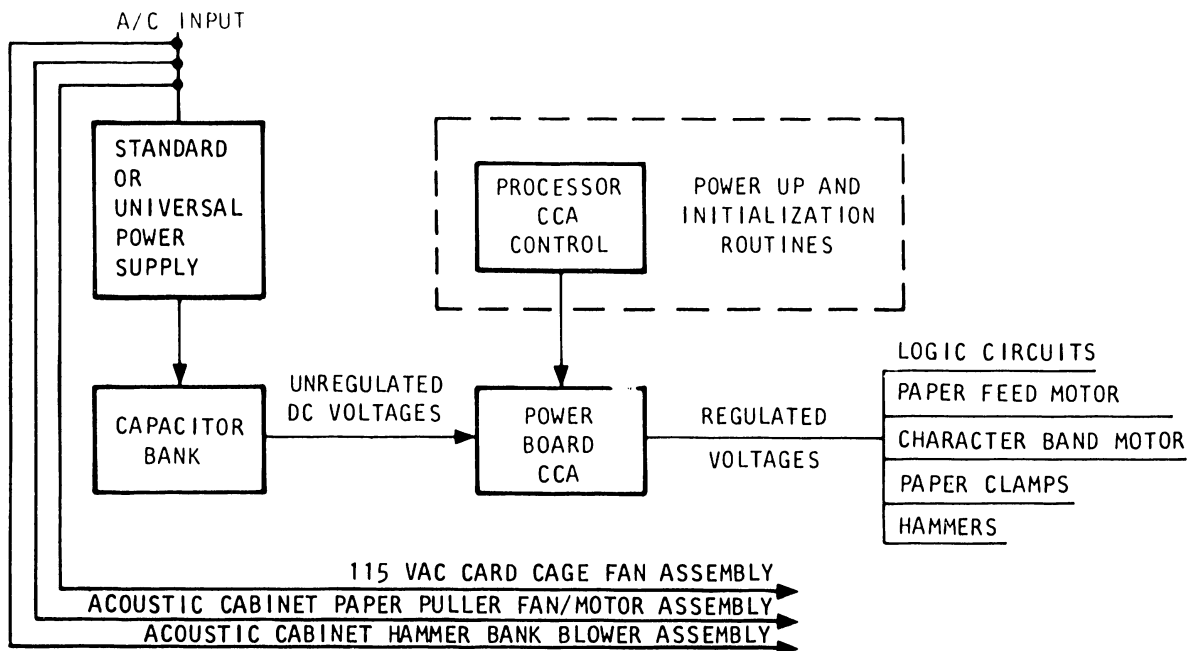


Figure 2-59. Power Subsystem Block Diagram

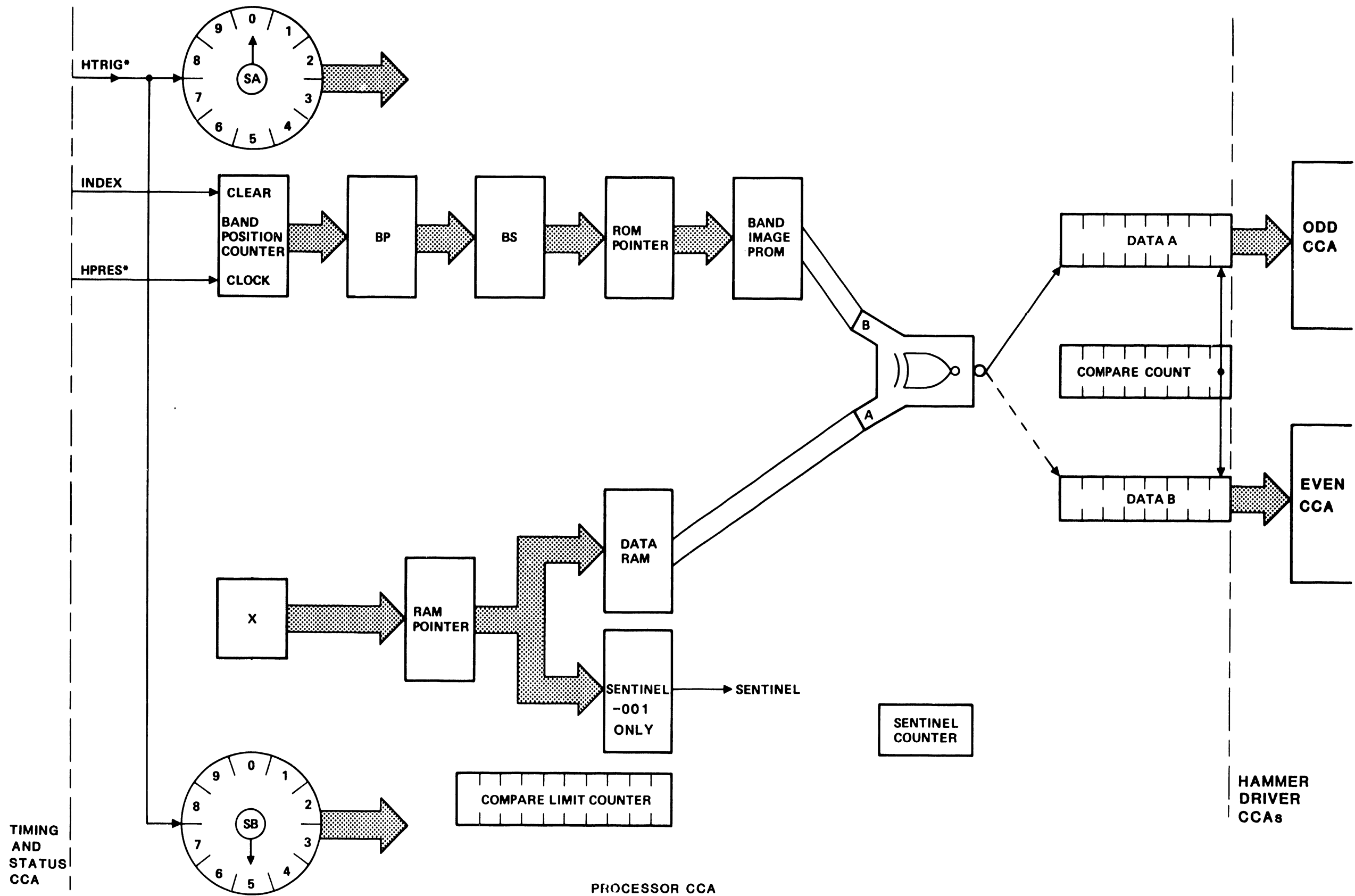


Figure 2-60. 600 LPM and 1000 LPM Print Analog

The following voltages are presented at the outputs of both the standard and universal power supplies:

- Raw +38V - Used by the voltage regulators in the Power Board CCA to produce regulated +12V, the +6.2V reference, and VCL.
- +38V - Used for the Hammer Driver CCAs, paper clamps, stepper motor and band drive.
- +9V - Used for the stepper motor and +5V regulator circuits.
- -9V - Used for miscellaneous analog applications.
- +9VEW - Used during power sequencing to signal the presence or loss of AC power to the printer.

In addition, the universal power supply is configured with a 38V regulator, different plug-in combinations for operation at 50/60 cycles and 115/230 volts, and a second thermal circuit breaker.

For both power supplies, overload protection is provided by the use of thermal circuit breakers and the following fuses:

- F1 - +38 volt protection at 12 Amp.
- F2 - -9 volt protection at 2 Amp.
- F3 - +9 volt protection at 20 Amp.

The following paragraphs describe the two (2) types of power supplies installed in 300 LPM and 600 LPM printers in the standard cabinet. The 1000 LPM printer uses only the universal power supply. Since a printer installed in the acoustic cabinet requires some differences in components, for example a Circuit Breaker/Switch Assembly, these alternatives will also be noted.

a. 115 VAC, 60 Hz Power Supply

The 155 VAC, 60 Hz power supply input is 90 VAC to 127 VAC at 60 ± 1.0 Hz. The input is applied through switch A10S1, circuit breaker A9CB1, and connectors P1, P6, P2, and P4 to the primary winding of constant voltage transformer (CVT) T1 (SH 50). In 300 LPM and 600 LPM printers installed in the acoustic cabinet, power is input through A27J1, A27CB1, and connectors P1, P6, P2, and P4 (SH A50). The input may also be passed through the optional line filter A9FL1.

One leg of the AC line (SH 51) from J1-1 is routed through plug J6-3 and J6-9, and then through J2-4 and J2-3. These interlocks ensure that the preload resistor A9R1, which improves supply regulation under light loads, and the fan motor are plugged in before AC power can be supplied to the primary winding of transformer A9T1.

A separate transformer winding connected to a four-microfarad capacitor, A9C1, provides the components necessary for correct functioning of the resonant transformer. The transformer's center-tapped secondary windings plug into the Rectifier CCA through connector P5. The two secondary windings present the AC voltages to the rectifiers.

Full wave rectifier CR1 provides the RAW +38 volts to the supply output connector J7-1 and J7-3 (SH 52). The +38 volts output is derived the same way, but is fed via F1 to J7-4 and J7-6.

Full wave rectifier CR2 provides the -9 volts through to J7-13 and the 9 volt early warning level through R1 to J7-15. F2 supplies protection to the -9V circuitry, and R1 limits excessive 9VEW current.

Full wave rectifier CR3 supplies +9 volts through F3 to J7-7 and J7-10. The 82 ohm resistor R2 acts as a bleeder resistor for the +9 volt filter capacitors.

The RAW +38V and +9V are connected by plug J7 to the Capacitor Bank Assembly (SH 57). Two 83,000 microfarad filter capacitors, C1 and C4, are connected in parallel for the +9 volt supply; and a 41,000 microfarad capacitor, C2, is used for +38V. A 27,000 microfarad capacitor, C3, is used for raw +38V.

The 600 LPM and 1000 LPM printers use an Auxiliary Capacitor Bank Assembly containing an additional 41,000 microfarad capacitor, C5, in parallel with C2 for the +38V supply and a 27,000 microfarad capacitor, C6, in parallel with C3 for the RAW +38V supply.

Connector J8 is provided to allow installation of the optional logic-to-frame ground connection. Figure 2-61 is a block diagram of the 115 VAC, 60 Hz power supply.

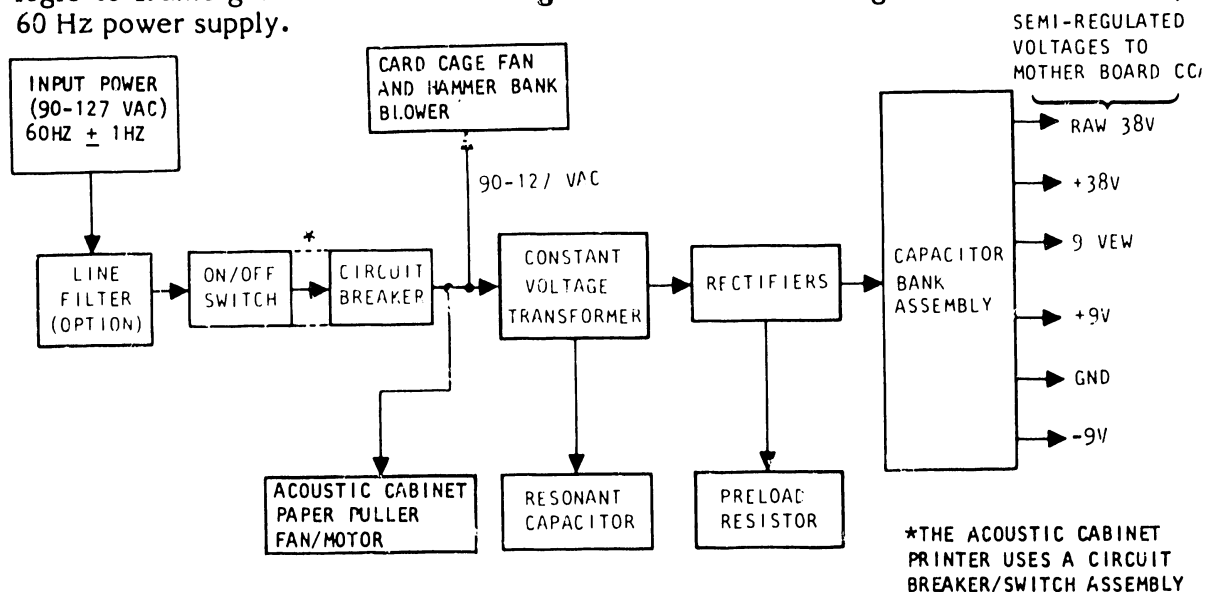


Figure 2-61. 115 VAC, 60 Hz Power Supply Block Diagram

b. Universal Power Supply

The optional universal power supply (SH 53 and SH 54) operates with an AC input of 90 VAC to 132 VAC or 180 VAC to 230 VAC at 50 ± 2 Hz or 60 ± 2 Hz. Voltage and frequency options are obtained by inserting transformer plugs P4, P5, and P9 into the appropriate connectors as shown in table 2-50.

TABLE 2-50. INPUT VOLTAGE AND FREQUENCY CONFIGURATIONS

Transformer Plug/Jack Configuration				
Input Voltage VAC	Input Frequency ± 2 Hz	Transformer Plugs		
		P4	P5	P9
90 - 132	50 Hz	J4A	J5A	J9A
180 - 230	50 Hz	J4B	J5A	J9A
90 - 132	60 Hz	J4A	J5B	J9B
180 - 230	60 Hz	J4B	J4B	J9B

The Paper Puller Assembly in acoustic cabinet printers with the universal power supply must be wired to be compatible with voltage and frequency combinations of the transformer. Figure 6-66 in section VI of volume II provides the wiring diagrams for the paper puler motor.

Figure 2-62 is a block diagram showing the major components of the universal power supply. Basic operation follows that of the standard power supply with the added requirement of a low frequency switching regulator located on the universal Rectifier CCA. The low frequency switching regulator is provided to stabilize the +38 volt output because a ± 2 Hz frequency variation (58 Hz to 62 Hz or 48 Hz to 52 Hz) applied to the ferro-resonant transformer, A9T1, produces more output variation than the printer's 38V circuits can tolerate.

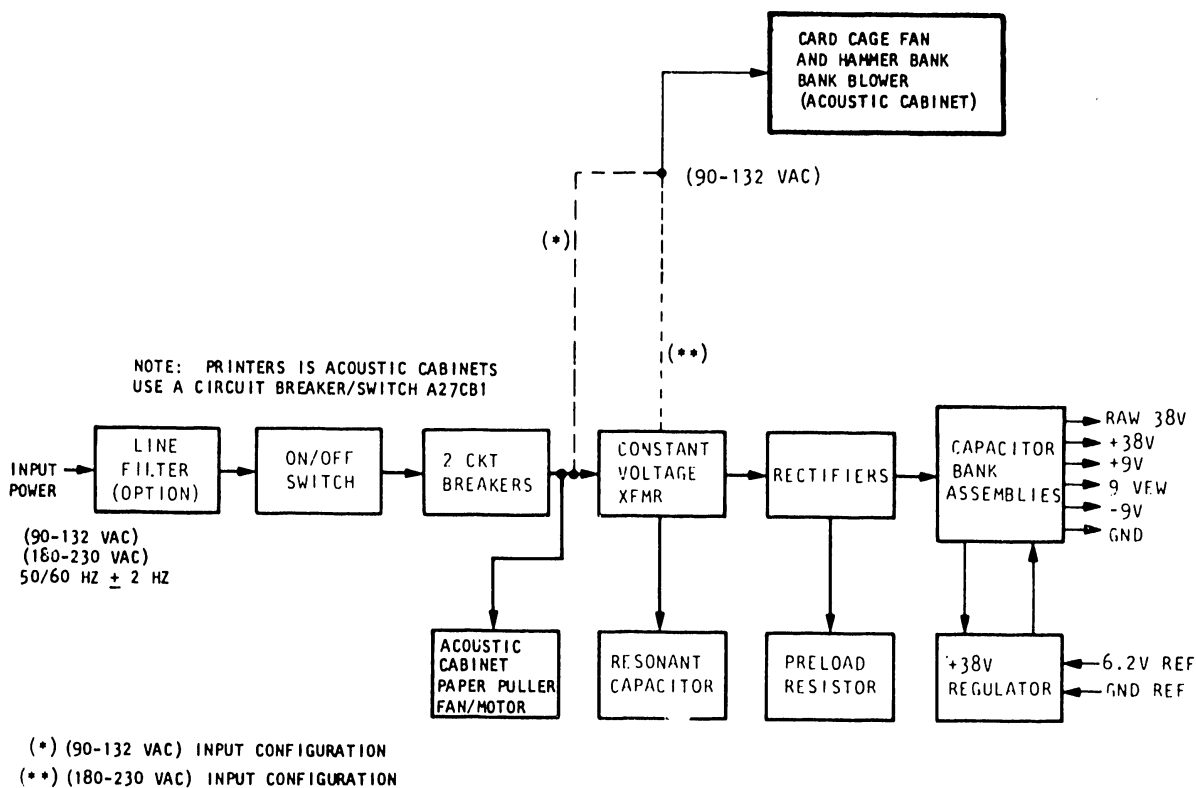


Figure 2-62. Universal Power Supply Block Diagram (Optional)

1. +38 Volt Regulator - The regulator (as shown in **figure 2-63 and SH 56**) converts a 44V to 60V RAW +38 volt source to a regulated +38 volts that is controlled by a 6.2 volt reference supplied from the Power Board CCA (**SH 38**). The +38 volt output, through a resistor-divider network consisting of R10, R22, R31, and R38, is dropped to 6.2 volts and fed to comparator U1-6. This condition is compared with the 6.2 volt reference at U1-7 and will keep U1-1 at a low level.

The +38 volt output is maintained at approximately +38.2 volts at R38. When +38 volts becomes less than about 38.1 volts, U1-6 becomes more negative than U1-7, causing U1-1 to go high. This condition also back-biases CR8 and turns on transistor Q5. Q5 then turns on Q7, allowing current to flow through inductor L1.

The current path is via the R14 current-sensing resistor, Q7 switching transistor, and inductor L1. When the current through R14 reaches approximately 6 amps, transistor Q1 turns on, driving comparator U1-6 more positive than U1-7. This condition causes U1-1 to go low, turning off Q5 and then Q7 and thereby opening the +38 volt current path.

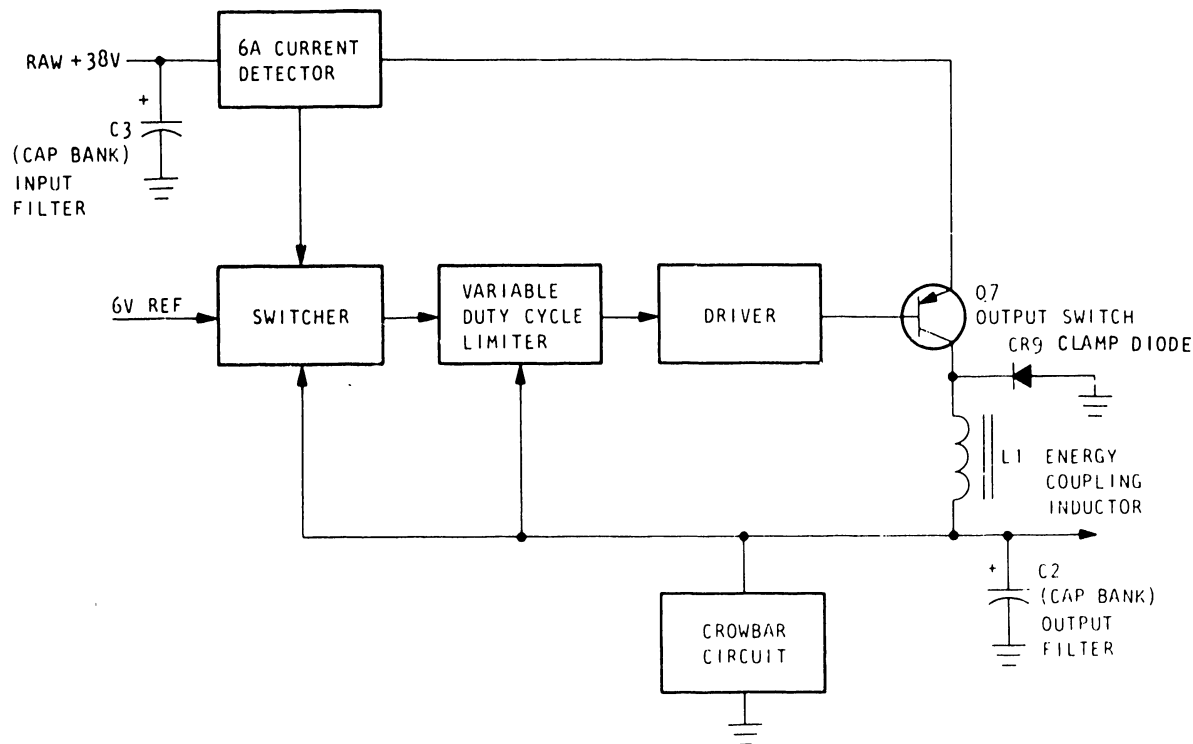


Figure 2-63. +38V Regulator Block Diagram

Inductor L1 will now discharge into filter capacitor C2 of the capacitor bank, and the transistor Q7 collector will be driven negative and clamped at ground by diode CR9. Q1 now turns off, once again making U1-6 more negative than U1-7.

U1-1 now goes high again, turning on Q5 and Q7. This operation will continue, thus creating a self-oscillating switching regulator circuit.

Whenever enough current passes into output filter capacitor C2 to increase its voltage to 38.3 volts, comparator U1-6 becomes more positive than U1-7. This condition causes U1-1 to go low, turning off Q5 and switching transistor Q7. The circuitry will now stay off until the voltage decays to 38.1 volts, at which time the entire process resumes again.

During power up, an overload condition, or whenever the +38 volt output is less than +32 volts, a delay is placed in the switching circuit to limit the regulator duty cycle. To achieve this limitation, U1-8 monitors the +38 volt line.

As long as the voltage is greater than +32 volts, comparator U1-8 will be more positive than U1-9. Therefore U1-14 will be low. When this low is fed to U1-11, its output at U1-13 will be kept low. When comparator U1-13 is low, Q2 is prevented from turning on, thus keeping comparator U1-2 off and disabling the duty cycle limiter.

Once the +38 volt line drops below +32 volts, U1-8 will become more negative than U1-9, placing a high level on Q1-14 and Q1-11. During the regulator cycle, Q1 turns on as soon as the current reaches 6 amps and comparator U1-1 goes low. This condition turns off Q5 and switching transistor Q7 via CR8. U1-10, now more negative than U1-11, outputs a high at U1-13 to the base of Q2, turning it on.

This condition allows capacitor C11 to charge up rapidly, causing comparator U1-4 to be more positive than Q1-5. As a result, a low is output at U1-2 to transistor Q5, preventing it from turning on and inhibiting any regulator action.

As inductor L1 discharges its energy, the +38 volt current starts to drop from 6 amps toward zero. Q1 now turns off, causing U1-1 to go high and, in turn, causing U1-13 to go low and turning off Q2. As soon as C11 discharges to a point where U1-4 becomes more negative than Q1-5, the output at U1-2 will become high. This condition will now allow Q5 and output switch transistor Q7 to turn on and begin a regulator cycle.

2. Protection Circuitry - In the event that the +38 volts should exceed +43 volts, the over-voltage protect crowbar circuit consisting of Q3, Q4, and Q6 is used to discharge the +38 volt line. The circuit is necessary to protect the Hammer Driver CCA circuits from any damage.

Under normal operating conditions, the base of transistor Q3 is kept at approximately +8.2 volts, which is slightly more positive than its emitter, keeping Q3 turned off. When the +38 volt supply reaches a +43 volt level, the base of Q3 becomes more negative than its emitter, turning it on. As a result, Q4 is turned on, turning on Q6. The +38 volt line is then discharged to ground through the current limiting resistor R38.

2.5 FORMAT CONTROL

Format control for B-Series printers is provided by a number of methods. The following paragraphs summarize these methods as they relate to the circuit card assemblies and the mechanical components of the printer.

2.5.1 Configuration Switches

Two (2) to four (4) configuration switches are mounted on the Interface CCAs. The setting of these switches establishes the default format conditions for the printer when other methods of format control are not used. The configuration switches have been discussed in the various interface circuit card assembly descriptions in this section and will not be repeated here. See the Interface CCA description that applies to the circuit card currently installed or desired. See also **logic diagram sheets 8, 11, B8, B11, B17 or 20.**

2.5.2 Control Panel Assembly

Switch S2 (**SH 3**) on the Control Panel Assembly is used to determine horizontal line spacing. The logic level of signal 6LPI* is input to the Interface CCA (**SH 9, B9, or 18**) and sent via the INBUS to the Processor CCA. The Processor CCA uses the 6 LPI* input to develop the phase control for the paper feed stepper motor.

The setting of S2 must be compatible with the setting of the forms length selector switch or a fault condition will occur. The STATUS indicator will display 08 for an undefined form length.

2.5.3 Forms Length Selector Switch (FLSS)

The optional Forms Length Selector Switch Assembly is mounted beneath the Control Panel Assembly and is accessible by opening the printer cover door. It consists of two (2) thumbwheel switches which are set independently of each other. The combined settings define the form length the printer will handle. The maximum form length selectable is 14 inches and the minimum form length is 3 inches.

The forms length select cable is connected to the Interface CCA at J3 (**SH 9**). The coded form size signals FLSEB1-7 (**SH 63**) are input to the FLS PROM MEM1 (**SH 9**). The data is gated onto the INBUS by signal FLSS* derived from the Device Enable Decoder U29 (**SH 7**). This data is then read by the Processor CCA to determine the form size.

If the optional FLS/VFU switch is provided on the FLSS assembly, the form size can be determined by the FLS or by the VFU (TCVFU or DAVFU). Signal FLSSSEL* (**SH 9**), when low, directs the Processor CCA to enable the Device Enable Decoder (U29) to output FLSS* to MEM1.

If VFU is selected, FLSSSEL* goes high, and the Processor CCA looks at the VFU input for form size. Without the FLS switch assembly and VFU options, the form length is decided by setting switch S2-6 on the Interface CCA.

2.5.4 Tape Controlled Vertical Format Unit

The Tape Controlled Vertical Format Unit (TCVFU) consists of an optical paper tape reader, associated electronics, and a VFU program in the firmware of the Processor CCA. The TCVFU allows the user to handle a variety of form lengths up to 144 lines and enables rapid paper slewing within individual forms. The tape reader uses 12 channel paper tape (DpC part number 800958-012), or its equivalent.

The maximum tape length in standard printers is 144 lines (24 inches @ 6 LPI and 18 inches @ 8 LPI). Each tape loop should have only one hole punched in the Channel 1 position to designate Top of Form. Bottom of Form should also be indicated on the tape in either Channel 2, 8, 11, or 12 based on the setting of the configuration switches on the Interface CCA.

In Centronics-Compatible printers, the paper tape used in the TCVFU is 12 channels wide with a maximum length of 126 print lines. Channel 1 on the tape is used for top of form (TOF). Channel 2 is used for vertical tab (VT). Channels 1 and 2 combine for bottom of form (BOF).

Data is read from the tape during a tape read routine and stored in the VFU memory (**SH 11, B11, or 20**). The tape read routine will take place automatically on power up. If no tape loop is installed, a "no tape in reader" condition will appear on the status indicator display. The operator may override this condition by pressing the ON/OFF LINE switch on the control panel.

In such case, the printer will come up to a READY condition with VFU memory not loaded. The standard format configuration set on the configuration switches will be used. The operator may also place a punched tape into the reader and cause the tape to be loaded into the VFU memory by pressing the Tape Read Request switch located on the tape reader head.

The VFU memory load will start when a hole is detected in Channel 1 (Top of Form). Memory load continues until the hole in Channel 1 is detected again. The printer makes a second pass on the tape to compare the information read with the data previously loaded in the VFU memory. If this comparison is successful, then the printer will come up to a READY condition. The tape reader will be turned off, and all mechanical activity will cease.

If the second read does not compare with the data loaded into the VFU memory on the first pass, then the printer will read the tape a third time, loading the data into the VFU memory and writing over the data present from the first pass. A fourth pass through the tape is done to verify the data which was loaded in the third pass. If this read is successful, the printer will come up READY. If the read is unsuccessful, the tape reader will be turned off and the fault condition will appear on the STATUS indicator display.

After the printer has achieved a successful read and compare, and the system is set to READY status, the VFU tape can be changed and re-read by pressing the Tape Read Request switch as long as the printer is off line. The new information will replace what was stored previously in the VFU memory.

Upon completion of a successful tape format load, the printer will generate a check sum word from data stored in the VFU memory. This is done by adding the binary representations of each 6-bit byte (1/2 of a tape line) word. Channels 1 to 6 of line 1 are added to Channels 7 to 12 of line 1 and the result is added to Channels 1 to 6 of line 2, etc. The end result is stored for later use as the check sum word which is used to ensure that no data is lost from the VFU memory and the form positions are correct.

TCVFU instructions are transmitted to the printer from the user system by activating the Paper Instruction (PI) line on the Interface CCA when the printer is on line. (Centronics-Compatible printers do not use the PI line in TCVFU operations.) The activation of the PI line is controlled by switch S1-7 on the Interface CCA.

As paper is advanced, a "current line" count is incremented in synchronization with the paper. This operation is similar to a rotating tape loop in a purely mechanical system. The advantage of the programmed TCVFU is the lack of mechanical motion in the tape reader during paper motion. Printers equipped with the TCVFU option may also be operated in the DAVFU mode described in **paragraph 2.5.5.**

2.5.5 Direct Access Vertical Format Unit

The Direct Access Vertical Format Unit (DAVFU) consists of a VFU program in the firmware of the Processor CCA and a VFU memory. The standard DAVFU allows the user to handle a variety of form lengths up to 143 lines and enables rapid paper slewing within the individual forms. The DAVFU, a standard feature in Centronics-Compatible printers, is limited to 126 lines. Instead of loading the VFU memory (**SH 11, B11, or 20**) from a tape loop as with the TCVFU, the DAVFU provides for direct loading from the user controller via the printer interface lines.

To start the DAVFU load, a Start Code of Hex 6E with Paper Instruction (PI) high is applied at the Interface CCA data lines. The printer will enter the DAVFU load routine, and all data transferred after the Start Code will be interpreted as tape Channels 1 through 6 of the first line, using data bits 1 through 6. The next byte transferred will be used for tape Channels 7 through 12. The next byte transferred will be Channels 1 through 6 of the second line, etc.

The data transfer will continue until the printer sees a Stop Code of Hex 6F with PI high. If the PI bit is high during the DAVFU load routine, the tape channel data must not look like a Start or Stop Code or it will be interpreted as such by the printer.

In Centronics-Compatible printers, the DAVFU Start Code is Hex 1D and the Stop Code is 1E. The number of tape data words is limited to 126 or 252 bytes. Instead of using a high PI line, data bit 7 must be high.

While in the DAVFU load routine, the receipt of a second Start Code will cause the next byte of data to be loaded into the first location of the VFU memory, allowing the user to restart the DAVFU load routine from the beginning.

Should the user system send a buffer clear signal to the printer during the DAVFU load routine, all format data and character data stored in the printer buffer will be cleared and the printer will return to the beginning of a normal data load routine.

In Centronics-Compatible configured printers, an INPUT/PRIME* signal will clear the printer buffer and return the printer to the idle routine. In idle, it will respond only to a user Select code or to the ON/OFF LINE switch.

The DAVFU interprets a "one" bit in Channel 1 as a Top of Form (TOF) indication. When the DAVFU memory load is finished, the first line loaded into the memory is assigned to the line on the form present at the print station. Therefore, it is suggested that, for ease of VFU memory-to-paper alignment, the user should provide the TOF indication in the first line of format memory data.

If the user system sends a DAVFU Stop Code during a character data load routine, and the VFU memory is loaded, the format memory will be recirculated to the beginning of the memory as previously loaded. The TOF and other channel locations will be reoriented with respect to the paper position currently at the print station.

The DAVFU load format requires two (2) data bytes per line transferred from the user system. If a DAVFU Stop Code is received at the Interface CCA after the first byte of the required two (2) byte transfer, the appropriate fault status number will be stored, and a carriage return simulated to print any data in buffer. The printer will go off line and not ready, and display the fault number on the STATUS indicator display.

If the user system attempts to send more than 143, or 126 in the Centronics-Compatible, format data words (286 data bytes or 252 data bytes), the printer will go into the fault routine.

Upon receiving the DAVFU Stop Code, the printer will generate a check sum word from data stored in the format memory. The check sum word is the sum of the binary representations of each 6-bit byte stored in the format memory. After the check sum word is stored in the registers, the printer will return to the normal load routine. All other operations of the DAVFU including step count and tape channel search are the same as for the TCVFU.

The various Interface CCAs have several configuration switches which will enable the user to select a variety of TCVFU format configurations. The switches are described in the Interface CCA descriptions in **paragraph 2.3.1**. Tape and data load formats can be found in the appropriate Maintenance Guide.

2.6 PROGRAM DESCRIPTION

PROMs, installed on the Processor CCA, furnish the master program that directs printer operation. As an aid to understanding printer operation, a program overview is provided in this section. The program is divided into nine (9) major functional routines and subroutines, and the purpose and tasks of each is described. Since there are variations in programs between the 20-bit and the 24-bit processors, the routines for each are described separately when necessary. Under each routine heading, whenever the routine is the same, the 24-bit processor description will

indicate this and start with the instruction that varies. Flow charts are also included. Dotted lines on the flow charts indicate the optional VFU operations. The following routines are described in sequence for each of the two (2) Processor CCAs:

- Initialization Routine
- Start Motor Routine
- Idle Routine
- Load Routine
- Self Test Routine
- Edit Routine
- Print Routine
- Format and Move Paper Routine
- System Status Check Routine

Figure 2-64 is a flow chart of the program overview to help place the routines in sequence.

2.6.1 Initialization Routine

To begin operation, the Processor CCA tests the printer system for the following required conditions:

1. Voltages at proper levels
2. Switches in proper settings
3. Band motor up to correct speed
4. Paper form size recorded
5. Character density verified
6. Character band identified
7. Interlocks closed
8. Timing signals generated

All these tests are made as part of the initialization routine and start motor subroutine. Initialization begins when the printer's POWER switch is set to ON or when the operator presses the ALARM/CLEAR switch. The processor-module program counter is set to address zero, and the program begins with the

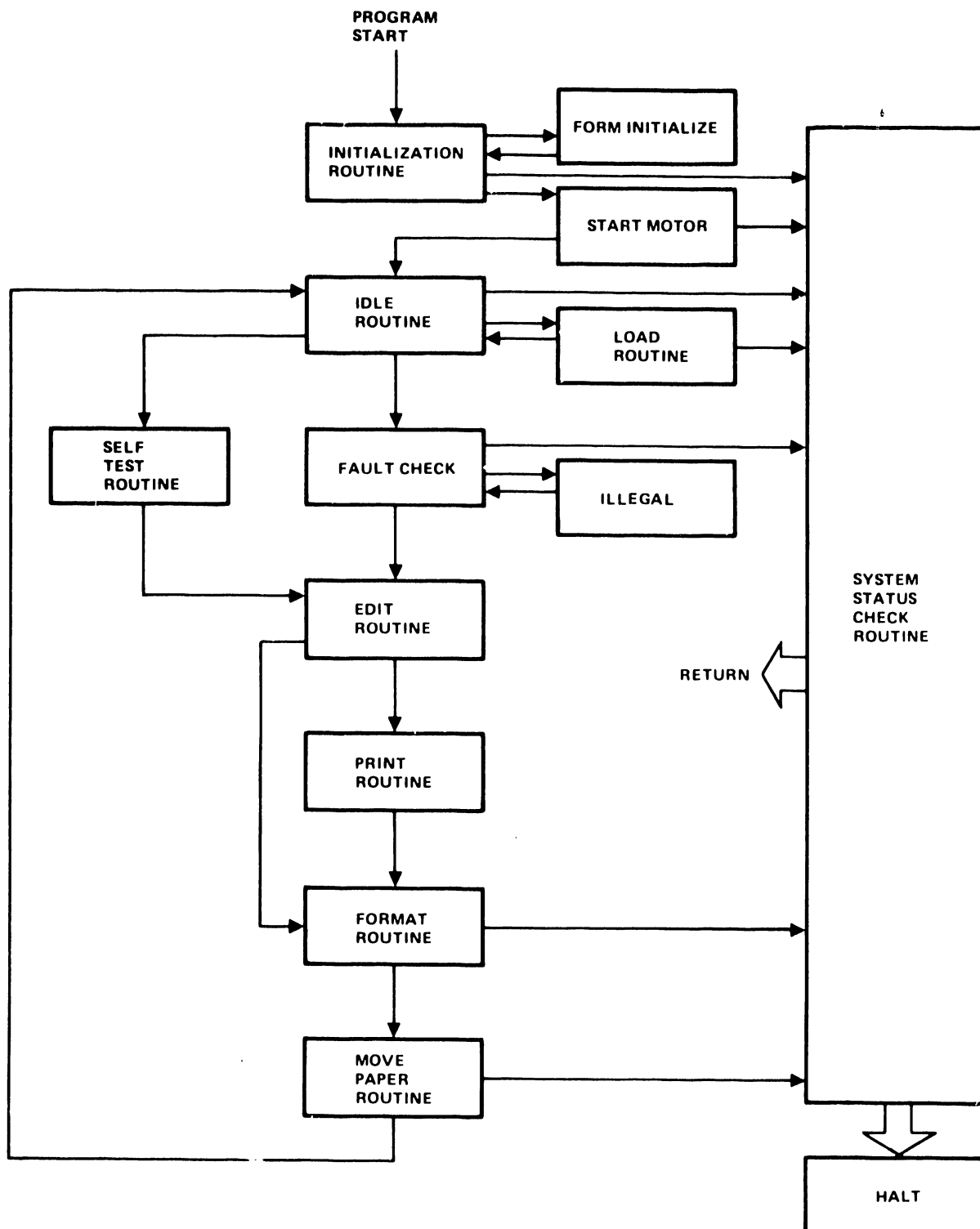


Figure 2-64. Program Overview

instruction sequences described below. **Figures 2-65 and 2-66** illustrate the initialization instruction sequence of the 20-bit Processor CCA and the 24-bit Processor CCA.

a. 20-Bit Processor CCA

1. Stabilization Delays - A first stabilization delay of one-half second allows time for voltages and logic to stabilize at their required levels and for processor registers and fault latches to clear. After a second delay of 55 microseconds, the processor executes voltage checks.

2. Voltage Checks - The processor tests secondary voltages to determine if they are at the required levels. If any of these is not OK, the program branches to the system status check routine and the related fault code appears on the control panel STATUS display indicator. The operator must set the POWER switch to OFF then ON to try to clear the fault. If voltage checks are OK, the program moves to store paper format information. The 24-bit processor program moves first to check the master clear switch flip-flop.

3. Format Setup

This operation follows the form initialize subroutine to determine the requirements for the paper format. The program checks the printer for the following:

- Optional TCVFU or DAVFU
- Optional FLS switch
- Default form length of 11 or 12 inches
- Skipover
- 6LPI or 8LPI
- VFU Special Format (Interface CCA Configuration Switches S3 and S4)

4. VFU RAMs Check OK? - If the printer is configured with the VFU option, the routine will execute a check of the VFU RAMs to ensure the validity of data read during user loading or tape loading of the RAMs.

5. Set Column to ODD (300 LPM Only) - The printer prints in odd columns first and then switches to print in even columns. This subroutine sets the printer to print in the odd columns first.

6. Column (300 LPM Only) - The column setup routine is called in here. The program will determine if there is a character-to-hammer alignment in the next odd print column.

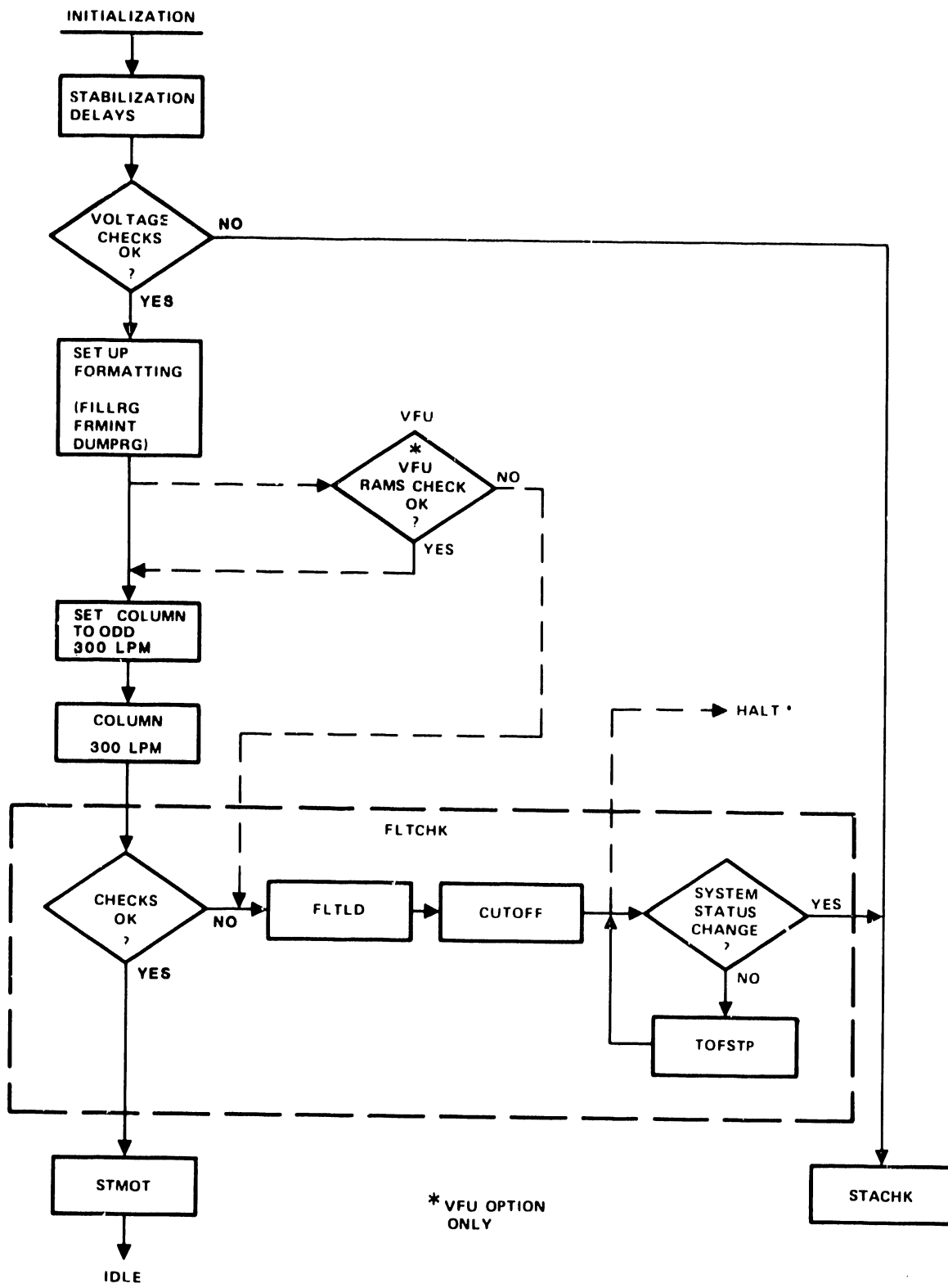


Figure 2-65. 20-Bit Processor CCA Intialization Routine

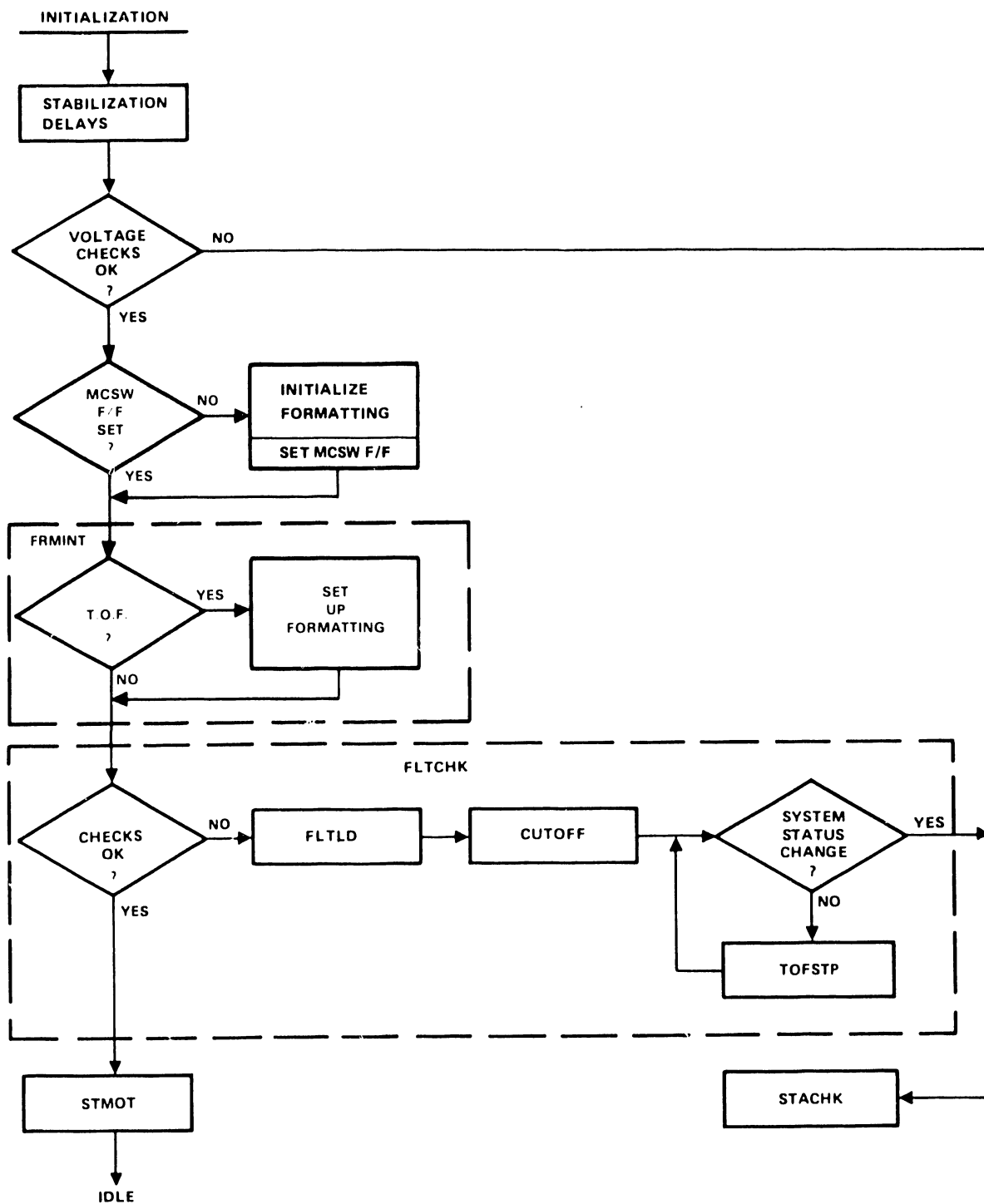


Figure 2-66. 24-Bit Processor CCA Initialization Routine

7. Fault Checks (FLTCHK) - The program proceeds to test the following for soft faults which are operator-correctable:

- Interlock switches closed
- Character band tensioned and band cover closed
- Print inhibit switch off
- Paper loaded

If a soft fault is found, the program shifts to load the fault code on the STATUS indicator and then calls for the cutoff subroutine. In this subroutine, the program goes off line, resets the READ? line, stops the character band, releases the paper clamps, and disables the hammer voltage supply (+38 volt).

NOTE

Not all the cutoff subroutine procedures may occur at this time.

Then the program proceeds to loop while waiting for a system status change or for the operator to actuate the PAPER STEP switch or TOP OF FORM switch. If there is no change in status, the operator will have to master-clear the printer and reset the program to zero to escape the "TOFSTP/System Status Change?" loop.

b. 24-Bit Processor CCA

The program sequence for the 24-bit Processor CCA moves through the Stabilization Delay and the Voltage checks and then moves to the Master Clear Switch Flip-Flop check. See **figure 2-66** for the routine flow chart.

1. Master-Clear-Switch Flip-Flop Set? - If the MCSW Flip-Flop is set (the ALARM/CLEAR switch has been pressed), the initialization routine restores to the format registers data from earlier printing. The processor moves format counts for current line, form size, carriage returns, and also VFU data from storage in RAM to the working registers.

If the MCSW Flip-Flop is not set, the processor clears its format count registers, status registers, and flag registers, and sets the MCSW Flip-Flop. The program then calls the FRMINT subroutine.

2. T.O.F.? - The processor checks for the current line count, and, if the paper position is "Top of Form," updates format data according to switch settings: 6 or 8 LPI, form length, skipover count, bottom-of-form count. It tests for the availability of VFU and FLSS format-control units and, if these are in use, updates format counts from their input.

If the form is not in its top position, the processor checks if FLSS or VFU units are installed and, if so, updates the related format counts. The program then calls the fault check (FLTCHK) subroutine.

3. Checks - The processor tests inputs from the printer system for indication of "soft" faults: activation of an interlock (for example, the hammer bank is not closed), or such conditions as paper low or ribbon motion error. If any of these conditions occurs, the processor interprets the cause, loads the appropriate status code for display on the control panel, and places the system off line.

4. System Status Change? - The processor also checks for "hard" faults (such as improper voltage or current levels) reported on the System Status Change line. In case of a fault condition, the program calls the system status check (STACHK) subroutine to interpret the fault, load the appropriate display, and place the printer off line.

5. TOFSTP? - If there is no hard fault, the processor tests for input signals from the control panel paper-motion switches, top of form and paper step. (The form can be advanced even if the printer is off line because of a soft fault.) If either signal is active, the program branches to a related subroutine to move the form. On return, the processor monitors system status until the detected fault is corrected.

6. STMOT - If the FLTCHK subroutine finds no faults, the program calls the STMOT (Start Motor) subroutine.

2.6.2 Start Motor Routine (STMOT)

If the fault checks (FLTCHK) show no faults, the program calls the band motor startup and band identity subroutine for execution. In the 300 LPM printers with the 20-bit Processor CCA, a check is made of the band identification marks to determine whether a 15 CPI compressed font band is installed. The 1000 LPM 24-bit processor has the added step of loading the illegal RAM. **Figures 2-67 and 2-68** show the Start Motor instruction sequence for both processors.

a. 20-Bit Processor CCA

See **figure 2-67** for the 20-bit processor STMOT flow diagram.

1. Start Band Motor - The processor generates the ENBNDR signal to the Timing and Status CCA, enabling the band drive electronics.

2. Time-Out for Band Acceleration - A half-second delay allows the band to come up to speed. The illegal code RAM is cleared and the "legal data" flag reset.

3. Transducer and Band Speed Check - A further delay allows time for transducer or band drive faults to appear. If these occur, the program branches to the status check routine to interpret the fault and cut off operation.

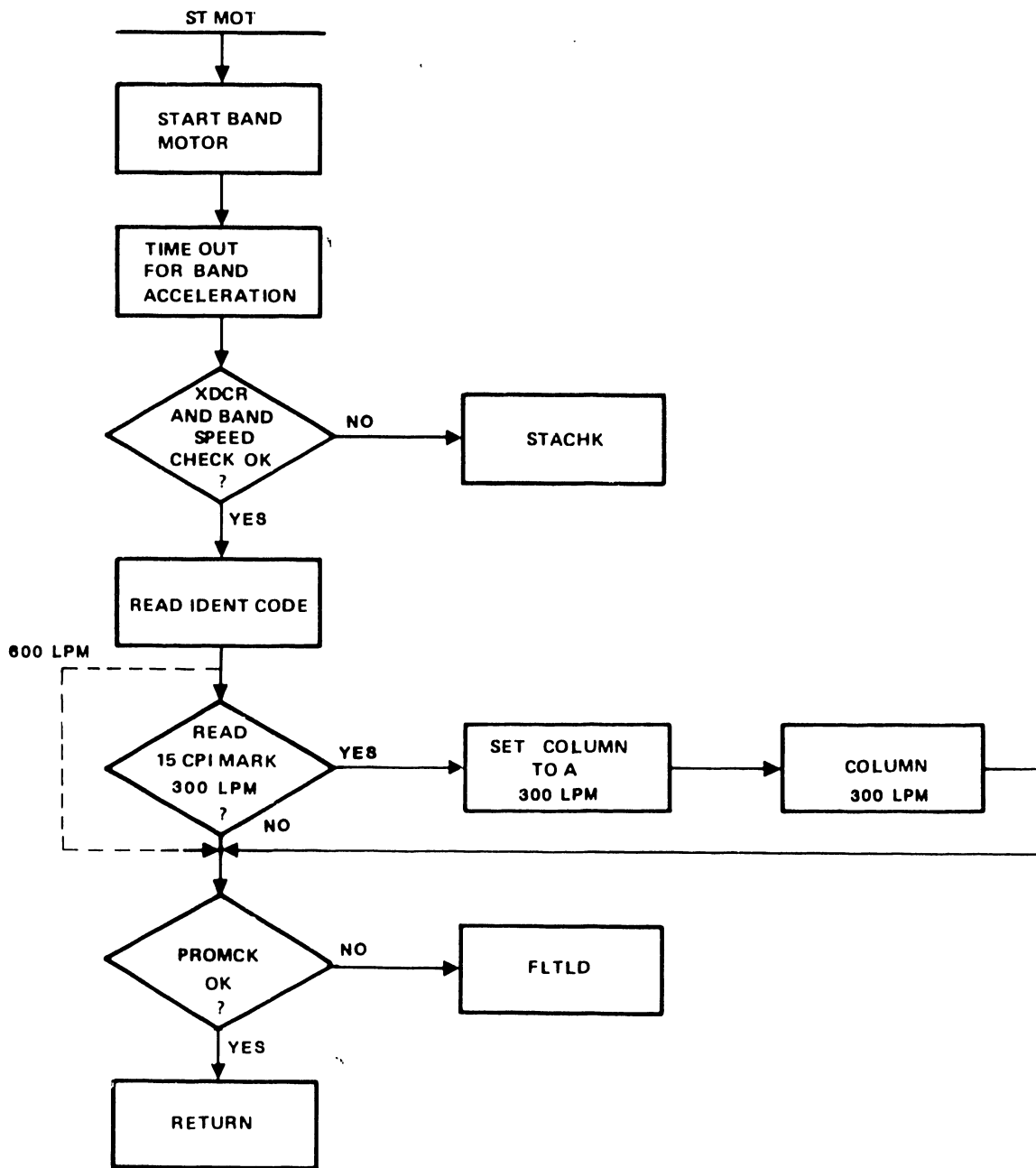


Figure 2-67. 20-Bit Processor Start Motor Routine

4. Read Ident Code - If there is no fault, the processor reads the identification marks from the moving band. If the identification code indicates that a 15 CPI band is installed, the program moves to select column A.

5. PROMCK (PROM Check) - The PROM address pointer is set to the location storing the user band ID code, and each installed band image PROM is enabled in turn. The processor compares the ID code from each PROM with the code read from the band until a match is found. The IDENT0/IDENT1 lines to the user are set to report the band in use. If none of the PROMs matches the band, the program calls the FLTLD (Fault Load) subroutine to display 05 ("Undefined Band Loaded") on the control panel STATUS indicator.

The program then calls for the status check subroutine to look for changes in status which may have occurred during initialization. If there is no change, the program exits to the idle routine.

b. 24-Bit Processor CCA

The Start Motor routine moves through Start Band Motor, Band Acceleration Time Out, Transducer and Band Speed Check, and Read Ident Code. It then executes the PROMCK and, if needed, FLTLD. This is followed by the Load Illegal RAM routine and return.

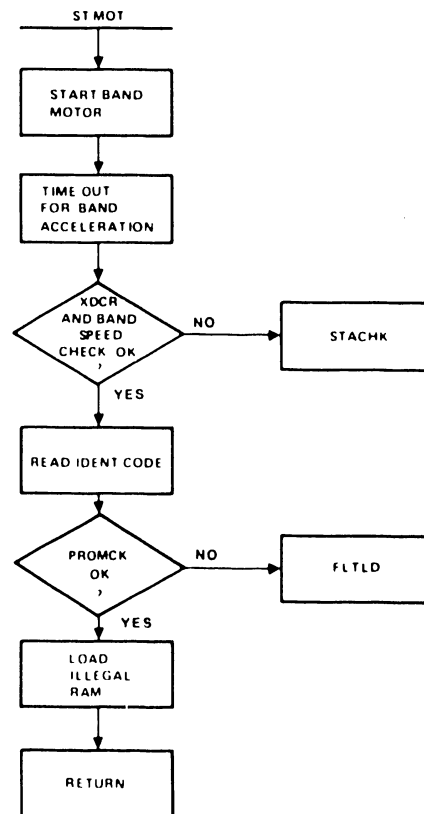


Figure 2-68. 24-Bit Processor Start Motor Routine

1. Load Illegal RAM - The PROM address pointer is set to the beginning of the PROM illegal table, which identifies "illegal" (not printable or executable) data. Using this area's contents as an index, the processor loads the illegal code RAM. A "legal" bit is set in every location that has a corresponding legal designation in the table in the PROM. The remaining "illegal" locations are left at logic 0.

2. Return - On completion, the program returns to the initialization routine and, after several housekeeping operations, exits to the idle routine.

2.6.3 Idle Routine

The function of the idle routine is to wait for operator action in order to go on line, step paper, or move paper to top of form. If there is no on line command, the program will keep cycling in the idle routine. The printer executes the idle routine by performing the following subroutines and instruction sequences. **Figure 2-69** illustrates the idle instruction sequence for both processors.

a. Fault Check (FLTCHK)

The program again calls in the fault check subroutine described in the initialization routine.

b. Set Ready

If no faults are found, the READY line to the user is set. Online can now be enabled.

c. Want to Go Online?

The processor samples the ONLINE switch signal from the printer control panel. If the signal is active, the program branches to the FILLRG subroutine to bring format data from RAM to the working registers and update the form size counts (FRMINT). The processor then samples the TOP OF FORM and PAPER STEP switch signals (subroutine TOFSTP). If either switch has been pressed, the program branches to the format routine to advance paper as required. On completion, the program returns to the idle routine to again await the ONLINE signal and to monitor system status.

If "Want to go Online?" is true, the program moves directly to the instruction sequences that enable it to exit to either the load routine or the self-test routine. It prepares its exit path in the following way.

1. Check Self Test and Print Inhibit Switches - The processor samples signals from the print inhibit and self test switches and also from the paper low switch. If paper is low, a flag register bit is set to allow only single-step advances to the end of the form during subsequent paper motion. The processor also checks for a flag bit indicating that the band has been identified and, if necessary, calls the start motor (STMOT) subroutine to make sure that the band and an installed Band Image PROM are compatible.

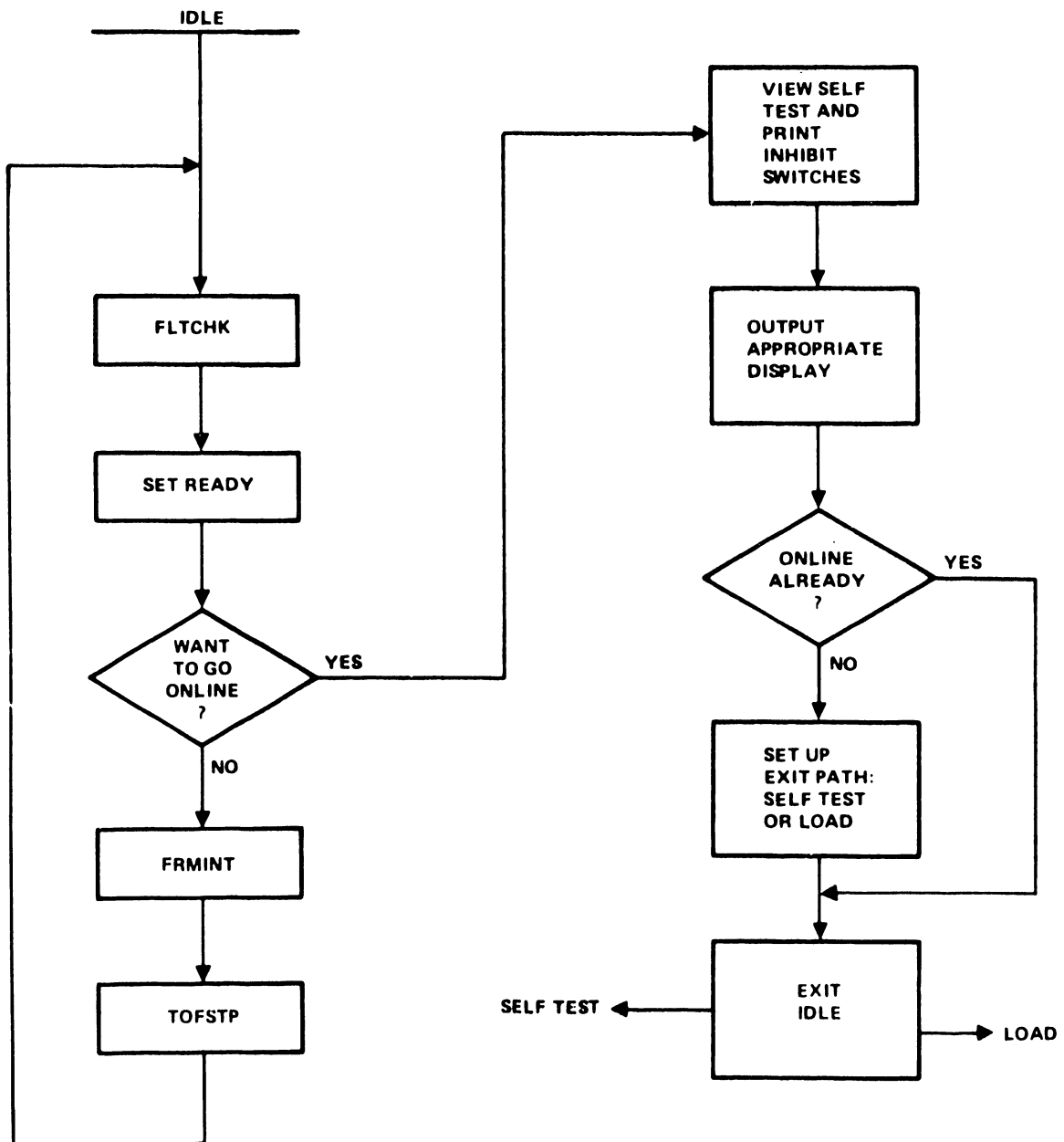


Figure 2-69. 20-Bit and 24-Bit Processor Idle Routine

If the self test switch has been set, the processor loads the appropriate status code for display. If self test was not selected, it loads the display code for "Online."

2. Output Appropriate Display - The code for the selected printer status is displayed on the control panel: 66 (self test with print inhibit), 67 (self test with printed output), or 77 (on line).

3. Online Already? - If the printer is not on line already, the program must set up the branch address for entry to its next routine. If it is already on line, this address has already been loaded in the sequencer address register. The program jumps to this routine.

4. Set Up Exit Path, Self Test or Load - The program loads the sequencer address register (i.e., the stack) with the entry address of the next routine: self test, if the switch has been set, or data load, if the switch has not been set.

5. Exit Idle - The program jumps to the address in the sequencer stack and begins the next routine.

2.6.4 Data Load Routine

On exit from the idle routine, if the printer self test is not activated, the program moves to the user data load routine. In this routine the user's print data are transferred into Processor CCA memory (RAM). In addition, if the printer configuration includes the optional Vertical Format Unit (VFU), the routine loads paper motion instructions into the VFU data portions of the processor RAM. Transfer of data follows the "handshake" protocol described in **paragraph 2.2**. Data is input during the user data load routine according to the following instruction sequences.

a. 20-Bit Processor CCA

Figure 2-70 illustrates the following instruction sequence for the 20-Bit Processor CCA.

1. Data Transfer/Increment RAM Pointer - A printer demand is raised, data is transmitted, and at the user STROBE signal time, data is transferred into the user data latch. The data is then moved on the RGBUS and inserted into the printer memory (RAM). With completion of the data transfer (DEMAND is reset), the RAM pointer is incremented to indicate the next memory address location for the next incoming data character.

2. Stop I/O? - While the last character sent is still in the user data latch, on the RGBUS, or in a RAM location, the data is checked to see if an interrupt of the current data transfer is needed. The conditions which would require an interruption of the current data transfer and begin the illegal subroutine are:

(a) BUFCLR (Buffer Clear) - BUFCLR will cause the program to clear the RAM address pointer and begin the load sequence again at the zero position of the RAM.

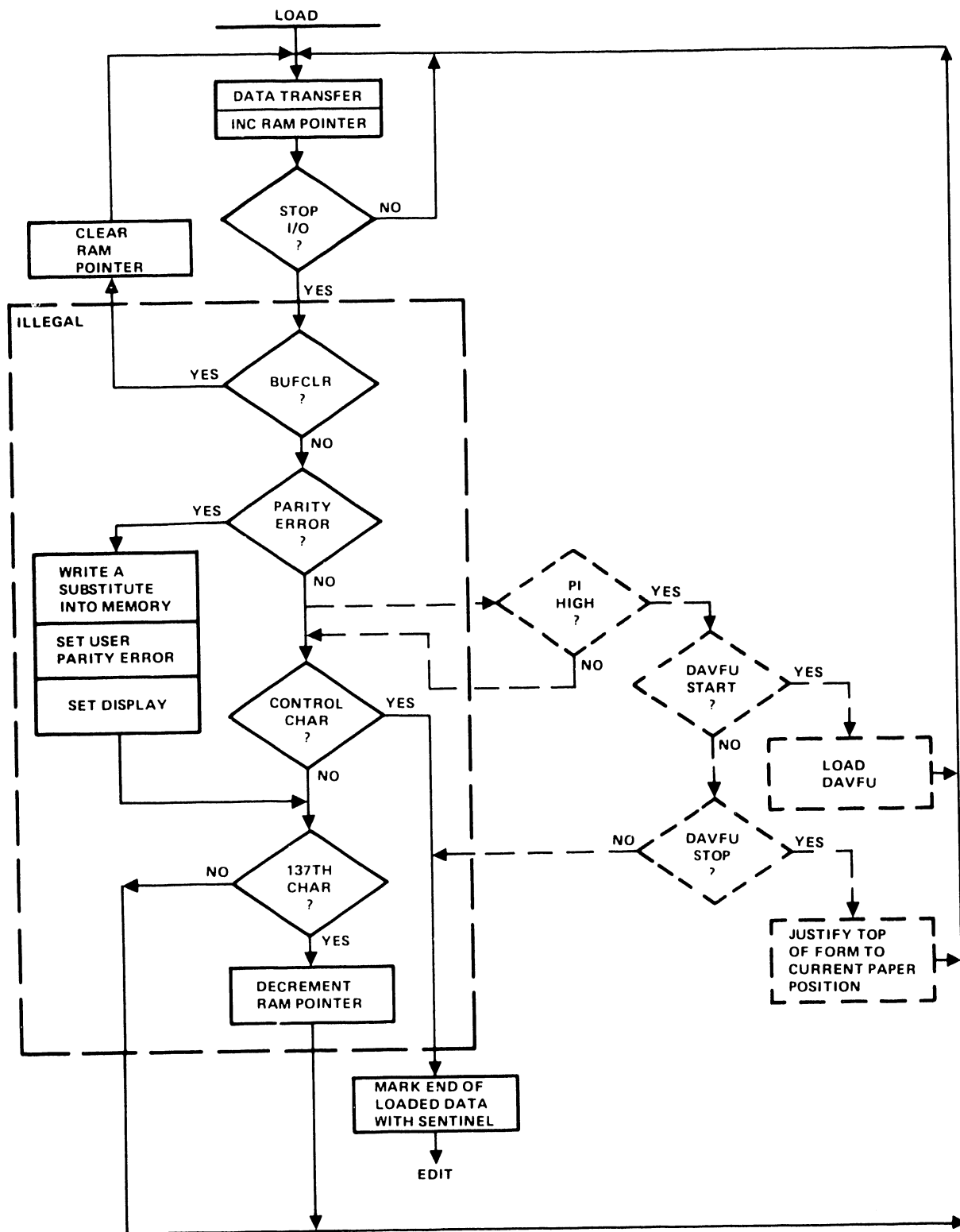


Figure 2-70. 20-Bit Processor Load Data Routine

(b) Parity Error - The transmitted data character is checked for parity and has an error. The illegal subroutine instructs the printer to write a substitute character in RAM (usually a space code stored in the band image PROM). A parity error signal (PARERR) is sent to the user, and the STATUS indicator is set to display parity error status code 23.

The illegal subroutine will then proceed to test for the "137th character" condition. If the parity error check reveals no error in the data transmission, the program sequences to check for a format code.

(c) DAVFU Subroutines - Beginning with "PI High?," the following routines are exercised if the printer is configured with the optional DAVFU.

(1) PI High? - The program checks for a user-transmitted paper instruction (PI). If PI is low, the routine returns to the non-DAVFU segments of the program beginning with "Control Character?". If PI is high, the routine moves to the next DAVFU instruction.

(2) DAVFU Start? - The routine will look for a start code to begin the DAVFU data load. If yes, the routine will proceed to DAVFU data load. If no, the routine will ask if the DAVFU data load has been terminated with a stop code.

(3) DAVFU Stop? - If the stop code has been transmitted, the routine will move to Justify the Paper Top-Of-Form with the current paper position determined by a check sum word stored in the VFU RAM. If there is no stop code, the DAVFU load data sequence is considered done, and the routine will move to Mark End Of Loaded Data With Sentinel or to the edit routine when the sentinel signal is not used.

(4) Load DAVFU - DAVFU data from the user will be loaded into the VFU RAMs. The low VFU RAM will be loaded with the first byte for channels 1 to 6, and the high VFU RAM will be loaded with the second byte for channels 7 to 12.

(d) Control Character? - The reading of a format control character (LF, FF, or CR) at the user data latch will terminate the load routine and cause the program to mark the end of the data load with a sentinel bit, if used, and will move to the edit routine. If there is no format control character, the program sequences to test for "137th character."

(e) 137th Character? - In the 137th Character condition, the user has sent more characters than available print columns without transmitting a format control character. The program then decrements the RAM address pointer to 136 and looks to the user data latch for a format control code in order to terminate the load routine.

It will repeat this cycle, ignoring all characters after the 136th character, until a format code is transmitted by the user. If there are 136 or fewer characters in the RAM, the program will cycle back to the start of the load routine for additional data transfer or will terminate data load if a control character has been received.

b. 24-Bit Processor CCA

Figure 2-71 illustrates the instruction sequence for the 24-bit processor data load routine.

1. Zero RAM Address - The memory address pointer is set to address the first RAM location that will store user data.

2. Strobe? - The transfer protocol requires that the user strobe signal follow the printer's demand. If STROBE is already high, the program waits by calling the fault check and status check subroutines to monitor printer status.

3. Raise Demand to User - When STROBE is inactive, the processor initiates data transfer by raising the demand signal.

4. Data Transfer - On the user strobe, data is transferred from the user data latch on the Interface CCA to the user data area of RAM on the Processor CCA. Signal demand is reset to inactive.

5. Stop I/O? - The processor checks for conditions that would cause further data transfer to be delayed or ended. Is the data code just received "illegal" (not printable because the specified character is not on the band)? Is it a control (paper instruction) character? Is there a parity error? If any of these conditions is true, the program branches to a related subroutine to process the data.

(a) Control Character? - If the received code is illegal (not printable), it may be a paper motion command. The program compares the code with control codes, fetched from the band image PROM, for Line Feed (LF), Form Feed (FF), and Carriage Return (CR). If a match is found the routine is finished.

(b) Insert Erase Code - An erase code is set in the RAM location just past the last user data address to mark the end of the line. The program then branches to the edit routine.

(c) VFU Flag Set? - If the illegal user data is not a control character, it may be a start or stop code for transfer of VFU format instructions. The processor tests one of its working registers for a flag bit indicating that the DAVFU option is available. If the flag is not set, the program continues with the non-DAVFU instructions beginning with "Insert Space Code." If the flag is set, the processor tests for the user-transmitted paper instruction signal PI.

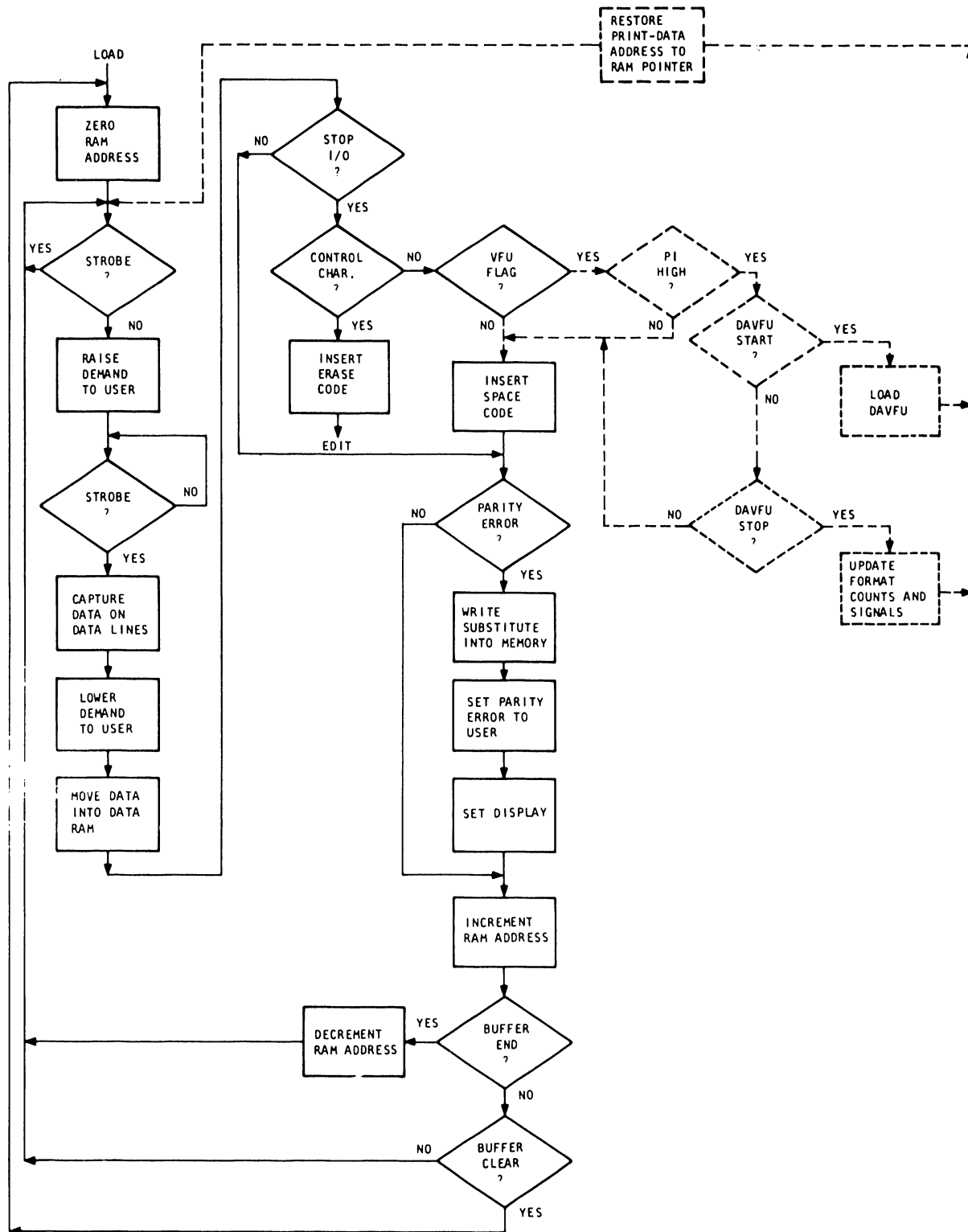


Figure 2-71. 24-Bit Processor Load Data Routine

6. PI High? - If the Paper Instruction signal is high, transmission of DAVFU data is expected. The processor prepares to load format instructions into the VFU portions of RAM. If PI is low, the program continues with the instructions beginning with "Insert Space Code."

(a) DAVFU Start? - The processor compares the user code with the DAVFU start code (Hex 6E). If the two match, the program begins loading DAVFU data into processor memory following the same handshake protocol used to transfer print data.

(b) DAVFU Stop? - If the user code does not match the start code, it is compared with the DAVFU stop code (Hex 6F). If these match, transfer of VFU data (begun by a previous start code) is over. Format information kept in processor memory is updated and interface signals to the user - Top of Form (TOF), Bottom of Form (BOF), and Paper Moving (PRMV) - are set or reset according to the current paper position and the settings of the configuration switches on the Interface CCA.

(c) DAVFU Load - Following a start code, format data from the user is loaded into reserved areas of RAM on the Processor CCA. Each VFU instruction has 12 bits (corresponding to tape channels 1 through 12 of a tape controlled VFU). The low six bits of this word are transmitted first and loaded into the "Low-VFU" RAM addresses. The high six bits are stored next in "High-VFU" RAM locations.

(d) Return to Data Load - When input of DAVFU is done, the processor returns to loading user print data.

7. Insert Space Code - If the illegal data code matches none of the control codes and is not a DAVFU start code or stop code, it specifies an unprintable character. A space code is fetched from the band image PROM and written into the user data RAM in place of the illegal code. A blank will appear in that print column.

8. Parity Error? - The processor samples the INBUS line carrying output from the parity checker on the Interface CCA.

9. Write Substitute into Memory - If a parity error is indicated, a parity error code is fetched from the band image PROM and substituted for the user code in the RAM. The processor sets the parity error signal to the user system and loads "23" ("I/O Parity Error, Data Load") for display on the control panel STATUS indicator.

10. Increment RAM Address/Buffer End? - If none of the conditions described above affects processing of the transmitted data code, or when processing is done, the program begins to load the next data code. The RAM address pointer is advanced to next memory location, and the buffer checked for the number of characters received. If a full line has been sent, the RAM address pointer is moved back to the last allowable location, and the program looks for transmission of a format control character to end the load routine. The program repeats the routine, ignoring each received print character until a control code is sent.

11. Buffer Clear? - If the user has transmitted the Buffer Clear signal, the whole line of data is to be retransmitted. The RAM address pointer is reset to the first address and data load begins again. If no Buffer Clear signal has been sent, the program loops back to load the next character code.

2.6.5 Self-Test Routine

The program moves from the idle routine to the self-test routine if the control panel TEST switch is set to one (1) of two (2) ON positions when the printer is off line. The processor then loads print data internally from the band image PROM instead of from the user system. Depending on the setting of the self test switch, this data is printed one (1) of three (3) patterns.

The fixed-character pattern gives repeated lines of one (1) letter (usually "H") and is selected when the switch is set to the left. The shifting-character pattern prints lines showing the actual character sequence on the band, but successive lines start with a new character, causing the print columns to appear to slide across the page. This pattern is selected when the switch is set to the right.

The band-sequence pattern gives full lines of each character on the band. It is selected by placing the printer ON LINE with the self test switch in either the right or left position and then moving the switch to the center position. Both the fixed-character and band-sequence patterns are printed at a reduced speed. The shifting-character pattern is printed at normal speed.

The self-test routine is comprised of two (2) main subroutines. Each has the purpose of loading the RAM print buffer with one line of the selected self test print pattern. The program repeatedly loops through the appropriate subroutine and, with each loop, stores one character code in the buffer. When the buffer is full, the program exits to the edit and print routine.

The subroutines work in similar ways with one important difference. In the subroutine for the shifting-character pattern, each loop through the instructions loads one (1) character code into a buffer location. After 136 loops at most, the buffer is full.

In the subroutine for the fixed-character and band-sequence patterns, each loop loads one (1) character code and three (3) space codes into four (4) adjacent buffer addresses. This is because these patterns are printed at reduced speed. Each line is printed in four (4) passes, following the method shown in **table 2-51**. On each pass, only one-fourth of the line is printed.

TABLE 2-51. REDUCED PRINT SPEED DATA LOAD

Enter Self Test Routine	Each Execution of Subroutine Loop Loads 4 Buffer Locations														When Buffer is Full						
	Line Buffer Locations																				
	1	2	3	4	5	6	7	8	9	10	11	12	-	-		-	-	133	134	135	136
1	X	X	X	H	X	X	X	H	X	X	X	H	-	-	-	-	X	X	X	H	Exit to First Print Pass
2	X	X	H	X	X	H	X	X	H	X	-	-	-	-	X	X	H	X	X	Exit to Second Print Pass	
3	X	H	X	X	X	H	X	X	X	H	X	X	-	-	-	-	X	H	X	X	Exit to Third Print Pass
4	H	X	X	X	H	X	X	X	H	X	X	X	-	-	-	-	H	X	X	X	Exit to Fourth Print Pass
	Loop 1				Loop 2				Loop 3				Loop 34								

X = Space -- No character is printed. H = Code for print character.

Since the line buffer holds up to 136 codes, this loop will be executed at most 34 times to complete one (1) line and allow exit for printing. Figure 2-72 shows the instruction sequence for the self-test routine for both 20-bit and 24-bit Processor CCAs.

a. Shifting Pattern?

The processor checks the setting of the self test switch to determine which pattern is selected. The program then branches to one (1) of the two (2) subroutines to load the line buffer with the appropriate output pattern.

b. Set Fixed-Character Address/Band Sequence Address

If the switch setting calls for the fixed-character or band-sequence printout, the address pointer for the band image PROM is set to the location of the single character, either "H" or the appropriate character in the sequence.

c. Set Shifting-Character Address

If the switch setting selects the shifting pattern, the PROM pointer is set to the address of the first character of the pattern.

d. Initialize/Update RAM Pointer

On the first pass through the routine, the data RAM address register is set to the first RAM location used for storing print data. On subsequent passes, the pointer is advanced to successive memory addresses.

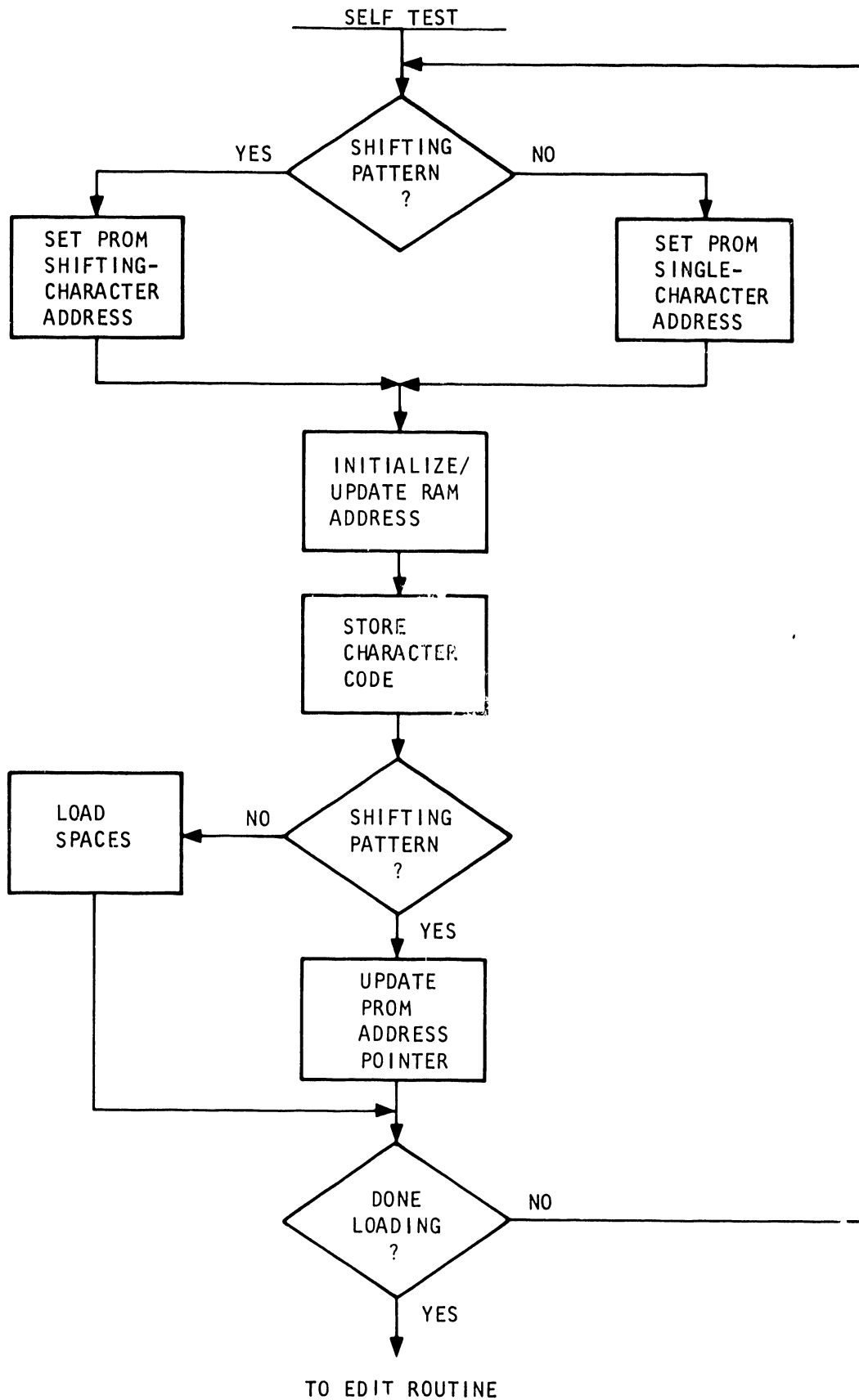


Figure 2-72. Self Test Routine

e. Store Character

The character code is moved from the band image PROM to the addressed location in the RAM.

f. Shifting Pattern?

For the fixed-character and band-sequence patterns, codes for filler spaces are loaded into the buffer locations adjacent to the address of the newly stored character code.

g. Update PROM Address Pointer

For the shifting-character pattern, the band image PROM's address pointer must be advanced to fetch a new character code. The character code stored in the line buffer on the next pass will be that of the next character on the band.

h. Done Loading?

If a full line of print data codes has been loaded, the program branches to the edit routine to prepare the data for printing. If the line buffer is only partly filled, the program loops back to load another character code following the steps described above. For the band-sequence pattern, the PROM pointer is updated only after one full line of code for a single character has been loaded and printed.

2.6.6 Edit Routine

The edit routine prepares the transmitted line of user data for printing by testing for three (3) special types of codes: the space code, the erase code, and, when the 96-character foldover is used, any code for lower-case letters. This edit routine applies to all B-Series printers with slight variations for 300 LPM and 600 LPM printers using the sentinel bit.

User data is held in the RAM as a complete "line." The space code simply indicates that the print column associated with a given RAM location should be left blank. The erase code is sent when the user wishes the entire line of data (or whatever portion of it has been transmitted) to be ignored.

The foldover option causes lower case letters sent by the user to be printed as upper case letters. Because 64-character bands provide only the upper case alphabet, when one of these bands is in use, any user character codes for lower case letters must be "folded over" to the code for upper case (one bit is inverted) for printing to be possible.

The program begins the edit routine by checking if any data is to be printed on the line. That is, is there an erase code, or do all RAM locations hold the space code? If the line is blank, the program branches to the format routine. If there is data to be printed, current to the paper feed motor is turned off, band tension is checked, the band motor is started (if it is off), and the character counter is cleared to zero.

An erase code is loaded into the RAM location just past the last location for user data to mark the end of the line. **Figure 2-73** illustrates the instruction sequence for the edit routine.

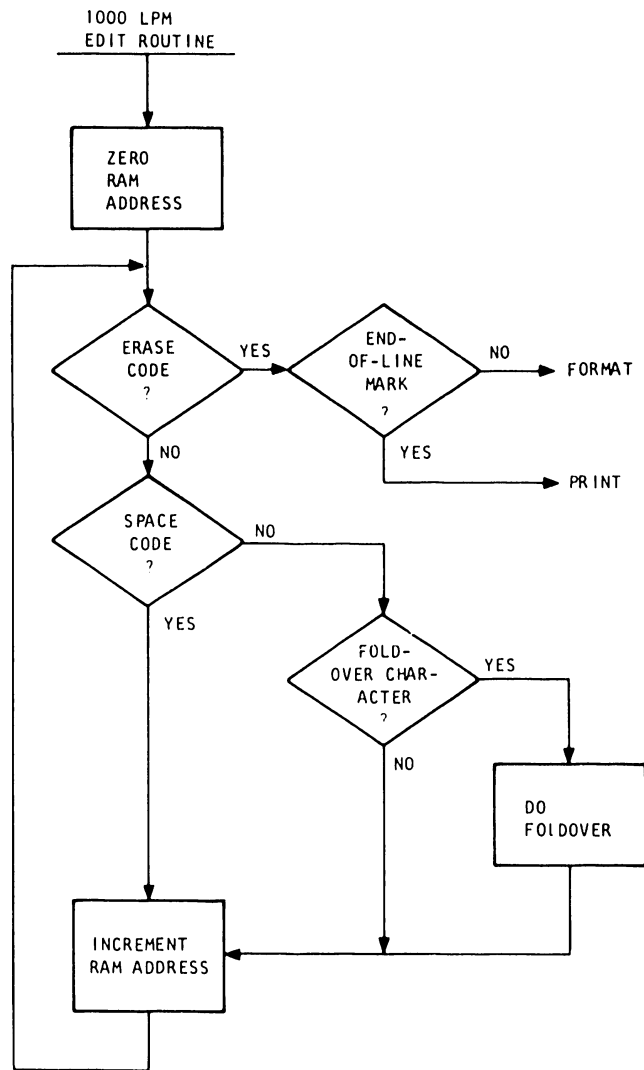


Figure 2-73. Edit Routine

a. Zero RAM Address

Each RAM location reserved for print data is checked in turn. To begin this loop, the memory address pointer is set to address the first RAM location.

b. Erase Code?

A unique "erase code" is fetched from its location in the band image PROM and compared in the ALU with the contents of the first RAM location. If they match -- the user code is the erase code -- the entire line of data will be ignored, and the program branches to the format routine. If they do not match, another test is performed: Is the user data word a space code?

c. Space Code?

A unique "space code" is fetched from the band image PROM and compared with the same user data code. If they match, the first print column in the line (corresponding to the first RAM location) will be blank. The space code in the first RAM location is erased, leaving "blank" data at that address. If the codes do not match, the program increments the character counter and checks if the character code must be "folded over."

d. Foldover Character

A special location in the band image PROM is addressed to determine if the foldover option is in use. If it is, and if the user character code is found to specify a lower case letter, the next instructions invert one bit in the code, converting it to ASCII upper-case form.

e. Increment RAM Address

Editing of the first user data code is now complete. The RAM address pointer is incremented to address the next data code location, and the program loops through the edit routine again. When the erase code marking the end of the line is reached, the program branches to the print routine.

2.6.7 Print Routine

Two (2) different print routines are used in B-Series printers. Since the 300 LPM uses only one (1) hammer bank with double spanning hammers and one (1) Hammer Driver CCA, its print routine differs from that of the 600 LPM and 1000 LPM printers. The following paragraphs described each routine.

a. 300 LPM Print Routine

The print routine develops printer hammer firing in the instruction sequence shown in **figure 2-74**.

1. Clamp On - First the program tests to ensure that the initial band drive power has brought the band up to speed. The paper clamps that hold the paper still and prevent multiform blousing during print time are allowed to energize. Then the printer band timer is cleared and a check is made to ensure that the band is at its proper speed.

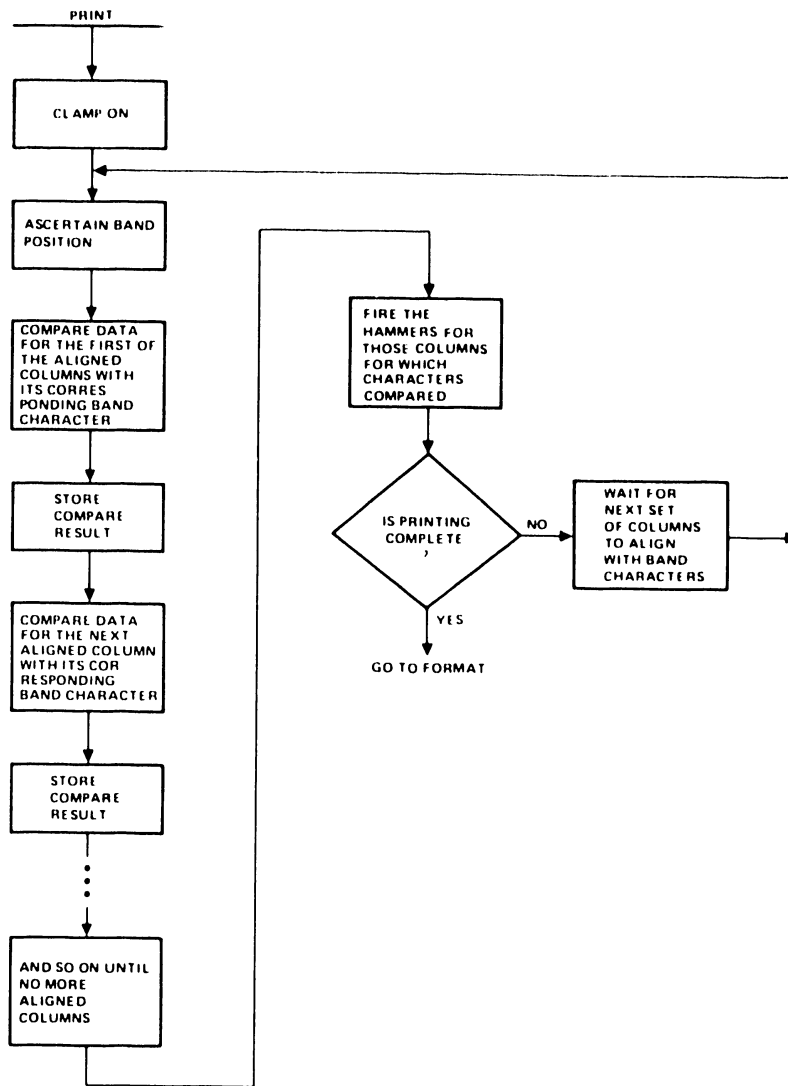


Figure 2-74. 300 LPM Print Routine

2. Ascertain Band Position - Next a count is kept of each hammer pulse reset signal (HPRES) to indicate a new character in front of a hammer at the start of the character period. This count tracks the band by noting each time when a new character is in front of hammer number one. In these sequences, the program also checks for 10-character-per-inch density and 15-character-per-inch density, and determines odd or even column printing.

3. Compare Data for the First of the Aligned Columns with its Corresponding Band Character - This sequence block effects a compare between the first character in hammer group A aligned with a hammer/print column and with the character pointed to in the data RAM. The sequence looks at the character, as identified from the band image PROM, and tries to match it with the character addressed by the data RAM pointer.

4. Store Compare Result - The result of the compare between the band character and the data RAM character is stored in the hammer data register at a location specified by the scan counter. The "S" register of the Processor CCA is also set to keep track of the hammer to be fired.

5. Compare Data for the Next Aligned Column with its Corresponding Band Character - The program now proceeds to effect a compare between the next character (located in character group B) aligned with a hammer/print column and with the character pointed to in the data RAM. Again the program looks at the character, as identified from the band image PROM, and tries to match it with the character addressed by the data RAM pointer.

6. Store Compare Result - This second compare is now stored in the hammer data register at the address specified by the scan counter.

7. Compare and Store for all Remaining Aligned Columns - A character compare is made successively from one column in each of the remaining hammer groups (C through O). The results are then stored.

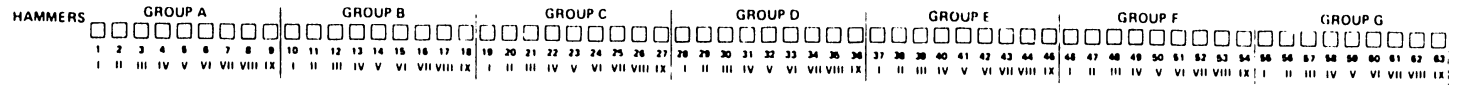
NOTE

One column (ODD, EVEN, or A, B, C) in each hammer group has now had a hammer alignment and character compare check. The hammer groups are identified from A through H, and each group has hammer sets I, II, III, IV, V, VI, VII, and IX associated with it. Each set contains two columns (or three in 15 CPI), one odd and one even. See figure 2-75.

8. Fire the Hammers for Those Columns in which Characters Compared - These sequences enable the Processor CCA to transfer its data register compare contents and its S count that indicates which hammers are set to fire. It issues a command (ODSREG) to load the S-register and decodes the A-outputs to fire the hammers. After the hammers are fired, the program executes a delay time to allow hammer return before the next firing.

9. Printing Complete for this Entire Column Phase? - The program moves on if all data RAM characters in the selected phase (ODD or EVEN COLUMN) have had a compare, and the aligned hammers have fired. If not, the program proceeds to repeat its test in the same phase for additional hammer alignments and character comparisons.

HAMMER GROUPS



- ALL I HAMMERS ARE TRIGGERED AT THE SAME TIME
- ALL II HAMMERS ARE TRIGGERED AT THE SAME TIME
- ALL III HAMMERS ARE TRIGGERED AT THE SAME TIME
- ALL IV HAMMERS ARE TRIGGERED AT THE SAME TIME
- ALL V HAMMERS ARE TRIGGERED AT THE SAME TIME
- ALL VI HAMMERS ARE TRIGGERED AT THE SAME TIME
- ALL VII HAMMERS ARE TRIGGERED AT THE SAME TIME
- ALL VIII HAMMERS ARE TRIGGERED AT THE SAME TIME
- ALL IX HAMMERS ARE TRIGGERED AT THE SAME TIME

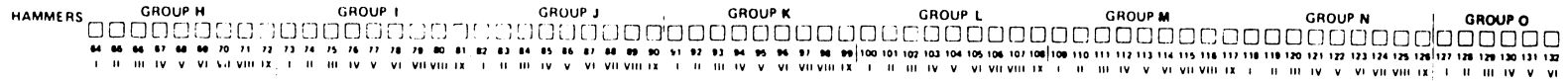


Figure 2-75. 300 LPM Hammer Groups

10. Wait for Next Set of Columns to Align with Band Characters - The program routine now looks to working register (R8) to determine which next set of columns (II, III, IV, etc.) are to align with band characters. It then loops back to "Ascertain Band Position" and again sequentially tests for alignment and comparison of a character with a hammer in the next hammer set in each hammer group. The previous sequences are repeated until each ODD or EVEN column set in each hammer group (**a through h**) has been tested for both a hammer alignment and a character comparison. The routine then initiates the necessary hammer firings, delays for hammer return, and tests to determine if all data characters in the RAM have been printed.

11. Is Printing Complete for all Columns? - Here, the program determines if printing has been accomplished for aligned/compared characters in both ODD and EVEN columns. In the case of 15 CPI print density, it will check columns A, B, and C. If the answer is "NO," a wait loop is generated to reset all hammers and to allow them to return to their rest position. The Processor CCA then advances the column phase from A to B or C. It then loops back to "ASCERTAIN BAND POSITION" to sequentially test for alignment and comparison of characters with the selected column position. If printing is complete, the program jumps to execute the FORMAT routine.

b. 600 LPM and 1000 LPM Print Routine

The 1000 LPM print routine controls firing of the hammers to print user data. Each of the hammers can be fired when two conditions have been met. First a band character must be precisely aligned with the hammer for one of the print columns. Second, the aligned band character must be the right one for that column; it must match the user code in the same position in the line buffer.

The work of the processor in finding these matches and firing hammers is organized in terms of groups of aligned band characters and hammers. As shown in **figure 2-58**, whenever a band character centers in front of the first hammer, a sequence of other band characters also becomes aligned with other hammers. When a band character centers in column one, other characters also line up in columns 10, 19, 28, 37, and so on for every ninth column. To determine which hammers can be fired, the processor makes a series of passes in which it checks every ninth column of the print line. In the first pass, or "sub-scan," it tests for data matches for columns 1, 10, 19 . . . to 127. In the second sub-scan, it examines columns 2, 11, 20 . . . to 128. This continues for nine sub-scans to make one full scan of all print columns. Whenever an aligned band character is found to match the user code at that position in the line buffer, the processor sets a bit in an assigned working register. At the end of each sub-scan, this data is transmitted to the Hammer Driver CCAs and the selected hammers are fired.

Because odd and even numbered hammers are controlled by different CCAs, the processor keeps separate counts of matches found in the odd and even positions of each sub-scan. Two working registers are used to hold these results and their contents are referred to as Data A and Data B.

The hammers themselves are grouped into pairs (or "sets") of an odd and an even hammer. One (1) S (set) pulse can fire either hammer in each set depending on whether the signal is sent to the odd or even Hammer Driver CCA. The hammers are also organized in eight groups. The hammer driver matrix shown in **figure 2-57** provides the control logic for selecting and firing hammers using output signals from the hammer data registers and the S1 to S9 signals.

The processor's sixteen working registers hold the various counts and address pointers used throughout the print routine. **Figure 2-76** is the flow chart for the 600 LPM and 1000 LPM print routine.

1. Set SA to 0, SB to 5 - Two "scratch pad" registers are used to hold indices to the two hammer sets tested at each step of a sub-scan. One register count, SA, is initialized to 0. The other, SB, is put to 5 to point to the set of hammers 9 and 10 columns beyond the first position.

2. Ascertain Band Position - The processor reads the value in the band position counter to determine which band characters are aligned with the columns to be checked.

3. Set Scan Count = 1 - Using another of the working registers, the processor sets an index to the pair of columns checked at each step of a sub-scan. The scan count is a data mask. When its value is 1 (binary 0000 0001), the processor stores results of tests on the first pair of columns, 1 and 10, in group A (refer to **figure 2-76**). When the mask value is shifted to 2 (0000 0010), data for the second two columns, 19 and 28, in group B, is stored, and so on through eight column groups. To begin the first sub-scan, the count is put at 1.

4. Compare Data for the First of the Aligned Columns with Adjacent Band Character - The processor checks for a match in the first column. Two registers are used as address pointers. One addresses the band image PROM location holding the code for the aligned band character. The other points to the user code in the first location of the line buffer. The two codes are fetched and compared in the ALU.

5. Store Compare Result in Data A - If the codes match, the processor sets the first bit (first odd match, group A) in the Data A register. If the codes do not match, no bit is set. In the first sub-scan, the Data A register will hold the results of comparisons for all odd positions in the sequence.

6. Compare Data for the Next Aligned Column with Adjacent Band Character - To check the next aligned column (nine positions past the first) the pointers for the band image PROM and user buffer are advanced to address the correct locations in each memory. The codes are fetched and, as before, compared in the ALU.

7. Store Compare Result in Data B - If the codes match, the first bit is set in the Data B register (first even match, group A). The Data B register will mark all even position matches in the first sub-scan.

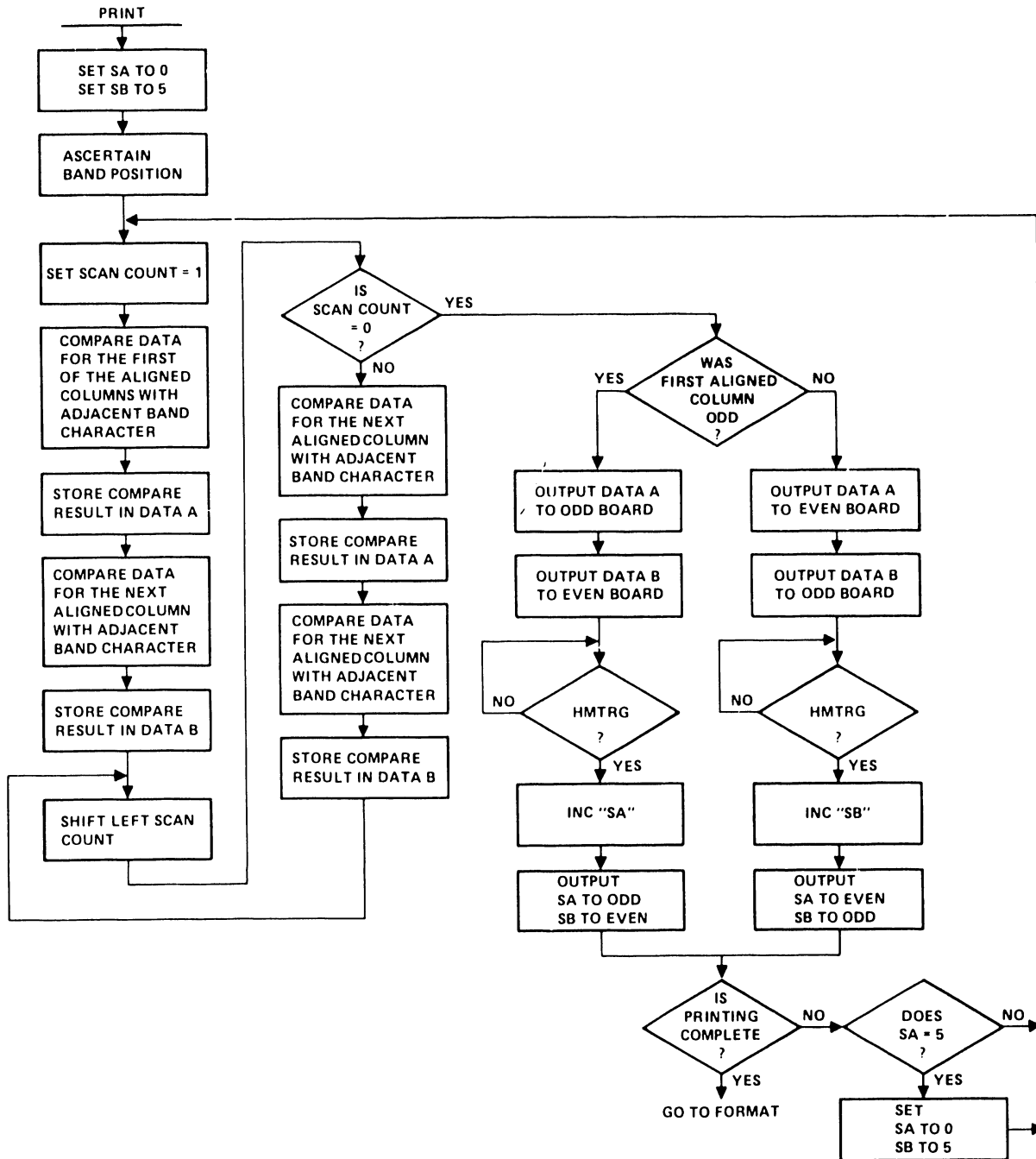


Figure 2-76. 600 LPM and 1000 LPM Print Routine

8. Shift Left Scan Count - The first two aligned columns now have been examined and the results marked. To test the second pair of aligned columns in group B, the scan count bit is shifted left. The mask now acts as an index to the second bit positions of the data A and data B registers.

9. Does Scan Count = 0? - When all eight pairs of aligned columns (groups A through H) have been tested, the mask bit will have been shifted eight times, clearing the register to zero, and the first scan will be complete. If the scan count is not zero, the processor continues to test for matches in the remaining hammer groups and marks the results in the Data A and B registers.

10. Was the First Aligned Column Odd? - When each sub-scan is done, hammer fire data has been stored for sixteen aligned columns. Before the processor can send this information to the Hammer Driver CCAs, however, it must determine whether the current sub-scan began on an odd or an even column.

11. Output Data A to Odd Board, Data B to Even Board - If the sub-scan began on an odd numbered column, the Data A register -- which stores data for odd positions in each sub-scan -- holds information for odd numbered hammers. This is the case in the first sub-scan, the third, the fifth, and so on. The Data B register stores data for even numbered hammers. The contents of both registers are transmitted directly to the respective odd and even Hammer Driver CCAs.

12. Output Data A to Even Board, Data B to Odd Board - If the sub-scan began on an even numbered column, the case is the reverse. Although the Data A register was loaded on odd numbered positions of the sub-scan, its data is for even numbered columns and must be output to the even Hammer Driver CCA. Information in the Data B register must be transmitted to the CCA controlling odd numbered hammers. The processor exchanges the data in the two registers before it is output.

13. HMTRG? - The program waits until signal HMTRG marks the instant when the scanned columns and band characters facing them are precisely aligned.

14. Increment SA/Increment SB - The processor increments either the SA or the SB pointer, depending on whether the sub-scan began on an odd or an even column. For sub-scan 1, SA increments to 1, SB stays at 5. These values point to the set columns to the hammer driver matrix that will be activated when the S pulses are transmitted: set column 1 on the odd CCA, set column 5 on the even CCA (see **figure 2-49**). In sub-scan 2, SB increments to 6. Hammers for the even columns of the scan now are enabled by data A, for the odd columns by data B.

15. Output SA to Odd/SB to Even - If the sub-scan began on an odd numbered column, the SA value is used to index the S pulse for the odd Hammer Driver CCA, the SB value to index the S pulse for the even CCA. The S pulses are transmitted -- S1 to odd, S5 to even in the first sub-scan -- and the hammers fired.

16. Output SA to Even, SB to Odd - If the sub-scan began on an even numbered column, the SA index is used for the even CCA, the SB for the odd. The S pulses are transmitted and the hammers fired.

17. Is Printing Complete? - With each sub-scan, the processor counts how many characters have been printed and calculates how many remain. When all the characters in the user data buffer have been printed, the program exits to the format routine.

18. Does SA = 5? If printing is still incomplete, the processor checks the value in the SA register. If SA = 5, one complete scan (nine sub-scans) has been done: SA has been incremented 5 times, SB 4 times. The pointers are reset to their initial values, and the program loops back to begin another pass and process remaining print data.

2.6.8 Format and Move Paper Routines

In the format and move paper routines, the processor decodes the user control word to determine paper motion to the next print line. The control character may specify a line feed (LF), form feed (FF), or carriage return (CR). Or, in the VFU mode of format control, it may be a tape channel command.

To begin the format routine, the program calls the FILLRG subroutine to move format counts from RAM to the processor's working registers. These counts include totals for the current line, previous line, number of carriage returns, and form size. They are updated, as required, with each movement of the form and allow the processor to calculate bottom and top of form positions. **Figure 2-77** illustrates the major instruction sequences in the format and move paper routines for the B-Series printers. In 300 LPM and 600 LPM printers, the paper clamps will be disabled before paper is moved.

a. Self Test?

The processor checks for a flag bit in one of its working registers, indicating that the self test switch has been set and the printer is operating in the self test mode. If the flag is set, the program moves to the instructions controlling a line feed. If the flag is not set, the processor begins decoding of the control code at the user data latch.

b. VFU Mode?

The processor checks the setting of another of its flag bits to determine if format operation is under VFU control. If the flag is not set, the program continues with non-VFU related instructions (**paragraph c** below). If the flag is set, the program moves to the following instruction sequences.

1. Tape Command? - The processor examines the information at the user data latch to determine if the control word is a tape channel command.

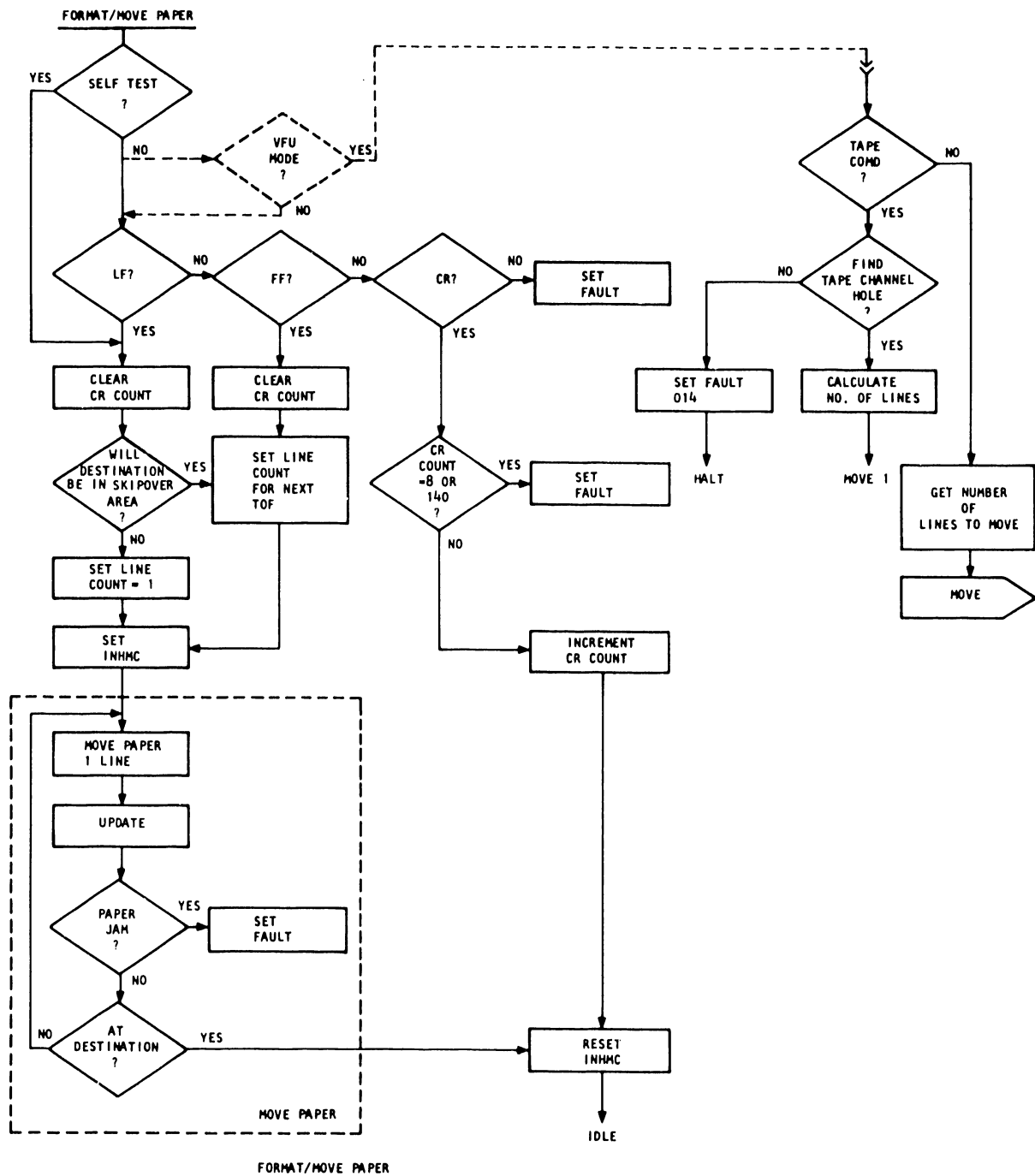


Figure 2-77. Format and Move Paper Routine

2. Find Tape Channel Hole - If the control word is a tape channel command, a search of the VFU RAMs is begun to find the tape channel data indicating the next print line. If the tape channel data cannot be found, the processor loads 14 ("Channel Not Found") for display on the control panel STATUS indicator, and the program branches to the fault check routine.

3. Calculate Number of Lines - If the tape channel data is found, the processor calculates the number of lines to be moved and the program branches to the move paper routine.

4. Get Number of Lines to Move - If the information at the user data latch is found not to be a tape command, the number of lines to be moved is contained in the control word itself. The processor calculates the required steps, checks the position of the form and skipover mode selected, then branches to the move paper routine to advance the form.

c. Line Feed/Form Feed/Carriage Return

Codes for each of the three (3) control characters that might be expected are also stored in the band image PROM. To identify the transmitted user code, the processor fetches each BIP code in turn to compare with the user code. A match identifies the operation to be performed, and the program branches to a related sequence of instructions for execution.

d. Set Fault

If the information at the user data latch matches none of the defined control codes, the program loads fault code 25 ("Format Code Not Recognized") for display on the control panel STATUS indicator, calls subroutine DUMPRG to return format counts to RAM for storage, then branches to the fault check routine to display the fault code and cut off operation.

e. Clear CR Count

If the specified operation will cause movement to a new line (line feed or form feed), the carriage return counter is cleared to zero.

f. Will Destination Be in the Skipover Area?

The format counts for the current line and last print line on the form are compared to determine whether the required form advance will place the next print position in the skipover area (adjacent to the perforation in the paper). If so, the processor calculates the number of steps needed to move the next print line to the top of the next page, and puts this value in the working register assigned to hold the step count. If the destination will not be in the skipover area, the step count is set to one (1).

g. Set Line Count for Next TOF

If the user control code calls for a form feed, the form must be advanced as many lines as are needed to put the next print line at the TOF position. Using the counts in its working registers, the processor calculates the required value and loads it into the step count register.

h. Set INHMC (Inhibit Master Clear)

Before enabling the paper feed electronics, the processor inhibits the input from the ALARM/CLEAR switch. If the switch is pressed while the form is moving, the processor still will generate the correct ramp down sequence of signals to complete paper motion.

i. CR Count = 8 on 140?

If the user control character specifies a carriage return, the processor reads the value in the working register holding the CR count. As defined by the settings of the Interface CCA configuration switches, a maximum of either 8 or 140 carriage returns can be allowed. If the carriage return about to be executed will move the count past the limit, the program branches to the fault check routine to display fault code 24 ("Too Many Consecutive Carriage Returns") and cut off operation.

If no fault will occur, the processor increments the CR counter and, having executed the format command, resets the INHMC signal and exits to the idle routine.

j. Move Paper One Line

In a sequence of phase shifts and delays, the processor enables the paper feed motor to advance the form one line at the specified density (6 or 8 LPI).

k. Update

The processor updates its format counts to reflect the current one line step. It subtracts one (1) from the step count value, adds one (1) to the current line count, and checks whether the current line is at the bottom of form position.

l. Paper Jam?

After each single line advance, or once each line when the form is slewing, the processor checks one of its flag registers for a paper motion flag bit. This bit is set when the paper motion sensor detects a sprocket hole, and so indicates that the form is moving correctly. The processor increments a paper motion count on each line step and, if the flag is set, resets it. If the flag is not set, the processor reads the motion count. If this equals eight (8) line feeds without paper motion, the form has jammed. The program branches to the fault check routine to display the fault code and cut off operation.

m. At Destination?

After each advance of one (1) line, the processor compares its count of steps moved to the number required by the format command. If the form has reached its new position, the INHMC signal is reset and the program exits to the idle routine. If more line steps are needed, the program loops back to the top of the move paper routine to repeat the instructions described here in **steps j through m**.

2.6.9 System Status Check (STACHK) Routine

At various times the program checks for changes in printer status. If some change is reported (on the System Status Change line), the program is interrupted and a system status check begun. See **figure 2-78** for the instruction sequence. The program tests for the nature of the fault as follows:

a. Clear Fault Latches

The processor clears all fault registers.

b. Legitimate Status Change?

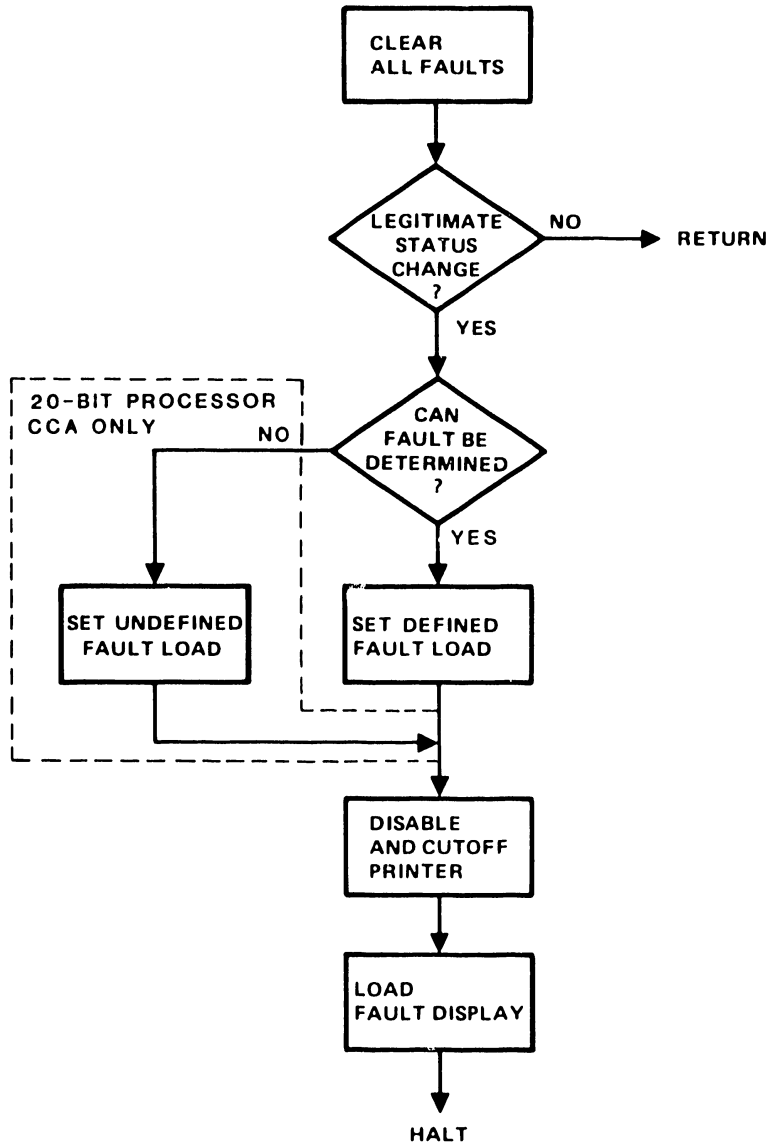
After a delay of 200 nanoseconds, the processor again samples the System Status Change signal. If it is now inactive, the program returns to the routine from which it called the STACHK routine. If the SYSTCH line is still active, the program moves to identify the fault.

c. Can Fault be Determined?

The processor checks each input at Status Port 1, testing for:

1. +38V fault
2. +12V fault
3. -9V fault
4. VCL fault
5. Hammer current fault
6. Paper motor fault and paper clamp fault in 300 LPM and 600 LPM printers
7. Band drive current fault
8. Band speed fault
9. Transducer fault

SYSTEMS STATUS CHECK ROUTINE



24509 286

Figure 2-78. System Status Check Routine

If any of these faults is detected, the related fault code is loaded into RAM and printer operation is cut off. If none of the faults is found, the program returns to its last exit point. In 300 LPM and 600 LPM printers with the 20-bit Processor CCA, an undefined fault (none of the above) will cause a STATUS display of "50" and halt printer operation.

d. Disable and Cut Off Printer

The processor module disables hammer fire, paper motion, and band movement.

e. Load Fault Display

The stored fault code is moved from RAM for display on the operator control panel. The program comes to a "halt" until the fault is corrected, and the system is reinitialized.

SECTION

III

**MAINT-
ENANCE**

SECTION III
MAINTENANCE

3.1 INTRODUCTION

This section contains the information necessary to maintain the B-Series printers in good working order. All procedures described in this section should be performed by qualified personnel who are thoroughly familiar with the printer operation and its mechanical configuration. Test equipment should be capable of giving reliable and accurate measurements.

NOTE

Exploded views of printer assemblies are available in **section VI** of volume II as an aid to maintenance personnel during removal and replacement procedures.

Individual Adjustment and Removal/Replacement procedures are listed alphabetically in **tables 3-2 and 3-3**. The procedures included in this section are in addition to the field service procedures found in the 300 LPM/600 LPM Line Printer Maintenance Guide, the 300 LPM/600 LPM Acoustic Cabinet Line Printer Maintenance Guide, and the 1000 LPM Line Printer Maintenance Guide.

3.2 RECOMMENDED TOOLS AND EQUIPMENT

Table 3-1 lists the tools and equipment recommended for the maintenance procedures included in this section. Each procedure also mentions the necessary tools and equipment needed to perform an adjustment or to remove/replace an assembly.

TABLE 3-1. RECOMMENDED TOOLS AND EQUIPMENT

Name	Size
Nut Driver	2.5mm, 3mm, 4mm, 4.5mm, 5mm, 5.5mm, 7mm, 8mm
Hex Driver	1mm, 2mm, 3mm, 4mm, 5mm
Allen Wrench 90°	5mm
Allen Wrench	5/64 inch
Socket Head Wrench	5.5mm

TABLE 3-1. RECOMMENDED TOOLS AND EQUIPMENT (Cont'd)

Name	Size
Box/Open End Wrench	7mm, 8mm, 10mm
Feeler Stock	0.51mm (0.020 inch), 0.64mm (0.025 inch), 0.5mm (0.02 inch), 1.0mm (0.040 inch), 2.5mm (0.100 inch)
Torque Screwdriver	1.0 to 30 inch/pounds (0.11 to 3.39 Newton/ meters) 1.0 to 40 inch/pounds (0.11 to 4.52 Newton/ meters)
Screwdriver	No. 2 Phillips
Hex Key (Torque Screwdrivers)	3mm, 4mm

3.3 ADJUSTMENT PROCEDURES

The adjustment procedures included in this section are not required, under normal circumstances, for field servicing. All in-field adjustments are described in the appropriate maintenance guide. If the adjustment required is not listed here, consult one of the following:

- 300 LPM/600 LPM Line Printer Maintenance Guide
- 300 LPM/600 LPM Acoustic Cabinet Line Printer Maintenance Guide
- 1000 LPM Line Printer Maintenance Guide

Table 3-2 lists the adjustment procedures included in this section and indicates the applicability of each adjustment according to model number. Refer to the appropriate paragraph when performing any of these procedures. A similar table is provided in each maintenance guide.

TABLE 3-2. ADJUSTMENT PROCEDURES

Procedure	300 LPM	600 LPM	1000 LPM	Paragraph
Paper Clamp Armature Assembly	X	X		3.3.1
Platen	X	X	X	3.3.2

3.3.1 Paper Clamp Armature Assembly Adjustment
(Figures 3-1 through 3-5)

NOTE

Once the paper clamp armature assembly has been set, under normal circumstances, it should not require readjustment.

- a. Set the POWER switch to the off position.
- b. Disconnect the AC power plug from the power source.
- c. Open the printer cover door.
- d. Open the hammer bank.
- e. Remove the ribbon cartridge and character band. Instructions are provided in the Operator's Guide.
- f. Using a 5mm Allen hex driver, remove the ribbon guide, if installed, from the top of the platen. If needed, see instructions provided in the Maintenance Guide.

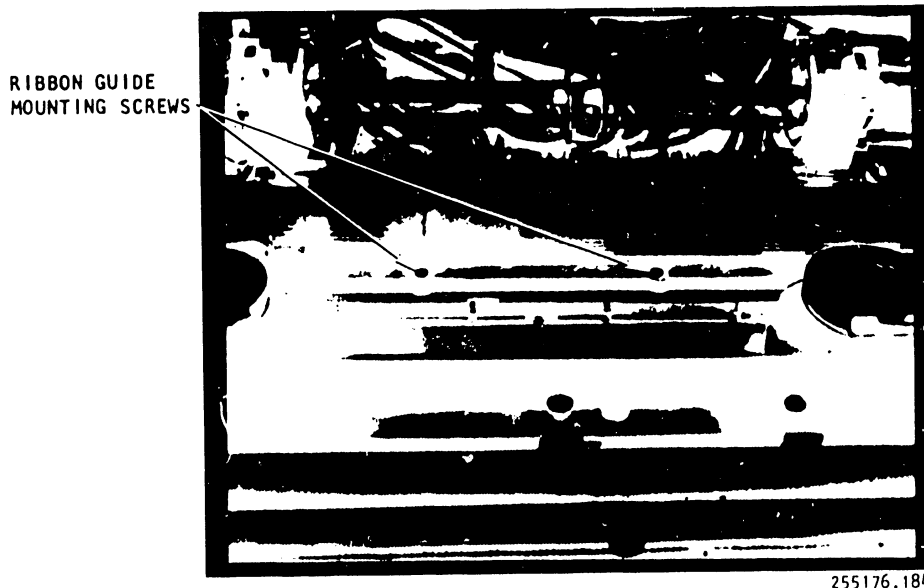


Figure 3-1. Paper Clamp Armature Assembly with Screw-Mounted Ribbon Guide

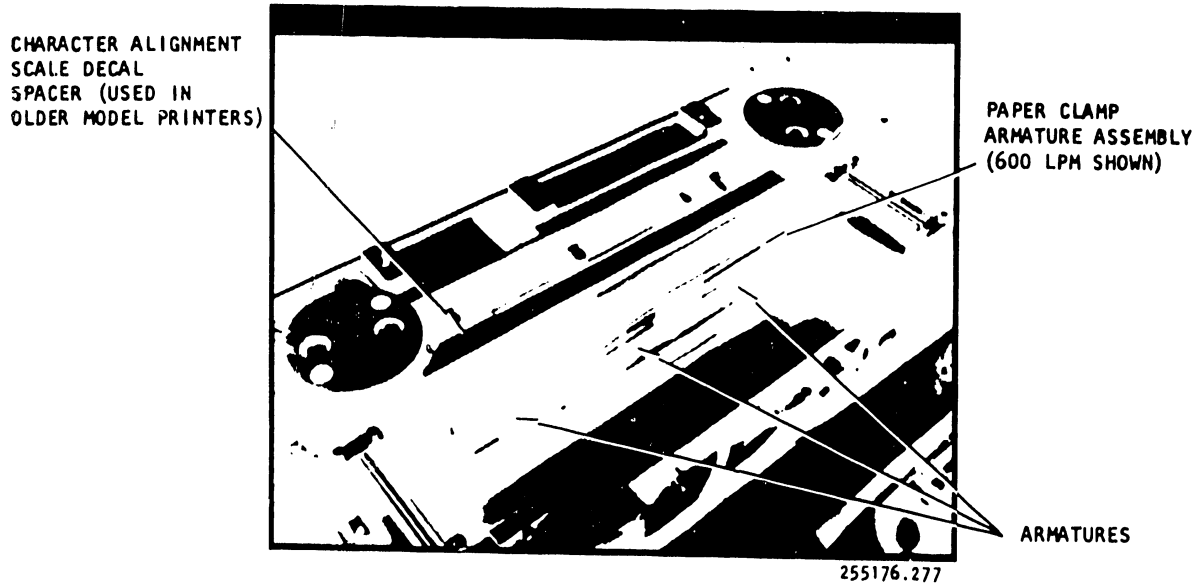


Figure 3-2.. Paper Clamp Armature Assembly

- g. Using a 3mm hex driver, loosen the four (4) screws which mount the Paper Clamp Armature Assembly to the printer frame.

CAUTION

Do not loosen the three (3) screws that mount the platen to the printer frame.

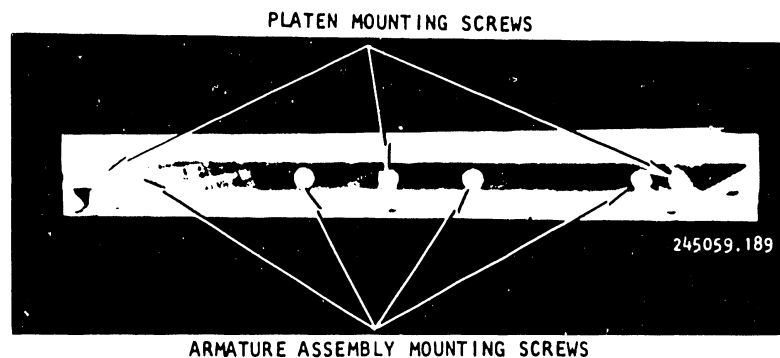


Figure 3-3. Armature Assembly Mounting Hardware

- h. On the left side, adjust the Paper Clamp Armature Assembly so that the top edge protrudes $0.64 \pm 0.03\text{mm}$ (0.025 ± 0.001 inch) from the lower edge of the plate. See figure 3-4.

- i. On the right side, adjust the Paper Clamp Armature Assembly so that the top edge protrudes $0.51 \pm 0.03\text{mm}$ (0.020 ± 0.001 inch) from the lower edge of the platen.
- j. Using a 3mm hex key and a torque wrench, tighten the four (4) Paper Clamp Armature Assembly mounting screws to a torque of 1.8 N/m.

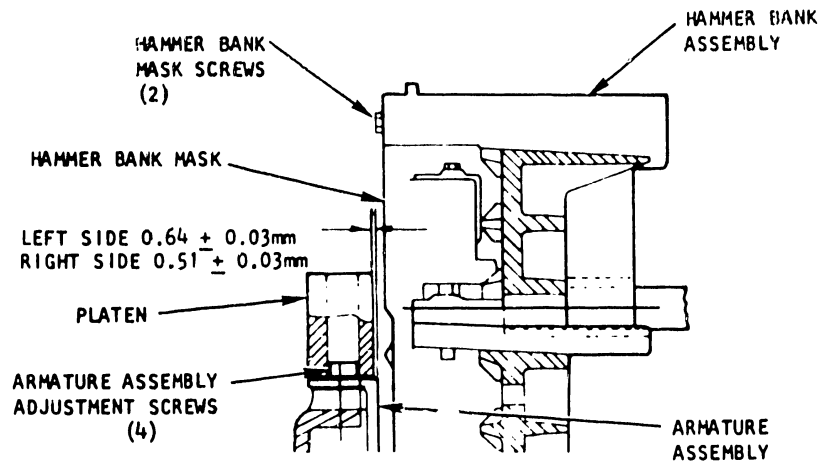


Figure 3-4. Paper Clamp Armature Assembly Adjustment

- k. Place a feeler gauge of appropriate size between the platen and the ribbon mask to check the adjustment on both sides and in the center of the armature assembly. See figure 3-5.
- l. Readjust as necessary.
- m. Install the ribbon guide, if used, and replace the alignment scale decal if needed. If necessary, see the Maintenance Guide for these procedures.
- n. Replace the character band and ribbon cartridge.
- o. Close the hammer bank.
- p. Close the printer cover door.
- q. Connect the AC power plug to the power source.

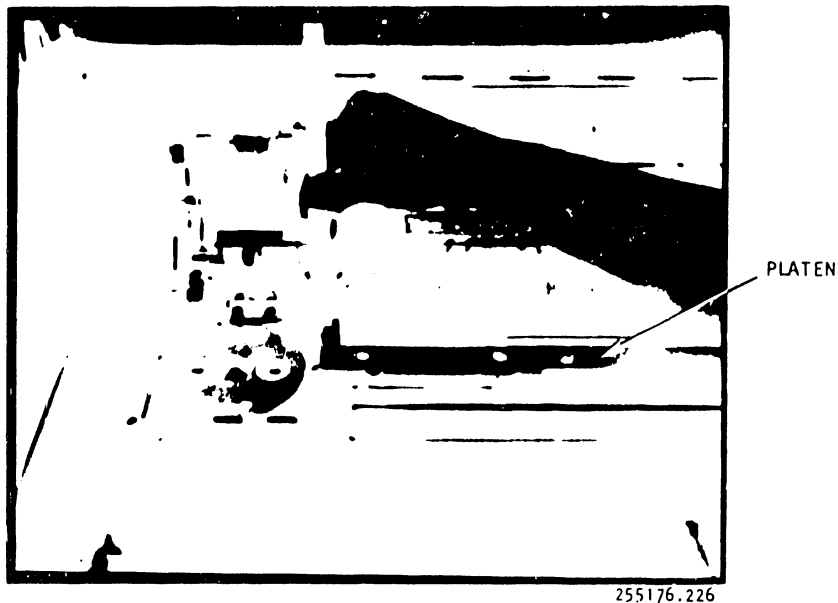


Figure 3-5. Paper Clamp Armature Assembly Adjustment Check

3.3.2 Platen Adjustment (Figure 3-6)

NOTE

The platen is normally not adjusted in the field. Once set in the factory, it should not require resetting. If the platen is moved, removed, or replaced, it must be set from the casting datum surface, **NOT** from the hammer bank face.

- a. Remove or raise the printer cover as directed in the Maintenance Guide.
- b. Remove the ribbon cartridge and the character band. See instructions in the Operator's Guide if needed.
- c. Remove the ribbon guide, if used, from the top of the platen. See **figure 3-1** or the appropriate Maintenance Guide.
- d. Remove the Paper Clamp Armature Assembly or the 1000 LPM Pressure Roller Assembly. See **paragraph 3.4.11** for the 300 LPM printer, **paragraph 3.4.12** for the 600 LPM printer, or the 1000 LPM Maintenance Guide for the 1000 LPM printer.
- e. Using a 4mm hex driver, loosen the three (3) screws which secure the platen to the casting.

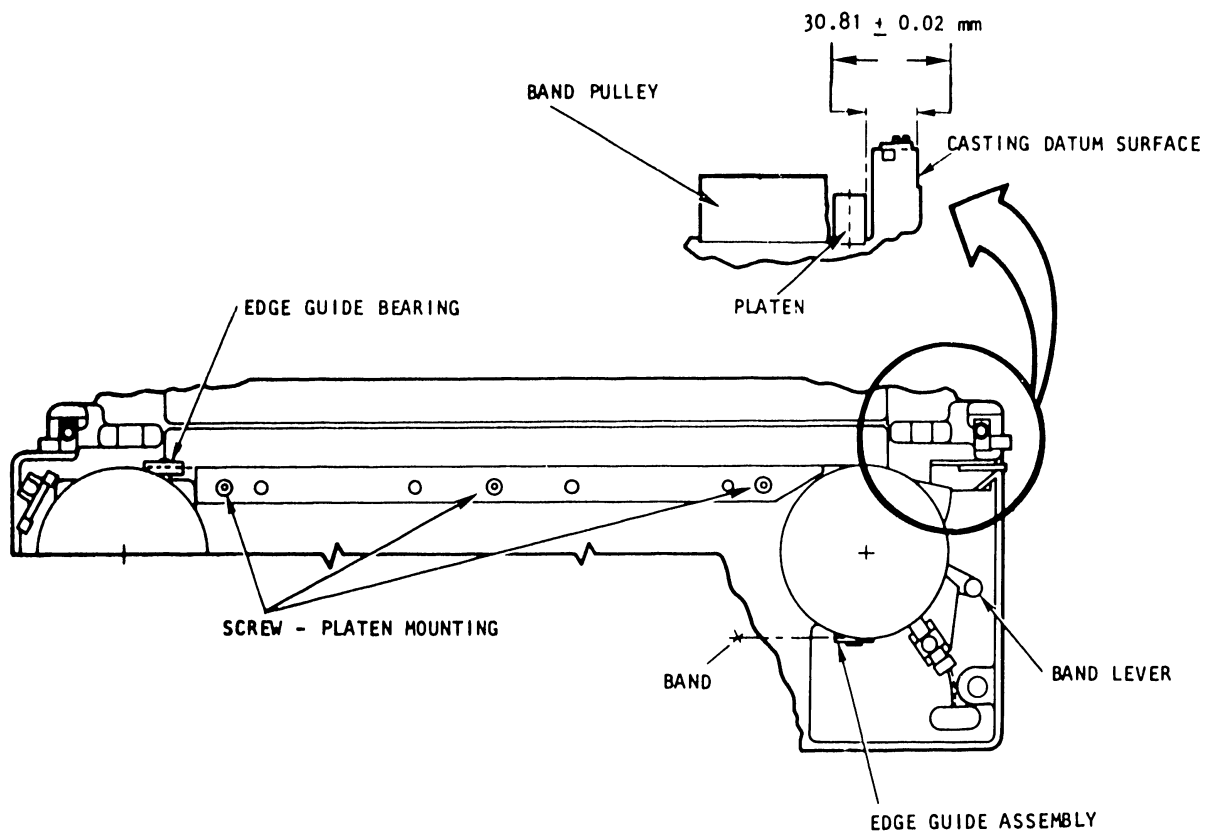


Figure 3-6. Platen Assembly Adjustment

- f. Set the platen clearance to 30.81 ± 0.02 mm (1.21 ± 0.0008 inches) from the datum casting surface as shown in **figure 3-6**.
- g. Using a 40 in/lb torque screwdriver and a 4mm hex key, tighten the three (3) screws loosened in **step e** to 4 N/m (35.4 in/lbs).
- h. Recheck the clearance and readjust if needed.
- i. Replace the Paper Clamp Armature Assembly or the Pressure Roller Assembly as directed in **paragraphs 3.4.11 or 3.4.12**, or the 1000 LPM Maintenance Guide.
- j. Adjust the Paper Clamp Armature Assembly. See **paragraph 3.3.1**. To adjust the Pressure Roller Assembly, see the 1000 LPM Maintenance Guide.
- k. Check, and, if needed, perform the Paper Clamp Solenoid Assembly adjustment procedure provided in the Maintenance Guide.
- l. Using a 5mm hex driver, install the ribbon guide as instructed in the Maintenance Guide.

- m. Install a new character alignment scale decal. See the Maintenance Guide instructions if needed.
- n. Install the character band and ribbon cartridge. Instructions are provided in the Operator's Guide.
- o. Replace or lower the printer cover as directed in the Maintenance Guide.

3.4 REMOVAL AND REPLACEMENT PROCEDURES

The following paragraphs describe the procedures to be followed when the assemblies listed in **table 3-3** must be removed or replaced. The procedures included here do not duplicate the procedures included in the various Maintenance guides. If the assembly or part needing replacement or removal is not listed in **table 3-3**, consult the appropriate Maintenance Guide.

TABLE 3-3. REMOVAL/REPLACEMENT PROCEDURES

Assembly	Applicability			Paragraph Number
	300 LPM	600 LPM	1000 LPM	
AC Power Switch (non-Acoustic)	X	X		3.4.1
AC Power Switch (Acoustic)	X	X	X	3.4.2
Control Panel (non-Acoustic)	x	x		3.4.3
Control Panel (Acoustic)	X	X	X	3.4.4
Hammer Bank Assembly	X	X	X	3.4.5
Interlock Transistion CCA	X	X	X	3.4.6
I/O Harness Assembly (non-Acoustic)	X	X		3.4.7
I/O Harness Assembly (Acoustic)	X	X	X	3.4.8
Mother Board CCA	X	X	X	3.4.9
300 LPM Paper Clamp Armature	X			3.4.10
300 LPM Paper Clamp Armature Assembly	X			3.4.11

TABLE 3-3. REMOVAL/REPLACEMENT PROCEDURES (Cont'd)

Assembly	Applicability			Paragraph Number
	300 LPM	600 LPM	1000 LPM	
600 LPM Paper Clamp Armature Assembly		X		3.4.12
Paper Clamp Solenoid Assembly	X	X		3.4.13
Paper Entrance Cover	X	X		3.4.14
600/1000 LPM Paper Low Switch		X	X	3.4.15
Paper Motion Sensor	X	X	X	3.4.16
Platen	X	X	X	3.4.17

3.4.1 AC Power Switch Removal/Replacement (Without Acoustic Cabinet) (Figure 3-7)

Removal

WARNING

Ensure that the AC power plug is removed from the power source.

- a. Remove the printer cover as directed in the Maintenance Guide.
- b. Remove the Control Panel Assembly and set it aside. See **paragraph 3.4.3** for instructions.
- c. Note the position of the four (4) slip-on leads to the power switch terminals and disconnect them.
- d. Squeeze the four (4) tensioned switch arms inward, and remove the switch assembly by pushing it toward the front of the printer.

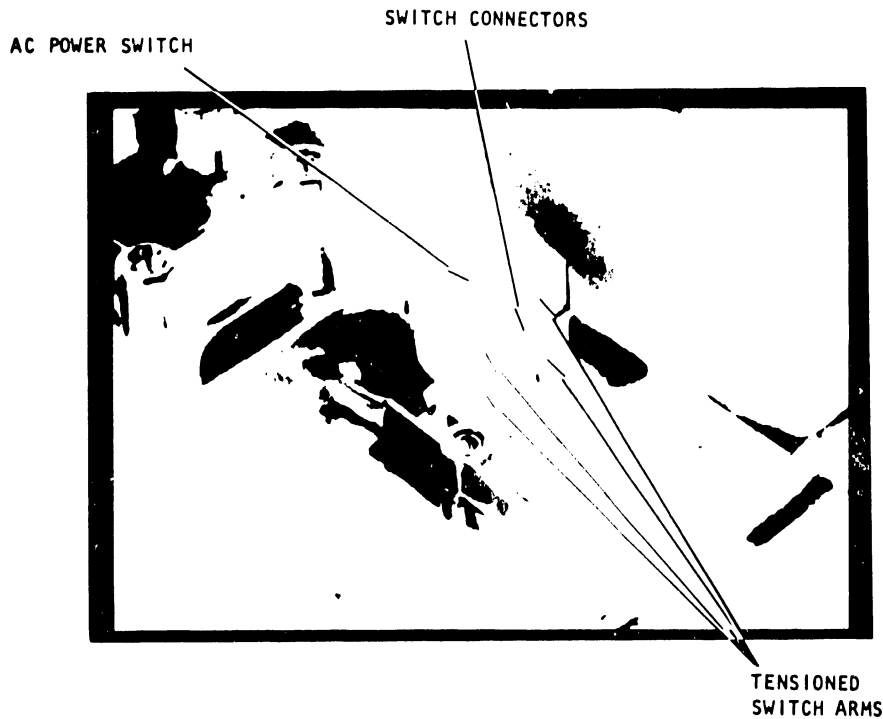


Figure 3-7. AC POWER Switch Removal/Replacement

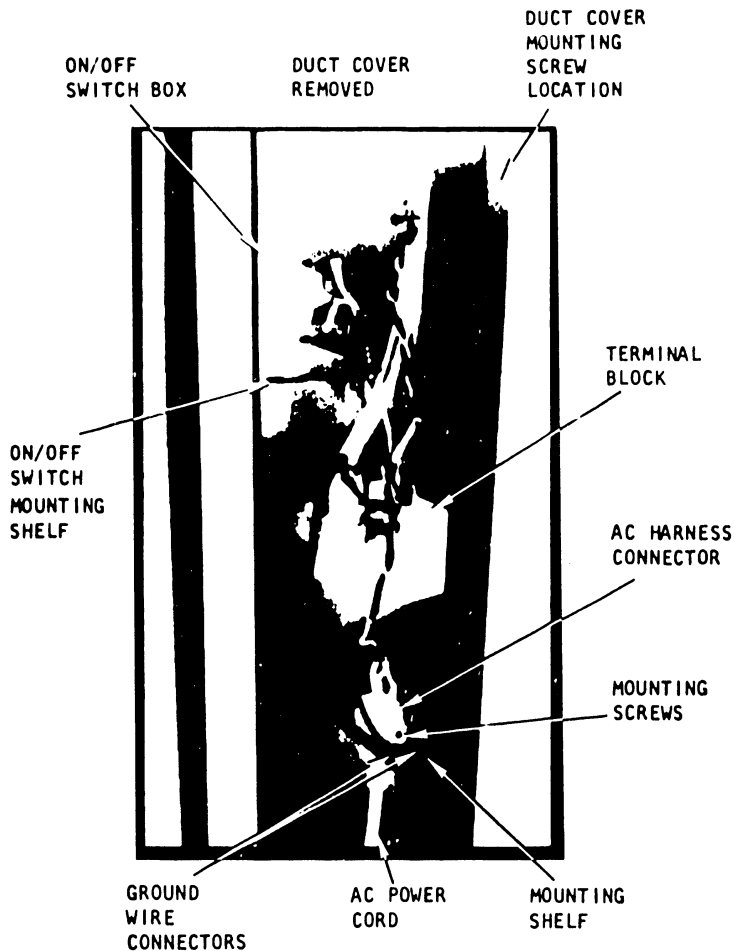
Replacement

- e. Hold the power switch with the connectors on the left and insert it from the front of the printer until it locks in place.
- f. Replace the four (4) slip-on leads in the positions from which they were removed in **step c.**
- g. Replace the Control Panel Assembly as directed in **paragraph 3.4.3.**
- h. Replace the printer cover as directed in the Maintenance Guide.
- i. Connect the AC power plug to the power source.

3.4.2 AC Power Switch and AC Distribution Harness Removal/Replacement (With Acoustic Cabinet)

Removal

- a. Set the POWER switch to OFF.
- b. Disconnect the power cord from the power supply.



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Figure 3-8. Acoustic Cabinet AC Power Cord and Power Distribution

- c. Open the cabinet rear door and remove the duct panel from the left side of the rear cabinet. See **figure 3-8**.
- d. Disconnect the AC power cord at the mounting shelf where the cord plugs into the AC Power Distribution Assembly.
- e. Using a 7mm nut driver on the screw head and an 8mm wrench on the lock nut, disconnect the ground wire coming out of the terminal block. (Note that a second ground wire from the transformer harness also fastens onto this shelf.)
- f. Remove the terminal ground wire.
- g. Using a 5.5mm (7/32 inch) socket head wrench, remove the screws mounting the AC harness connector to the shelf.

- h. Locate the second terminal block opposite to and just below the ON/OFF switch box.
- i. Disconnect the two (2) AC harness load wires from the terminal block.
- j. Hold the ON/OFF switch box and mounting shelf on the inside of the cabinet and, with a 5mm nut driver, remove the two (2) mounting screws on the outside.
- k. Remove the AC switch and power distribution harness.

Replacement

- l. Position the ON/OFF switch box and mounting shelf inside the cabinet panel and, using a 5mm nut driver, replace the two (2) mounting screws. See **figure 3-8**.
- m. Reconnect the two (2) AC harness wires to the terminal block located opposite to and just below the switch box inside the cabinet.
- n. Position the AC harness connector on its shelf and, using a 5.5mm (7/32 inch) socket head wrench, replace the two (2) mounting screws.
- o. Using a 7mm nut driver and an 8mm wrench, reconnect the terminal block ground wire to the mounting shelf.
- p. Reconnect the AC power cord to the AC Power Distribution Harness Assembly connector.
- q. Replace the duct panel on the left side of the rear cabinet.
- r. Make sure that the ON/OFF switch is set to OFF and reconnect the AC power cord to the power outlet.

3.4.3 Control Panel Removal/Replacement (without Acoustic Cabinet)

Removal

- a. Set the POWER switch to the off position and disconnect the power cord from the power source.
- b. Remove the printer cover as directed in the Maintenance Guide.
- c. Remove the electronics card cage cover.
- d. Disconnect the control panel cable plug P4 from the Interface CCA.

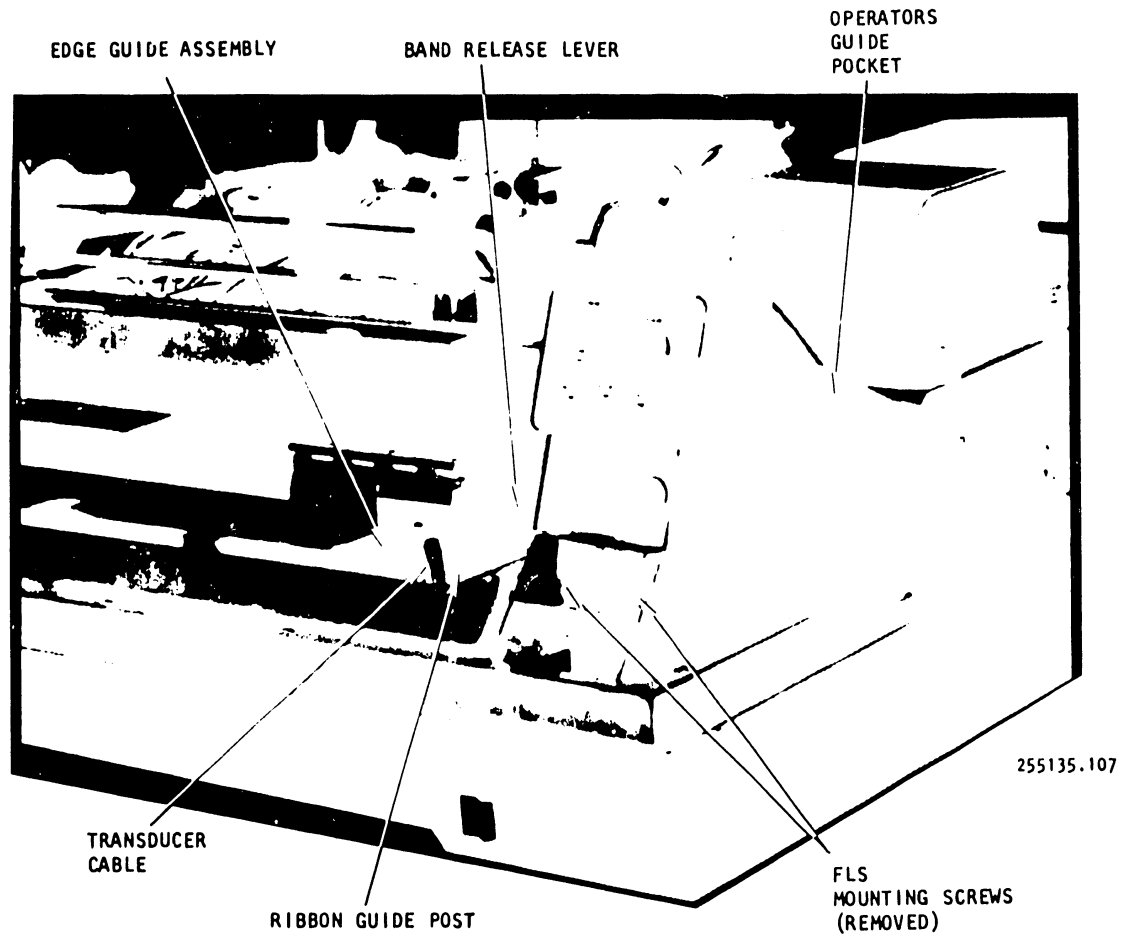
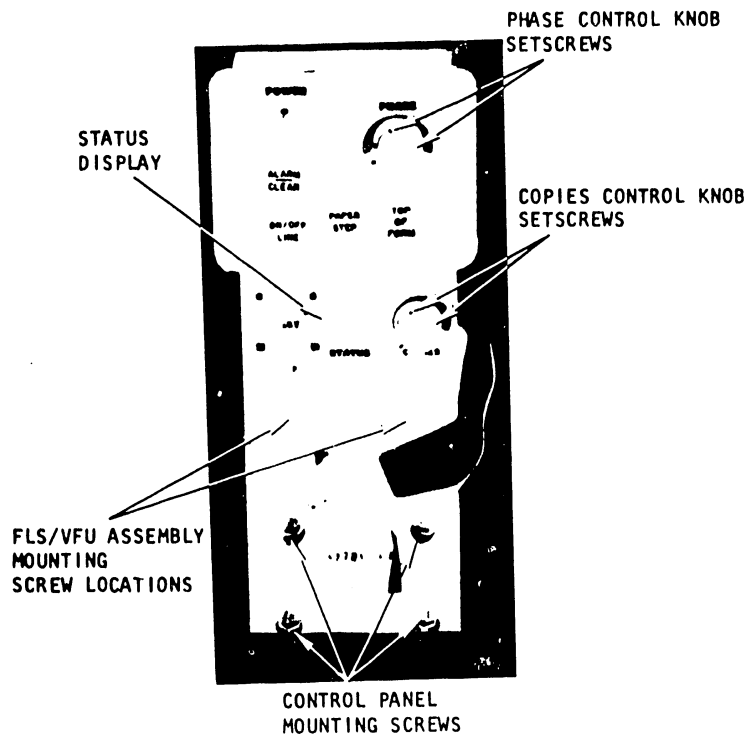


Figure 3-9. Control Panel Assembly Location

NOTE

When the optional Forms Length Selector Switch Assembly FLS is installed, it must be removed in order to have access to the Control Panel Assembly mounting screws. Access to the FLS switch requires that the Operator's Guide pocket be removed first. See **step i and j** and then return to **step e**.

- e. Using an 8mm nut driver, remove the two (2) screws mounting the FLS Switch Assembly to the Control Panel Assembly. (This step requires that the Operator's Guide pocket be removed first.) See **figure 3-9**.



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Figure 3-10. Control Panel Assembly Removal/Replacement

- f. Using an 8mm nut driver, remove the four (4) screws that fasten the Control Panel Assembly to the printer base (**figure 3-10**). This step removes the entire assembly with the CCA and cable.
- g. To remove the Control Panel Circuit Card Assembly, use a 1mm hex driver to loosen the two (2) setscrews that mount the COPIES and PHASE control knobs. Remove the knobs by pulling forward.
- h. Remove the switch caps by pulling straight forward. The four (4) switch caps removed are labelled ALARM/CLEAR, ON/OFF LINE, PAPER STEP, and TOP OF FORM.

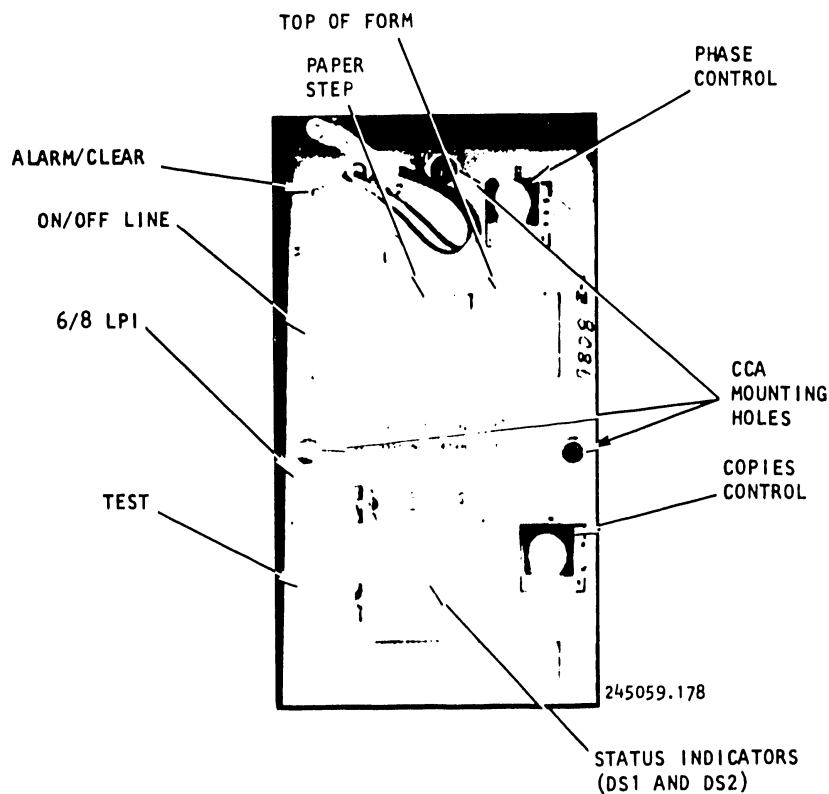


Figure 3-11. Control Panel CCA Removal/Replacement

- i. With a 5.5mm nut driver, remove the three (3) screws that secure the Control Panel CCA and the Operator's Guide pocket to the control panel base (**figure 3-11**).
- j. Remove the Operator's Guide pocket and set aside. If the FLS Switch Assembly is installed, return to **step e**.
- k. Remove the Control Panel CCA and its cable.
- l. Remove the STATUS indicators DS1 and DS2 by unplugging them from the Circuit Card Assembly.

Replacement

- m. Using an 8mm nut driver, mount the Control Panel Assembly without the CCA to the printer base.
- n. Using an 8mm nut driver, mount the optional FLS Switch Assembly if installed.

- o. Position the Control Panel CCA and the Operator's Guide pocket, and secure the three (3) screws removed in **step i** with a 5.5mm nut driver.
- p. Plug STATUS indicators DS1 and DS2 into the Control Panel CCA. See **figure 3-11**.
- q. Replace the four (4) switch caps removed in **step h**.
- r. Replace the COPIES and PHASE control knobs, adjust to correct positions, and secure them with the setscrews loosened in **step g**. See **figure 3-10**.
- s. Connect the control panel cable to plug P4 on the Interface CCA.
- t. Replace the electronics card cage cover.
- u. Replace the printer cover. See the Maintenance Guide for instructions if needed.
- v. Reconnect the power plug to the power switch and resume normal printer operations.

3.4.4 Control Panel Assembly Removal/Replacement
(With Acoustic Cabinet) (Figure 3-12)

Removal

- a. Set the POWER switch to OFF.
- b. Disconnect the power cord from the power source.
- c. Open the printer cover door, then raise the printer top cover as directed in the Maintenance Guide.
- d. Remove the paper guide shield.
- e. Remove the electronics card cage cover.

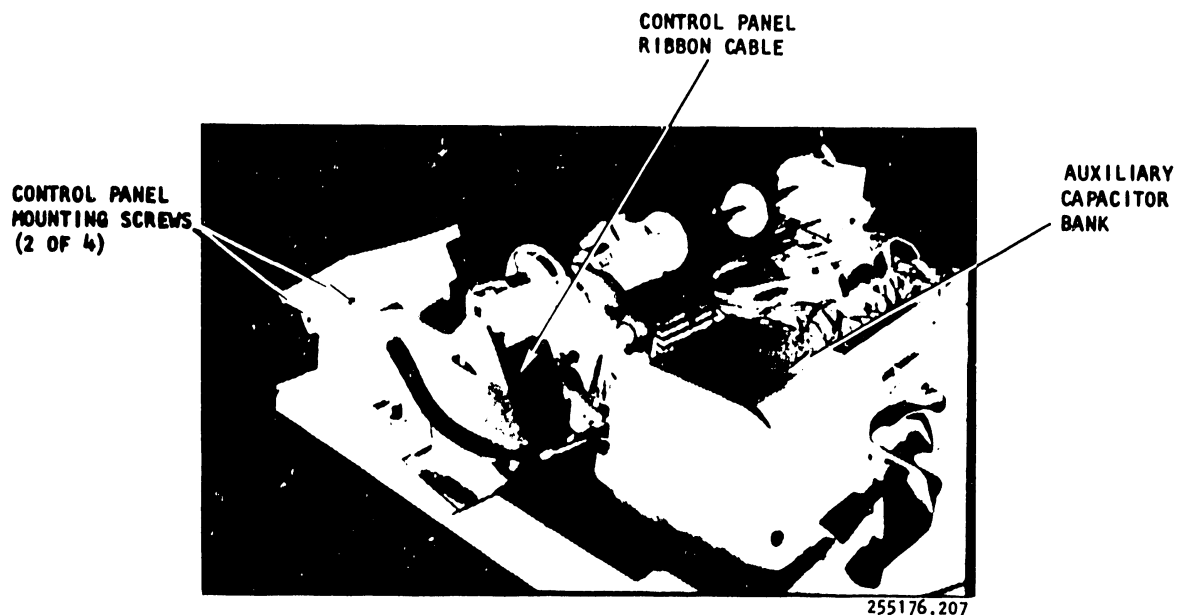


Figure 3-12. Acoustic Cabinet Control Panel Assembly Removal/Replacement (Printers in Acoustic Cabinet)

- f. Disconnect the control panel ribbon cable from P4 on the Interface CCA.
- g. Remove the auxiliary capacitor bank. See the Maintenance Guide for instructions if needed.
- h. Using a 7mm nut driver, loosen but do not remove the four (4) screws attaching the Control Panel Assembly to its mounting bracket. Lift out the control panel unit.
- i. Using a 5mm nut driver, remove the three (3) screws on the back of the assembly. Separate the metal assembly housing from the assembly itself, and lay the housing in the space in front of the power supply cover.
- j. Using a 1mm hex driver, loosen the two (2) set screws that fix the COPIES and PHASE control knobs to their shafts, and remove the knobs.
- k. Remove the (4) control buttons labelled ALARM/CLEAR, ON/OFF LINE, PAPER STEP, and TOP OF FORM. See figure 3-10 for locations.
- l. Using a 7mm nut driver, remove the three (3) hex head spacers, washer, and grounding clips from the back of the Circuit Card Assembly.

- m. Lift the Circuit Card Assembly out of the molded control panel.
- n. The STATUS indicators DS1 and DS2 may be removed by unplugging them from the front of the Circuit Card Assembly. See **figure 3-11**.

Replacement

- o. If the STATUS indicators DS1 and DS2 were removed, plug them into the circuit card sockets. See **figure 3-11**.
- p. Fit the Circuit Card Assembly into the molded housing, and replace the grounding clips, washer, and three (3) hex head screws.
- q. Replace the ALARM/CLEAR, ON/OFF LINE, PAPER STEP, and TOP OF FORM buttons. See **figure 3-10**.
- r. Replace the COPIES and PHASE knobs on their shafts. Adjust to the correct position and tighten in place with the 2mm hex driver.
- s. Seat the control panel in the metal housing and replace the three (3) screws removed in **step i**. Use a 5mm nut driver.
- t. Replace the Control Panel Assembly in the mounting bracket. Make sure the washers and screw heads on each side are to the outside of the bracket. With the 7mm nut driver, tighten the four (4) screws.
- u. Route the control panel ribbon cable over the power supply cover.
- v. Replace the auxiliary capacitor bank. See the Maintenance Guide for instructions if needed.
- w. Reconnect the control panel cable plug P4 to the top edge of the Interface CCA.
- x. Replace the electronics card cage cover and the paper guide shield.
- y. Lower the printer top cover. See instructions in the Maintenance Guide or in **section IV** of volume II.
- z. Close the cover door and check the clearance between the door and the Control Panel Assembly. Adjust the position of the Control Panel Assembly if necessary.
- aa. Reconnect the AC power cord to the power source and resume printer operations.

3.4.5 Hammer Bank Assembly Removal/Replacement
(Figures 3-13, 3-14, and 3-15)

Removal

- a. Raise or remove the printer cover as instructed in the Maintenance Guide.
- b. Remove the Paper Feed Assembly as directed in the Maintenance Guide.
- c. Remove the hammer bank interlock switch plug A19P3 from the Interlock Transition CCA. See **figure 3-16**.
- d. Cut and remove the cable tie which holds the interlock switch cable to the top of the Hammer Bank Assembly.
- e. Open the hammer bank. Using an 8mm nut driver, remove the two (2) screws that secure the hammer bank mask and remove the mask.

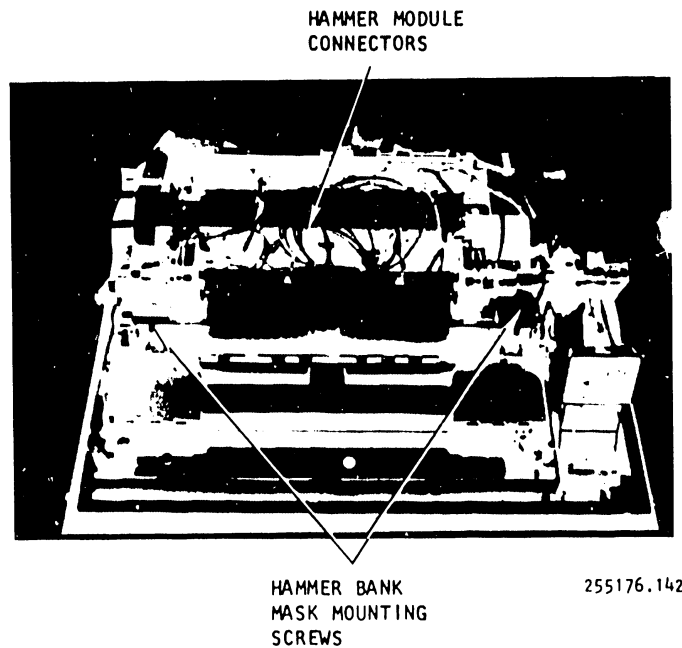


Figure 3-13. Hammer Bank Assembly Removal/Replacement

- f. Unplug all the hammer module connectors from the Hammer Driver CCA(s).

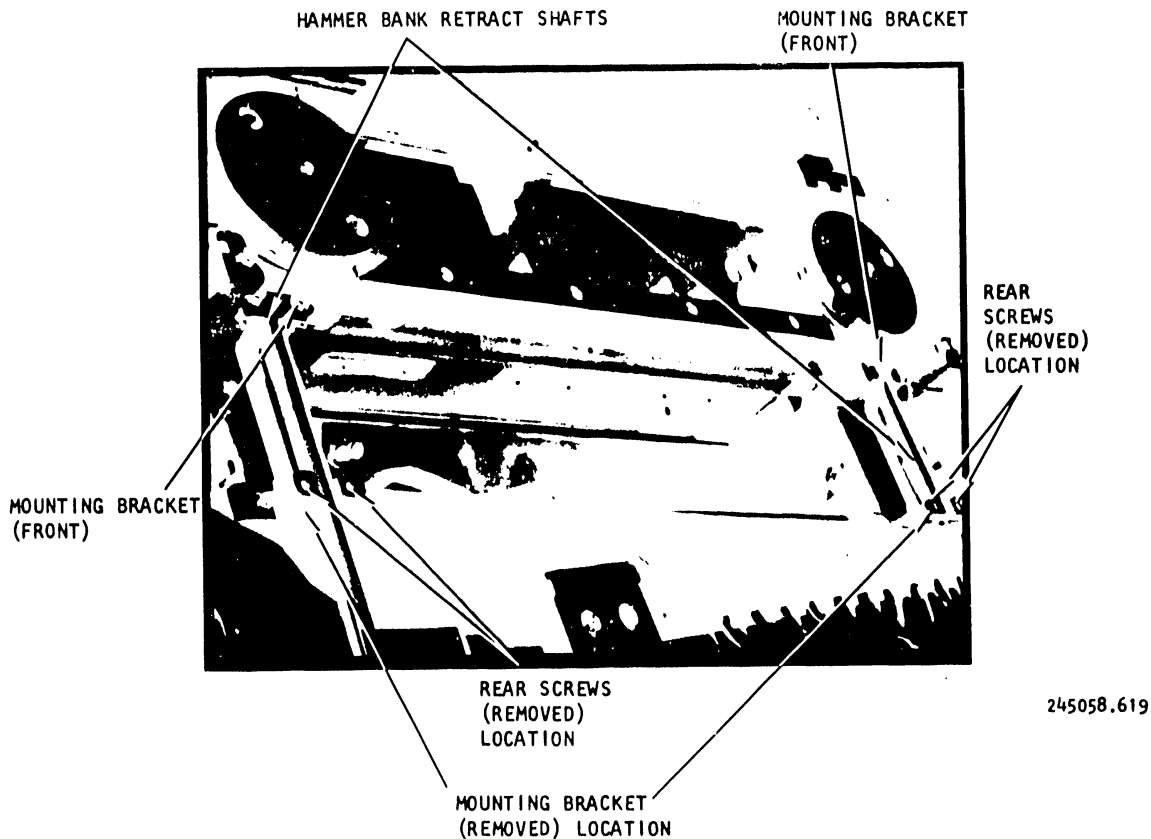


Figure 3-14. Hammer Bank Removal/Replacement
(Older 300 LPM Model Shown)

- g. Disconnect the paper clamp solenoid cable plugs P3A and P3B from the Power Board CCA.
- h. Using a 7mm nut driver remove the four (4) front and four (4) rear hammer bank mounting screws and the four (4) guide shaft hold-down clamps.
- i. Lift the Hammer Bank Assembly carefully and remove from the printer.
- j. Remove the hammer bank guide shafts.
- k. On 300 LPM and 600 LPM printers, use a 4mm hex driver to loosen the two (2) screws that mount the Paper Clamp Solenoid Assembly to the hammer bank and slide the solenoid assembly from its mounting bracket on the hammer bank. The 1000 LPM printer's Pressure Plate Assembly may be removed in the same manner.

Replacement

- l. If removed in **step k**, attach the Paper Clamp Solenoid Assembly or Pressure Plate Assembly to the Hammer Bank Assembly with the two (2) screws loosened in **step k**.
- m. Place the hammer bank guide shafts into position.
- n. Carefully position the hammer bank in the printer base, ensuring that the actuator assembly is properly positioned in the retract plate.

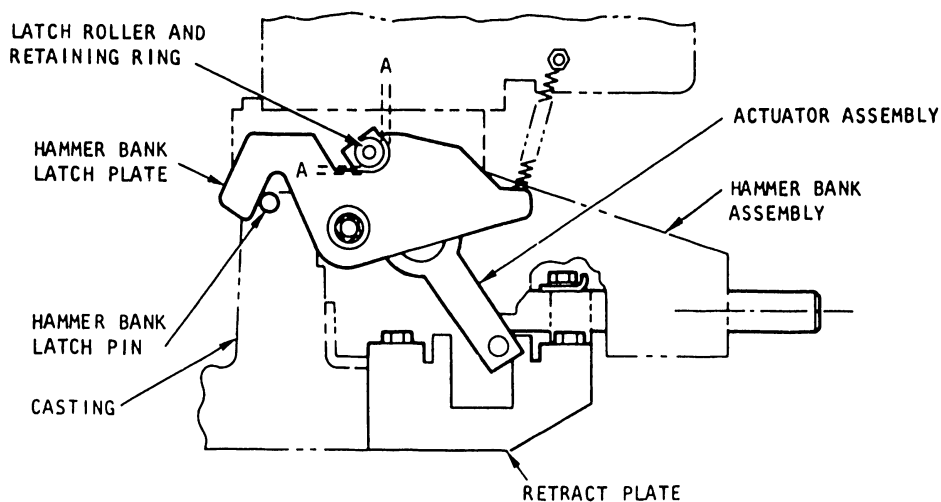


Figure 3-15. Hammer Bank Actuator Assembly Position

- o. Install the two (2) front and two (2) rear guide shaft mounting brackets with their mounting screws. Ensure that the hammer bank guide shafts are pushed firmly against the front clamp stops.
- p. Slide the hammer bank forward and backward to ensure smooth operation, and tighten the right side mounting clamp screws in the following order: left rear, right rear, left front and right front.
- q. Perform the same procedure to tighten the left side mounting clamp screws.
- r. Verify that the hammer bank moves freely. Readjust if necessary.
- s. Install the hammer bank interlock switch plug A19P3 on the Interlock Transition CCA.

- t. Use a cable tie to remount the hammer bank interlock switch cable to the bracket on the top of the hammer bank.
- u. Reconnect the hammer module connectors to the Hammer Driver CCA.
- v. Using a 4mm nut driver, mount the Paper Feed Assembly loosely with the four (4) screws that secure it to the hammer bank. Perform the Paper Feed Assembly adjustment. See instructions in the Maintenance Guide.
- w. Replace or lower the printer cover.
- x. Connect the AC power plug to the power source.

3.4.6 Interlock Transition CCA Removal/Replacement (Figure 3-16)

Removal

- a. Raise or remove the printer cover as directed in the Maintenance Guide.
- b. Disconnect all the plugs from the Interlock Transition CCA.

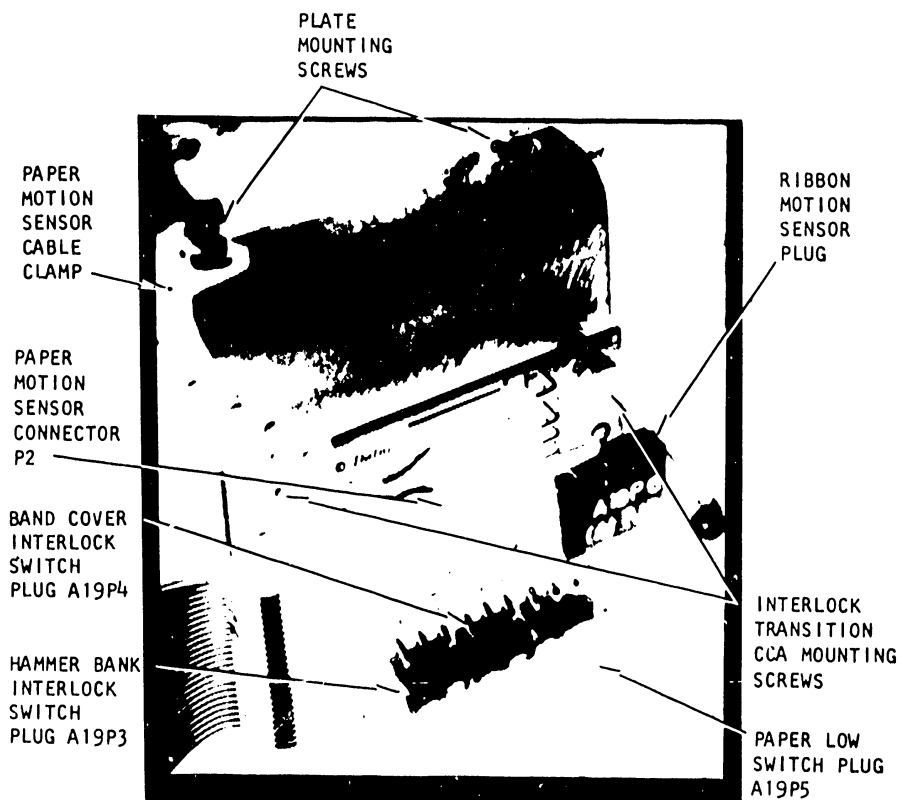


Figure 3-16. Interlock Transition CCA

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- c. Using a 7mm nut driver, remove the two (2) screws that secure the Interlock Transition CCA mounting plate to the printer casting.

NOTE

The clamp for the paper motion sensor cable is also removed at this time.

- d. Remove the Interlock Transition CCA and plate assembly.
- e. Using a 7mm nut driver, remove the two (2) screws which secure the Interlock Transition CCA to its mounting plate, and remove the CCA.

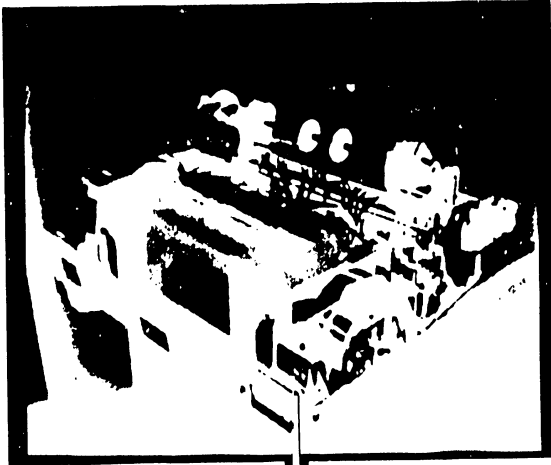
Replacement

- f. Mount the Interlock Transition CCA to its mounting plate with the two (2) screws removed in **step e**. See **figure 3-16**.
- g. Secure the Interlock Transition CCA and the paper motion sensor cable clamp to the printer casting with the two (2) screws removed in **step c**.
- h. Reconnect all plugs disconnected in **step b**.
- i. Lower or replace the printer cover. See the Maintenance Guide.
- j. Connect the AC power plug to the power source.

3.4.7 I/O Harness Assembly Removal/Replacement (Printers in Standard Cabinet) (Figure 3-17)

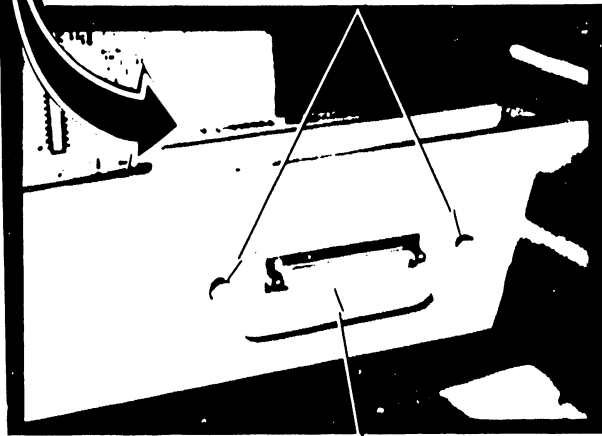
Removal

- a. Raise or remove the printer cover as directed in the Maintenance Guide.
- b. Remove the electronics card cage cover.
- c. Raise the Interface CCA out of the Mother Board CCA and remove plug P5 from connector J5.
- d. Using an 8mm nut driver, remove the two (2) screws that mount the I/O Harness Assembly connector to the printer base. See **figure 3-17**.
- e. Remove the I/O Harness Assembly.



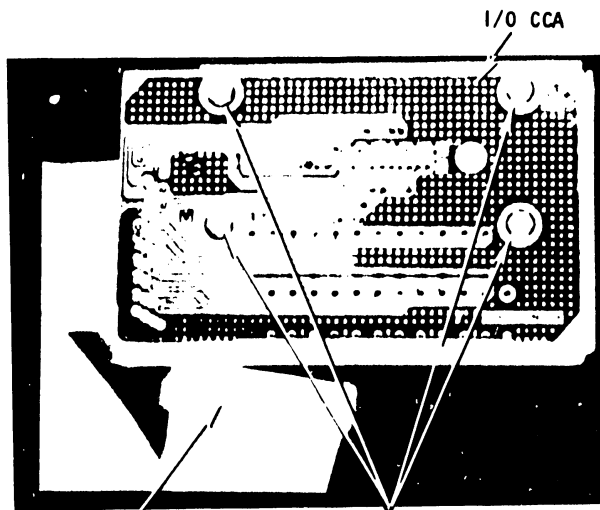
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I/O CONNECTOR ASSEMBLY
MOUNTING SCREWS



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I/O CONNECTOR



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I/O CONNECTOR P5

I/O CCA
MOUNTING SCREWS

Figure 3-17. I/O Harness Assembly, Printers in Standard Cabinet

- f. Using a 7mm nut driver, remove the four screws which secure the I/O Harness CCA to its mounting bracket if it is necessary to replace the I/O Harness CCA.

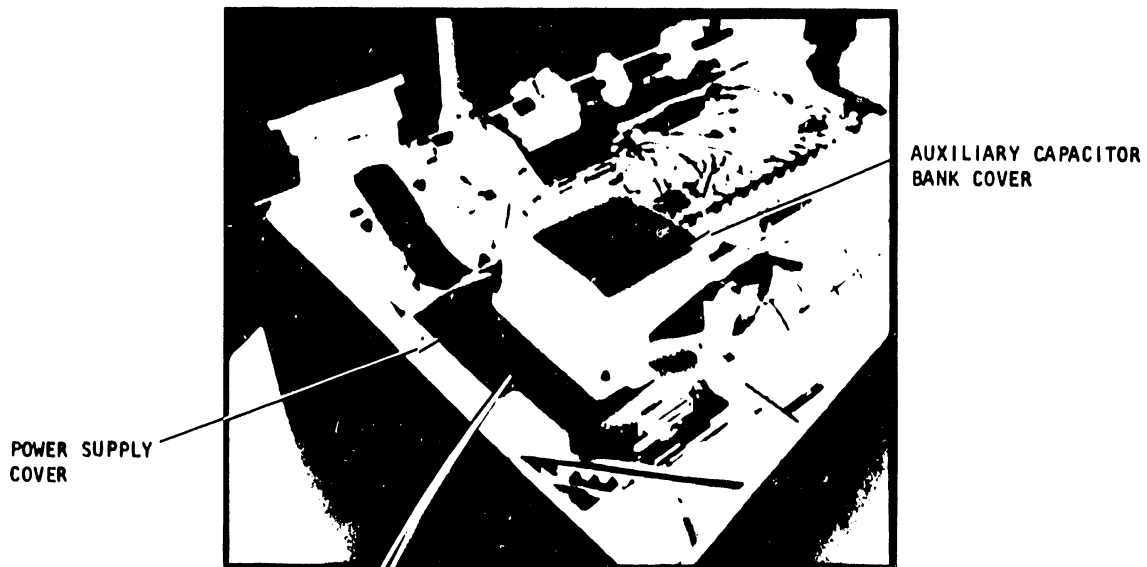
Replacement

- g. Secure the I/O Harness CCA to its mounting bracket with the four (4) screws removed in **step f**.
- h. Place the I/O Harness Assembly into position on the printer base casting and mount with the two screws removed in **step d**.
- i. Connect plug P5, removed in **step c**, to the Interface CCA.
- j. Reseat the Interface CCA into the Mother Board CCA.
- k. Replace the electronics card cage cover.
- l. Lower or replace the printer cover as instructed in the Maintenance Guide.

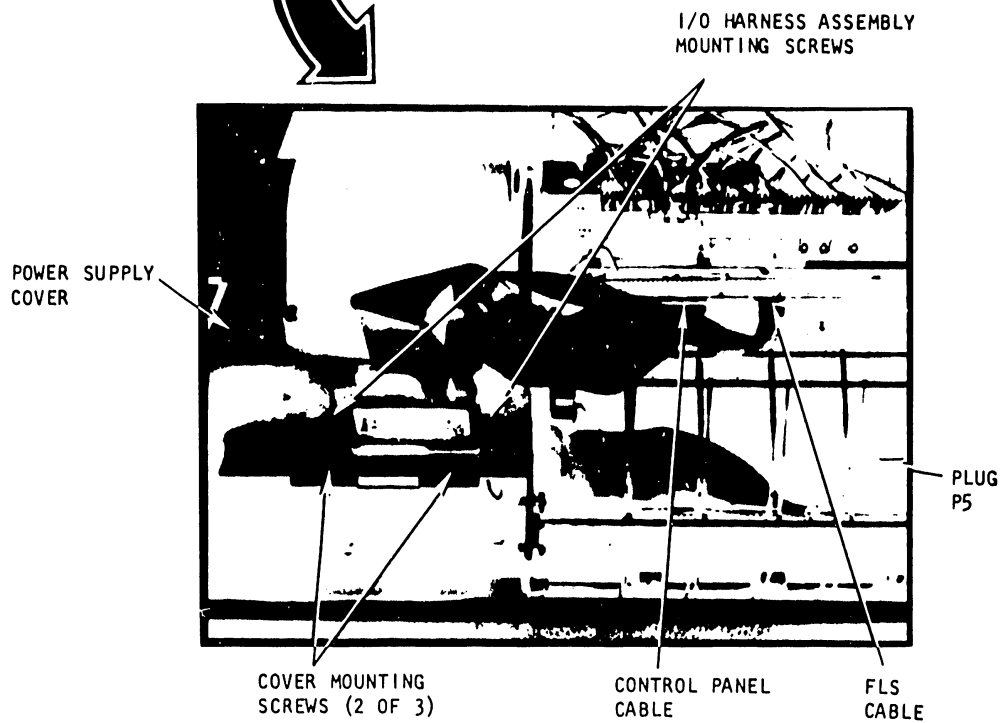
3.4.8 I/O Harness Assembly Removal/Replacement (Printers in Acoustic Cabinet) (Figure 3-18)

Removal

- a. Raise or remove the printer cover as directed in the Maintenance Guide.
- b. Remove the electronics card cage cover.
- c. Remove the control panel cable and the TCVFU and FLS cable, if these options are installed, from the top of the Interface CCA. See **figure 3-18**.
- d. Lift the Interface CCA out of its slots in the Mother Board CCA. Remove plug P5 from connector J5 at the bottom of the circuit card.
- e. Using an 8mm nut driver, remove the three (3) hex head screws fastening the power supply cover.
- f. Turn the power supply cover over to gain access to the I/O Circuit Card Assembly. (On 600 LPM or 1000 LPM printers, leave the auxiliary capacitor bank and cover in place on top of the power supply cover.)
- g. Using an 8mm nut driver, remove the two (2) screws that mount the I/O Harness Assembly connector to the power supply cover.



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Figure 3-18. I/O Harness Assembly, Printers in Acoustic Cabinet

- h. Remove the I/O Harness Assembly.
- i. Using a 7mm nut driver, remove the four (4) screws which secure the I/O Harness CCA to its mounting bracket if it is necessary to replace the I/O Harness CCA.

Replacement

- j. Secure the I/O Harness CCA to its mounting bracket with the four (4) screws removed in **step i**.
- k. Place the assembly in position inside the power supply cover. Fasten it in place with the screws removed in **step g**.
- l. Position the power supply cover on its mounts and replace the three (3) screws removed in **step e**.
- m. Connect plug P5, removed in **step d**, to the Interface CCA. See **figure 3-18**.
- n. Reseat the Interface CCA into the Mother Board CCA.
- o. Replace the electronics card cage cover.
- p. Lower or replace the printer cover. See instructions in the Maintenance Guide.

3.4.9 Mother Board CCA Removal/Replacement (Figure 3-19)

Removal

- a. Set the POWER switch to OFF.
- b. Disconnect the AC power cord from the power source.
- c. Raise or remove the printer cover. See the appropriate Maintenance Guide for instructions if needed.
- d. Remove the Paper Guide Shield.
- e. Remove the electronics card cage cover.
- f. Remove the cable plugs from the top of the Interface CCA. There will be at least two (2) plugs, one (1) from the Interlock CCA (P1) and one (1) from the Control Panel Assembly (P4). The tape reader and FLS switch plugs (P2 and P3) may also be installed.
- g. Remove the Interface CCA from the Mother Board CCA slot. Disconnect the I/O Harness Assembly plug P5 from the connector at the bottom of the Interface CCA before removing the CCA from the card cage area.

- h. Remove the Processor CCA.
- i. Disconnect the transducer cable plug P1 from the Timing and Status CCA. Remove the CCA.
- j. Disconnect the band drive motor cable plug P1, the paper feed motor cable plug P4, and, in 300 LPM and 600 LPM printers, the paper clamp solenoid cable plugs P3A and P3B. Remove the CCA.
- k. On 1000 LPM printers, remove the Hammer Bank Blower Assembly by loosening the mounting screws with an 8mm hex driver. Leave the wires connected to the blower assembly and lay it on the band cover at the front of the printer.
- l. Remove the Hammer Driver CCA(s) with the connectors intact. Lay the CCA(s) on the front of the printer.
- m. Remove the capacitor bank wire harness connector P1 from the Mother Board CCA.
- n. Remove the relay K1 from the Mother Board CCA.

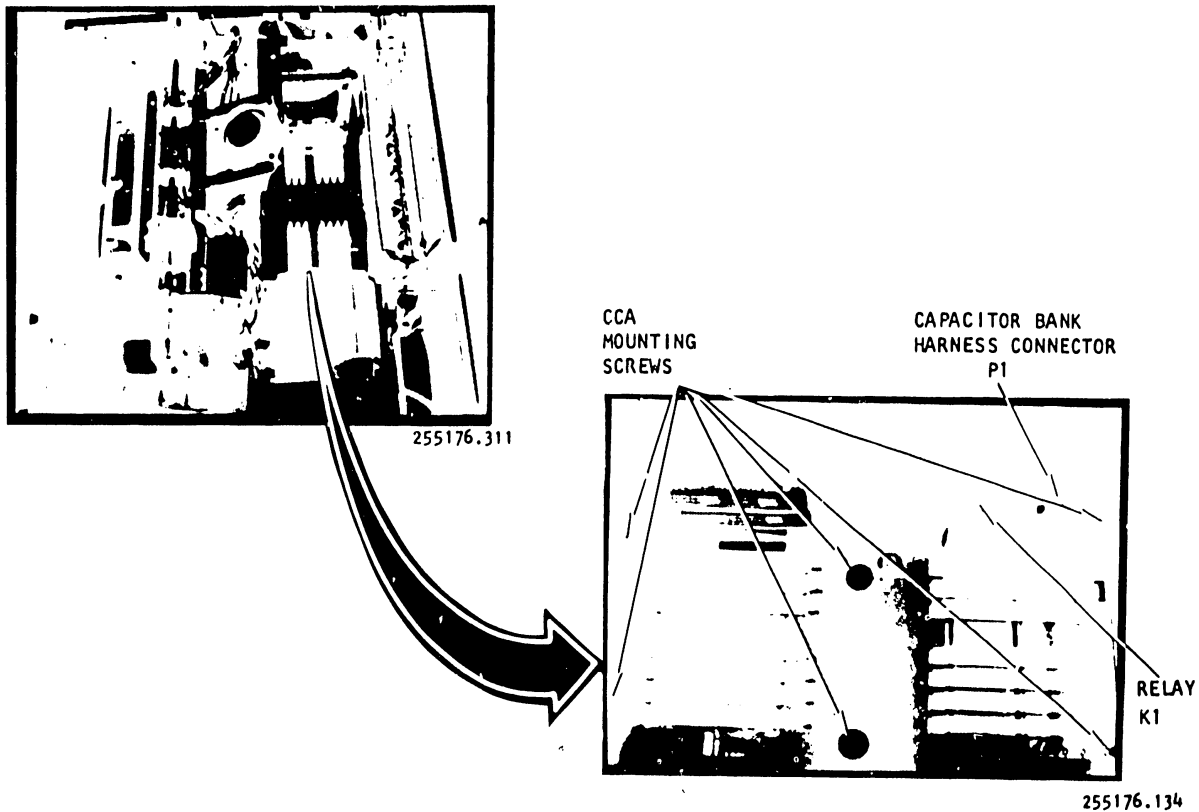


Figure 3-19. Mother Board CCA
(Acoustic Cabinet Shown)

- o. Using an 8mm nut driver, remove the six (6) screws that mount the Mother Board CCA to the printer base. Remove the CCA.

Replacement

- p. Place the Mother Board CCA into position in the printer base. Secure with the six (6) screws removed in **step o**.
- q. Replace the relay K1 and the capacitor wire harness plug P1.
- r. Replace the Hammer Driver CCA(s).
- s. Reposition the Hammer Bank Blower Assembly and secure in place by tightening the mounting screws. Make sure the three (3) washers are positioned correctly. See **figure 6-3** in volume II if needed.
- t. Replace the Power Board CCA. Reinstall the band drive motor cable and the paper feed motor cable plugs removed in **step j**. In 300 LPM and 600 LPM printers, the paper clamp solenoid cable plugs P3A and P3B must be reinstalled also.
- u. Replace the Timing and Status CCA. Connect the transducer cable plug P1.
- v. Replace the Processor CCA.
- w. Connect the I/O Harness Assembly cable plug to the J5 connector on the bottom of the Interface CCA. Replace the Interface CCA. Reconnect all cable plugs removed in **step f**.
- x. Replace the electronics card cage cover and Paper Guide Shield.
- y. Replace or lower the printer cover. See instructions provided in the Maintenance Guide or **section IV** of volume II.
- z. Reconnect the AC power cord to the power source and resume normal operations.

3.4.10 300 LPM Paper Clamp Armature Removal/Replacement (Figure 3-20)

Removal

- a. Remove the Paper Clamp Armature Assembly as directed in **steps a through h of paragraph 3.4.11**.

- b. Using a number 2 Phillips screwdriver, remove the two (2) screws that secure the mounting clamp and the Armature Spring Assembly to the armature mount. Repeat the procedure for each of the other armature spring assemblies if necessary. See **figure 3-20**.

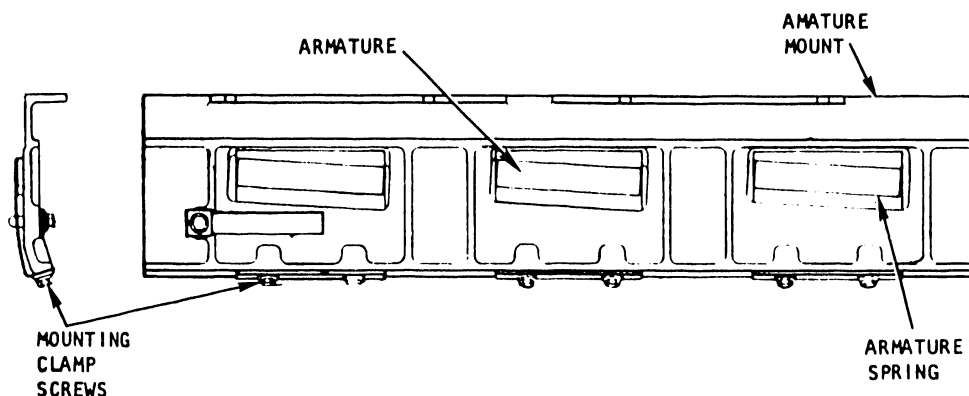


Figure 3-20. 300 LPM Paper Clamp Armature Assembly

- c. Pull the armature away from the double-faced tape which secures it to the armature spring. Remove the tape from the spring.

Replacement

- d. Clean all dirt or adhesive residue from the bonding surfaces of the armature spring and the armature.
- e. Install the armature on the armature spring with 0.5 inch polyester double-faced tape. Ensure that the tape does not protrude over the edges of the armature spring.
- f. Position the armature spring assembly and the armature clamp on the armature mount. The armature spring should not protrude beyond the lower inside edge of the armature mount.
- g. While holding the assembly in place, use a torque screwdriver with a number 2 Phillips attachment to secure the assembly with the two (2) armature mounting screws removed in **step b**. Tighten the screws to 5 in/lbs torque.
- h. Repeat the procedure for each Armature Spring Assembly removed.
- i. Replace the Paper Clamp Armature Assembly as directed in **steps i through o of paragraph 3.4.11**.

3.4.11 300 LPM Paper Clamp Armature Assembly Removal/Replacement

Removal

- a. Set the POWER switch to the off position.
- b. Disconnect the AC power plug from the power source.
- c. Open the printer cover door.
- d. Open the hammer bank.
- e. Remove the ribbon cartridge and character band as directed in the Operator's Guide.
- f. Remove the ribbon guide from the top of the platen. Instructions can be found in the Maintenance Guide. Also see **figure 3-1**.
- g. Using a 3mm hex driver, loosen the four (4) screws that secure the Paper Clamp Armature Assembly to the mechanics frame.

CAUTION

DO NOT loosen the three (3) screws which mount the platen to the printer frame.

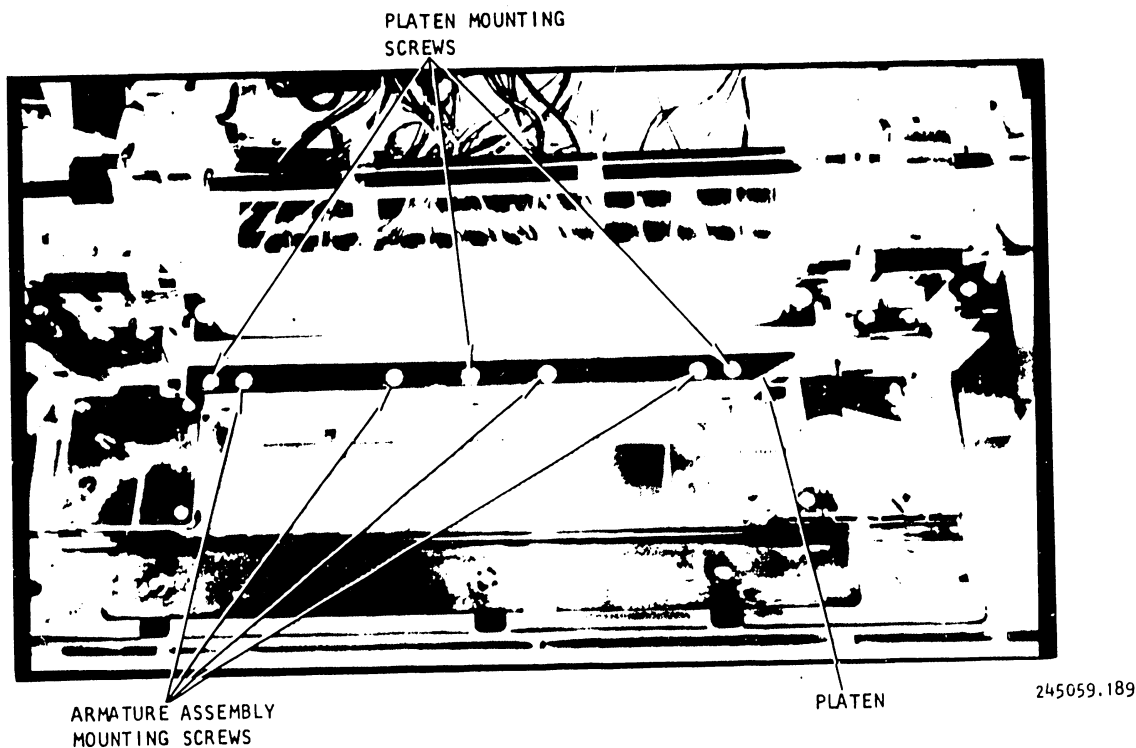


Figure 3-21. Paper Clamp Armature Assembly (Thick Platen)

- h. Slide the Paper Clamp Armature Assembly from under the platen and remove it from the printer.

Replacement

- i. Slide the armature assembly under the platen and secure it with the four (4) screws loosened in **step g**. See **figure 3-21**.
- j. Perform the Paper Clamp Armature Assembly adjustment procedure as directed in **paragraph 3.3.1**.
- k. Reinstall the ribbon guide if used, and a new character alignment scale decal. See the Maintenance Guide for instructions.
- l. Install the character band and ribbon cartridge. Instructions are provided in the Operator's Guide.
- m. Close the hammer bank.
- n. Close the printer cover door.
- o. Connect the AC power plug to the power source.

3.4.12 600 LPM Paper Clamp Armature Assembly Removal/Replacement (Figure 3-22)

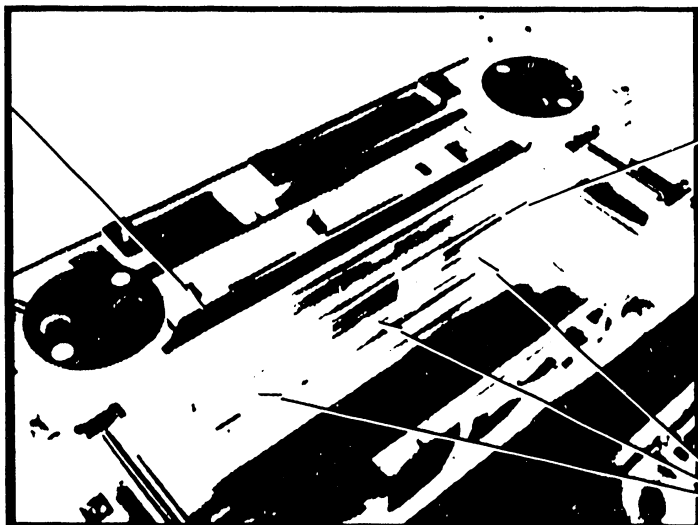
Removal

- a. Raise or remove the printer cover as directed in the Maintenance Guide.
- b. Open the hammer bank.
- c. Remove the paper low switch cable plug A19P5 from the Interlock Transition CCA. See **figure 3-16**.
- d. Remove the ribbon cartridge and character band as directed in the Operator's Guide.
- e. Using a 5mm hex driver, remove the ribbon guide from the platen as directed in the Maintenance Guide.
- f. Using a 3mm hex driver, remove the four (4) screws which secure the Paper Clamp Armature Assembly to the mechanics frame. See **figure 3-21**.

CAUTION

DO NOT loosen the three (3) screws which mount the platen to the printer frame.

CHARACTER ALIGNMENT
SCALE DECAL
SPACER (USED IN
OLDER MODEL PRINTERS)



PAPER CLAMP
ARMATURE ASSEMBLY

ARMATURES

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Figure 3-22. 600 LPM Paper Clamp Armature Assembly

- g. Slide the assembly from under the platen. Be careful not to catch plug A19P5 as it is pulled along the printer base.
- h. Remove the Paper Clamp Armature Assembly from the paper throat area.

NOTE

Any further disassembly of the 600 LPM armature assembly is not recommended.

Replacement

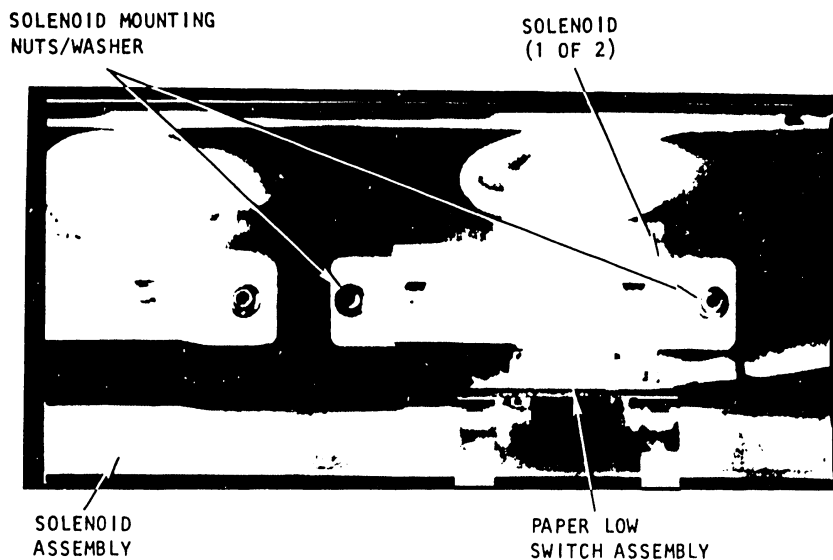
- i. Position the Paper Clamp Armature Assembly in the paper throat area and route the paper low switch cable under the platen and along the printer base to the Interlock Transition CCA.
- j. Slide the armature assembly under the platen and secure it loosely with the four (4) screws removed in **step f**.
- k. Perform the paper clamp armature adjustment procedure as directed in the Maintenance Guide.
- l. Install the ribbon guide, if used, and a new alignment scale decal if needed. See the Maintenance Guide for instructions.

- m. Install the character band and ribbon cartridge as directed in the Operator's Guide.
- n. Connect the paper low switch cable plug A19P5 to the Interface Transition CCA. See figure 3-16.
- o. Close the hammer bank.
- p. Lower or replace the printer cover. Instructions are provided in the Maintenance Guide.
- q. Connect the AC power plug to the power source.

3.4.13 Paper Clamp Solenoid Removal/Replacement
(300 LPM and 600 LPM Printers Only) (Figures 3-23 and 3-24)

Removal

- a. Using a 4mm hex driver, remove the Paper Clamp Solenoid Assembly as directed in the Maintenance Guide.
- b. Using a 6mm nut driver, remove the two (2) nuts and washers which mount the solenoid to the solenoid mounting assembly.



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Figure 3-23. 300 LPM Paper Clamp Solenoid Assembly

Replacement

- c. Place the solenoid in position and secure with the two (2) nuts and washers removed in **step b**.
- d. Replace the Paper Clamp Solenoid Assembly as instructed in the Maintenance Guide.
- e. Perform the Paper Clamp Solenoid Assembly adjustment procedure. See the Maintenance Guide for instructions.

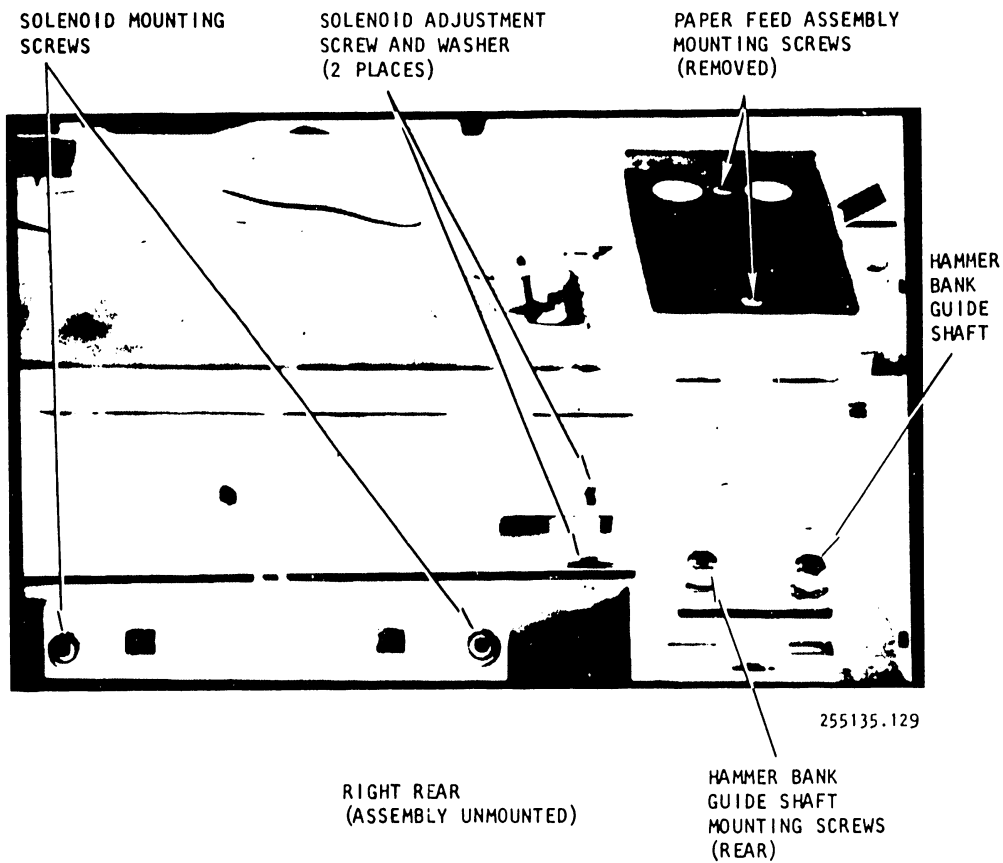


Figure 3-24. 600 LPM Paper Clamp Solenoid Assembly Removal/Replacement

3.4.14 Paper Entrance Cover Removal/Replacement (Figure 3-25)

Removal

- a. Set the POWER switch to the off position.
- b. Disconnect the AC power plug from the power source.
- c. Open the paper entrance cover.
- d. Using an 8mm nut driver, loosen the four (4) screws which secure the paper entrance cover hinge brackets.
- e. Close the paper entrance cover.
- f. Slip the end hooks of the two (2) end springs from their corresponding hooks on the hinge brackets.
- g. Carefully unhook the paper entrance cover from the two (2) hinge brackets.

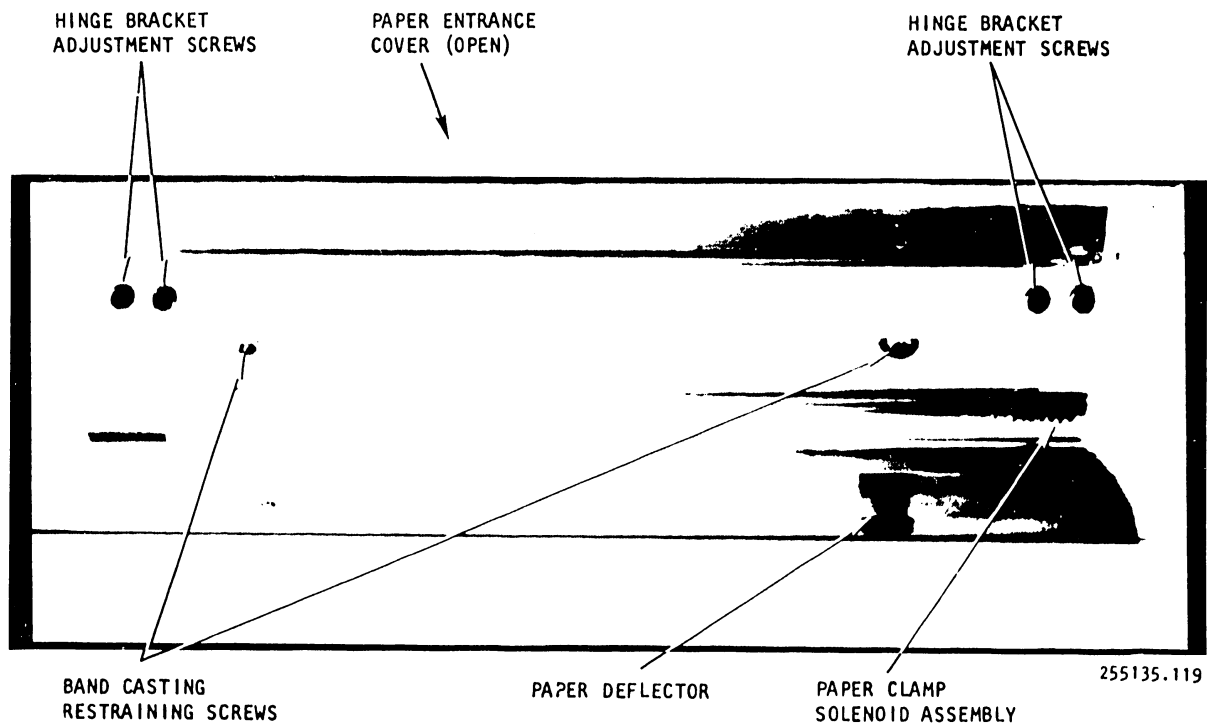


Figure 3-25. Paper Entrance Cover Assembly
(Under Base Assembly)

Replacement

- h. Hook the paper entrance cover onto the two (2) hinge brackets.
- i. Close the paper entrance cover.
- j. Pull on the two (2) end springs and slip their end hooks on the hinge brackets.
- k. Perform the Paper Entrance Cover Assembly adjustment procedure as directed in the Maintenance Guide.
- l. Connect the AC power plug to the power source.

3.4.15 600 LPM/1000 LPM Paper Low Switch Assembly Removal/Replacement (Figure 3-26)

Removal

- a. Raise or remove the printer cover as directed in the Maintenance Guide.
- b. Remove the Paper Clamp Armature Assembly as directed in **paragraph 3.4.12**. Instructions for removing the 1000 LPM Pressure Roller Assembly are in the 1000 LPM Maintenance Guide.
- c. Using a 5.5mm nut driver, remove the two (2) screws and the washers which secure the paper low switch to the armature or pressure roller mounting. See **figure 3-26**.

CAUTION

Do not bend the paper low switch actuator lever.

- d. Remove the Power Low Switch Assembly.

Replacement

- e. Place the Paper Low Switch Assembly and the cable clamp into position on the armature or pressure roller mounting.
- f. Secure the Paper Low Switch Assembly and the cable clamp loosely with the screws and washers removed in **step c**.

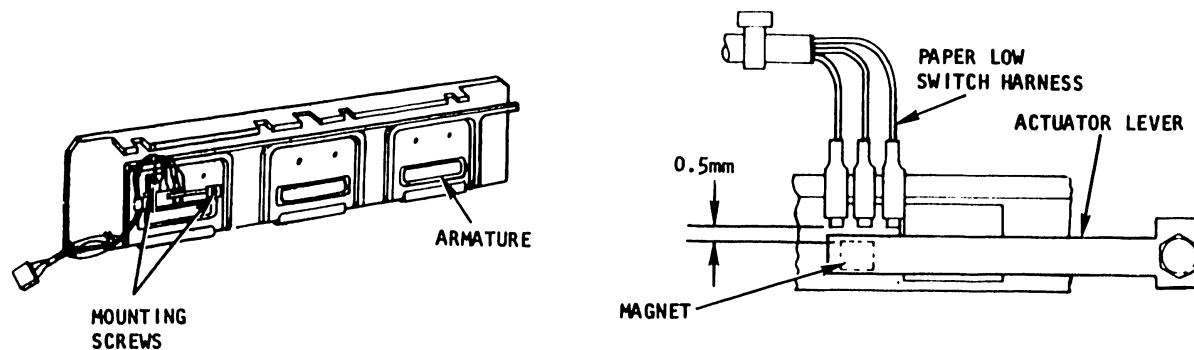


Figure 3-26. 600 LPM and 1000 LPM Paper Low Switch

- g. Using a feeler gauge, ensure that a 0.5mm gap exists between the magnet on the switch actuator lever and the switch.
- h. Tighten the two mounting screws.
- i. Replace the Paper Clamp Armature Assembly as directed in paragraph 3.4.12.
- j. Lower or replace the printer cover. See the Maintenance Guide for instructions if needed.
- k. Connect the AC power plug to the power source.

3.4.16 Paper Motion Sensor Removal/Replacement (Figure 3-27)

Removal

- a. Raise or remove the printer cover as directed in the Maintenance Guide.
- b. Disconnect the paper motion sensor cable plug P2 from the Interlock Transition CCA. See figure 3-16.

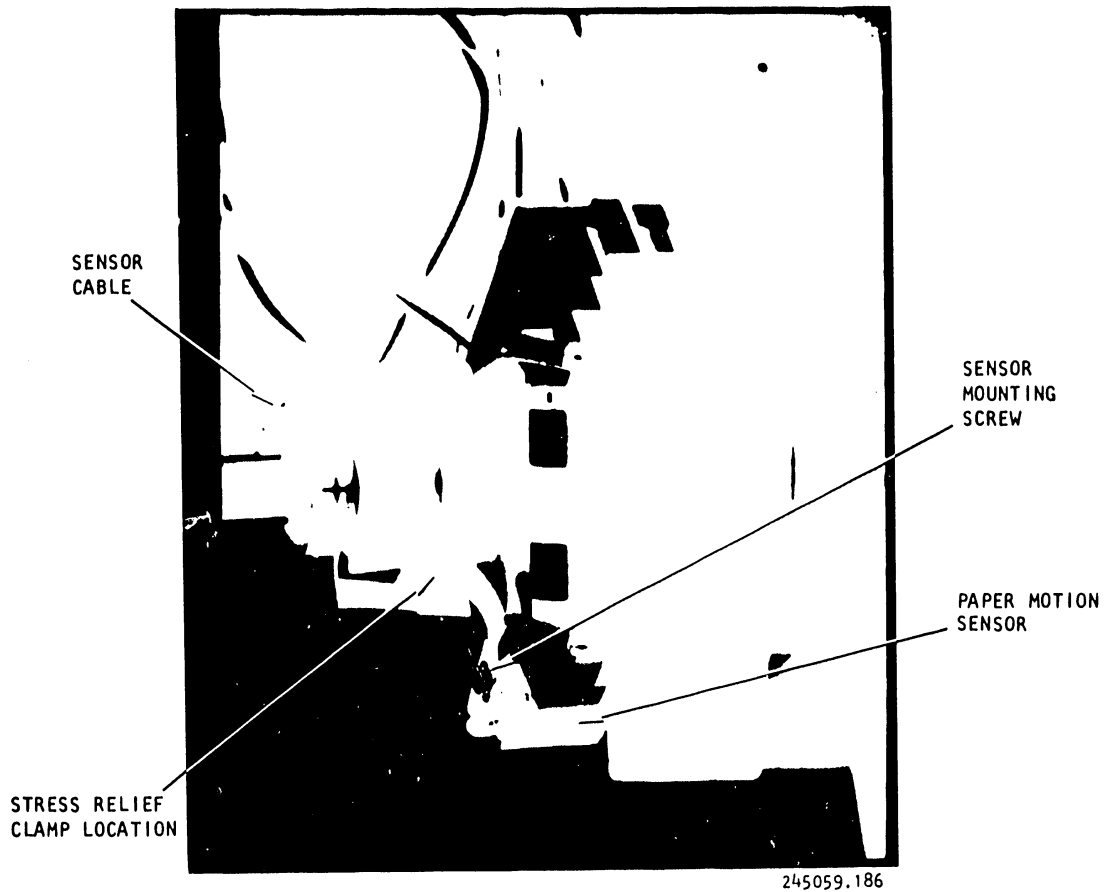


Figure 3-27. Paper Motion Sensor Removal/Replacement

- c. Slide the left Paper Feed Tractor Assembly toward the center of the printer to allow easy access to the paper motion sensor mounting screw.
- d. Remove the cable stress relief clamp.
- e. Using a 4.5mm nut driver, remove the two (2) screws that secure the paper motion sensor to the left paper feed tractor assembly, and remove the sensor and its cable.

Replacement

- f. Secure the paper motion sensor and its cable to the left tractor assembly with the screws removed in **step e**.
- g. Replace the cable stress relief clamp removed in **step d**.
- h. Reposition the left Paper Feed Tractor Assembly.

- i. Reconnect the paper motion sensor cable plug P2 to the Interlock Transition CCA.
- j. Lower or replace the printer cover.
- k. Connect the AC power plug to the power source.

3.4.17 Platen Removal/Replacement
(Figures 3-28 and 3-29)

NOTE

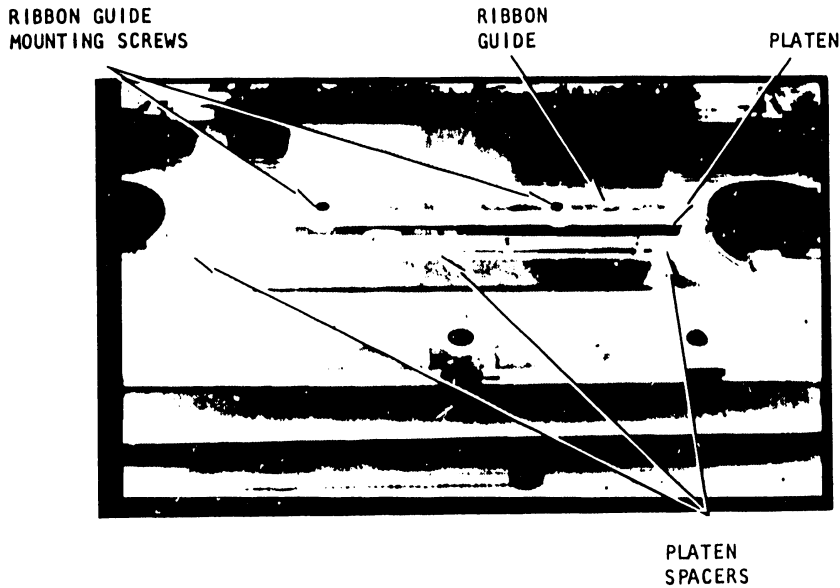
THE PLATEN IS NOT NORMALLY A
FIELD-REPLACEABLE COMPONENT.
Once set, the platen should not need
resetting.

Removal

- a. Raise or remove the printer cover as directed in the Maintenance Guide.
- b. Remove the ribbon cartridge and character band as directed in the Operator's Guide.
- c. Examine the platen. It will be one (1) of four (4) configurations. Gain access to the platen and the 1000 LPM Pressure Roller Assembly or the platen and the 300 LPM and 600 LPM Paper Clamp Armature Assembly as follows:
 1. Thick platen: peel off the Character Alignment Scale Decal. See **figure 3-3**.
 2. Thin platen with press-fit ribbon guide: use moderate force and lift the ribbon guide free of the platen. This will also remove the Character Alignment Scale decal which is attached to the guide. See **figure 3-2**.
 3. Thin platen with screw-mounted ribbon guide: pierce the character alignment scale decal at columns 30 and 92. Then follow directions in the appropriate Maintenance Guide if needed. See **figure 3-1**.
 4. Vespel-lined platen with screw mounted ribbon guide: follow the directions for the thin platen with the screw-mounted ribbon guide.

NOTE

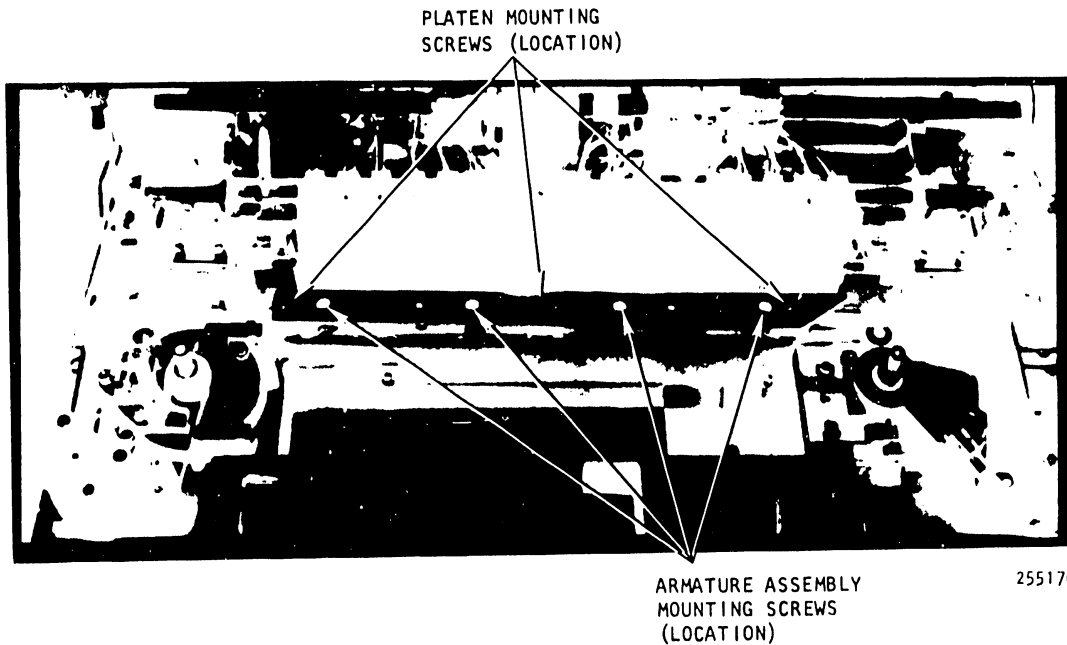
The thin platens and the Vespel-lined platen use three (3) spacers under the platen and over the mounting holes.



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Figure 3-28. Platen

- d. Remove the Paper Clamp Armature Assembly. See paragraphs 3.4.11 and 3.4.12. For 1000 LPM printers, remove the Pressure Roller Assembly as directed in the 1000 LPM Maintenance Guide.



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Figure 3-29. Platen without Screw-Mounted Ribbon Guide

- e. Using a 4mm hex driver or 8mm nut driver, remove the three (3) screws that mount the platen to the printer casting.
- f. Remove the platen. If the thin platen is being removed, the platen spacers can be left in position over the mounting holes.

Replacement

- g. Place the platen and the platen spacers, if required, in position in the printer casting.
- h. Secure the platen loosely with the three (3) screws removed in **step e**.
- i. Perform the platen adjustment procedure. See **paragraph 3.3.2** for instructions.
- j. Replace the Paper Clamp Armature Assembly or the Pressure Roller Assembly. Instructions are given in **paragraphs 3.4.11 or 3.4.12**. The Pressure Roller Assembly replacement instructions are in the 1000 LPM Maintenance Guide.
- k. Adjust the Paper Clamp Armature Assembly. See **paragraph 3.3.1**. For the 1000 LPM Pressure Roller Assembly adjustment, see the 1000 LPM Maintenance Guide.
- l. Install the ribbon guide, if used, and a new character alignment scale decal as instructed in the Maintenance Guide.
- m. Replace the ribbon cartridge and character band. See the Operator's Guide if needed.
- n. Lower or replace the printer cover. See the Maintenance Guide or **section IV** in volume II.
- o. Connect the AC power plug to the power source.

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BETICAL
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SPARES

LIST

BY

WANG

P/N

The following tables provide conversion between Wang and DP part numbers.

Recommended Spares List by Wang P/N

WANG P/N	OEM P/N	DESCRIPTION
726-1100	249235-001	PNL CNTRL CCA CO
726-1101	251165-001	HAM'R DR CCA CO
726-1102	256440-001	INTLK TRANS CCA CO
726-1102-1	273340-001	INTERLOCK TRANSITION PCB
726-1103	251995-001	PCA MB
726-1104	257375-001	PWR BD
726-1105	257315-001	PROCESSOR CCA
726-1106	251725-001	RECT (STD) CCA
726-1107	257520-001	TIMING & STATUS CCA
726-1108	257265	I FACE CENTER CCA
726-1109	251985-001	REC UNIV CCA
726-1110	257290-001	DCDING PRM KT (OPT)
726-1111	247930-001	VFU CCA
726-1112	248008-001	SCRW BACKSTOP
726-1113	250005-002	BAND 64 EDD REPL BY 7262600
726-1114	251704-009	BRNG KIT
726-1115	251704-011	BRNG MT RIGHT
726-1116	242462-001	BUSHING MT LEFT
726-1117	251704-023	BELT RIB OR KIT
726-1118	801669-001	BELT TIMING
726-1119	801675-001	BTN ALARM CLEAR
726-1120	801675-002	BTN ON/OFF LINE
726-1121	801674-001	BTN PAPER STEP
726-1122	801674-002	BTN TOP OF FORM
726-1123	801743-003	CAP 27,000 VF 75V
726-1124	801743-001	CAP 83,000 UF 15V
726-1125	251035-001	CAP BANK ASSY
726-1126	801732-004	CKT BRKR
726-1127	257301-001	C PNL ASSY
726-1128	257385-001	DECAL CHAR ALIGN
726-1129	247967-001	DECAL C/PNL BOT
726-1130	247966-002	DECAL C/PNL TOP
726-1131	256472-001	DECAL RIB & STATUS
726-1132	801746-001	DISPLAY DIGITAL
726-1133	246039-001	FAN ASSY
726-1134	801379-002	IC HAMMER DR
726-1135	251704-001	HAM'R MOD KIT
726-1136	251704-014	HARDWARE PACK MIS
726-1137	246125-001	HARN ASSY
726-1138	242443-001	HARN ASSY CAPBANK
726-1139	249221-001	HARN ASSY
726-1140	256210-001	HARN ASSY I/O
726-1141	246381-002	HARN ASSY PAPER
726-1142	251072-001	HARN ASSY PS
726-1143	251830-001	IDLER SHAFT ASSY
726-1144	801655-001	KNOB
726-1145	801766-001	LED GREEN
726-1146	246164-002	MTR ASSY BAND
726-1147	246200-004	MTR ASY PAPER FEED
726-1148	251704-002	PLY PAPER FEED

WANG P/N	OEM P/N	DESCRIPTION
726-1149	251941-001	SEN PAPER MOTION
726-1150	251704-006	PIV ARM & SPR.(REPL BY 7261203)
726-1151	250503-002	PROM BND IMAGE 64
726-1152	249320-001	PRM KIT FLSSW/OVFU
726-1153	257294-001	PLY + DR ASSY
726-1154	800795-301	RELAY
726-1155	251071-001	RES ASSY PWR PRELD
726-1156	801850-002	RES VARI COPIES
726-1157	801850-001	RES VAR PHASE
726-1158	251705-002	RIB DR ASSY(REPL BY 7261182)
726-1159	257251-001	RIB MASK ASSY
726-1160	251704-005	RIB RLR KIT
726-1161	251704-012	SCRW/NUT/WA PACK
726-1162	251925-001	SOL ASSY
726-1163	251704-013	SPR RETAIN RING
726-1164	246290-001	SPROCKET ASSY L
726-1165	246267-001	SPROCKET ASSY R
726-1166	800129-004	SW BAND INTLK
726-1167	801767-001	SW BASE PBTN (REPL BY 3252456)
726-1168	801768-001	SW BASE PBTN
726-1169	800679-003	SW HAMR
726-1170	801899-001	SW PAPER LOW
726-1171	801704-001	SW G2 POS.
726-1172	801704-002	SW G3 POS
726-1173	251704-007	XFMR CV STD
726-1174	800018-001	XSTOR FOR PWR BD.
726-1175	810100-001	XSTOR FOR PWR BD
726-1176	251704-4	XDUCER (REPLACED BY 7261200)
726-1178	247968-001	OBS USE 7252591
726-1179	251025-001	PBS ISE 7252591
726-1180	247962-001	PAPR SUPPORT GUIDE
726-1181	242454-001	CLCH P-FEED W/SHAFT
726-1182	251705-001	RIB DR ASSY
726-1183	801732-003	CKT BRKR UNIV
726-1184	246380-001	MTR ASSY VFU
726-1186	801649-001	VFU HD READER ASSY
726-1187	251076-001	HARN PS
726-1188	251075-001	RES ASSY PWR PRELD
726-1189	251704-008	XFMR CV UNIV
726-1190	257315-001	HARN I/O W/TERM
726-1190	257315-001	HARN I/O W/TERM REPL BY 7261105
726-1191	256440-001	DUPL USE 7261102
726-1192	244444-002	HAM'R BANK ASSY
726-1193	801760-405	CAP RES'T 60HZ
726-1194	251704-005	RLR PINCH (REPLACED BY 7261160)
726-1195	251823-001	REPLACED BY 7261203
726-1199	251976-001	XDUCER HARN ASSY
726-1200	251704-004	XDUCER BRKT KIT
726-1201	801508-406	SCRW SET XDUCER
726-1202	251704-10	BUSH'G (PLAS) + RET
726-1203	251704-006	PIV AEM + SPR
726-1204	256511-001	SPR PIV ARM (REPL BY 7261206)
726-1205	247880-001	
726-1205	251165-001	PCA HAM'R DR
726-1206	256511-001	RIB SENCOR
726-1207	257290-001	PROM DECODE

WANG P/N	OEM P/N	DESCRIPTION
726-1208	251704-015	HAM'R MOD KIT 600LP
726-1209	251704-016	HAM'R MOD KIT 600LP
726-1210	248023	HAM'R BANK ASSY B6
726-1211	257435-001	HDER KIT B300
726-1212	257435-003	HDER KTI B300
726-1213	257436-001	HDER KIT B300
726-1214	257436-003	HDER KIT B600
726-1215	251190-001	MOTHERBOARD 600LP
726-1216	251926-001	CLAMP SOL MASK ASSY
726-1217	250531-001	PROM PRCSR 300LP REPL/7261221
726-1218	250581-999	PROM PRCESSR 600LP(RPL/7261222)
726-1219	257320-001	PWR BD 250LPM
726-1220	10K6	FLTR 10 AMP
726-1221	250584-999	PROM PROC
726-1221-1	273370-999	B300 PROCESSOR PROMS (KIT)
726-1222	250583-999	PROM PROC
726-1222-1	273372-999	B600 PROCESSOR PROMS (KIT)
726-1223	257435-004	HDR KIT T&S
726-1224	257436-004	HDR KIT HAMR DR
726-1225	247963-001	GUIDE CLIP
726-1226	257208-001	HINGE (L)
726-1227	257208-002	HINGE (R)
726-1228	257344-001	PCA TERM & HARN
726-1229	810447-001	TINSL STAT
726-1230	238840-001	BACKSTOP SCREW
726-1230	248008-001	
726-1231	800625-005	BEARING, DRUM
726-1232	801632-001	BELT, DRUM 96
726-1233	800299-013	BELT PAPER FEED
726-1234	800092-257	CAP, 71K VF, 2
726-1235	800092-407	CAP, 48K VF, 1
726-1236	800092-758	CAP, 30K, VF,
726-1237	242060-002	CAP PACK ASSY
726-1238	237600-001	CCA, B.P. M. DR,
726-1239	237595-001	CCA, B.P., M. DR
726-1240	251625-003	CCA, CONFIG, MICRO P
726-1241	237640-001	CCA, EMITTER, PF
726-1242	238005-001	CCA, HAMMER DR
726-1243	244535-	CCA, I/O
726-1244	236847-001	CCA, PWR DIST
726-1245	257715-001	CCA REGULATOR
726-1246	237635-001	CCA, SENSOR, PF
726-1247	237865-001	CCA, VDE HAMMER SUPP
726-1248	237865-001	CCA, VDE HAMMER SUPP
726-1249	800797-005	CKT/BRKR
726-1250	241523-001	CNTRL PNL ASSY
726-1251	243370-002	DRUM X-DUCER SPARES
726-1252	800316-080	FUSE, 8 AMP REGULATO
726-1253	800316-150	FUSE, 15 AMP REGULAT
726-1254	800917-151	FUSE, 15AM 50 H3, ST
726-1255	237851-171	HAMMER MODULE
726-1256	800163-006	LAMP, IND
726-1257	801082-001	LAMP, LED VISIBLE
726-1258	247568-001	LAT. ADJ. HOUSING KI
726-1259	801346-001	MTR, BLWR
726-1260	800954-001	MTR, DRUM
726-1261	801325-001	MTR, PAPER FEED

WANG P/N	OEM P/N	DESCRIPTION
726-1262	81002-001	MTR, RIB
726-1263	238039-002	PAPER TENSIONER
726-1264	243362-001	PRES. PLATE, TRACTOR
726-1265	243364-001	PRES. PLATE, TRACTOR
726-1266	801010-001	RELAY, 12V, OPOT
726-1267	247335-001	SPOOL RIB
726-1268	800502-010	SW., 6/8 LPI
726-1269	800129-001	SW., DG INT
726-1270	800502-011	SW., FORMS R
726-1271	237810-001	SW., PAPER OUT ASSY
726-1272	233585-005	SW., PAPER, TOP LEFT
726-1273	800129-007	SW., PLENUM
726-1274	243365-001	TRACTOR ASSY, RI
726-1275	243365-002	TRACTOR ASSY, LE
726-1276	801456-002	TRACTOR CHAIN, .151
726-1277	247526-001	TRACTOR SPR
726-1278	801139-001	XFORMER, PWR
726-1279	237950-001	CCA, CAM SENSOR
726-1280	237650-001	CCA, CNTRL
726-1281	237655-002	CCA, RIB SENSOR
726-1282	801150-001	MTR, AC
726-1283	800617-006	BELT
726-1284	247587-001	MTR ASSY
726-1285	240125-006	TAPE READER
726-1286	801680-001	STATIC ELIMINATOR BA
726-1287	237728-001	PAPER MOTION SENSOR
726-1288	801096-003	PWR PAK
726-1289	251407-017	CCA, CONFIGURED SOFT
726-1290	246714-001	ROLLER DR. ASSY
726-1291	246710-001	ROLLER PRES. ASSY
726-1292	257069-002	PROM, MICROPROCESSOR
726-1293	257069-002	PROM, MICROPROCESSOR
726-1294	257069-003	PROM, MICROPROCESSOR
726-1295	243348-001	PROM, VFU
726-1296	243348-002	PROM, VFU
726-1297	243348-003	PROM, VFU
726-1298	800316-120	FUSE, 12A, 250N
726-1299	800917-020	FUSE, 2A, 250V S/B
726-1507	268596-002	RIB SEN & CBL ASSY
726-1508	818009-001	CAR HOME SENSOR
726-1509	268792-001	CNTRL PNL
726-1510	268704-001	LOGIC PCB
726-1511	268866-001	ANALOG PCB
726-1512	268312-001	SERIAL INTRFC PCB
726-1513	268291-002	MOTHERBOARD
726-1514	268182-002	PWR SUPPLY
726-1515	268869-001	P/W MTR & XDUCER
726-1516	268899-001	PAPER GUIDE ASSY
726-1517	268501-001	PAPER OUT SW & CBL AS
726-1518	268352-004	PINCH ROLLER & SUPPORT ASSY
726-1519	818562-001	PWR SW
726-1520	268657-002	PRTR WHEEL HUB
726-1521	268598-002	RIB MTR & CBL ASSY
726-1522	268119-001	RIB DR BUSHING ASSY
726-1523	268884-001	SPR KIT
726-1524	818595-001	SW
726-1525	265234-001	HAMMER ASSY

WANG P/N	OEM P/N	DESCRIPTION
726-1526	268361-005	PLATEN ASSY
726-1527	268224-002	CBL ASSY
726-1528	268715-001	CBL ASSY
726-1529	268497-001	CBL ASSY
726-1530	268562-001	CBL ASSY
726-1531	268876-001	CAR INTCON BD
726-1532	268109-003	CHANNEL
726-1533	268850-001	FTA PLUNGER KIT
726-1534	268383-002	C/D MTR XDUCER
726-1535	265157-003	P/D MTR ASSY
726-1536	268843-001	BAIL ROLLERS
726-1537	268849-001	BAIL ARM KIT
726-1538	268848-001	PAPER RELEASE LEVER
726-1539	268746-001	C/D CBL KIT
726-1540	268278-001	P/D IDLER GEAR
726-1541	268847-001	C/D PLY
726-1542	268597-002	SOLENOID ASSY
726-1543	268765-003	PROM, LOGIC (U-2)
726-1544	269144-001	PROM KIT, SERIAL INTRFC
726-1545	818550-001	FAN
726-1546	818553-001	LINE FILTER
726-1547	269339-001	PAPER SHEILD
726-1548	268498-002	PWR MODULE
726-1549	818559-001	VOLTAGE SELECT
726-1550	800238-014	BELT RIBBON DRIVE
726-1551	904263-002	FIELD RIB SEN RETRO KIT W/MASK
726-1552	256332-001	FORMS COMPRESSOR B-600
726-1553	273920-001	STACKER PS-LOG PCB
726-1554	800295-019	CLUTCH ASSY RIBBON DR
726-1555	273888-001	COUPLING ASSY
726-1556	263725-001	TRANSFORMER ASSY
726-1557	269792-003	RS232 INTRF ASSY WITH FIRM WARE
726-1558	810762-002	DELICTOR PHOT COL. 136
726-1559	810817-001	SURGE RESISTOR ASSY (FCO 6651)
726-1560	277738-XXX	PROCESSOR PROM KIT (NEW)
726-1561	274290-001	T & S PROM
726-1562	274290-002	T & S PROM (NEW)
726-1563	277923-001	CAP PAD ASSY (NEW)
726-1564	800129-004	SWITCH COVER INTERLOCK
726-1700	800917-200	FUSE, 20A S/B
726-1701	263089-001	CVR LATCH N.S.(RPL BY 7261702)
726-1702	267451-001	LATCH AND KEEPER KIT
726-1703	800742-001	NPN XSISTOR
726-1704	801592-001	IC74S301N
726-1705	242580-001	HINGE ASSY LEFT(RPL BY 7261226)
726-1706	242580-002	HINGE AS RIGHT(RPL BY 7261227)
726-1707	800132-001	XSISTOR DPC 205
726-1708	800192-001	XSISTOR DPC 209
726-1709	800533-003	RES.5 PHM
726-1710	801749-001	DI IN3880
726-1711	801821-001	XTAL ODC BD
726-1712	801753-001	BUS BAR TWO COND.
726-1713	801713-001	IC RAM 256X4 mos
726-1714	2N3253	XSISTOR
726-1715	800210-205	RES 20HM 1%
726-1716	801592-001	IC RAM 256X1

WANG P/N	OEM P/N	DESCRIPTION
726-1717	246126-001	FLEXIBLE LINK(RPL BY 7261153)
726-1718	800133-001	XSISTOR DPC
726-1720	800084-382	RES 680 OHM 1&
726-1721	801737-040	CON. PCB HDR
726-1722	800917-200	FUSE 20A3AG(RPL BY 7261700)
726-1723	801634-001	ICIM370
726-1724	257380-001	PAPER CLAMP COIL
726-1725	800171-022	PLY GROUNDED 54 T
726-1726	257435-005	HDER KIT
726-1727	267372-001	RIB SENSE HARN
726-1728	263476-001	BAND DR MTR ASSY
726-1729	257570-001	BAND DR PLY
726-1730	801669-006	RIB DR BELT
726-1731	263455-0C1	RIB DR ASSY
726-1732	246381-002	PAPER OUT SW(RPL BY 7261141)
726-1733	810205-001	B-600 PAPER OUT FC
726-1734	251127-002	B-600 PAPER OUT FC A
726-1735	251086-001	B-600 AUX CAP PACK
726-1736	257454-001	BOTTOM OF FORM GUIDE
726-1737	263458-001	RIB DR PLY
726-1738	263006-001	IDLER ASSY POSI RIBB
726-1739	263477-001	TENSION ARM (RPL BY 7261728)
726-1740	263363-001	SPR TENSION RIBBO
726-1741	263388-201/25743	COVER PRTR W/FORM
726-1742	251120-200/25741	DOOR PRTR W/FORMA
726-1745	801580-001	BEARING, PAPER PULLE
726-1746	810538-001	BEARING, TRACTOR, FL
726-1747	810360-001	BELT, PAPER FEED
726-1748	801669-002	BELT, PAPER PULLER
726-1749	810728-001	BELT, TRACTOR
726-1750	800299-019	BELT, TRACTOR ADJ
726-1751	810468-001	CBL, TRACTOR
726-1752	248994-001	CAM, TILT IDLER
726-1753	801743-006	CAP, 37K UFO, 75V
726-1754	248789-001	CAP, PACK ASSY
726-1755	801760-156	CAP, X-FORMER 15MFD,
726-1756	267965-001	CCA, BAND GATE ELEC.
726-1757-1	274395-002	CCA HAMMER CONTROL
726-1758	267565-002	CCA, HAMMER DR (INVALID OEM #)
726-1759	267550-001	CCA, MOTHER BOARD
726-1760	270130-001	CCA, PAPER FEED
726-1762-1	270070-001	CCA PROCESSOR
726-1762-2	274490-001	CCA PROCESSOR
726-1763	270449-001	CCA, CNTRL PNL
726-1764	270310-001	CCA TIMING & STATUS
726-1764-1	277685-001	CCA TIMING AND STATUS
726-1765	800797-006	CKT/BRKR
726-1766	248625-001	CLUTCH ASSY, HORIZ P
726-1767	248469-001	SLIP CLUTCH ASS, PAP
726-1768	263865-001	DECAL, UPR CNTRL
726-1769	263866-001	DECAL, LWR CNTRL
726-1770	270188-001	DECAL, REAR CNTRL
726-1771	266607-001	FAN ASSY
726-1771-1	270457-002	FAN ASSY
726-1772	801086-003	LINE FILTER
726-1773	270118-003	HARDWARE PACK, KIT
726-1774	270077-001	HDER KIT

WANG P/N	OEM P/N	DESCRIPTION
726-1775	268045-001	HOSE, AIR
726-1776	263932-001	INDUCTOR ASSY, DISCH
726-1777	800669-002	KNOB, PAPER FEED
726-1778	810356-001	LAMP, CNTRL PNL
726-1779	267933-001	LATCH ASSY, BAND GAT
726-1780	266511-001	MTR, BAND DR
726-1780-1	274375-001	MTR, BAND DR
726-1781	266512-001	MTR, BAND POSITION
726-1781-1	274382-001	MTR, BAND POSITION
726-1782	248471-001	MTR, PAPER FEED
726-1783	810341-001	MTR, PAPER PULLER
726-1784	810351-001	MTR, RIB DESKEW
726-1785	810384-001	MTR, RIB DAIVE
726-1786	251941-001	PAPER MOTION SENSOR
726-1787	810422-001	POT, COPIES CNTRL
726-1788	248409-001	PLY, BAND DR
726-1789	248410-001	PLY, BAND IDLER
726-1790	248671-001	PLY, BELT/CBL
726-1791	248622-001	PLY, IDLER, TRACT
726-1792	266590-001	PLY, PAPER FO MOT
726-1793	248477-001	PLY, TRACTOR DR.
726-1794	270297-001	PLY, PULLER 84 TO
726-1795	248609-001	PLY, PULLER 30 TO
726-1796	810345-001	RELAY, RIB REVERS
726-1797	800795-302	RELAY, 55 VOLTS PHOT
726-1798	810391-001	RIB EDGE SENSOR
726-1799	810392-002	RIB EDGE SENSOR
726-1830	270118-004	SCREW/NUT WASHER PAC
726-1831	248349-001	SPOOL RIB DR
726-1832	270118-002	SPR KIT
726-1833	810496-001	GAS SPR, TOP COVE
726-1834	810548-001	SW, BAND GATE, I
726-1835	810205-002	SW, PAPER-OUT
726-1836	810748-001	SW, DESKEW (ON/N)
726-1837	800502-003	SW, TOGGLE (ON/O)
726-1838	800502-017	SW, TOGGLE (ON/O)
726-1839	800502-018	SW, TOGGLE
726-1840	810500-002	SW, REAR CNTRL
726-1841	270125-001	SHIELD, RIB
726-1846	268076-001	XDUCER ASSY
726-1847	810511-001	XFORMER, CVT
726-1848	801096-004	PWR SUPPLY, STATIC
726-1849	263668-001	LINE COUNTER KIT
726-1850	801669-005	BELT, STACKER
726-1851	810471-001	CBL, SENSOR, STACK
726-1852	810468-002	CBL, SHELF, STACKE
726-1853	263700-001	CCA, L.E.D. DR,
726-1854	270090-001	CCA, PHOTO PICKUP,S
726-1855	263705-001	CCA, PWR & LOGIC,
726-1856	800917-010	FUSE, 1A STACKER
726-1857	810645-001	MTR W/GEAR BOX, ST
726-1858	248958-001	PLY, CBL, STACK
726-1859	248966-001	PLY, STACKER
726-1860	248976-001	PLY, IDLER, STACK
726-1861	266618-001	PLY ASSY, MTR,
726-1862	810582-001	SW, CUT OFF, STA
726-1863	800931-001	SW, ROCKER ON/OF

WANG P/N	OEM P/N	DESCRIPTION
726-1865	270041-110	SKIN SET
726-1866	263966-201	TOP COVER (TOP HALF)
726-1867	263965-201	TOP COVER (BOTTOM HA)
726-1868	263970-200	BEZEL
726-1869	267990-201	HINGE GUARD
726-1870	263967-200	LEFT SIDE PNL
726-1871	263968-200	LEFT QUARTER PNL
726-1872	270043-200	RIGHT SIDE PNL
726-1873	270044-200	RIGHT QUARTER PNL
726-1874	263978-200	DOOR PNL ACCESS
726-1875	263971-200	REAR COVER
726-1876	270440-001	CCA INTERFACE
726-1877	244514001	IDLER ROLLER
726-1878	274196-001	PWR CBL SIBLINK
726-1879	270435-001	CBL ASSY INTERFACE
726-1880	268025-001	CCA, COLUMN INDICATOR

**RECOMMENDED
SPARES LIST
BY DATA PRODUCTS
P/N**

The following tables provide conversion between Wang and DP part numbers

Recommended Spares List by Data Products P/N

OEM P/N	WANG P/N	DESCRIPTION
10K6	726-1220	FLTR 10 AMP
233585-005	726-1272	SW., PAPER, TOP LEFT
236847-001	726-1244	CCA, PWR DIST
237595-001	726-1239	CCA, B.P., M. DR
237600-001	726-1238	CCA, B.P. M. DR,
237635-001	726-1246	CCA, SENSOR, PF
237640-001	726-1241	CCA, EMITTER, PF
237650-001	726-1280	CCA, CNTRL
237655-002	726-1281	CCA, RIB SENSOR
237728-001	726-1287	PAPER MOTION SENSOR
237810-001	726-1271	SW., PAPER OUT ASSY
237851-171	726-1255	HAMMER MODULE
237865-001	726-1247	CCA, VDE HAMMER SUPP
237865-001	726-1248	CCA, VDE HAMMER SUPP
237950-001	726-1279	CCA, CAM SENSOR
238005-001	726-1242	CCA, HAMMER DR
238039-002	726-1263	PAPER TENSIONER
238840-001	726-1230	BACKSTOP SCREW
240125-006	726-1285	TAPE READER
241523-001	726-1250	CNTRL PNL ASSY
242060-002	726-1237	CAP PACK ASSY
242443-001	726-1138	HARN ASSY CAPBANK
242454-001	726-1181	CLCH P-FEED W/SHAFT
242462-001	726-1116	BUSHING MT LEFT
242580-001	726-1705	HINGE ASSY LEFT(RPL BY 7261226)
242580-002	726-1706	HINGE AS RIGHT(RPL BY 7261227)
243348-001	726-1295	PROM, VFU
243348-002	726-1296	PROM, VFU
243348-003	726-1297	PROM, VFU
243362-001	726-1264	PRES. PLATE, TRACTOR
243364-001	726-1265	PRES. PLATE, TRACTOR
243365-001	726-1274	TRACTOR ASSY, RI
243365-002	726-1275	TRACTOR ASSY, LE
243370-002	726-1251	DRUM X-DUCER SPARES
244444-002	726-1192	HAM'R BANK ASSY
244514001	726-1877	IDLER ROLLER
244535-	726-1243	CCA, I/O
246039-001	726-1133	FAN ASSY
246125-001	726-1137	HARN ASSY
246126-001	726-1717	FLEXIBLE LINK(RPL BY 7261153)
246164-002	726-1146	MTR ASSY BAND
246200-004	726-1147	MTR ASY PAPER FEED
246267-001	726-1165	SPROCKET ASSY R
246290-001	726-1164	SPROCKET ASSY L
246380-001	726-1184	MTR ASSY VFU
246381-002	726-1141	HARN ASSY PAPER
246381-002	726-1732	PAPER OUT SW(RPL BY 7261141)
246710-001	726-1291	ROLLER PRES. ASSY
246714-001	726-1290	ROLLER DR. ASSY
247335-001	726-1267	SPOOL RIB

OEM P/N	WANG P/N	DESCRIPTION
247526-001	726-1277	TRACTOR SPR
247568-001	726-1258	LAT. ADJ. HOUSING KI
247587-001	726-1284	MTR ASSY
247880-001	726-1205	
247930-001	726-1111	VFU CCA
247962-001	726-1180	PAPR SUPPORT GUIDE
247963-001	726-1225	GUIDE CLIP
247966-002	726-1130	DECAL C/PNL TOP
247967-001	726-1129	DECAL C/PNL BOT
247968-001	726-1178	OBS USE 7252591
248008-001	726-1112	SCRW BACKSTOP
248008-001	726-1230	
248023	726-1210	HAM'R BANK ASSY B6
248349-001	726-1831	SPOOL RIB DR
248409-001	726-1788	PLY, BAND DR
248410-001	726-1789	PLY,BAND IDLER
248469-001	726-1767	SLIP CLUTCH ASS, PAP
248471-001	726-1782	MTR, PAPER FEED
248477-001	726-1793	PLY, TRACTOR DR.
248609-001	726-1795	PLY, PULLER 30 TO
248622-001	726-1791	PLY, IDLER, TRACT
248625-001	726-1766	CLUTCH ASSY, HORIZ P
248671-001	726-1790	PLY, BELT/CBL
248789-001	726-1754	CAP, PACK ASSY
248958-001	726-1858	PLY, CBL, STACK
248966-001	726-1859	PLY, STACKER
248976-001	726-1860	PLY, IDLER, STACK
248994-001	726-1752	CAM, TILT IDLER
249221-001	726-1139	HARN ASSY
249235-001	726-1100	PNL CNTRL CCA CO
249320-001	726-1152	PRM KIT FLSSW/OVFU
250005-002	726-1113	BAND 64 EDD REPL BY 7262600
250503-002	726-1151	PROM BND IMAGE 64
250531-001	726-1217	PROM PRCSR 300LP REPL/7261221
250581-999	726-1218	PROM PRCESSR 600LP(RPL/7261222)
250583-999	726-1222	PROM PROC
250584-999	726-1221	PROM PROC
251025-001	726-1179	PBS ISE 7252591
251035-001	726-1125	CAP BANK ASSY
251071-001	726-1155	RES ASSY PWR PRELD
251072-001	726-1142	HARN ASSY PS
251075-001	726-1188	RES ASSY PWR PRELD
251076-001	726-1187	HARN PS
251086-001	726-1735	B-600 AUX CAP PACK
251120-200/25741	726-1742	DOOR PRTR W/FORMA
251127-002	726-1734	B-600 PAPER OUT FC A
251165-001	726-1101	HAM'R DR CCA CO
251165-001	726-1205	PCA HAM'R DR
251190-001	726-1215	MOTHERBOARD 600LP
251407-017	726-1289	CCA, CONFIGURED SOFT
251625-003	726-1240	CCA, CONFIG, MICRO P
251704-001	726-1135	HAM'R MOD KIT
251704-002	726-1148	PLY PAPER FEED
251704-004	726-1200	XDUCER BRKT KIT
251704-005	726-1160	RIB RLR KIT
251704-005	726-1194	RLR PINCH (REPLACED BY 7261160)
251704-006	726-1150	PIV ARM & SPR.(REPL BY 7261203)

OEM P/N	WANG P/N	DESCRIPTION
251704-006	726-1203	PIV AEM + SPR
251704-007	726-1173	XFMR CV STD
251704-008	726-1189	XFMR CV UNIV
251704-009	726-1114	BRNG KIT
251704-011	726-1115	BRNG MT RIGHT
251704-012	726-1161	SCRW/NUT/WA PACK
251704-013	726-1163	SPR RETAIN RING
251704-014	726-1136	HARDWARE PACK MIS
251704-015	726-1208	HAM'R MOD KIT 600LP
251704-016	726-1209	HAM'R MOD KIT 600LP
251704-023	726-1117	BELT RIB OR KIT
251704-10	726-1202	BUSH'G (PLAS) + RET
251704-4	726-1176	XDUCER (REPLACED BY 7261200)
251705-001	726-1182	RIB DR ASSY
251705-002	726-1158	RIB DR ASSY(REPL BY 7261182)
251725-001	726-1106	RECT (STD) CCA
251823-001	726-1195	REPLACED BY 7261203
251830-001	726-1143	IDLER SHAFT ASSY
251925-001	726-1162	SOL ASSY
251926-001	726-1216	CLAMP SOL MASK ASSY
251941-001	726-1149	SEN PAPER MOTION
251941-001	726-1786	PAPER MOTION SENSOR
251976-001	726-1199	XDUCER HARN ASSY
251985-001	726-1109	REC UNIV CCA
251995-001	726-1103	PCA MB
256210-001	726-1140	HARN ASSY I/O
256332-001	726-1552	FORMS COMPRESSOR B-600
256440-001	726-1102	INTLK TRANS CCA CO
256440-001	726-1191	DUPL USE 7261102
256472-001	726-1131	DECAL RIB & STATUS
256511-001	726-1204	SPR PIV ARM (REPL BY 7261206)
256511-001	726-1206	RIB SENCOR
257069-002	726-1292	PROM, MICROPROCESSOR
257069-002	726-1293	PROM, MICROPROCESSOR
257069-003	726-1294	PROM, MICROPROCESSOR
257208-001	726-1226	HINGE (L)
257208-002	726-1227	HINGE (R)
257251-001	726-1159	RIB MASK ASSY
257265	726-1108	I FACE CENTER CCA
257290-001	726-1110	DCDING PRM KT (OPT)
257290-001	726-1207	PROM DECODE
257294-001	726-1153	PLY + DR ASSY
257301-001	726-1127	C PNL ASSY
257315-001	726-1105	PROCESSOR CCA
257315-001	726-1190	HARN I/O W/TERM
257315-001	726-1190	HARN I/O W/TERM REPL BY 7261105
257320-001	726-1219	PWR BD 250LPM
257344-001	726-1228	PCA TERM & HARN
257375-001	726-1104	PWR BD
257380-001	726-1724	PAPER CLAMP COIL
257385-001	726-1128	DECAL CHAR ALIGN
257435-001	726-1211	HDER KIT B300
257435-003	726-1212	HDER KTI B300
257435-004	726-1223	HDR KIT T&S
257435-005	726-1726	HDER KIT
257436-001	726-1213	HDER KIT B300
257436-003	726-1214	HDER KIT B600

OEM P/N	WANG P/N	DESCRIPTION
257436-004	726-1224	HDR KIT HAMR DR
257454-001	726-1736	BOTTOM OF FORM GUIDE
257520-001	726-1107	TIMING & ST TUS CCA
257570-001	726-1729	BAND DR PLY
257715-001	726-1245	CCA REGULATOR
263006-001	726-1738	IDLER ASSY POSI RIBB
263089-001	726-1701	CVR LATCH N.S.(RPL BY 7261702)
263363-001	726-1740	SPR TENSION RIBBO
263388-201/25743	726-1741	COVER PRTR W/FORM
263455-001	726-1731	RIB DR ASSY
263458-001	726-1737	RIB DR PLY
263476-001	726-1728	BAND DR MTR ASSY
263477-001	726-1739	TENSION ARM (RPL BY 7261728)
263668-001	726-1849	LINE COUNTER KIT
263700-001	726-1853	CCA, L.E.D. DR,
263705-001	726-1855	CCA, PWR & LOGIC,
263725-001	726-1556	TRANSFORMER ASSY
263865-001	726-1768	DECAL, UPR CNTRL
263866-001	726-1769	DECAL, LWR CNTRL
263932-001	726-1776	INDUCTOR ASSY, DISCH
263965-201	726-1867	TOP COVER (BOTTOM HA)
263966-201	726-1866	TOP COVER (TOP HALF)
263967-200	726-1870	LEFT SIDE PNL
263968-200	726-1871	LEFT QUARTER PNL
263970-200	726-1868	BEZEL
263971-200	726-1875	REAR COVER
263978-200	726-1874	DOOR PNL ACCESS
265157-003	726-1535	P/D MTR ASSY
265234-001	726-1525	HAMMER ASSY
266511-001	726-1780	MTR, BAND DR
266512-001	726-1781	MTR, BAND POSITION
266590-001	726-1792	PLY, PAPER FO MOT
266607-001	726-1771	FAN ASSY
266618-001	726-1861	PLY ASSY, MTR,
267372-001	726-1727	RIB SENSE HARN
267451-001	726-1702	LATCH AND KEEPER KIT
267550-001	726-1759	CCA, MOTHER BOARD
267565-002	726-1758	CCA, HAMMER DR (INVALID OEM #)
267933-001	726-1779	LATCH ASSY, BAND GAT
267965-001	726-1756	CCA, BAND GATE ELEC.
267990-201	726-1869	HINGE GUARD
268025-001	726-1880	CCA, COLUMN INDICATOR
268045-001	726-1775	HOSE, AIR
268076-001	726-1846	XDUCER ASSY
268109-003	726-1532	CHANNEL
268119-001	726-1522	RIB DR BUSHING ASSY
268182-002	726-1514	PWR SUPPLY
268224-002	726-1527	CBL ASSY
268278-001	726-1540	P/D IDLER GEAR
268291-002	726-1513	MOTHERBOARD
268312-001	726-1512	SERIAL INTRFC PCB
268352-004	726-1518	PINCH ROLLER &SUPPORT AS
268361-005	726-1526	PLATEN ASSY
268383-002	726-1534	C/D MTR XDUCER
268497-001	726-1529	CBL ASSY
268498-002	726-1548	PWR MODULE
268501-001	726-1517	PAPER OUT SW & CBL AS

OEM P/N	WANG P/N	DESCRIPTION
268562-001	726-1530	CBL ASSY
268596-002	726-1507	RIB SEN & CBL ASSY
268597-002	726-1542	SOLENOID ASSY
268598-002	726-1521	RIB MTR & CBL ASSY
268657-002	726-1520	PRTR WHEEL HUB
268704-001	726-1510	LOGIC PCB
268715-001	726-1528	CBL ASSY
268746-001	726-1539	C/D CBL KIT
268765-003	726-1543	PROM, LOGIC (U-2)
268792-001	726-1509	CNTRL PNL
268843-001	726-1536	BAIL ROLLERS
268847-001	726-1541	C/D PLY
268848-001	726-1538	PAPER RELEASE LEVER
268849-001	726-1537	BAIL ARM KIT
268850-001	726-1533	FTA PLUNGER KIT
268866-001	726-1511	ANALOG PCB
268869-001	726-1515	P/W MTR & XDUCER
268876-001	726-1531	CAR INTCON BD
268884-001	726-1523	SPR KIT
268899-001	726-1516	PAPER GUIDE ASSY
269144-001	726-1544	PROM KIT, SERIAL INTRFC
269339-001	726-1547	PAPER SHEILD
269792-003	726-1557	RS232 INTRF ASSY WITH FIRM WARE
270041-110	726-1865	SKIN SET
270043-200	726-1872	RIGHT SIDE PNL
270044-200	726-1873	RIGHT QUARTER PNL
270070-001	726-1762-1	CCA PROCESSOR
270077-001	726-1774	HDER KIT
270090-001	726-1854	CCA, PHOTO PICKUP,S
270118-002	726-1832	SPR KIT
270118-003	726-1773	HARDWARE PACK, KIT
270118-004	726-1830	SCREW/NUT WASHER PAC
270125-001	726-1841	SHIELD, RIB
270130-001	726-1760	CCA, PAPER FEED
270188-001	726-1770	DECAL, REAR CNTRL
270297-001	726-1794	PLY, PULLER 84 TO
270310-001	726-1764	CCA TIMING & STATUS
270435-001	726-1879	CBL ASSY INTERFACE
270440-001	726-1876	CCA INTERFACE
270449-001	726-1763	CCA, CNTRL PNL
270457-002	726-1771-1	FAN ASSY
273340-001	726-1102-1	INTERLOCK TRANSITION PCB
273370-999	726-1221-1	B300 PROCESSOR PROMS (KIT)
273372-999	726-1222-1	B600 PROCESSOR PROMS (KIT)
273888-001	726-1555	COUPLING ASSY
273920-001	726-1553	STACKER PS-LOG PCB
274196-001	726-1878	PWR CBL SIBLINK
274290-001	726-1561	T & S PROM
274290-002	726-1562	T & S PROM (NEW)
274375-001	726-1780-1	MTR, BAND DR
274382-001	726-1781-1	MTR, BAND POSITION
274395-002	726-1757-1	CCA HAMMER CONTROL
274490-001	726-1762-2	CCA PROCESSOR
277685-001	726-1764-1	CCA TIMING AND STATUS
277738-XXX	726-1560	PROCESSOR PROM KIT (NEW)
277923-001	726-1563	CAP PAD ASSY (NEW)
2N3253	726-1714	XSISTOR

OEM P/N	WANG P/N	DESCRIPTION
800018-001	726-1174	XSTOR FOR PWR BD.
800084-382	726-1720	RES 680 OHM 1&
800092-257	726-1234	CAP, 71K VF, 2
800092-407	726-1235	CAP, 48K VF, 1
800092-758	726-1236	CAP, 30K, VF, .
800129-001	726-1269	SW., DG INT
800129-004	726-1166	SW BAND INTLK
800129-004	726-1564	SWITCH COVER INTERLOCK
800129-007	726-1273	SW., PLENUM
800132-001	726-1707	XSISTOR DPC 205
800133-001	726-1718	XSISTOR DPC
800163-006	726-1256	LAMP, IND
800171-022	726-1725	PLY GROUNDED 54 T
800192-001	726-1708	XSISTOR DPC 209
800210-205	726-1715	RES 20HM 1%
800238-014	726-1550	BELT RIBBON DRIVE
800295-019	726-1554	CLUTCH ASSY RIBBON DR
800299-013	726-1233	BELT PAPER FEED
800299-019	726-1750	BELT, TRACTOR ADJ
800316-080	726-1252	FUSE, 8 AMP REGULATO
800316-120	726-1298	FUSE, 12A, 250N
800316-150	726-1253	FUSE, 15 AMP REGULAT
800502-003	726-1837	SW, TOGGLE (ON/O)
800502-010	726-1268	SW., 6/8 LPI
800502-011	726-1270	SW., FORMS R
800502-017	726-1838	SW, TOGGLE (ON/O)
800502-018	726-1839	SW, TOGGLE
800533-003	726-1709	RES.5 PHM
800617-006	726-1283	BELT
800625-005	726-1231	BEARING, DRUM
800669-002	726-1777	KNOB, PAPER FEED
800679-003	726-1169	SW HAMR
800742-001	726-1703	NPN XSISTOR
800795-301	726-1154	RELAY
800795-302	726-1797	RELAY, 55 VOLTS PHOT
800797-005	726-1249	CKT/BRKR
800797-006	726-1765	CKT/BRKR
800917-010	726-1856	FUSE, 1A STACKER
800917-020	726-1299	FUSE, 2A, 250V S/B
800917-151	726-1254	FUSE, 15AM 50 H3, ST
800917-200	726-1700	FUSE, 20A S/B
800917-200	726-1722	FUSE 20A3AG(RPL BY 7261700)
800931-001	726-1863	SW, ROCKER ON/OF
800954-001	726-1260	MTR, DRUM
801010-001	726-1266	RELAY, 12V, OPOT
801082-001	726-1257	LAMP, LED VISIBLE
801086-003	726-1772	LINE FILTER
801096-003	726-1288	PWR PAK
801096-004	726-1848	PWR SUPPLY, STATIC
801139-001	726-1278	XFORMER, PWR
801150-001	26-1282	MTR, AC
801325-001	726-1261	MTR, PAPER FEED
801346-001	726-1259	MTR, BLWR
801379-002	726-1134	IC HAMMER DR
801456-002	726-12762	TRACTOR CHAIN, .151
801508-406	726-1201	SCRW SET XDUCER

OEM P/N	WANG P/N	DESCRIPTION
801580-001	726-1745	BEARING, PAPER PULLE
801592-001	726-1704	IC74S301N
801592-001	726-1716	IC RAM 256X1
801632-001	726-1232	BELT, DRUM 96
801634-001	726-1723	IC1M370
801649-001	726-1186	VFU HD READER ASSY
801655-001	726-1144	KNOB
801669-001	726-1118	BELT TIMING
801669-002	726-1748	BELT, PAPER PULLER
801669-005	726-1850	BELT, STACKER
801669-006	726-1730	RIB DR BELT
801674-001	726-1121	BTN PAPER STEP
801674-002	726-1122	BTN TOP OF FORM
801675-001	726-1119	BTN ALARM CLEAR
801675-002	726-1120	BTN ON/OFF LINE
801680-001	726-1286	STATIC ELIMINATOR BA
801704-001	726-1171	SW G2 POS.
801704-002	726-1172	SW G3 POS
801713-001	726-1713	IC RAM 256X4 mos
801732-003	726-1183	CKT BRKR UNIV
801732-004	726-1126	CKT BRKR
801737-040	726-1721	CON. PCB HDR
801743-001	726-1124	CAP 83,000 UF 15V
801743-003	726-1123	CAP 27,000 VF 75V
801743-006	726-1753	CAP, 37K UFO, 75V
801746-001	726-1132	DISPLAY DIGITAL
801749-001	726-1710	DI IN3880
801753-001	726-1712	BUS BAR TWO COND.
801760-156	726-1755	CAP, X-FORMER 15MFD.
801760-405	726-1193	CAP RES'T 60HZ
801766-001	726-1145	LED GREEN
801767-001	726-1167	SW BASE PBTN (REPL BY 3252456)
801768-001	726-1168	SW BASE PBTN
801821-001	726-1711	XTAL ODC BD
801850-001	726-1157	RES VAR PHASE
801850-002	726-1156	RES VARI COPIES
801899-001	726-1170	SW PAPER LOW
81002-001	726-1262	MTR, RIB
810100-001	726-1175	XSTOR FOR PWR BD
810205-001	726-1733	B-600 PAPER OUT FC
810205-002	726-1835	SW, PAPER-OUT
810341-001	726-1783	MTR, PAPER PULLER
810345-001	726-1796	RELAY, RIB REVERS
810351-001	726-1784	MTR, RIB DESKEW
810356-001	726-1778	LAMP, CNTRL PNL
810360-001	726-1747	BELT, PAPER FEED
810384-001	726-1785	MTR, RIB DAIVE
810391-001	726-1798	RIB EDGE SENSOR
810392-002	726-1799	RIB EDGE SENSOR
810422-001	726-1787	POT, COPIES CNTRL
810447-001	726-1229	TINSL STAT
810468-001	726-1751	CBL, TRACTOR
810468-002	726-1852	CBL, SHELF, STACKE
810471-001	726-1851	CBL, SENSOR, STACK
810496-001	726-1833	GAS SPR, TOP COVE
810500-002	726-1840	SW, REAR CNTRL
810511-001	726-1847	XFORMER, CVT

OEM P/N	WANG P/N	DESCRIPTION
810538-001	726-1746	BEARING, TRACTOR, FL
810548-001	726-1834	SW, BAND GATE, I
810555-001	726-1864	X-FORMER, STACKER
810582-001	726-1862	SW, CUT OFF, STA
810645-001	726-1857	MTR W/GEAR BOX, ST
810728-001	726-1749	BELT, TRACTOR
810748-001	726-1836	SW, DESKEW (ON/N)
810762-002	726-1558	DELICTOR PHOT COL. 136
810817-001	726-1559	SURGE RESISTOR ASSY (FCO 6651)
818009-001	726-1508	CAR HOME SENSOR
818550-001	726-1545	FAN
818553-001	726-1546	LINE FILTER
818559-001	726-1549	VOLTAGE SELECT
818562-001	726-1519	PWR SW
818595-001	726-1524	SW
904263-002	726-1551	FIELD RIB SEN RETRO KIT W/MASK



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