

Service Newsletter

No. 121

August 11, 1978

2200/2600 #23

2200VP/MVP FAN REPLACEMENT WITH LARGE I/O CONTROLLERS

Some 2200 System I/O controllers are slightly larger than others. Because of this, when five or more of these boards are to be installed in a 2200 VP or MVP, the fan must be changed to accommodate the longer boards. The procedure for changing the fan is as follows:

Parts Necessary:

Fan - WL# ~~400-1013~~ *400-1029*
4 Screws - WL# 650-3169
4 Keps Nuts 6-32 - WL# 652-0032

1. Unplug line cord from outlet.
2. Remove all I/O boards..
3. Unplug cord and remove skeleton fan WL# 400-1010.
4. To aid in spacer removal, insert screws (650-3169) into spacers.
5. Tap spacers from inside chassis with a hammer several times until they pop through side of chassis.
6. Remove spacers.
7. Install venturi type fan WL# 400-1013 using holes left by removed spacers (airflow to outside of chassis). Fasten into place using screws (650-3169) and Keps Nuts (652-0032).
8. Attach fan cord.
9. Install I/O boards.
10. Check for proper air flow.

WANG

LABORATORIES, INC

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ORIGINATOR: Lattie Dean REVIEWED BY: Jim Smith

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ALL OFFICES X HOME OFFICE _____ EACH EMPLOYEE _____

SUBJECT: LVP CHECKLIST PAGE 1 OF 4

LVP/MVP SYSTEM CHECK LIST

1. PCB's must be updated to current E Rev.

PCB #	Current E Rev.	Must be at least	Comments
210-6789	0	0	R5 Proms
210-6790	7	6	
210-6791-1	3	3	Use-1 only
210-6792	5	4	
210-6793-1	4	3	Must be E Rev 4 for expanded memory
210-7397	6	6	New Style MVP/Reg.
210-7397-1	2	2	Special
210-6798	4	2	Need Rev 4 for 16K Ram
210-7587	1	1	
210-7588	3	3	
210-7588-1	3	3	
210-7887	7	7	SVP
210-7789A	3	3	SVP
210-7890	4	4	
210-7697	7	7	LVP Regulator
210-7797	0	0	LVP C's
210-7796	0	0	LVP C's
210-7925	2	2	LVP/SVP
210-8696A	0	0	R9 Proms
210-8694	3	3	LVP/SVP
210-8794	2	2	LVP/SVP

210-7397 - There is a preliminary ECN to this Regulator to raise the foldback point of the 12 Volt P/S.

- Change R37 to 2.2K Pin 11 L9
- Change C20 to 1 uf Pin 9 L9

2. On MVP's, the MXE's and MXD's must be installed next to the CPU. Change the fan over the I/O to a 400-1001 if more than 2 large controllers are installed. See TAC NL 30125, Section IV.A.3. Drill or knockout the old mounting so the fan will be as close to the fram as possible.

3. On the LVPC, replace both fans with 400-1011 105 CFM Roton MU2A2 for better air flow. Refer to TAC NL 30208, Section IV.A.3.

4. Verify that the shields are connected on both ends of the RS232 cables. This shield must be grounded at the Terminal and the CPU Controller.

5. Static proof all 2236D and 2236DE Terminals. A heavy duty staple gun and 1/4 inch uncoated staple makes for a much better job. The screws for the RS232 cable must be tight on both ends.

6. 2236DE's and DW's must be verified for all updates.

The current Prom level for the 270-0753 is R5's.

<u>2236DE</u>	<u>2236DW</u>
L9 - 6013 R5	L9 - 6013 R5
L10 - 6079 R5	L10 - 6014 R5
2236DE	210-7743C
2236DW	210-7743A

The power supply in the 2336 is a high failure item. Do not overlook the P/S for intermittent problems isolated to one terminal.

7. On the MVP +/- 0 Volts should be tied to chassis ground.

8. Verify with a scope that the LVP power supply ripple is within specification especially the +24V DC.

9. All cables must be tight at both the controller and device. Printers and 2280 DPU cables must be updated to a 220-0105-3. This cable has better shielding and has more noise immunity.

10. The MXD must be updated with the 2 caps if it has a 7591 Daughter board. See FCO 1035.

11. The 2280 Phoenix must have the shielded DPU cables installed and the line filter installed in the DPU.

12. The CPU must be checked for ripple with a scope. The 120V 6000 uf caps are high failure item.

13. The 2280 DPU E Rev's are:

	<u>E Rev.</u>	<u>Comment</u>
210-7416	2	Motherboard
210-7421	3	
210-7422	4	
210-7423	4	R7 Prom
210-7424	9	
210-7415	0	
210-7715	4	MUX DPU
210-7717	2	MUX DPU
210-7718	1	MUX DPU

14. If there is a mag tape, the I/O cable must be grounded at the CPU and the tape unit. A 2280 DPU cable clamp with a short piece of wire can be used to ground it at the CPU to a controller thumb screw.

15. On MVP's, verify that the 2 power transistors on the heat sink are 375-1072 (2N5685), and not a 375-1048 (2N5301).

16. If there is a Band Printer then both the static kit (part #728-0006, PSN 111C10-4) and the cover latch kit (part #726-1702, refer to TAC NL 20209, Section III.C.10) must be installed if needed.

17. On MXD's verify continuity of Port 2 Pin 7 to the other 3 Ports. Should boards be missing a jumper to Pin 7 Port 2, it will cause intermittent problems on Port 2 only.

18. Anodized controller rails should be cleaned to insure good contact when thumb screws are tightened.

19. Chassis ground on 2236MXD not secure should go to Pin 11, Section 3 to rail and RS232 Pin. (Active not resolved).

20. Pin 11, Section 3 of I/O section on LVP's not connected to chassis ground. (Active not resolved).

21. On LVP's the reference voltage on the 210-8694, 8794 must be set to exactly 4 Volts with a range of at least 1 1/2 turns on the floppy and Winchester VCO Pot.

22. Some MVPC update kits were shipped without the longer card support bracket to support the additional cards in a MVPC. The part number for this bracket is 270-0732. This bracket should be installed on the "next call", on any MVPC that does not already have it installed.

Thanks to Lattie Dean, DTS Greensboro District for his inputs.

4103 (IV.A.3)

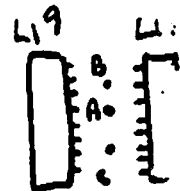
2236 MUX D - FOR 19.2 K



LABORATORIES, INC.

SWITCH SET AT 4800 + JUMP
BETWEEN L18 + L19 FROM A - B
FOR 4800 FROM A - C

2236DE BAUD RATE SWITCHES



SWITCH NUMBER					PARITY	DATA BITS	BAUD RATE
5	4	3	2	1			
OFF	OFF	ON	OFF	OFF	NONE	8	19.2K
X OFF	OFF	ON	OFF	ON	ODD	8	19.2K
OFF	OFF	ON	ON	OFF	EVEN	7	19.2K
OFF	OFF	ON	ON	ON	ODD	7	19.2K
OFF	ON	OFF	OFF	OFF	NONE	8	9600
X OFF	ON	OFF	OFF	ON	ODD	8	9600
OFF	ON	OFF	ON	OFF	EVEN	7	9600
OFF	ON	OFF	ON	ON	ODD	7	9600
OFF	ON	ON	OFF	OFF	NONE	8	4800
X OFF	ON	ON	OFF	ON	ODD	8	4800
OFF	ON	ON	ON	OFF	EVEN	7	4800
OFF	ON	ON	ON	ON	ODD	7	4800
ON	OFF	OFF	OFF	OFF	NONE	8	2400
X ON	OFF	OFF	OFF	ON	ODD	8	2400
ON	OFF	OFF	ON	OFF	EVEN	7	2400
ON	OFF	OFF	ON	ON	ODD	7	2400
ON	OFF	ON	OFF	OFF	NONE	8	1200
X ON	OFF	ON	OFF	ON	ODD	8	1200
ON	OFF	ON	ON	OFF	EVEN	7	1200
ON	OFF	ON	ON	ON	ODD	7	1200
ON	ON	OFF	OFF	OFF	NONE	8	600
X ON	ON	OFF	OFF	ON	ODD	8	600
ON	ON	OFF	ON	OFF	EVEN	7	600
ON	ON	OFF	ON	ON	ODD	7	600
ON	ON	ON	OFF	OFF	NONE	8	300
X ON	ON	ON	OFF	ON	ODD	8	300
ON	ON	ON	ON	OFF	EVEN	7	300
ON	ON	ON	ON	ON	ODD	7	300



MEMO TO: DISTRIBUTION
 FROM: SAM GAGLIANO - 2200 COMPUTER MARKETING
 SUBJECT: CONFIGURING 2200 SYSTEMS
 DATE: JANUARY 18, 1979

This memo is to serve as an update to my memo of October 2, 1978, regarding the need for the VP/MVP-A Extended Configuration Chassis when configuring 2200 VP or MVP systems. If you recall, it was initially stated that an "A" chassis was mandatory if over 64k of memory and/or a Model 2280 disk system were contained in any new configuration. Effective today, we will modify this rule somewhat as a result of information obtained from our Research and Development group. The limitation still remains but is nowhere as restrictive as before and much more clearly defined.

We would like to introduce a new method of configuring VP and MVP systems. This method is a positive way of determining whether or not an "A" type chassis will be required in configuring your systems. The procedure is based on assigning each peripheral controller a "configuration weight". In configuring your systems simply add all of the peripheral "configuration weights" to arrive at a total system "weight". The standard VP/MVP CPU will support up to a configured weight of 100. If your total configured weight exceeds 100 a VP-A or MVP-A Extended Chassis must be used. You can use these basic rules to configure "T" systems also. The maximum configured weight for a "T" system is 65. If this value is exceeded, then a VP system must be used. In all cases user memory will not contribute any configuration weight to the overall system. This includes MVP memory to 256KB.

The following listing specifies the "configuration weight" of most of the available 2200 peripherals.

<u>CRT</u>	<u>Description</u>	<u>Controller</u>	<u>Rating</u>
2226A	CRT Size 64x16	22C34	17
2226B	CRT Size 80x24	22C33	22
<u>Card Readers</u>			
2244A	Card Reader	22C06	14

CONFIGURING 2200 SYSTEMS
Page 2

	<u>Description</u>	<u>Controller</u>	<u>Rating</u>
<u>Keyboards</u>			
*2223	Keyboard		8
*2215/15E	Keyboard		7
*2222/22E	Keyboard		8
<u>Mass Storage Devices</u>			
2209	9-Track 800 BPI	2250	8
2209A	Buffered 9-Track 1600 BPI		17
*2230	Disk Drive	22C03	4
2230 MXA/A-1	Disk Multiplexer	--	8
2230 MXB/B-1	Disk Multiplexer	--	5
*2240	Diskette Drive	22C03	4
*2260(-2)	Disk Drive	22C03	6
*2260B(-2)	Disk Drive	22C03	6
2260BC(-2)	Disk Drive	22C13	28
2260C(-2)	Disk Drive	22C12	28
2270	Diskette Drive	22C03	4
2270A	Diskette Drive	22C03	4
2270A-D	Diskette Drive	22C03	4
2280	Disk Drive	22C14	5
(-2 versions require rating of single version disk)			
<u>Output Devices</u>			
*2201	Output Writer	22C01	8
2201L	Output Writer	22C02	6
*2202	Plotting Output Writer	22C01	8
2221W	Matrix Printer	22C02	6
2231W (All)	Matrix Printer	22C02	6
2251	Matrix Printer	22C02	6
2261W	High Speed Matrix	22C02	6
2263-1/2	High Speed Matrix	22C02	6
2281(P)	Daisy Wheel	22C02	6
2272-1/2	Drum Plotter	22C02	6
2282	Graphic CRT	22C02	6
2232B	Flatbed	22C01	8
<u>Interfaces</u>			
2207A	RS232C	--	8

CONFIGURING 2200 SYSTEMS

Page 3

<u>Interfaces (cont.)</u>	<u>Description</u>	<u>Controller</u>	<u>Rating</u>
2250	8 Bit Parallel	--	8
2252A	BCD	--	6
2254	IEEE	--	7
2227/B	Async TC	--	8
2228/B	Async, Bysnc TC	--	16
2228/C	Async, Bysnc TC	--	18
2236 MXD	MVP Terminal Multiplexer	--	18

Multiple Controllers

22C31	Triple Controller- Printer, Keyboard, Diskette	--	13
22C11	Dual Controller - Printer, Diskette	--	5

***discontinued products**

This table should be used in the following way. First, make a list of all the peripherals that the configuration will have. Then determine if either the triple or the dual controller can be used; if these controllers can be used then substitute their ratings in place of the ratings for the individual devices (keyboard, disk, printer). Then add the ratings of all other devices. Please note that the 2260BC disk drive might include a 2230 MXA (rating of 8).

A few statements on the above listing:

- . Model 2236D's are not listed as they use the MXD for a controller.
- . We have listed certain discontinued products because of the large number of "upgrades" we are booking. Be sure the particular devices you are including are compatible if using an MVP.
- . Be certain to include in your configuration weight the multiple controllers since they encompass up to three peripherals in one I/O slot. If a triple or double

CONFIGURING 2200 SYSTEMS

Page 4

controller is used always reflect the configuration of the overall controller.

- . On upgrade or add-on, this chart should be used to determine if the new configuration still fits into the maximum configuration weight.
- . Printers connected to consoles do not contribute to total system configuration weight.
- . Model 2210 consoles require CRT, keyboard and floppy disk controllers.
- . Memory size of any CPU does not carry any configured weight.
- . Good judgement must be used on any configurations bordering the maximum. Ask yourself, "What are the possibilities of an upgrade in the future?"
- . Note that you must not exceed the number of I/O slots provided in the CPU you are working with.

One other consideration is the use of 2228B or 2228C controllers and, on the MVP, the use of the 2236MXD. In all cases never configure a system which contains more than a grand total of three (3) of the above controllers in a T, VP, or MVP, or five (5) such controllers in a VP-A or MVP-A.

Now that we've got a procedure, a few sample configurations should illustrate how the configuring system works.

1. Average VP System

<u>Component</u>	<u>Configured Weight</u>
VP-8 CPU	0
2226B Console	22
2270-2 Diskette Triple Controller	13
2221W Printer Triple Controller	13
2260C Disk 22C13	<u>28</u>
Total Configured Weight	63
Total Number of I/O Slots	3

VP-A not required



2. Average MVP System

<u>Component</u>	<u>Configured Weight</u>
MVP-8 CPU	0
2236MXD Terminal Multiplexer	18
3x2236D Console	0
2270A-1D Diskette Dual Controller	5
2261W Printer Dual Controller	
2260BC Disk 22C13	<u>28</u>
Total Configured Weight	51
Total Number of I/O Slots	4

MVP-A not required

3. Large MVP System

<u>Component</u>	<u>Configured Weight</u>
MVP-64 CPU	0
2236MXD	18
2236MXD	18
8x2236D	0
2280	5
2260BC	28
2230 MXA-1	8
2228B	16
2209A	17
2261W	<u>6</u>
Total Configured Weight	116
Total Number of I/O Slots Required	8

MVP-A is required

4. Large "T" System

<u>Component</u>	<u>Configured Weight</u>
2200T-8 --	0
2226B	22
2270-3 Triple Controller	13
2221W Triple Controller	

CONFIGURING 2200 SYSTEMS

Page 6

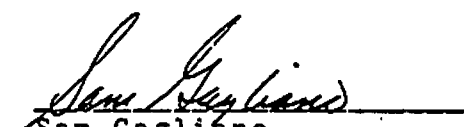
4. Large "T" System

<u>Component</u>	<u>Configured Weight</u>
2260BC	28
2230 MXA-1	8
2200WS-4	<u>0</u>
Total Configured Weight	71
Total Number I/O Slots Required	4

A VP or MVP is recommended in this configuration.

Hopefully, this configuration scheme will serve not to confuse but rather help you determine whether or not the proper CPU has been selected. The near term benefit, particularly in the case of the VP or MVP, will be quicker deliveries. Extended Configuration Chassis for the VP/MVP-A will not begin to be delivered for at least 4-6 weeks. At that time we will begin working on a very large backlog. Therefore, if we can ship standard MVP's rather than MVP-A's we will be in a better position to fill orders more rapidly.

Although we have attempted to list as many popular peripheral devices as possible, there are some minor ones including special products not listed as of yet. For any not listed, please feel free to contact me on those.



Sam Gagliano
2200 Product Marketing

SG:pn

IV.A.3

2200 SYSTEMS-MAINFRAMES-VP/MVP/LVP CPU'S.

TOPIC: NUMBER OF TERMINALS ALLOWED ON 2200MVP

With the incorporation of O.S. Release 1.9, the 2200 MVP can support up to thirteen (13) 2236D/DE Interactive Terminals. This is accomplished by allowing for a third 2236MXD Multiplexer/Controller to be used.

There is one prerequisite for increasing the number of terminals on a system to 13 -- an MVPA chassis is required. Refer to Model 2200MVP Maintenance Manual, CE# 03-0C71-1 (VI.A.3), Section 8 for information concerning the MVP-to MVPA conversion procedure.

The increase from a maximum of 9 to a maximum of 13 2236DE Interactive Terminals allowed on the 2200MVP system, requires an additional 2236MXD, and different address settings on the 2236MXD and 22C32 Controllers.

The 2236MXD addresses are set by means of a five-section switchbank (SW1), located on the WL #210-7290-1A board. For systems to have 13 2236DE terminals, set the first 2236MXD to address HEX (00) . The second to address HEX (40), and the third to address HEX (80). Set the address of the 22C32 controller to HEX (C0).

2236MXD DEVICE ADDRESSES	SWITCH SETTINGS					22C32 DEVICE ADDRESS	SWITCH SETTINGS			
	S-1	S-2	S-3	S-4	S-5		S-1	S-2	S-3	S-4
HEX (00)	0	0	0	0	0	HEX (C0)	1	0	0	1
HEX (40)	1	0	0	0	0					
HEX (80)	0	1	0	0	0					

* 0 = OFF; 1 = ON.

Gilles Carrier
2200 Product Support



NEW PRODUCT NOTICE

PRODUCT: MVP TRIPLE CONTROLLER

NO: 18

MODEL NO: 22C32

DATE: 11/2/79

I. DESCRIPTION

The 22C32 Triple Controller is a new option available to the VP/MVP product line. As in the 7042 Triple Controller for the 2200 and VP systems, the 22C32 can support a terminal, a disk drive, and a printer. The major difference between the two controllers is that the 22C32 supports the 2236D/DE Interactive Terminal.

Using a 22C32 controller, a VP System can support one 2236D/DE terminal. An MVP System using the 22C32 can support a maximum of nine terminals because the terminal controller portion of the 22C32 will function with two 2236MXD multiplexer/controllers which support four terminals each. The 22C32 Triple Controller can also be used with a single 2236MXD device on an MVP to provide support for five terminals. A 2236D/DE terminal connected to a VP or MVP by a 22C32 cannot be used as a remote terminal.

The Model 22C32 Triple Controller consists of two PCBs: a 210-7515 motherboard containing the printer and disk interface electronics, and a 210-7516A daughterboard containing the Z80-based 2236D/DE interface electronics. The terminal controller portion of the 22C32 is equivalent to one port of a 2236MXD; however, the communications rate is fixed at 19200 bps.

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The address of the 2236D/DE portion of the 22C32 is selected by means of a five-bank switch located on the bottom right of the 210-7515 PCB. For systems with a single terminal, the controller address switches are set to 00; that is, all five switches in the bank must be OFF. In a five terminal system, using one 2236 MXD controller and one 22C32 controller, the address switches of the 22C32 controller are set to 40 (switch #1 ON; all others OFF). In a nine terminal system using two 2236 MXD controllers and one 22C32 controller, the address switches of the 22C32 controller are set to 80 (switch #2 ON; all others OFF). Refer to Section 3.4.2 of the 2200 MVP Maintenance Manual (03-0071-1) for the proper setting of the device address switches.

Both the printer address and the disk address are switch-selectable by means of two 8-bank switches. The switches are located on the lower right side of the 210-7515 PCB, above and to the right of the 2236D/DE address switch. The lower switch selects the printer address and the upper switch selects the disk address. Refer to Section 3.4.2 of the 2200 MVP Maintenance Manual (03-0071-1) for the proper setting of the device address switches.

Refer to NPN #9 for information concerning requirements for the 2236DE terminal.

II MAINTENANCE

No special tools or test equipment are needed for servicing the 22C32 Triple Controller.

III LOGISTICS

A. Recommended Spares List

See attached RSL

B. Disposition of Defective Parts

Standard PC Board repair procedures will be followed.

IV DELIVERY

The 22C32 Triple Controller was introduced to the field in September.

V TRAINING

There will be no formal training classes on the 22C32 Triple Controller. It will be included in the MVP training curriculum.

RECOMMENDED SPARES LIST - BRANCH

LEVEL B

<u>WLI</u>	<u>NAME & DESCRIPTION</u>	<u>QTY/1-5 UNITS</u>
212-3012	MVP Triple Controller	1

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DATA SHEET

ONE INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851, TEL (617) 851-4111, TWX 710 343-6769, TELEX 94-7421

The Model 9020-24 24 Hour Time of Day Clock provides a convenient method of reading the time of day from the CRT of a 2200 System. Once set (usually after system power-on), the clock provides the time of day in hours, minutes, and seconds, on request. The logic of the Model 9020-24 resides on a controller board which plugs into any available I/O slot in a 2200 series CPU and WCS systems (except PCS, PCS-II, WS and WCS-15).

The Model 9020-24 accepts and outputs time in a 24-hour format. The time is set by a PRINT verb followed by an alphanumeric variable consisting of four digits. The four digits indicate the hours and minutes; seconds are automatically set to 00 whenever the time is set. The SET TIME address is hardwired to 237.

The time on the Model 9020-24 may be set by the following routine:

```
10 INPUT "WHAT TIME IS IT", AS: SELECT PRINT 237:  
PRINT AS: SELECT PRINT 005  
RUN (EXEC)
```

This statement prompts WHAT TIME IS IT? to which the operator enters four digits in hours - minutes format HHMM. Note that it is important to reselect the CRT address 005 after the time is set, otherwise all PRINT statements in subsequent programs will RESET the clock time.

To read the time, an INPUT statement is used with either a numeric or alphanumeric variable to receive the time. The Read Time address is hardwired to 236. The time is "output" to the receiving variable in hours, minutes, and seconds in HHMMSS format. The time on the Model 9020-24 may be read by the following routine:

```
20 SELECT INPUT 236: INPUT A: SELECT INPUT 001  
RUN (EXEC)
```

MODEL 9020-24
24 HOUR TIME OF DAY CLOCK

DATA SHEET

The SELECT INPUT 236 specifies the device address of the clock to enter in the time for the INPUT statement. Note again that it is important to reselect the keyboard address 001 after the time is read, otherwise all INPUT data requested in subsequent statements will be provided by the clock.

Alternately, MAT INPUT, KEYIN or \$GIO may be used to request a time input.

By using cursor positioning HEX codes in the "read time" routine, the operator can output the time anywhere on the CRT, or output the time to a printer on hard copy reports, as required. Also, colons may be inserted between the hours and minutes and between the minutes and seconds, for easier reading.

SPECIFICATIONS

Power Requirements

Model 9020-24 board operates from the CPU Power Supply.

Operating Environment

50° F to 90° F (10° C to 32° C)
30% to 80% relative humidity, non-condensing.

ORDERING SPECIFICATIONS

A 24 hour time of day clock capable of interfacing with any 2200 series CPU. It must provide the time of day in 24 format in hours, minutes, and seconds on request by the operator.

Wang Laboratories reserves the right to change specifications without prior notice.

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WEEKLY COMPUTER TELEX #42
PG. 2

MVP RELEASE 1.9.

There is a known bug in the operating system that when you press reset from one terminal the other workstations will give you almost any type of error when trying to access the disk. A new operating system is in the making, but exactly when it will be released is not known.

2236DE

The following information on installing and servicing 2236DE terminals is valid as of August 1, 1980.

The current E REV of the 210-7592 and E REV of 2 will not cause problems as long as the terminal is not used as a primary console and does not have a local printer or plotter attached.

Manufacturing will continue to ship E REV 2 until the next art work update. It is Customer Engineering's responsibility to update the PCB's if the update is needed.

ECN History:

E REV 1	ECN 12304	PROM change
E REV 2	ECN 12482	To improve video
E REV 3	ECN 12947	Allows DE to be used as primary terminal
E REV 4	ECN 13176	to enable DE to work with plotters

ECN #13269 updated the proms on the 2236MXD. All MXD's should be updated to R6 prom's. They must be R6 prom's to use a DE terminal.

To use a DE terminal, the operating system should be 2.2 for a VP or 1.9 for an MVP.

If a customer is experiencing problems with the special features, screen dump to local printer, box function inoperative or graphic character inoperatives, the level of the operating system should be verified before accepting a service call. If the operating system is the latest release, then the first thing to be checked after arriving on site is the prom level. If a request for service is made because the KB clicker or audible alarm is low or inoperative, have the operator check the controls on the rear of DE before accepting a service call.

2.1 BAUD RATE SWITCH SETTINGS

Up to eight Model 2236D Interactive Terminal Consoles can be configured with the 2200 MVP CPU. Four 2236D Terminals can be connected to one 2236MXD controller, with a maximum of two 2236MXD controllers in the system.

2.1.1 2236D TERMINAL 5-BANK BAUD RATE SWITCH

The two leftmost switches must always be ON. The baud rate of the corresponding port of the 2236 MXD controller must match the baud rate of the terminal.

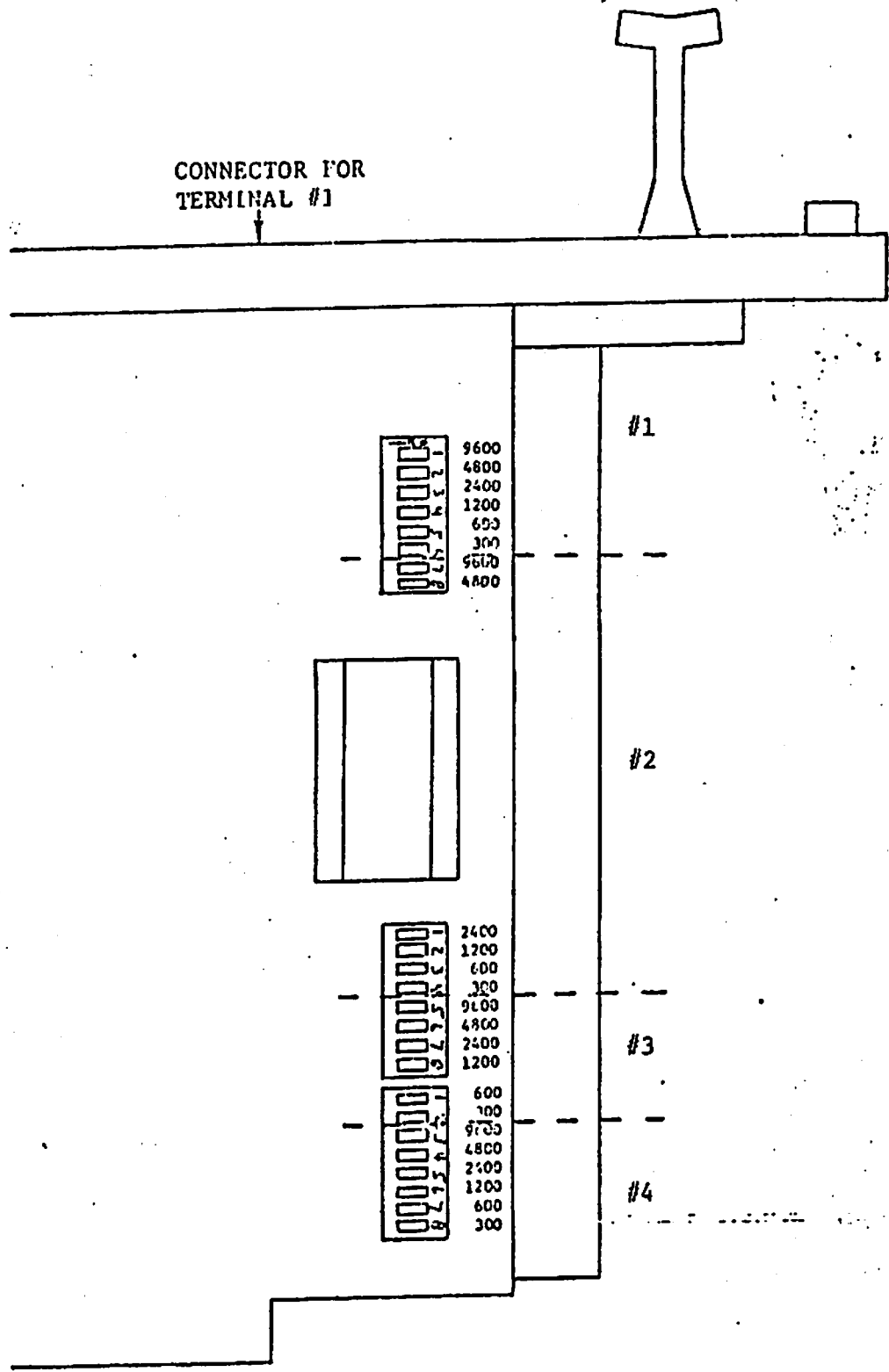
Access to the baud rate switch in the 2236D is through the large plug-button on the rear of the cover. Remove the plug and set the three rightmost switches of the five bank switch as follows (the two leftmost switches are ON):

for terminal baud rate must be same as MUX D

Switch:	1	2	3	4	5	Baud Rate
	ON	ON	OFF	OFF	OFF	300
	ON	ON	OFF	OFF	ON	600
	ON	ON	OFF	ON	OFF	1200
	ON	ON	OFF	ON	ON	2400
	ON	ON	ON	OFF	OFF	4800
	ON	ON	ON	OFF	ON	9600

2.1.2 2236MXD CONTROLLER BAUD RATE SWITCHES

There are three 8-bank switches located on the 2236MXD controller. The three switches are divided into four groups of six switches each, each group corresponding to a connector on the top panel.



CONNECTOR FOR
TERMINAL #1

#1

#2

#3

#4

7290 BAUD RATE SWITCH IDENTIFICATION

FIG. 2.1

WANG

LABORATORIES, INC.

TO: ALL KEY COMPUTER PEOPLE
FROM: KEITH JONES
SUBJECT: 2200 MVP CONVERSIONS
DATE: MARCH 19, 1978

Conversions for the 2200 MVP are now being shipped from the home office. There is only one minor problem, which is that they are only shipping the appropriate memory boards.

E.C.N.s must be performed to the 6790, 6791, 6793-1, and the 6798 P.C. boards. These changes must be done at the local service office prior to installing the conversion at the customer's site. The E.C.N.s to the 6790 and the 6791 have some parts that are normally not stocked at the local office level. Therefore, if you need the parts for the conversion, order them via the Rush Request system, UO-2, "MVP SMALL PARTS CONVERSION KIT."

In addition to the E.C.N.s, the bootstrap proms (378-2045, 2046, and 2047, on the 6789 board), must be at revision level 1, and the MVP operating system can be no lower than revision 1.6. Order these UO-2 if you need them.

If the need ever arises, when ordering boards for a customer down situation, please specify, on the Telex, the memory size of the unit that you are working with, to insure that you receive boards that have the proper E.C.N.s installed.

If there are any questions please feel free to contact me.

REGARDS,

KEITH JONES
EASTERN AREA TECHNICAL SPECIALIST

cc: AREA STAFF
ERIK GARTHE
ALAN DONATI

WANG

LABORATORIES, INC.

MVP CONVERSION PARTS LIST

1 - 300-1909 .0033 uf capacitor
1 - 376-0123 7427 I.C.
2 - 330-3022 2.2K ohm resistor

WANG

LABORATORIES, INC.

2200 MVP BOARD LAYOUT

I/O

6793-1

6792

6791

6790

6789

6788 (CM1)

6788 (CM2)

6787 (DM1)

6787 (DM2)

P.S.

210-6790 E-Rev 5

1. Change C4 to .0033 uf (300-1909). C4 is located on the schematic at coordinates I3.
2. Add a wire from L51 pin 7 to connector pin X3.
3. Add a wire from L51 pin 9 to connector pin 203.
4. Cut the etch between L18A pin 9 and connector pin 122.
5. Add a wire from L49 pin 9 to connector pin 122.
6. Add a wire from L49 pin 10 to L28 pin 6.
7. Add a wire from L49 pin 11 to L39 pin 8.
8. Change the E Rev level sticker from 4 to 5.

210-6791 E-Rev 3

1. Insert a 7427 (376-0125) into location L21A. Pin 1 should be located toward the bottom of the board. Connect pin 7 to + 0V and pin 14 to + 5V.
2. Cut the etch connected to L53 pin 2, at pin 2.
3. Add a wire from L32 pin 13 to L53 pin 2.
4. Add a wire from L32 pin 12 to connector pin H2.
5. Add a wire from L32 pin 12 to L21A pin 12.
6. Jumper L21A pins 3 and 13 together.
7. Add a wire from L32 pin 11 to L21A pin 6.
8. Add a wire from L21A pin 1 to L41 pin 2.
9. Add a wire from L21A pin 2 to L41 pin 6.
10. Add a wire from L21A pin 13 to L41 pin 7.
11. Add a wire from L21A pin 4 to L22 pin 4.
12. Add a wire from L21A pin 5 to L22 pin 6.
13. Add a wire from L22 pin 3 to connector pin 82.
14. Add a wire from L22 pin 5 to connector pin 13.
15. Add a 2.2K resistor (330-3022) between L22 pin 3 and +5V.
16. Add a 2.2K resistor (330-3022) between L22 pin 5 and +5V.
17. Change the E Rev level sticker from 2 to 3

210-6793-1 E-Rev 5

1. Add a wire from L39 pin 3 to L35 pin 10.
2. Add a wire from L39 pin 4 to connector pin R3.
3. Add a wire from L39 pin 5 to L35 pin 6.
4. Add a wire from L39 pin 6 to connector pin H3.
5. Change the E Rev level sticker from 0 to 1.

210-6798 E-Rev 5

1. Add a wire from 6793-H₃ to 6791-8₂ to 6787 (DM1) - M₂ to 6787 (DM2) - M₂.
2. Add a wire from 6793-R₃ to 6791-1₃ to 6787 (DM1) - N₂ to 6787 (DM2) - N₂.
3. Add a wire from 6791-H₂ to 6787 (DM1)-L₂ to 6787 (DM2)-L₂.
4. Add a wire from 6790-20₃ to 6788 (CM1)-N₂.
5. Add a wire from 6790-X₃ to 6788 (CM1)-R₂.
6. Add a wire from 6788 (CM1)-E₂ to 6788 (CM2)-E₂.
7. Add a wire from 6790-12₂ to 6787 (DM1)-J₂ to 6787 (DM2)-J₂.
8. Add a wire from 6788 (CM2)-2₃ to 6787 (DM1)-K₂ to 6787 (DM2)-K₂.
9. Add a wire from 6787 (DM1)-14₂ to 6787 (DM2)-R₂.
10. Add a wire from 6787 (DM1)-S₂ to +0V.
11. Add a wire from 6790-C₂ to 6788 (CM1)-S₂.
12. Add a wire from 6790-17₂ to 6788 (CM1)-16₂.
13. Add a wire from 6790-16₂ to 6788 (CM1)-15₂.
14. Change the E REV level from 2 to 3.

2336DW ERGO TERMINAL

PART NUMBERS AND SWITCH SETTINGS (CORRECTED AND IMPROVED)

The switch settings for the 2336DW ERGO in both Newsletter #20 and the Product Maintenance Manual from which they were taken are incorrect. The correct settings are shown in the chart below.

Thanks to Brian Weir of the Brockton office and Gabe Moran of Burlington North for the corrected settings. Also thanks to Rick Mansfield of Burlington South for bringing to our attention the need to order 270-0753 when ordering the terminal control board. See below. The new Ergo Workstation is out in the field and is basically the same as a 2236DW with the added Ergo features of tilting screen and detachable keyboard. Local terminals on MVP/LVP may be a maximum of 2000' while on VP/SVP maximum local distance is 50'. The controller board for these terminals must have it's proms up to current standards to support these terminals.

1. MUX D daughterboard - 210-7591A R7 proms 378-2140/41/42/43
2. Triple controller daughterboard - 210-7516A R1 proms 378-4092/93
3. Triple controller daughterboard - 210-7816A R1 proms 378-2591/2449/50/51
4. SVP controller board - 210-7789A R1 proms 378-4092/93

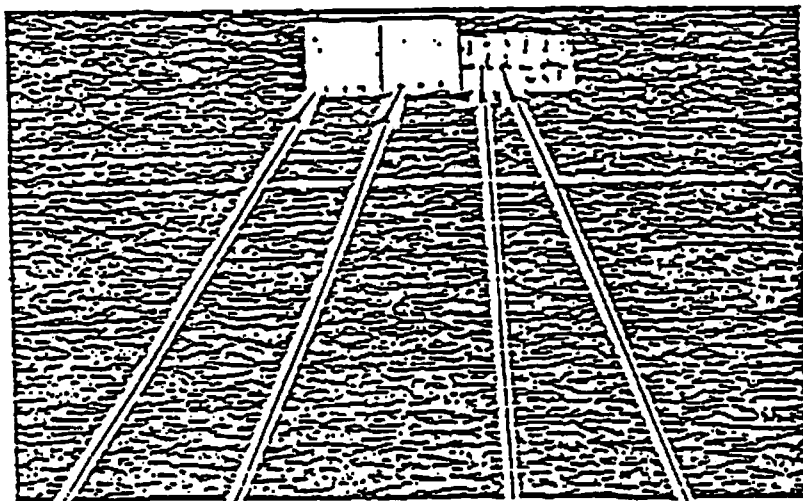
Parts List

- Terminal Control Board *210-7743A (should have following proms - 378-5080R1, 378-6013R5 (L9) and 378-6014R5 (L10))
- Standard Keyboard 725-2637
- Expanded Keyboard 725-2652 (identified by uppercase characters on numeric keypad)
- 12" Monitor Board 210-7456
- 12" Tilting CRT Assembly 270-0633
- Power Supply 270-0734

*Use 270-0753 to order as this will give the 210-7743A with attached hardware

The first Ergo terminals released on the 2200 product line were actually repackaged 2236DE/DW's using the same 7592 board. The model number on this unit should be 2886. There seems to have been some mislabeling with model numbers with some 2336DW's being labeled 2886.

Switch Settings



SWITCH			BAUD RATE
3	4	5	
DOWN	DOWN	DDWN	300
UP	DOWN	DDWN	600
DOWN	UP	DDWN	1200
UP	UP	DDWN	2400
DDWN	DDWN	UP	4800
UP	DDWN	UP	9600
DDWN	UP	UP	19.200

CLICKER PBT
SPEAKER PBT

UP	DOWN
EVEN PARITY	ODD PARITY

UP	DOWN
8 DATA BITS	7 DATA BITS

MVP/LVP

2236MXE CONTROLLER

The 2236MXE Terminal Controller has recently hit the field and will support 2236D, DE, DW and 2336DW terminals. The controller has its own 48K of RAM to allow it to perform several functions previously performed by the CPU. Some of the enhancements provided with this controller are:

1. "Time of Day" clock circuitry (optional battery back-up).
2. Baud Rate for each port switch and software selectable.
3. 8K prom provides bootstrap functions, power up diagnostics, and remote diagnostics.
4. Ability to set any terminal as Primary User.

With initial power on, the power on diagnostics will be run, which takes about 6 seconds and checks the majority of the MXE hardware. While this is taking place an LED at the top of the external edge is lit and if there are no problems the LED will go out after the 6 seconds.

To use the MXE board however, MVP 2.4 operating system is necessary as otherwise when RUN is keyed from the LOAD MVP/LOAD diagnostic menu the system will just hang up. Thanks to Tim Coughlin of the Providence office for his help with this information.

Switch settings

# of MXE	Switch Bank 1			
	1	2	3	4
First	off	off	off	off
Second	on	off	off	off
Third	off	on	(off)	(off)
			(not used)	

-over-

MVP/LVPWorkstations Intermittently Hanging Up

If you have a customer experiencing an intermittent problem with workstations hanging up it may be because of R7 proms being used with the 210-7591 daughterboard on the MUX D board. Try downgrading the R7 proms to R6 or replacing the 210-7591 with the 210-7291 daughterboard. This is a temporary fix.

NOTE: The 2236DW Workstations requires R7 proms and the 210-7591 board so you can not make these changes if the customer has DW terminals.

Option C

Option C which allows up to 64K Control Memory and 512K Data Memory has recently been made available on MVP and LVP CPU's. The extra control memory is necessary to support COBOL and BASIC-3.

With both the MVP and LVP a new motherboard is required and in the case of the MVP a-chassis as well. The new motherboards have 7 I/O slots.

On all CPU's with option C, 2 new boards are required to handle the increased memory. The new Extended Instruction Counter Board, 210-7797, replaces the 6790 and the new Extended Memory Controller Board, 210-7796, is installed between the 2 Control Memory Slots and the 4 data memory slots.

For proper operation of Option C the following list should be helpful.

1. MVP must have MVPC chassis with motherboard (7 I/O slots) 270-0465
LVP must have LVPC card cage/motherboard ass'y(7 I/O slots) 270-0467
2. MVPC must have a 210-7397 regulator which will not come with upgrade.
3. MVPC/LVPC must have the Extended Memory Controller Board, 210-7796 (inserted in slot between 2 control memory slots and 4 data memory slots).
4. MVPC/LVPC must have the new Instruction Counter Board 210-7797 (replaces the 210-6790 board)
5. MVPC/LVPC with data memory greater than 256K must have a 210-6793-1 updated to at least E-REV 4.
6. ~~MVP/LVPC with data memory greater than 256K must have a 32K Control Memory Board. Control memory must be at least 512K to support Cobol and Basic 3. If only 1 Control Memory Board is needed* it must be installed in control memory slot #2 next to the 210-7796 boards. 210-7588 must be E REV 3~~
7. MVPC/LVPC with data memory greater than 256K must have a 210-6789 board with at least R4 proms. (R3 may work but might have some bugs)

R3 OK

8. MVPC/LVPC with 64K control memory or greater than 256K of data memory must use software release MVP 2.3 to utilize the added memory.
9. The 210-6790 must be at least E-REV 5 and the 210-6791 must be at least E-REV 3 to support greater than 64K data memory.
10. All LVPs use +5V2 for any I/O slot after the first 3 I/O slots. This voltage can be measured at connector J3 pins 1 and 3 on the regulator board or pin B, of the I/O connectors.

[REDACTED]

LVP/MVP

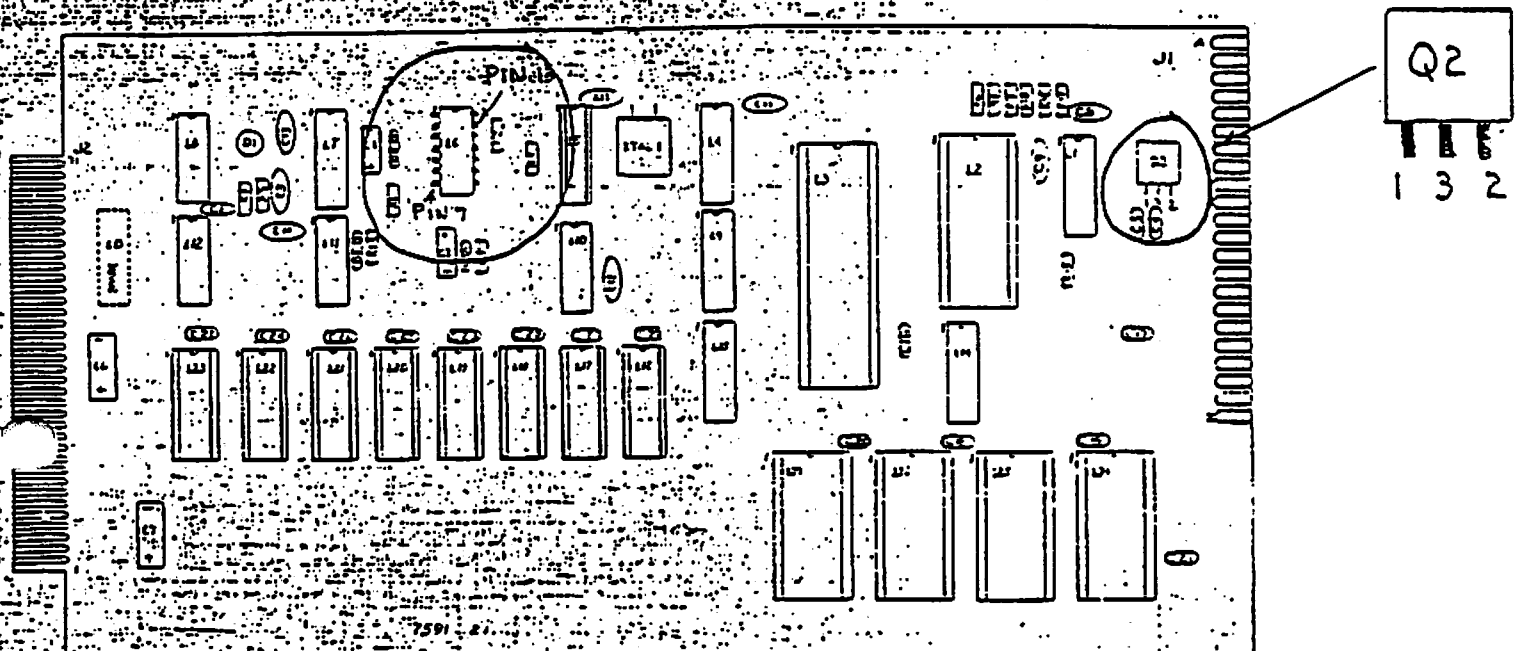
HANG UP PROBLEM WITH MUXD CONTROLLER

A legitimate solution has been found for terminals hanging up using the MUXD board with 210-7591 daughterboard and R7 proms. Previously the solution was to either downgrade the proms or the daughterboard if both weren't needed for 2200 Word Processing.

The fix involves installing two capacitors on the 210-7591 PCA (see picture)

- 1 Add a 390 pf capacitor (WLI 300-1390) between L6-pin 13 and plus/minus 0 volts. (use L6 pin 7 for +/- 0V)
- 2 Add a 35uf capacitor (WLI 300-3009), negative side to Q2 - pin 2 (-5V output) and positive side to plus/minus 0V. (use Q2 pin 1 for +/- 0V).

Another aid in eliminating intermittent hangups may be to insert the MUX D Board into the first I/O slot closest to 210-6793 board of the CPU section. After insertion, adjust 12 volts at the last I/O slot to approximately 12.1 volts. 12 volts can be adjusted at connector 3, bottom connector, of I/O slot, pin 15. (bottom pin). Ground reference is pin 13 (3rd from bottom).

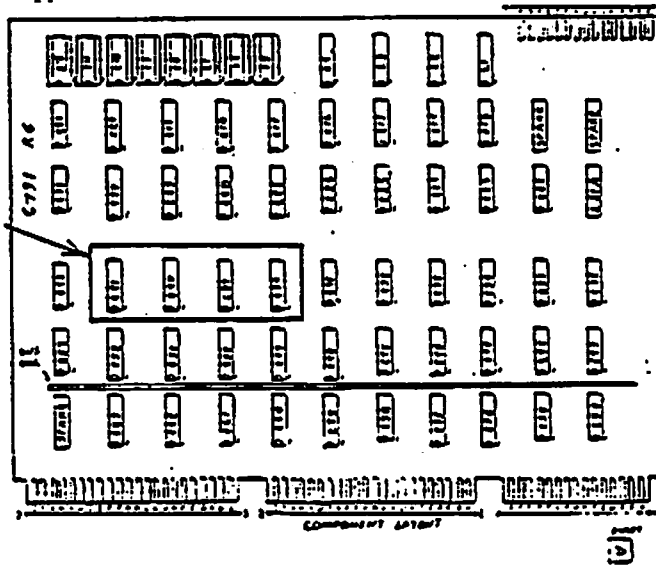


INTERMITTENT PARITY ERRORS (PEDM) WITH C CHASSIS

If experiencing intermittent parity errors with a C chassis, updating the 6791 board to a 6791-1 might help. Although any board in the CPU can cause a PEDM, a problem has been found with some 6791 boards which updating should correct. To upgrade from a 6791 to a 6791-1 change the 4 chips at L38, L39, L40, and L41 to Fairchild's. The 6791 board must be at least an E-REV 3 to be used in a LVPC. All C chassis should have the 6791-1 board.

Fairchild Chip - 376-0203-1

Fairchild chips can be identified by the letter F on them followed by the number 74191 PC.



2336DE/DW ERGO TERMINALS

PROBLEM KEYING RESET WITH SYSTEM LOADED AS VP

There has been a problem found with the 2336 Ergo Terminals where if the system is loaded as a VP keying reset will cause "INIT" to be printed on the screen.

This only happens with MUXD controllers as the MUXE works ok. Home office is aware of the problem.

If this problem is encountered do not attempt to fix it as it is normal and anyone with a MUX D controller would normally be loading their system as an MVP.

Thanks to Gabe Moran of Burlington North and Dan Dwyer of Brockton for their assistance with this information.

MVPC/LVPC

CONTROL AND DATA MEMORY ERRORS WITH 512K

There is a possible problem with MVPC/LVPC with 512K Memory.

Most common symptoms are:

PECM AA XXXX or PEDM AA XXXX

and removing the fourth memory board eliminates the problem. As long as the fourth slot is empty any 3 of the boards work fine.

Problem appears to be sensitivity with the 6791 board and trying several 6791's may produce a working solution.

R&D is working on the problem now.

NEW FANS

There is a new skeleton fan for the VP/MVP systems which provides more airflow and will allow installation of larger controllers (TC, 2260C controllers) under the fan section. Wang part # for fan is 400-1001.

MVP/LVP & VP/SVP OPERATING SYSTEM RELEASE 2.2/2.4

The following is the memo and marketing release on the new MVP/LVP operating system release 2.2, and the new VP/SVP operating system release 2.4.

One of the new features is the CPU identification number. This number is contained in the PROMs located on the 210-6789 PCB. The PROM numbers and location are as follows:

L27	378-2045-R3
L28	378-2046-R3
L29	378-2047-R3

These PROMs were updated to R3 in MUB release #19, dated April 30, 1981.

If your customer is using a vendor's software package that is software protected, and the 210-6789 PCB becomes defective and must be replaced, these PROMs must be removed from the defective PCB and installed on the new PCB. Failure to do so will result in the inability to run the vendor's software protected programs.

A new numeric function, #ID, returns the CPU identification number. Each 2200 CPU is assigned a number (a random integer between 1 and 65535) at the time of manufacture. Machines produced prior to the implementation of this feature return a value of 0, but such machines can be field upgraded to have non-zero #ID's. CPU ID's are not guaranteed to be unique, but it is highly unlikely two given machines will have the same number.

This function allows software to tell one CPU from another. The ability to distinguish one CPU from another is useful in restricting software to specific installations and in telling one CPU from another when disk multiplexers are used.

256K MVP MEMORY ERROR DECODE

This communique is a preliminary explanation of how to decode memory error messages to point out a bad RAM on the 210-7587 board. Refer to the MVP Maintenance Manual for explanations of the error messages that are not covered here.

(AECM aaaa bbbb xxxxxx)

where: aaaa = address of instruction in error
bbbb = conflicting address
xxxxxx = XOR of the expected and read instructions

This error indicates that writing to location bbbb seems to modify location aaaa. The '1' bits in the xxxxxx field of the display indicate which bit(s) has been modified. The error could also occur if a chip at location aaaa had a marginal failure.

(AEDM ss.aaaa ss.bbbb xx)

Where: ss = memory bank containing error (00 = bank 1, 40 = bank 2, 80 = bank 3, C0 = bank 4). NOTE: This is the same for all Data Memory error messages.
aaaa = address of the data in error
bbbb = conflicting address
xx = XOR of the expected and read data

This error indicates that writing to location bbbb seems to modify location aaaa. The '1' bits in the xx field of the display indicate which bit(s) have been modified. The error could also occur if a chip at location aaaa had a marginal failure.

BOARD #1

BOARD #2

BANK #

7587

ADDR.

BANK #

7587

ADDR.

2



8000-FFFF

4



8000-FFFF

2



0000-7FFF

4



0000-7FFF

1



8000-FFFF

3



8000-FFFF

1



0000-7FFF

3



0000-7FFF

SAMPLE ROW

EVEN ADDRESSES

0, 2, 4, 6, 8, A, C, E

ODD ADDRESSES

1, 3, 5, 7, 9, B, D, F



CHART 2

WANG

LABORATORIES, INC. MEMORANDUM

TO: ALL EASTERN AREA CUSTOMER ENGINEERS

FROM: SCOTT TAGEN

SUBJECT: VP MEMORY BOARDS

DATE: FEBRUARY 16, 1978

377-0314T RAM chips have been distributed to all field offices to enable you to repair VP RAM boards. Model 2200 CPU Field Level Maintenance Guide No.2 describes clearly how to decode the RAM microcode diagnostics. An example is shown below:

8 BIT ADDRESSING TEST

ERROR BETWEEN 8000 AND 8004 (02) #0000

MAT C + S

ERR PC's 8008 = 8000 (DF/DD) BIT(S) 02 #0001

ROWPAT TEST

FAILURE AT PC's 8004 (00/02)
BIT(S) 02 #0000

All of these tests point to L57 on the 6787 #2. There will be times when regardless of what diagnostic is loaded the display will come up with PECM or PEDM errors. If the problem is in data memory, grounding L41 Pin 3 on the 6789 board will disable data memory parity, and allow the diagnostic to call out the bad chip.

A way to possibly get around control memory parity is to try to run one of the field service diagnostics, (SF 12 for disk address 310). The user diagnostics string together all three memory tests, so if the 24 bit addressing test hangs up, it might be better to run the tests individually.

If you attempt to repair a board and fail, indicate what you tried on the repair tag. Also, if you have a bunch of bad chips DO NOT load them into the sockets, send them separately. When a board has many bad chips the odds of blowing etches are significantly increased, and these can be tough to repair.

Any memory boards of any kind that can be field repaired will allow Area Shop Technicians more time to repair the more complicated boards. This will result in a faster turnaround time for repairs.

Regards,

Scott

SCOTT TAGEN

EASTERN AREA SHOP SUPERVISOR

ST/mr

cc: Branch Managers
District Managers
Area Staff

TO: FIELD PERSONNEL
FROM: JOHN PROULX
DATE: FEBRUARY 28, 1979
SUBJECT: 2200 MVP CONVERSION (256K)

The attached pages contain information necessary to upgrade existing MVP Systems to MVP Systems that can accept up to 256K of User Memory. All changes must be incorporated for correct operation.

The conversion kit will only contain the Data Ram boards necessary for the upgrade. The customer chassis must be upgraded and the updated CPU boards (6790, 6791, and 6793-1) must be added.

It is recommended that only the customer chassis be updated at the customer site. The CPU boards should be updated and checked with the additional memory prior to the installation. Upon installation, swap the CPU boards and bring the non-updated boards back to your office for updating. After updating they can be used for the next conversion.

If you have any questions, I can be reached at the Home Office, System Support Group.

NOTE: The MVP Operating system must be at Revision 1.6 or higher and the Bootstrap proms must be 378-2045 R1, 378-2046 R1, and 378-2047 R1.

2270 - IBM COMPAT
60B-6298 - R1 PROMS

Regards,

John Proulx

- I/O
- 6793
- 6792
- 6791
- 6790
- 6789
- 6788 (CM1)
- 6788 (CM2)
- 6787 (DM1)
- 6787 (DM2)
- P.S.

TOP VIEW

For access to the motherboard, remove the bottom access panel by removing the feet on the underside of unit. All modifications described below can be performed without removing the motherboard from the chassis.

1. Add a wire from 6793-H ψ 3 \uparrow to 6791-8 ψ 2 \uparrow to 6787 (DM1) - M ψ 2 \uparrow to 6787 (DM2)-M ψ 2 \uparrow .
2. Add a wire from 6793-R ψ 3 \uparrow to 6791-1 ψ 3 \uparrow to 6787 (DM1)-N ψ 2 \uparrow to 6787 (DM2)-N ψ 2 \uparrow .
3. Add a wire from 6791-H ψ 2 \uparrow to 6787 (DM1)-L ψ 2 \uparrow to 6787 (DM2)-L ψ 2.
4. Add a wire from 6790-20 ψ 3 \uparrow to 6788 (CM1)-N ψ 2 \uparrow .
5. Add a wire from 6790-X ψ 3 \uparrow to 6788 (CM1)-R ψ 2 \uparrow .
6. Add a wire from 6788 (CM1)-E ψ 2 \uparrow to 6788 (CM2)-E ψ 2 \uparrow .
7. Add a wire from 6790-12 ψ 2 \uparrow to 6787 (DM1)-J ψ 2 \uparrow to 6787 (DM2)-J ψ 2 \uparrow .
8. Add a wire from 6788 (CM2)-2 ψ 3 \uparrow to 6787 (DM1)-K ψ 2 \uparrow to 6787 (DM2)-K ψ 2 \uparrow .
9. Add a wire from 6787 (DM1)-14 ψ 2 \uparrow to 6787 (DM2)-R ψ 2 \uparrow .
10. Add a wire from 6787 (DM1)-5 ψ 2 \uparrow to \pm 0V.
11. Add a wire from 6790-C ψ 2 \uparrow to 6788 (CM1)-S ψ 2 \uparrow .
12. Add a wire from 6790-17 ψ 2 \uparrow to 6788 (CM1)-16 ψ 2 \uparrow .
13. Add a wire from 6790-16 ψ 2 \uparrow to 6788 (CM1)-15 ψ 2 \uparrow .
14. Change the E REV level from 2 to 3.

210-6720 5

1. Change C4 to .0033 uf (300-1909). C4 is located on the schematic at coordinates I3.
2. Add a wire from L51 pin 7 to connector X43f.
3. Add a wire from L51 pin 9 to connector 2043f.
4. Cut the etch between L18A pin 9 and connector 1242f.
5. Add a wire from L49 pin 9 to connector 1242f.
6. Add a wire from L49 pin 10 to L28 pin 6.
7. Add a wire from L49 pin 11 to L39 pin 8.
8. Change the E REV level from 4 to 5.

210-6721 3

1. Insert a 7427 (376-0125) into location L21A. Pin 1 should be located toward the bottom of the board. Connect pin 7 to $\pm 10V$ and pin 14 to +5V.
2. Cut the etch connected to L53 pin 2 at pin 2.
3. Add a wire from L32 pin 13 to L53 pin 2.
4. Add a wire from L32 pin 12 to connector H42f.
5. Add a wire from L32 pin 12 to L21A pin 12.
6. Jumper L21A pins 3 and 13 together.

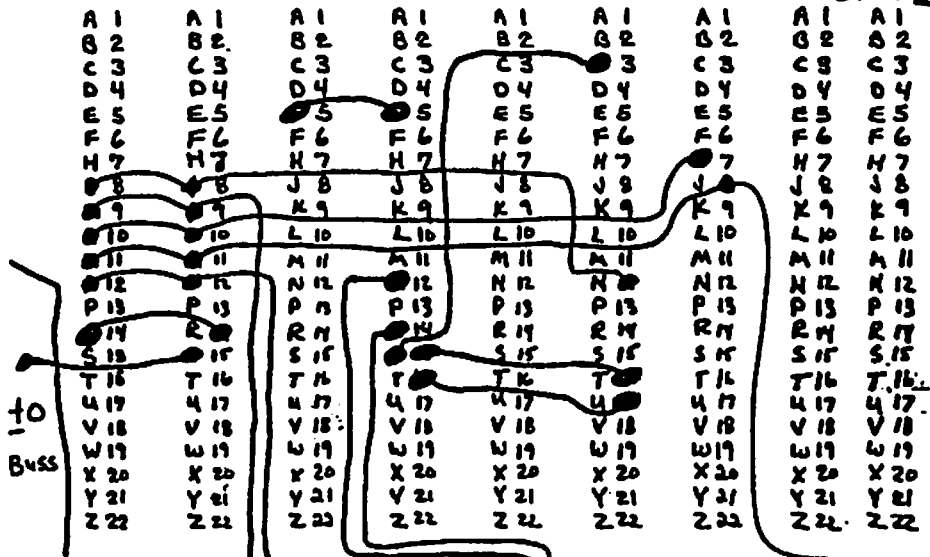
7. Add a wire from L32 pin 11 to L21A pin 6.
8. Add a wire from L21A pin 1 to L41 pin 2.
9. Add a wire from L21A pin 2 to L41 pin 6.
10. Add a wire from L21A pin 13 to L41 pin 7.
11. Add a wire from L21A pin 4 to L22 pin 4.
12. Add a wire from L21A pin 5 to L22 pin 6.
13. Add a wire from L22 pin 3 to connector 8 Ψ 3 Γ .
14. Add a wire from L22 pin 5 to connector 1 Ψ 3 Γ .
15. Add a 2.2K resistor (330-3022-4B) between L22 pin 3 and +5V.
16. Add a 2.2K resistor between L22 pin 5 and +5V.
17. Change the E REV level from 2 to 3.

210-6793-1 1

1. Add a wire from L39 pin 3 to L35 pin 10.
2. Add a wire from L39 pin 4 to connector R Ψ 3 Γ .
3. Add a wire from L39 pin 5 to L35 pin 6.
4. Add a wire from L39 pin 6 to connector H Ψ 3 Γ .
5. Change the E REV level from 0 to 1.

DM2	DM1	CM2	CM1	6789	6790	6791	6792	6793
6787	6787	6788	6788	6789	6790	6791	6792	6793
A1	A1	A1	A1	A1	A1	A1	A1	A1
B2	B2	B2	B2	B2	B2	B2	B2	B2
C3	C3	C3	C3	C3	C3	C3	C3	C3
D4	D4	D4	D4	D4	D4	D4	D4	D4
E5	E5	E5	E5	E5	E5	E5	E5	E5
F6	F6	F6	F6	F6	F6	F6	F6	F6
H7	H7	H7	H7	H7	H7	H7	H7	H7
J8	J8	J8	J8	J8	J8	J8	J8	J8
K9	K9	K9	K9	K9	K9	K9	K9	K9
L10	L10	L10	L10	L10	L10	L10	L10	L10
M11	M11	M11	M11	M11	M11	M11	M11	M11
N12	N12	N12	N12	N12	N12	N12	N12	N12
P13	P13	P13	P13	P13	P13	P13	P13	P13
R14	R14	R14	R14	R14	R14	R14	R14	R14
S15	S15	S15	S15	S15	S15	S15	S15	S15

1



2

A1	A1	A1	A1	A1	A1	A1	A1	A1
B2	B2	B2	B2	B2	B2	B2	B2	B2
C3	C3	C3	C3	C3	C3	C3	C3	C3
D4	D4	D4	D4	D4	D4	D4	D4	D4
E5	E5	E5	E5	E5	E5	E5	E5	E5
F6	F6	F6	F6	F6	F6	F6	F6	F6
H7	H7	H7	H7	H7	H7	H7	H7	H7
J8	J8	J8	J8	J8	J8	J8	J8	J8
K9	K9	K9	K9	K9	K9	K9	K9	K9
L10	L10	L10	L10	L10	L10	L10	L10	L10
M11	M11	M11	M11	M11	M11	M11	M11	M11
N12	N12	N12	N12	N12	N12	N12	N12	N12
P13	P13	P13	P13	P13	P13	P13	P13	P13
R14	R14	R14	R14	R14	R14	R14	R14	R14
S15	S15	S15	S15	S15	S15	S15	S15	S15
T16	T16	T16	T16	T16	T16	T16	T16	T16
U17	U17	U17	U17	U17	U17	U17	U17	U17
V18	V18	V18	V18	V18	V18	V18	V18	V18
W19	W19	W19	W19	W19	W19	W19	W19	W19
X20	X20	X20	X20	X20	X20	X20	X20	X20
Y21	Y21	Y21	Y21	Y21	Y21	Y21	Y21	Y21
Z22	Z22	Z22	Z22	Z22	Z22	Z22	Z22	Z22

3

6798 MVP mother board - Bottom View

WANG

LABORATORIES, INC.

TO: DISTRICT TECHNICAL SPECIALIST (COMPUTER)
FROM: KEITH JONES
DATE: APRIL 20, 1979
SUBJECT: MVP SYSTEM ECN'S

Since the weekly telex came out, about insuring that all ECN's be done prior to installing operating system release 1.6, many questions have arisen concerning the actual revisions of the boards.

Enclosed you will find the major portions of the MVP System with their respective PC Board numbers, latest revision level, and all ECN numbers in order of execution.

Also enclosed, is an ECN directory which has been sorted by ECN Number, and where the ECN can be located. The "MUX Bulletin" referred to in this section is the MUX bulletin that I sent to you a couple of month ago. The "MVP Section" refers to the single sheet ECN's attached to this memo.

This will be updated periodically as I receive new ECN's.

If there are any additions that need to be made or any other products you would like to see this on, please let me know.

Regards,



KEITH JONES
AREA TECHNICAL SPECIALIST

KJ:rb
#2505A

Enclosure

cc: Joe McDermott
Gene Bartos
Scott Tagen

E.C.N. DIRECTORY

E.C.N. No.	WHERE TO FIND E.C.N.
2625	T.P.M. PAGE 500-10
2835	T.P.M. PAGE 500-10
3161	T.P.M. PAGE 500-10A
3563	T.P.M. PAGE 500-16
4271A	T.P.M. PAGE 500-22
4464	T.P.M. PAGE 2230-10
4536	T.P.M. PAGE 2230-11
4808	T.P.M. PAGE 2230-12
5287	T.P.M. PAGE 2230-12
5692	T.P.M. PAGE 2230-12
5860	T.P.M. PAGE 2230-12
5876	T.P.M. PAGE 2200-61
6044	T.P.M. PAGE 2200-62
6045	T.P.M. PAGE 2200-64
6046	T.P.M. PAGE 2200-64
6062	T.P.M. PAGE 2200-64
6369	T.P.M. PAGE 2200-66
6378	T.P.M. PAGE 2230-13
6381	T.P.M. PAGE 2200-66
6461	T.P.M. PAGE 2200-66
6462	T.P.M. PAGE 2200-67
6533	T.P.M. PAGE 2200-67
6604	T.P.M. PAGE 2230-14
6605	T.P.M. PAGE 2230-14
6629	T.P.M. PAGE 2230-14
6856	T.P.M. PAGE 2230-15
6859	T.P.M. PAGE 2200-68
6860	T.P.M. PAGE 2200-69
6949	T.P.M. PAGE 2200-69
6950	T.P.M. PAGE 2200-69
7112	T.P.M. PAGE 2200-70
7115	T.P.M. PAGE 2200-70
7168	T.P.M. PAGE 2230-15
7176A	T.P.M. PAGE 2230-16
7189	T.P.M. PAGE 2200-71
7190	T.P.M. PAGE 2200-71
7190A	T.P.M. PAGE 2200-71
7280	T.P.M. PAGE 2200-72
7285	T.P.M. PAGE 2200-72
7297	T.P.M. PAGE 2200-71
7306	T.P.M. PAGE 2200-72
7318	T.P.M. PAGE 2200-72
7319	T.P.M. PAGE 2270- 9
7426	T.P.M. PAGE 2200-74
7434	T.P.M. PAGE 2200-74
7444	T.P.M. PAGE 2200-74

VP/MVP CPU

BOARD NO.	E-REV	E.C.N.				
6787	1	6461				
6787-1	1	6461				
6788	2	6462	7434			
6788-1	0					
6789	0					
6790	6	6045	6950	7285	9460A	9661 10054
6791	3	6369	9460A	9661		
6792	4	6044	7306	7444	7658	
6793	2	6062	6949			
6793-1	2	9460A	9661			
6797	2	6533	7521			
6798	3	6046	9460A	9661		
7397	1	7529	10796			
7498	0					
7587	0					

(R1 proms did not increment the E-REV.)

MVP MXD CONTROLLER

7290-1	1	8057A				
7291D	2	8036A	10288			(R5 proms did not increment the E-REV.)

2236D TERMINAL

7067	6	5876	6381	7112	7297	7280	7524
7156	1	8975					
7158	5	7115	7318	7426	7498	7819	
7292-1	5	8056A	8056B	8232	9210	9934	

2260 C/BC CONTROLLER

7486	4	9392	9462	9628	10263	
7487	0					
7488	3	9500	9700	10263		

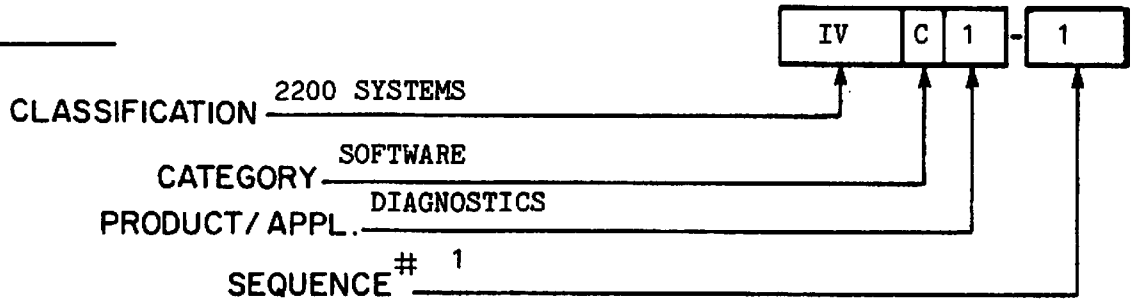
2260B

0341	5	2625	2835	3161	3563	4271
6295	3	5860	6378	6605		
6295-1	5	5860	6378	6605	7168	7176A
6296	1	4536	10600			
6297-3	1	6629				
6298	2	4464	5287			(R1 proms did not increment the E-REV.)
6349	2	6604	6856			
6349-1	1	6856				
6398-1	2	4808	5692			

7456A	T.P.M. PAGE 2200-75
7457	T.P.M. PAGE 2200-75
7498	T.P.M. PAGE 2200-75
7508	MVP SECTION PAGE 2
7521	T.P.M. PAGE 2200-75
7524	T.P.M. PAGE 2200-76
7529	MVP SECTION PAGE 3
7655	T.P.M. PAGE 2270-10
7658	T.P.M. PAGE 2200-77
7758	T.P.M. PAGE 2200-77
7819	T.P.M. PAGE 2200-78
7821	T.P.M. PAGE 2270-11
8036A	T.P.M. PAGE 2200-79
8051	T.P.M. PAGE 2200-80
8056A	MVP SECTION PAGE 8
8056B	MVP SECTION PAGE 4
8057A	T.P.M. PAGE 2200-80
8114	T.P.M. PAGE 2270-13
8232	MVP SECTION PAGE 5
8401	SERVICE NEWSLETTER 110C
8449	SERVICE NEWSLETTER 110C
8450	SERVICE NEWSLETTER 110C
8454	SERVICE NEWSLETTER 110C
8517A	T.P.M. PAGE 2270-14
8666	SERVICE NEWSLETTER 110C
8733	MVP SECTION PAGE 6
8975	MVP SECTION PAGE 7
9010	SERVICE NEWSLETTER 110C
9075	SERVICE NEWSLETTER 110C
9210	I.S.N. 179A
9256	SERVICE NEWSLETTER 110C
9392	MVP SECTION PAGE 9
9460	MVP SECTION PAGE 10
9500	MVP SECTION PAGE 11
9515	SERVICE NEWSLETTER 110C
9628	MVP SECTION PAGE 12
9650	SERVICE NEWSLETTER 110C
9651	SERVICE NEWSLETTER 110C
9661	MVP SECTION PAGE 14
9700	MVP SECTION PAGE 15
9934	MVP SECTION PAGE 16
9997	SERVICE NEWSLETTER 110C
9998	SERVICE NEWSLETTER 110C
10054	MVP SECTION PAGE 17
10224	SERVICE NEWSLETTER 110C
10225	SERVICE NEWSLETTER 110C
10263	MVP SECTION PAGE 19
10518	SERVICE NEWSLETTER 110C
10600	MVP SECTION PAGE 23
10796	MVP SECTION PAGE 24

PRODUCT SERVICE NOTICE

DATE : 9/1/80



TITLE:

MODEL 2200 VP/LVP/MVP/SVP CPU DIAGNOSTICS

NOTE:

This PSN supercedes Section 6 of Model 2200MVP Maintenance Manual, CE# 03-0071-1 (IV.A.3), and Sections 2.8 and 2.9 of Model 2200VP Maintenance Manual, CE #03-0039 (IV.A.3).

There are three classes of diagnostic tests available for the Model 2200 VP/LVP/MVP/SVP CPU's: 1) "BOOTSTRAP" diagnostics (resident in the firmware of the CPU's), 2) Microcode diagnostics (contained on the Operating System diskettes), and 3) BASIC-2 Language diagnostics (available on single-sided, single-density (SSSD) diskette WL #702-0080 and on dual-sided, double-density (DSDD) diskette WL #702-0075). This PSN explains the functions of, and the operating procedures for, the Microcode and BASIC-2 Language diagnostics. The contents of this PSN are outlined in greater detail on the following page. Information concerning the "BOOTSTRAP" diagnostics can be found in the appropriate CPU maintenance manual (see documentation category IV.A.3).



	PAGE
1. MICROCODE DIAGNOSTICS	3
1.1 GENERAL DESCRIPTION	3
1.2 LOADING PROCEDURES	4
1.3 NORMAL (CORRECT OPERATION) AND ERROR DISPLAYS	9
1.3.1 CPU DIAGNOSTIC	9
1.3.2 CONTROL MEMORY DIAGNOSTICS	11
1.3.3 DATA MEMORY DIAGNOSTICS	17
1.3.4 REGISTERS DIAGNOSTICS	24
1.4 DETAILED TEST DESCRIPTION	28
1.4.1 CPU DIAGNOSTIC	28
1.4.2 CONTROL MEMORY DIAGNOSTICS	28
1.4.3 DATA MEMORY DIAGNOSTICS	31
1.4.4 REGISTERS DIAGNOSTICS	33
2. MEMORY ERROR CHIP IDENTIFICATION (MECI) PROGRAM	36
3. BASIC-2 LANGUAGE DIAGNOSTICS	40
3.1 LOADING/OPERATING PROCEDURES	40
3.2 NORMAL (CORRECT OPERATION) DISPLAYS	41

1. MICROCODE DIAGNOSTICS

1.1 GENERAL DESCRIPTION

The Microcode diagnostics are microcoded routines that test the hardware components of the CPU and attempt to pinpoint any malfunction. These routines are divided into two classes: User diagnostics, and Field Service diagnostics. In general, the User diagnostics comprise a chain of tests which are executed without operator intervention. (The selected sequence repeats until RESET is keyed.) The Field Service diagnostics will repetitively execute only a specified test until RESET is keyed. The menu for either of the diagnostic classes (User or Field Service) may be selected via a special function (SF') key when the BOOTSTRAP request "KEY SF'?" is displayed.

The User diagnostics are divided into three categories: 'CPU', 'Control Memory', and 'Data Memory' (User Memory). The Field Service diagnostics are divided into the same categories as the User diagnostics with the addition of a fourth--'Registers'. These categories are, in turn, subdivided into individual tests (ref: TABLE 1). The desired category or test within a category (dependent on what class of diagnostics is loaded--User or Field Service) is selected, via a special function key, from the appropriate diagnostic menu (User or Field Service).

TABLE 1 DIAGNOSTIC TESTS

<u>CLASS</u>	<u>CATEGORY</u>	<u>TEST(S)</u>
User & Field Service	CPU	CPU
User & Field Service	Control Memory	ADDRESSING MAT C&S ROWPAT
User & Field Service	Data Memory	ADDRESSING MAT C&S ROWPAT
Field Service Only	Registers	REGISTERS AUXILIARY REGISTERS STACK REGISTERS

1.2 LOADING PROCEDURES

NOTE:

Refer to the appropriate CPU maintenance manual in documentation category IV.A.3 for more complete information concerning BOOTSTRAP operation.

There are three functions that may be selected at the time the BOOTSTRAP request "KEY SF'?" is displayed.

- 1) Load BASIC-2.
- 2) Load User diagnostics menu.
- 3) Load Field Service diagnostics menu.

Either the User or Field Service menu may be selected by depressing the appropriate special function key, as listed in TABLE 2, in response to the "KEY SF'?" message.

TABLE 2 SPECIAL FUNCTION KEY DESIGNATIONS

<u>SF' KEY</u>	<u>LOADS</u>	<u>FROM DISK ADDRESS</u>
00	BASIC-2	310
01	BASIC-2	B10
02	BASIC-2	320
03	BASIC-2	B20
04	BASIC-2	330
05	BASIC-2	B30
08	BASIC-2	350
09	BASIC-2	B50
10	BASIC-2	360
11	BASIC-2	B60
12	BASIC-2	370
13	BASIC-2	B70
16	User menu	310
17	User menu	B10
18	User menu	320
19	User menu	B20
28	Field Service menu	310
29	Field Service menu	B10
30	Field Service menu	320
31	Field Service menu	B20

If BASIC-2 is selected by the operator, access to either of the other two groups is not possible without reinitializing the central processor (via CPU power off/on, or \$INIT).

If either the User menu or Field Service menu is selected, access to either of the other two groups is possible by keying RESET and then by selecting either another diagnostic menu or BASIC-2. (No reinitialization is necessary in this case.)

BOOTSTRAP ignores all undefined function keys while waiting for a response to the "KEY SF'?" message. Should a function key be depressed that specifies an unused HEX address (no device at that address), BOOTSTRAP will halt; BOOTSTRAP always waits for a ready condition from the disk. In case the wrong SF' key is pressed, keying RESET restores the "KEY SF'?" message to the display of the "system console".

When either the User or Field Service menu is selected, the appropriate diagnostic menu is displayed (ref: FIGURES 1 & 2).

```
KEY SF'?
```



```
USER DIAGNOSTIC MENU
```



```
'00 CPU DIAGNOSTIC           '02 DATA MEMORY DIAGNOSTIC
```

```
'01 CONTROL MEMORY DIAGNOSTIC
```

FIGURE 1 USER MENU SCREENLOAD

When the User diagnostics menu is selected, the operator may select:

- SF'00 to load and run the CPU diagnostic.
- SF'01 to load and run the Control Memory diagnostics.
- SF'02 to load and run the Data Memory diagnostics.

<u>USER DIAGNOSTIC CATEGORY</u>	<u>SEQUENCE PERFORMED</u>	<u>RUNNING TIME</u>
CPU	Loads and runs the CPU diagnostic only. Runs continuously.	3 passes per second
Control Memory	Loads ADDRESSING, MAT C&S and ROWPAT. Runs ADDRESSING for 5 loops, MAT C&S for 5 loops, and ROWPAT for 1 loop, then repeats sequence.	3 minutes per pass
Data (User) Memory	Loads ADDRESSING, MAT C&S and ROWPAT. Runs ADDRESSING for 5 loops, MAT C&S for 5 loops, and ROWPAT for 1 loop; the entire sequence then repeats.	Size-dependent

KEY SF'?

FIELD SERVICE DIAGNOSTIC MENU

'00 CPU DIAGNOSTIC	'05 MAT C&S 8
'01 ADDRESS 24	'06 ROWPAT 8
'02 MAT C&S 24	'07 REGISTERS
'03 ROWPAT 24	'08 AUXILIARY REGISTER
'04 ADDRESS 8	'09 STACK REGISTER

FIGURE 2 FIELD SERVICE MENU SCREENLOAD

When the Field Service diagnostics menu is selected, the operator may individually select:

- SF'00 to load and run the CPU diagnostic.
- SF'01 to load and run the Control Memory ADDRESSING diagnostic.
- SF'02 to load and run the Control Memory MAT C&S diagnostic.
- SF'03 to load and run the Control Memory ROWPAT diagnostic.
- SF'04 to load and run the Data Memory ADDRESSING diagnostic.
- SF'05 to load and run the Data Memory MAT C&S diagnostic.
- SF'06 to load and run the Data Memory ROWPAT diagnostic.
- SF'07 to load and run the REGISTERS diagnostic.
- SF'08 to load and run the AUXILIARY REGISTERS diagnostic.
- SF'09 to load and run the STACK REGISTERS diagnostic.

Note that in the Field Service diagnostics, special function key '15 is defined uniquely to allow chaining of Registers diagnostics. After selecting one of the Registers diagnostics, keying RESET and then SF'15 will cause all three Registers diagnostics to run sequentially.

FIELD SERVICE
DIAGNOSTIC
CATEGORY

SEQUENCE PERFORMED

RUNNING TIME

CPU	Loads and runs CPU diagnostic only. Runs continuously.	3 passes per second
Control Memory	Loads ADDRESSING, MAT C&S, and ROWPAT. Runs only the selected diagnostic (continuously).	ADDRESSING-- 3 seconds per pass MAT C&S-- .5 seconds per pass ROWPAT-- 2.5 minutes per pass
Data (User) Memory	Loads ADDRESSING, MATC&S and ROWPAT. Runs only the selected diagnostic continuously.	Size-dependent
Registers	Loads REGISTERS, AUXILIARY REGISTERS and STACK REGISTERS. Runs only the selected diagnostic (continuous-run).	REGISTERS-- .07 seconds per pass AUXILIARY REGISTERS-- .5 seconds per pass STACK REGISTERS-- 1 second per pass

Note that in order to select another test, one of the two diagnostic menus must first be reselected. Therefore, after each test, key RESET, key the appropriate SF' key for selection of a menu, then select the desired test from the menu just selected.

When RESET is keyed during any diagnostic program, the "KEY SF'?" message will be displayed.

If HALT/STEP is keyed during any of the Registers diagnostics, the program will be interrupted only after an error has been detected and displayed. To resume execution after the program has been halted, key HALT/STEP again.

1.3 NORMAL (CORRECT OPERATION) AND ERROR DISPLAYS

1.3.1 CPU DIAGNOSTIC

NORMAL DISPLAY:

While the program is being loaded,

LOADING: CPU DIAGNOSTIC (date)

will be displayed along with the diagnostic menu; then:

*** CPU DIAGNOSTIC ***

PASS LLLL

IMMED REG XX

REG INSTR XX

X-REG INSTR XX

MASK BR XX

REG BR XX

IMMED R/W XX

REG R/W XX

AUX/STACK R/W XX

where: LLLL = Number of completed loops
 XX = Microinstruction currently
 being tested (ref: TABLE 3).

ERROR DISPLAY:

*** CPU DIAGNOSTIC ***

PASS LLLL

IMMED REG XX

REG INSTR XX

X-REG INSTR XX

MASK BR XX

REG BR XX

IMMED R/W XX

REG R/W XX

AUX/STACK R/W XX

where: LLLL = Number of completed loops
 XX = Microinstruction currently
 being tested (ref: TABLE 3).

Should the system be unable to execute a particular instruction, the CRT cursor will stop at XX of the failing instruction. Should the title fail to appear, any of the following could be at fault: ORI, AC, SB, SR, B, BT, BF, BNE, BLER, or BNR.

TABLE 3 2200LVP/SVP INSTRUCTION SET

Instr. Code	Instr. Tested	Instr. Class	Instr. Code	Instr. Tested	Instr. Class
00	ORI	IMMEDIATE REGISTER	4B	OR(R/W)	REGISTER R/W
01	XORI		4C	XOR(R/W)	
02	ANDI		4D	AND(R/W)	
03	A		4E	SC(R/W)	
04	DACI		4F	DAC(R/W)	
05	DSCI		50	DSC(R/W)	
06	ACI		51	AC(R/W)	
07	MI		52	M(R/W)	
08	OR	REGISTER	53	SHIFT(R/W)	
09	XOR		54	LPI(R/W)	
0A	AND		55	SR(R/W)	
0B	SC		56	TAP, TPA, XPA(R/W)-00	
0C	DAC		57	-01	
0D	DSC		58	-02	
0E	AC		59	-03	
0F	M		5A	-04	
10	SHIFT	5B	-05		
12	ORX	EXTENDED REGISTER	5C	-06	
13	XORX		5D	-07	
14	ANDX		5E	-08	
15	SCX		5F	-09	
16	DACX		60	-0A	
17	DSCX		61	-0B	
18	ACX		62	-0C	
19	MX		63	-0D	
1A	SHIFT X		64	-0E	
1B	BF/BT		MASK BRANCH	65	-0F
1C	BNE/BEQ	66		-10	
1D	BNR/BER	REGISTER BRANCH	67	-11	
1E	BLR		68	-12	
1F	BLRX		69	-13	
20	BLER		6A	-14	
21	BLERX		6B	-15	
43	ORI(R/W)		6C	-16	
44	XORI(R/W)		6D	-17	
45	ANDI(R/W)		6E	-18	
46	AI(R/W)	IMMEDIATE R/W	6F	-19	
47	DACI(R/W)		70	-1A	
48	DSCI(R/W)		71	-1B	
49	ACI(R/W)		72	-1C	
4A	MI(R/W)		73	-1D	
			74	-1E	
			75	-1F	
			76	STACK(R/W)	

1.3.2 CONTROL MEMORY DIAGNOSTICS

NORMAL DISPLAY:

While the program is being loaded,

```
LOADING: CONTROL MEMORY DIAGNOSTIC (date)
```

will be displayed along with the diagnostic menu; then:

```
*** CONTROL MEMORY DIAGNOSTIC ***           MEMORY SIZE = OXXXX
NO ERR'S   PRESS 'P' TO PRINT ERRORS AT /215 ('T' FOR /204).

PRESS 'CONTINUE' TO START
```

where: XXX = the amount of memory.

After keying CONTINUE, the last line displayed is changed to:

```
(name of test) (PASS LLLL)--
```

where: LLLL = Number of loops completed
 (name of test) = The appropriate test name. If the User menu was selected, this name will change automatically as the tests are completed.

ERROR DISPLAYS:

If an error is detected, the error message will be displayed under the same test name. The test will be restarted, and if another error occurs, that message will be displayed under the first error message. This procedure repeats until the screen is full. At this point, CONTINUE may be keyed to continue the test.

Occasionally, MAT C&S will display two error messages on the same line when it cannot isolate the problem completely; the more likely error is displayed first.

Information detailing how to correlate a specific error message to a defective RAM can be found at the end of this subsection. There, a chart is available that allows for translation of an error message to a specific RAM chip location.

When the system detects a Control Memory failure, one of the following error messages is displayed:

AECM -- Addressing Error in Control Memory
BECM -- Bit Error in Control Memory
PECM -- Parity Error in Control Memory
VECM -- Verify Error in Control Memory

1) AECM aaaa bbbb xxxxxx

Where: aaaa = The address of the instruction in error
bbbb = The conflicting address
xxxxxx = An XOR of the expected and actually-read instruction

This error indicates that writing to Control Memory location bbbb seems to modify location aaaa. The "1" bits in the xxxxxx field of the display indicate which bit(s) have been modified. The error could also occur if a chip at location aaaa had a marginal failure.

2) BECM aaaa xxxxxx

Where: aaaa = The address of the instruction in error
xxxxxx = An XOR of the instruction actually read from memory with the instruction that was expected to be there.

This error implies that a bit error was detected while reading Control Memory. The "1" bits in the xxxxxx field of the display indicate which bit(s) are incorrect.

3) PECM aaaa ddddd

Where: aaaa = The address of the instruction with bad parity.
 ddddd = The instruction located at aaaa. The instruction is reread when displayed and thus may not be the same as when the error occurred.

This error implies that bad parity was detected during execution of the diagnostic. Bad parity may be the result of:

- a) Bits dropped
- b) Bits picked up
- c) Bad parity written
- d) Bad parity-check logic

4) VECM aaaa

Where: aaaa = An address in the section of Control Memory that does not verify correctly.

Normally, this error will only be reported when the loading of a system program from disk into Control Memory is not successful.

Control Memory Diagnostic Error Interpretation

Following is an example and charts explaining how to decode the memory diagnostic error messages to point out exactly which RAM has failed. The example given relates specifically to the newer-version Control Memory board (WL #210-7588). The procedure is the same for the older-version Control Memory board (WL #210-6788).

EXAMPLE: error message--BECM 02D7 0C0000

The error was a Bit Error in Control Memory.

The address of the failing location was 02D7 (HEX).

The XOR of the expected and actually-read data was 0C0000 (HEX).

FIGURE 3 shows that the failing location is contained in the top two rows of RAM's (error was between 0000 and 3FFFF (HEX)).

By inserting the XOR result (0C0000) into the blocks depicting the ROW SECTIONS, it can be seen that row section E (located in the second row from the top of the board) contains the faulty RAM's.

The bits that failed were 4 and 8 (from XOR--HEX(C) is equal to bits 4 and 8 ON); therefore, the bad RAM's are in the second row from the top of the board, and are the fifth and sixth RAM's from the right side of the board.

If the failing address was between 4000 and 7FFF (HEX), the procedure for determining which RAM was faulty is the same as described above, except the RAM would be located in the bottom two rows.

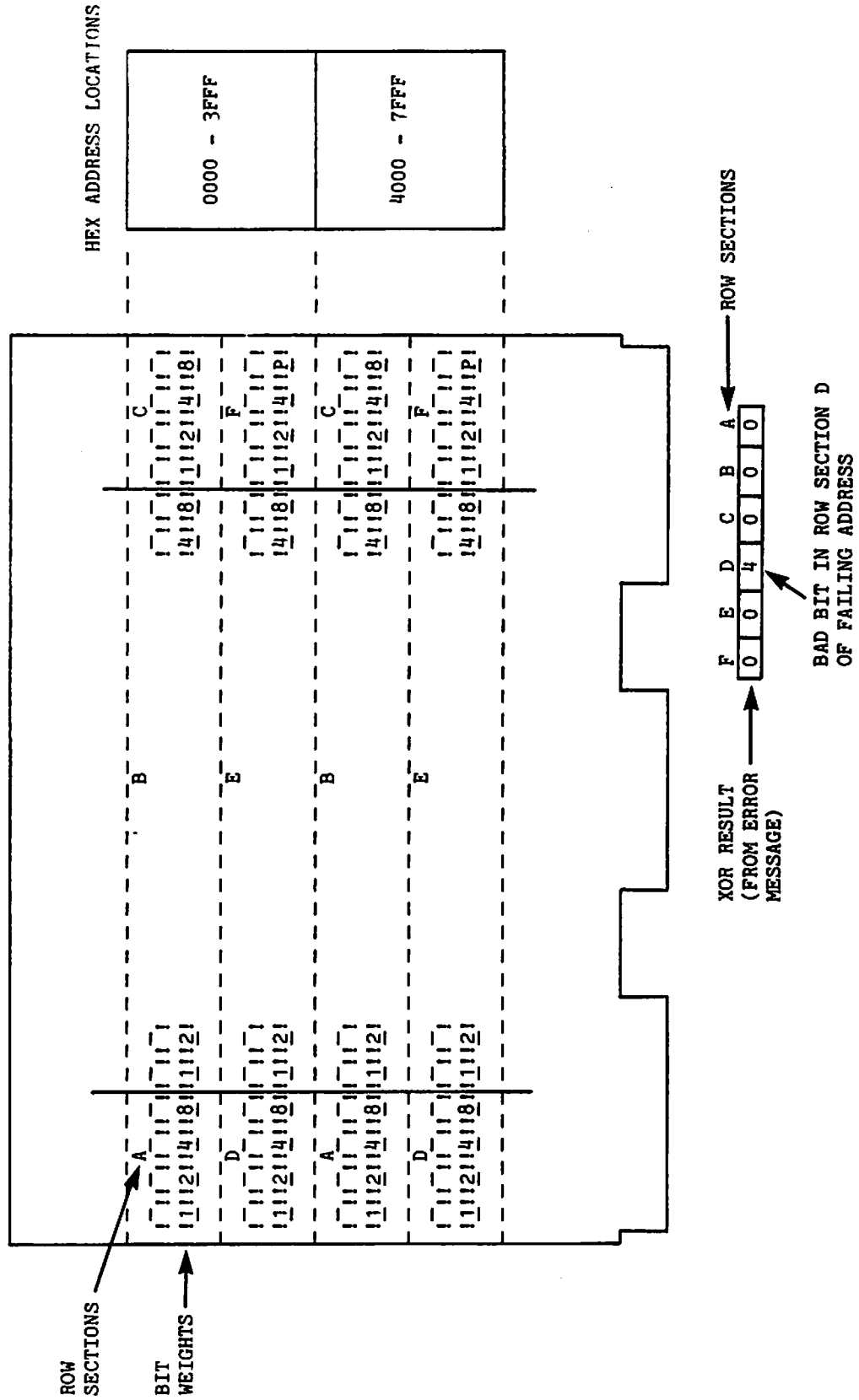


FIGURE 3 WL #210-7588 CONTROL MEMORY ADDRESS CONFIGURATION

HEX ADDRESS LOCATIONS

WHEN LOADED IN DATA MEM. BOARD SLOT #1	WHEN LOADED IN DATA MEM. BOARD SLOT #2
0000 - 0FFF	3000 - 3FFF
1000 - 1FFF	2000 - 2FFF
4000 - 4FFF	5000 - 5FFF

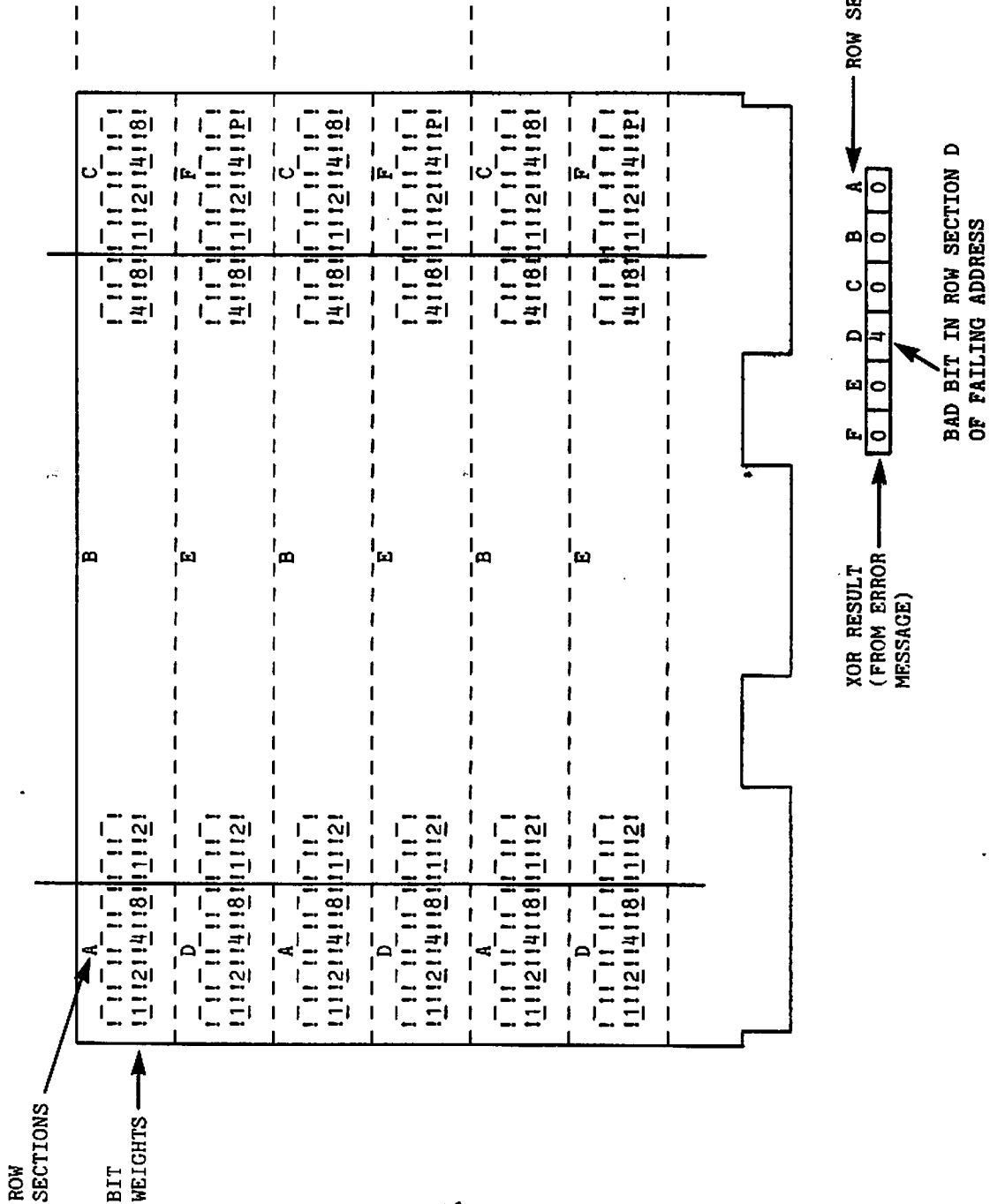


FIGURE 4 WL #210-6788 CONTROL MEMORY ADDRESS CONFIGURATION

2) BEDM ss.aaaa xxyy

Where: ss = Memory bank containing the error (00 = bank #1; 40 = bank #2; 80 = bank #3; C0 = bank #4)
 aaaa = Address of the data in error
 xxyy = XOR of the data actually read from User/Data memory with the data that was expected to be there.
 xx = Corresponds to the byte at location aaaa
 yy = Corresponds to the byte at location aaaa+1

This error implies that a memory error was detected while reading User/Data Memory. The "1" bits in the xxyy field of the display indicate which bit(s) are not correct. If all the bits are zero, one of the two parity bits associated with the pair of bytes read is incorrect.

3) PEDM ss.aaaa

Where: ss = Memory bank containing the error (00 = bank #1; 40 = bank #2; 80 = bank #3; C0 = bank #4)
 aaaa = Data memory address (i.e., the current value of the PC's) at the time of the error. This is probably, but not necessarily, the address of the memory location with bad parity.

This error implies that bad parity was detected during a read of 8-bit User/Data Memory. Bad parity may be the result of:

- a) Bits dropped
- b) Bits picked up
- c) Bad parity written
- d) Bad parity-check logic

NOTE:

In order to determine which bit is bad, a technician may ground L41 pin 3 on the 6789 board; this action disables parity-error logic. If this is performed, a different error message will be displayed.

4) REDM ss.aaaa xx

Where: ss = Memory bank containing the error (00 = bank #1; 40 = bank #2; 80 = bank #3; C0 = bank #4)
 aaaa = Address of the data in error
 xx = XOR of the data in memory with the data that was expected to be there.

This error implies that a memory error was detected while reading User/Data Memory. The "1" bits on the xx field of the display indicate which bits are not correct. If all the bits are zero, a bit in the other byte of the pair of bytes is incorrect.

5) VEDM ss.aaaa

Where: ss = Memory bank containing the error (00 = bank #1; 40 = bank #2; 80 = bank #3; C0 = bank #4)
 aaaa = Address of the data in error

Normally, this error will only be reported when the loading of system program constants from disk into Data Memory is not successful.

Data Memory Diagnostic Error Interpretation

Following is an example and charts explaining how to decode the memory diagnostic error messages to point out exactly which RAM has failed. The example given relates specifically to the newer-version Data Memory board (WL #210-7587). The procedure is the same for the older-version Data Memory board (WL #210-6787).

EXAMPLE: error message--BEDM 40.A3C4 8204

The error was a Bit Error in Data Memory.

The failing address is located in bank #2 (40.).

The address of the failing location was A3C4 (HEX).

The XOR of the expected and actually-read data was 8204 (HEX).

FIGURE 5 shows that the failing address is in the top two rows of RAM's (error was in bank #2).

The figure also shows that the failing location is contained in the top row of RAM's (error was between 8000 and FFFF (HEX)).

The failing address was even (A3C4); therefore, the faulty RAM('s) is somewhere on the left side of the top row of RAM's.

The bits that failed were 2 and 80 (from first two digits of XOR--HEX(82) is equal to bits 2 and 80 ON); therefore, the bad RAM's are in the top row, and are the second and eighth RAM's from the left side of the board.

In this example there is one additional RAM that failed.

The last two digits of the XOR (04) indicate that bit 4 in location A3C5 (address + 1) also failed.

The corresponding RAM is in the top row, seventh from the right side (odd address) of the board.

HEX ADDRESS LOCATIONS
AND BANK NUMBERS

WHEN LOADED IN DATA MEM. BOARD SLOT #1	WHEN LOADED IN DATA MEM. BOARD SLOT #2
8000 - FFFF (BANK #2)	8000 - FFFF (BANK #4)
0000 - 7FFF (BANK #2)	0000 - 7FFF (BANK #4)
8000 - 7FFF (BANK #1)	8000 - 7FFF (BANK #3)
0000 - 7FFF (BANK #1)	0000 - 7FFF (BANK #3)

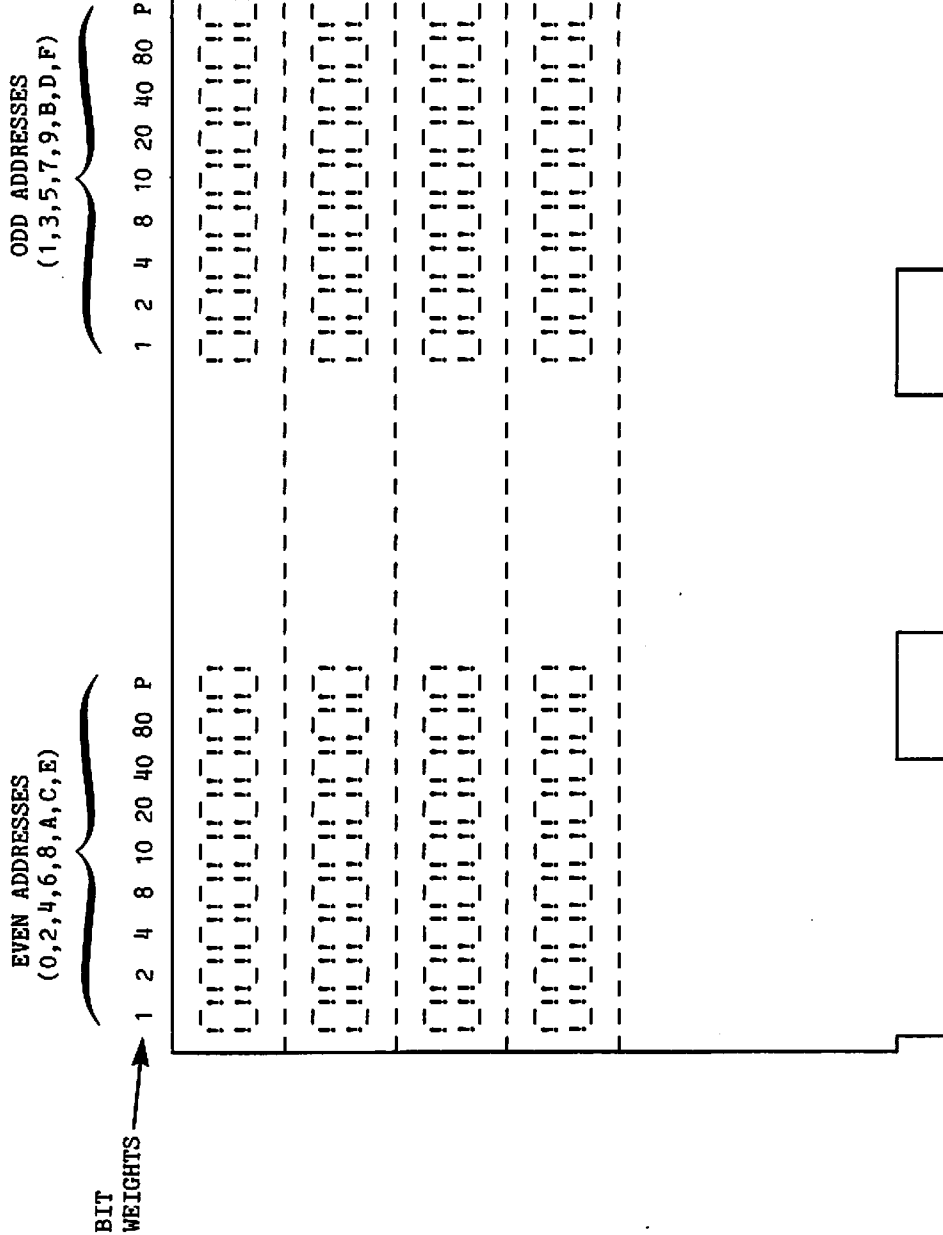


FIGURE 5 WL #210-7587 DATA MEMORY ADDRESS CONFIGURATION

HEX ADDRESS LOCATIONS
AND BANK NUMBERS

WHEN LOADED IN DATA MEM. BOARD SLOT #1	WHEN LOADED IN DATA MEM. BOARD SLOT #2
4000 - 5FFF (BANK #1)	C000 - DFFF (BANK #1)
6000 - 7FFF (BANK #1)	E000 - FFFF (BANK #1)
0000 - 1FFF (BANK #1)	8000 - 9FFF (BANK #1)
2000 - 3FFF (BANK #1)	A000 - BFFF (BANK #1)

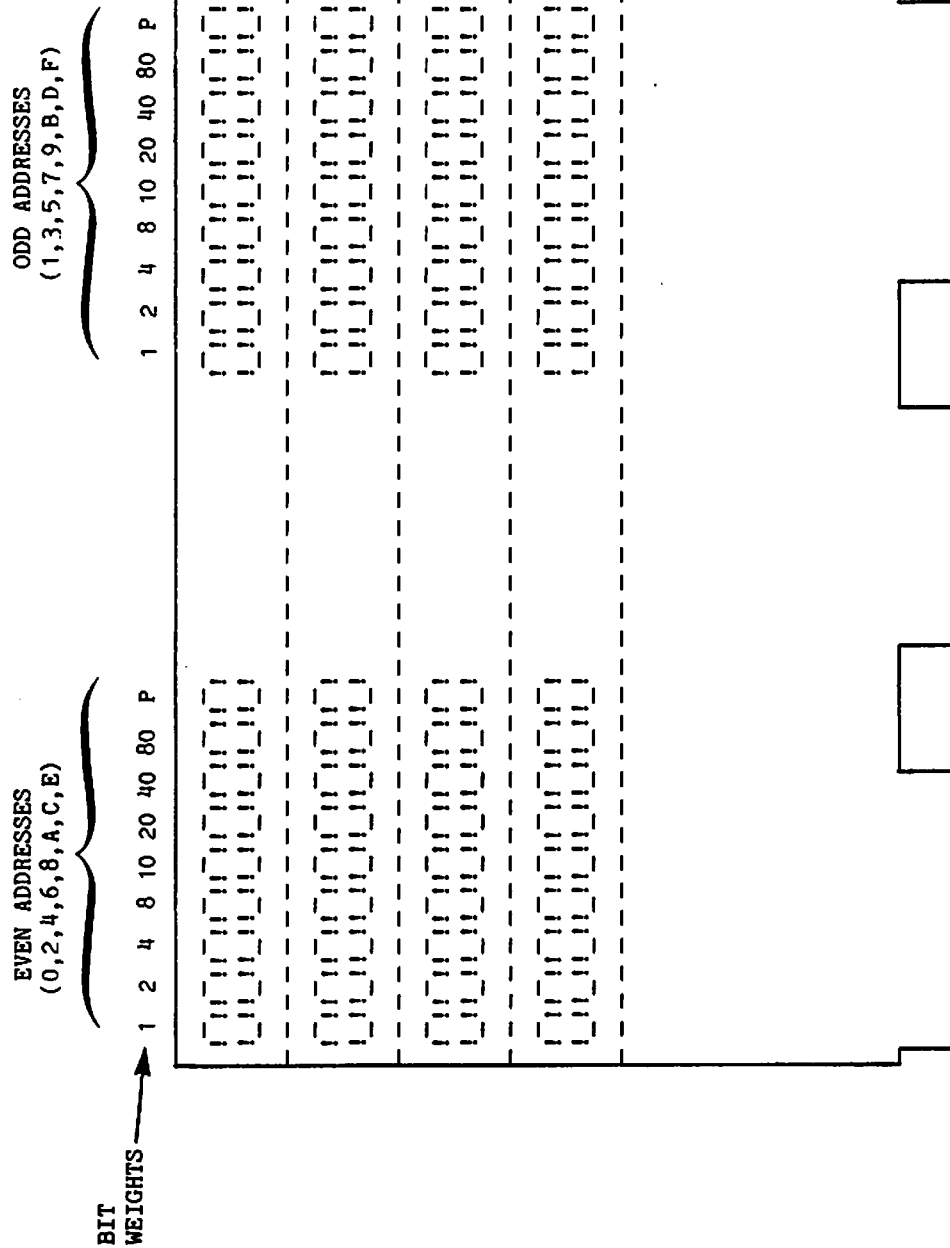


FIGURE 6 WL #210-6787 DATA MEMORY ADDRESS CONFIGURATION

1.3.4 REGISTERS DIAGNOSTICS

REGISTERS test--

NORMAL DISPLAY:

While the program is being loaded,

LOADING: REGISTER DIAG. (date) AT (time)

will be displayed along with the diagnostic menu; then:

REGISTER TEST

LLLL where: LLLL = number of completed loops

ERROR DISPLAYS:

1) REGISTER TEST

FFFF

REGISTER TT AND CC ERROR (XX)

LLLL

where: FFFF = Number of completed loops at time of error

TT = Name of register under test

CC = Name of conflict register

XX = Contents of register CC

This error is caused when testing register TT, register CC was found not to contain the expected.

2) REGISTER TEST
 # FFFF
 REGISTER TT ERROR (XX)
 # LLLL

where: FFFF = Number of completed loops at time of error
 TT = Name of register under test
 XX = Contents of register CC

This error is caused when the register under test fails to hold the test pattern.

AUXILIARY REGISTERS test--

NORMAL DISPLAY:

AUXILIARY TEST
 # LLLL where: LLLL = number of completed loops

ERROR DISPLAYS:

1) AUXILIARY TEST
 # FFFF
 AUX TT FAILURE (XXXX)
 # LLLL

where: FFFF = Number of completed loops at time of error
 TT = Auxiliary register under test
 XXXX = XOR of expected and actual data pattern

This error occurs when the Auxiliary register under test is found not to contain the expected test pattern.

2) AUXILIARY TEST
FFFF
AUX TT AND AUX CC FAILURE (XXXX)
LLLL

where: FFFF = Number of completed loops at time of error
TT = Auxiliary register under test
CC = Conflict register
XXXX = XOR of expected and actual data pattern

This error is caused when Auxiliary register CC was found not to contain the expected test pattern.

3) AUXILIARY TEST
FFFF
STACK AND AUX TT FAILURE (XXXX)
LLLL

where: FFFF = Number of completed loops at time of error
TT = Auxiliary register under test
XXXX = XOR of expected and actual data pattern

This error is caused when a Stack level was found not to contain the expected test pattern.

STACK REGISTERS--

NORMAL DISPLAY:

STACK TEST
LLLL where: LLLL = Number of completed loops

ERROR DISPLAYS:

1) STACK TEST
FFFF
STACK FAILURE (XXXX)
LLLL

where: FFFF = Number of completed loops at time of error
XXXX = XOR of expected and actual data pattern

This error is caused when a Stack level fails to maintain the expected pattern.

2) STACK TEST
FFFF
AUX YY FAILURE (XXXX)
LLLL

where: FFFF = Number of completed loops at time of error
YY = Auxiliary register
XXXX = XOR of expected and actual data pattern

This error is caused when a particular Auxiliary register fails to maintain the expected pattern.

1.4 DETAILED TEST DESCRIPTION

1.4.1 CPU DIAGNOSTIC

This diagnostic is designed to test the instruction set of the 2200LVP. The test sequence is as follows:

- a) Test Immediate Register instructions.
- b) Test Register instructions.
- c) Test Extended Register instructions.
- d) Test Branch instructions.
- e) Test Immediate Register instructions with Read/Write.
- f) Test Register instructions with Read/Write.
- g) Test Mini Instructions with Read/Write.
- h) Return to step a).

1.4.2 CONTROL MEMORY DIAGNOSTICS

ADDRESSING--

This diagnostic floods Control Memory RAM with alternate 1's and 0's (two opposed patterns) and then executes a read--after the writing for each pattern is completed--from location 0800 (HEX) to the last location in Control Memory and vice versa, searching for a memory location which may have been changed by writing into some other location. This is accomplished in the following manner:

- a) Flood memory with HEX 5A's (0101 1010₂).
- b) Starting at location 0800 (HEX) and searching forward to the end of Control Memory, read each location and check for the 5A pattern. If a location verifies "O.K." when checked, write an A5 (1010 0101) at that same location.
- c) Starting at the end of Control Memory (this does not include BOOTSTRAP addresses) and searching backward to Control Memory location 0800 (HEX), read each location and check for the A5 pattern. If a location verifies "O.K." when checked, write a 5A (HEX) at that same location.

MAT C&S--

This diagnostic is designed to test from the end of the diagnostic program to the end of Control Memory, and is accomplished as follows:

- a) The length of a random pattern to be written into all Control Memory locations is determined; this length is from 1 to 256 8-bit random characters.
- b) The random pattern is written into a section of Control Memory.
- c) The last-written section of memory is read, and then the random pattern is written into the next section of memory.
- d) Repeat step c) until all Control Memory locations are filled with the random pattern.
- e) Read the contents of the first memory section that was written into, and then verify that that the contents of every location in that section of memory is identical to the original random pattern.
- f) Using the pattern in the first-written section of Control Memory as the standard to which the contents of other locations in Control Memory will be compared, read each remaining memory section and verify that each location contains the same, original random pattern.
- g) Steps e) and f) are repeated five times (reread count); that accomplished, the test restarts at step a).

ROWPAT--

This diagnostic performs a bit-by-bit test of Control Memory, searching for a bit location in a row or column common to the "Test Cell", which may have been changed when this "Test Cell" was written into. In order to understand the nature of this test, the following terms should be understood.

Test Cell - The bit location being tested in a memory chip (2⁴ chips simultaneously).

Conflict Cell - The bit location in a memory chip being tested for conflict with the Test Cell.

Row - A row of addresses within the memory chip, one of which is the test cell row address.

Column - A column of addresses within the memory chip, one of which is the test cell column address.

Board Row - One of the three rows of 24 memory chips located on a Control Memory pc board.

Test Pattern - The pattern expected to be found in all other cells (conflict cells). Either 0 or 1 depending on which pass the program is executing.

Memory Test Area - From address 1000 to the end of memory if the program is in low memory, and from 0000 to 1000 if program is in high memory.

The diagnostic is performed as follows:

- a) Flood the current memory test area with zeroes.
- b) Read the current test cell for the flood pattern.
- c) Compliment the flood pattern and write into the test cell.
- d) Read the test cell for the test pattern.
- e) Read the conflict cell for the flood pattern.
- f) Repeat steps d) and e) making the conflict cell the next location within the column and then within the row.
- g) Write the flood pattern at the test cell.
- h) Repeat steps b) through g), making the test cell the next location within the row until the test cell has stepped through each memory location within that row.
- i) Repeat steps b) through h) for each row within the memory test area.
- j) Flood the current memory with ones (1's) and repeat steps a) through j).
- k) Move the test program from low memory to high memory and repeat steps a) through j).
- l) Move the test program from high to low memory.

1.4.3 DATA (USER) MEMORY DIAGNOSTICS

ADDRESSING--

This diagnostic floods Data Memory RAM with alternate 1's and 0's (two opposed patterns) and then executes a read--after the writing for each pattern is completed--from start to end of User Memory and vice-versa, searching for a memory location that may have been changed when writing into a different location. This addressing test is specifically accomplished as follows:

- a) Flood memory with 5A's (0101 1010).
- b) Starting at the beginning of User Memory and searching forward to the end, each location is read and checked for the 5A pattern. If the location verifies "O.K." when checked, an A5 (1010 0101) is written at that location.
- c) Starting at the end and searching backward to the beginning of User Memory, each location is read and checked for the A5 pattern. If the location verifies "O.K." when checked, a 5A is written at that location.

MAT C&S--

This diagnostic is designed to test from start to end of User Memory, and is accomplished as follows:

- a) Determine the length of a random pattern to be written to all of User Memory. The length is from 1 to 256 8-bit random characters.
- b) Write the random pattern into a section of User Memory.
- c) Read the last-written section of User Memory and write into the next section.
- d) Repeat step c until all of User Memory is filled with the random pattern.
- e) Read the contents of the first section of User Memory that was written and verify that it is correct by regenerating the pattern.
- f) Using the pattern in the first-written section of memory as the original, read the remaining sections of memory and verify their accuracy against the first.

- g) Repeat steps e and f five times (reread count) and then repeat the entire procedure, starting at step a, above.

ROWPAT--

This diagnostic tests every User Memory bit location having a row or column address common to the row or column address of the test cell. Typically, one such bit location may have been changed when writing into the test cell. To better understand the nature of this test, the following terms must be understood.

Test Cell - The bit location being tested (16 chips simultaneously).

Conflict Cell - The bit location being tested for conflict with the Test Cell.

Row - A row of addresses within the memory chip; one particular location in the row is the test cell.

Column - A column of addresses within the memory chip; one particular location in the column is the test cell.

Chip Row - One of the four rows of 18 memory chips located on each Data (User) Memory board.

Test Pattern - The pattern expected to be found in the test cell. Either one or zero depending on which pass the program is executing.

Flood Pattern - The pattern expected to be found in all other cells (conflict cells). Either zero or one, depending on which pass the program is executing.

The diagnostic is performed as follows:

- a) Flood all of User Memory with zeroes.
- b) Read the current test cell for the flood pattern.
- c) Compliment the flood pattern and write that into the test cell.

- d) Read the test cell for the test pattern.
- e) Read the conflict cell for the flood pattern.
- f) Repeat steps d) and e), making the conflict cell the next location within the column, and then within the row.
- g) Write the flood pattern at the test cell.
- h) Repeat steps b) through g), making the test cell the next location within the row until the test cell has stepped through each memory location within the row.
- i) Repeat steps b) through h) for each row in User Memory.
- j) Flood all User Memory locations with one's and repeat steps b) through i).

1.4.4 REGISTERS DIAGNOSTICS

REGISTERS--

This diagnostic is designed to test the F0-F7, CH, CL, PH, PL, SL and K registers in such a manner that it may be determined whether or not bits have gone bad, or whether a conflict in addressing (of registers) exists. It is accomplished in the following manner:

- a) Flood all registers with all zeroes.
- b) For each register:
 - 1. Set the test pattern to 00.
 - 2. Set the test register to the test pattern value.
 - 3. Verify that the test register holds the test pattern value.
 - 4. Verify that the other registers have not been changed.
 - 5. Add 01 to the test pattern value.
 - 6. Repeat steps 2 through 5 until test pattern equals 00.
 - 7. Repeat steps 1 through 6 until all registers have been tested.

Note that the SH register is not tested, due to the ability of system hardware to change its bit status.

AUXILIARY REGISTERS--

This diagnostic is designed to check the Auxiliary registers to determine whether each Auxiliary register will:

- a) Hold a particular pattern.
- b) Have any effect on any other auxiliary register.
- c) Have any effect on any stack level.

Two separate patterns are used by the routine:

- a) Test pattern - One of 8 patterns (below) which is expected to be in the Auxiliary register under test.

- | | | |
|----|-----------|-----------|
| 1. | 0000 0001 | 0000 0001 |
| 2. | 0000 0010 | 0000 0010 |
| 3. | 0000 0100 | 0000 0100 |
| 4. | 0000 1000 | 0000 1000 |
| 5. | 0001 0000 | 0001 0000 |
| 6. | 0010 0000 | 0010 0000 |
| 7. | 0100 0000 | 0100 0000 |
| 8. | 1000 0000 | 1000 0000 |

- b) Conflict pattern - Either all 0's or all 1's, depending on what pass the program is executing.

The tests are executed as follows:

- a) All Auxiliary registers and the Stack are initialized with the conflict pattern.
- b) The current test Auxiliary register is written with the current test pattern.
- c) The test Auxiliary register is read as follows:
 - 1. TPA - writes the test pattern.
 - 2. PC's are complemented.
 - 3. XPA - reads the test pattern.

4. PC's are checked against the expected pattern.
 5. TAP - reads the complemented test pattern.
 6. PC's are complemented again.
 7. PC's are checked against the expected pattern.
-
- d) The remaining Auxiliary registers and the stack are checked to determine whether or not they still contain the conflict pattern.
 - e) Steps b) through d) are repeated until all test patterns have been tested.
 - f) Steps b) through e) are repeated until all 32 Auxiliary registers have been tested.
 - g) The conflict pattern is complemented and steps a) through f) are repeated.

STACK REGISTERS--

This diagnostic is designed to check the Stack, to determine whether each Stack level will:

- a) Hold a particular pattern.
- b) Have an effect on any other Stack level.
- c) Have an effect on any Auxiliary register.

2. MEMORY ERROR CHIP IDENTIFICATION (MECI) PROGRAM

MECI is not a diagnostic, but is a program that provides a means, other than using memory-board layout charts, for locating a defective RAM. (The program is resident on 2200 CPU BASIC/BASIC-2 Language Diagnostic diskettes, WL #702-0080--SSSD, and WL #702-0075--DSDD). MECI requests the exact configuration of Control and Data Memory, then waits for the operator to key in an error message that occurred during a memory diagnostic or during the loading of BASIC-2. That accomplished, the program "points out" the failing RAM by displaying a graphic of the memory board with '?' at the location of the failing RAM.

The following stipulations apply to the MECI program.

- a. Hardware Requirement: 2200 VP/LVP/MVP/SVP with 16K memory and an 80 x 24 CRT.
- b. The operator must specify the disk file from which data will be compared against PECM data (if the error occurred while trying to load from disk). If no file is desired, key in 'spaces' and then RETURN; the file name defaults to "BASIC-2 (@@)".
- c. Press any non-SF key to clear the display and enter a 'next' error; or, press any SF key to enter a different memory configuration.
- d. When in the EDIT SYSTEM ERROR mode, simply key in the error message that was displayed when the memory fault was detected (keying RETURN after each field). After the entire error message has been entered, key RETURN; MECI will point out, in the display of terminal #1, which RAM failed.

MECI Loading/Operating Procedure

1. Insert the diagnostic diskette into the system drive.
2. Key SELECT DISK (diskette drive address), RETURN.

3. Key LOAD RUN, RETURN.
4. If using an SSSD diagnostic diskette, the following prompt will be displayed:

```
SELECT OPTION TO TEST?
```

- | | |
|--|----------------|
| 1. 2200C | 2. 2200T |
| 3. 2200VP/LVP/MVP/SVP | 4. MEMORY DIAG |
| 5. VP/LVP/MVP/SVP BAD RAM DISPLAY (MECI) | |

Key 5, RETURN to select MECI. The Data Memory configuration screen prompt (see following) will then be displayed.

If using a DSDD diagnostic diskette, the following prompt will be displayed:

```
DSDD FIELD SERVICE DIAGNOSTIC CATALOG
TO LOAD AND RUN, PRESS S.F. KEY CORRESPONDING TO CATEGORY.
```

- ```
S.F. ' 1 FOR CPU DIAG
S.F. ' 2 FOR MASS STORAGE DEVICES DIAG
S.F. ' 3 FOR PERIPHERAL DIAG
```

Depress SF '1 to select the CPU diagnostic. The following prompt will be displayed.

```
DSDD CPU DIAGNOSTICS
SELECT OPTION TO TEST?
```

- ```
1. BASIC-2 DIAG
2. MEMORY DIAG
3. BAD RAM DISPLAY (MECI)
```

Key 3, RETURN to select MECI. The following screen prompt will be displayed.

*** MECI -- MEMORY ERROR CHIP IDENTIFIER ***

	SIZE	BOARD #1	BOARD #2
' 0	16K	6787 (16K)	
' 1	32K	6787-1 (32K)	
' 2	32K	7587 (32K)	
' 3	48K	6787-1 (32K)	6787 (16K)
' 4	64K	6787-1 (32K)	6787-1 (32K)
' 5	64K	6787-1 (32K)	7587-1 (32K)
' 6	64K	7587-2 (64K)	
' 7	96K	6787-1 (32K)	7587-3 (64K)
' 8	96K	7587-4 (96K)	
' 9	128K	6787-1 (32K)	7587-5 (96K)
'10	128K	7587-6 (128K)	
'11	160K	7587-6 (128K)	7587 (32K)
'12	160K	6787-1 (32K)	7587-6 (128K)
'13	192K	7587-6 (128K)	7587-2 (64K)
'14	256K	7587-6 (128K)	7587-6 (128K)

Enter the data memory configuration, SF'?

5. Depress the appropriate SF' key to select the Data Memory configuration of the failing CPU. The following prompt will be displayed.

*** MECI -- MEMORY ERROR CHIP IDENTIFIER ***

	SIZE	BOARD #1	BOARD #2
' 0	16K	6788 (8K)	6788 (8K)
' 1	16K	7588 (16K)	
' 2	20K	6788-1 (12K)	6788 (8K)
' 3	20K	7588-1 (20K)	
' 4	24K	6788-1 (12K)	6788-1 (12K)

Enter the control memory configuration, SF'?

6. Depress the appropriate SF' key to select the Control Memory configuration of the failing system. The following prompt will be displayed.

Edit SYSTEM ERROR. *** SYSTEM ERROR (PECM) ***

7. Key in the error message that was displayed when the memory fault was detected (keying RETURN after each field). After the entire error message has been entered, key RETURN; MECI will point out, in the display of terminal #1, which RAM failed (see following screen displays).

Error in 7587,Board 1 *** SYSTEM ERROR (BEDM 40.A3C4 8204) ***

```

-----
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
! ! (?)! ! ! ! ! ! (?)! ! ! ! ! (?)! ! ! ! ! ! !
-----
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
-----
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
-----
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
-! !-----! !-----! !-----! !-----!
!-----! !-----! !-----!

```

Error in 7588,Board 1 *** SYSTEM ERROR (BECM 02D7 0C0000) ***

```

-----
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
-----
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
! ! ! ! ! ! ! ! ! ! ! (?)! (?)! ! ! ! ! ! !
-----
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
-----
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! ! !
! !-----! !-----! !-----! !-----!
!-----! !-----! !-----!

```


3. BASIC-2 LANGUAGE DIAGNOSTICS

NOTE:

These diagnostics can and should be run concurrently on all LVP/MVP system terminals.

This particular diagnostic will stop on any error relating to the BASIC-2 interpreter. The source of any BASIC-2 interpreter malfunction may be traced to a fault (or faults) at any level of CPU hardware operation.

3.1 LOADING/OPERATING PROCEDURES

1. Insert the diagnostic diskette into the system drive.
2. Key SELECT DISK (diskette drive address), RETURN.
3. Key LOAD RUN, RETURN.
4. If using an SSSD diagnostic diskette, the following prompt will be displayed:

SELECT OPTION TO TEST?

- | | |
|--|----------------|
| 1. 2200C | 2. 2200T |
| 3. 2200VP/LVP/MVP/SVP | 4. MEMORY DIAG |
| 5. VP/LVP/MVP/SVP BAD RAM DISPLAY (MECI) | |

Key 3, RETURN to select the appropriate type of CPU (VP/LVP/MVP/SVP). The program will then ask whether a hardcopy output of the test results is needed (see prompt following). Key the appropriate letter and the diagnostic will start to run.

If using a DSDD diagnostic diskette, the following prompt will be displayed:

DSDD FIELD SERVICE DIAGNOSTIC CATALOG
TO LOAD AND RUN, PRESS S.F. KEY CORRESPONDING TO CATEGORY.

- S.F. ' 1 FOR CPU DIAG
S.F. ' 2 FOR MASS STORAGE DEVICES DIAG
S.F. ' 3 FOR PERIPHERAL DIAG

Depress SF '1' to select the CPU diagnostic. The following prompt will be displayed.

```
DSDD CPU DIAGNOSTICS
SELECT OPTION TO TEST?
```

1. BASIC-2 DIAG
2. MEMORY DIAG
3. BAD RAM DISPLAY (MECI)

Key 1, RETURN to select the BASIC-2 diagnostic. The following prompt will be displayed:

```
DO YOU WISH A HARDCOPY OUTPUT OF THE TEST RESULTS ('Y' OR 'N')?
```

5. Key the appropriate letter and the diagnostic will start to run.

3.2 NORMAL (CORRECT OPERATION) DISPLAYS

The following displays will appear during a test run of the BASIC-2 Language diagnostic.

```
*** TESTING BASIC-2 ***                                PASS# x

REM..... OK          DIM..... OK
GOTO..... OK         COM,COMCLEAR... OK
GOSUB,RETURN... OK  I/O STMT SYNTAX OK
DEFFN..... OK       EXPRESSIONS.... OK
FOR,NEXT..... OK    DEFFN',GOSUB... OK
IF/THEN,ELSE... OK  ON GOTO,GOSUB.. OK
DATA,READ,RSTOR OK  ROTATE..... OK
LET,&..... OK       INIT..... OK
STR,LEN..... OK     AND,OR,XOR,BOOL OK
BIN,VAL..... OK     ADD,BIN..... OK
ALL,HEX..... OK     PRINTUSING TO.. OK
NUM,POS..... OK     CONVERT..... OK
VER..... OK         HEXPACK/UNPACK. OK
ALPHA-EXPR..... OK  PACK,UNPACK.... OK
SELECT..... OK      ERROR,ERR..... --- TESTING
```

*** TESTING BASIC-2 SORT ***

PASS# x

MATCOPY..... OK
 MATSEARCH..... OK
 MATMOVE..... OK
 MATCONVERT..... OK
 MATSORT..... OK
 MATMERGE..... --- TESTING

*** BASIC-2 \$PACK/\$UNPACK DIAGNOSTIC ***

PASS # x

\$PACK (INTERNAL FORM)..... OK
 \$UNPACK (INTERNAL FORM)..... OK
 \$PACK (DELIMITER FORM)..... OK
 \$UNPACK (DELIMITER FORM)..... OK
 \$PACK (FIELD FORM)..... OK
 \$PACK (FIELD FORM, CONT.)..... OK
 \$UNPACK (FIELD FORM)..... OK
 \$UNPACK (FIELD FORM, CONT.)..... OK
 \$PACK/\$UNPACK (SKIP FIELD, MISC.)..... OK
 \$FORMAT..... --- TESTING

*** TESTING BASIC-2 / \$GIO ***

PASS# x

OXYZ..... OK
 11XZ..... OK
 14YZ..... OK
 15YZ..... OK
 16XX..... OK
 17XX..... OK
 19YZ..... OK
 1CYZ..... OK
 1DYZ..... OK
 1EYZ..... OK
 1FYZ..... OK
 18YZ..... OK
 1BY1..... OK
 1BY2..... --- TESTING

*** TESTING BASIC-2 / \$GIO ***

PASS# x

SYNTAX OK
 LITERAL OK
 VARIABLE OK
 STRING --- TESTING

XC
A
FY
G/L

PRODUCT SERVICE NOTICE

DATE: 11/20/81

CLASSIFICATION 2200 SYSTEMS

CATEGORY MAIN FRAMES

PRODUCT/APPL. 2200MVP

SEQUENCE # 7

IV - A - 3 - 7

RECEIVED BY

DEC 03 1981

CHESTER KASPRZAK

TITLE:

INSTALLATION OF OPTION 'C' INTO 2200MVP SYSTEM

ADVANCE COPY

SCOPE

This PSN describes the field implementation of Memory Option C into the 2200MVP CPU. A finalized version of this document will be published as an addendum to the Model 2200MVP Product Maintenance Manual, number 03-0071-1.

The present class code for the 2200MVP maintenance manual is (IV-A-3-M). A minor change to the present class code will result when supplied with Memory Option C addendum. The 2200MVP system designation changes to 2200MVPC.

GENERAL DESCRIPTION

The control and data (user) memories in the present 2200MVP Systems have a maximum control memory size of 32K and Data Memory of 256K. Option C upgrades the present 2200MVP System by increasing the available memory to 64K and 512K respectively. Option C provides the increased control memory necessary to support both the 2200 COBOL and BASIC-3 languages. Included with Option C is a multiuser operating system with disk volume and file management capabilities, 2200 COBOL and BASIC-3. The Option C updated MVP CPU's have seven I/O slots for peripheral controller boards. The updated 2200MVP CPU will be known as 2200MVPC CPU.

CHESTER KASPRZAK

Field Equipment Upgrades

Option C field installation kits for 2200MVP Systems are ordered by the following part numbers:

WL P/N 205-5027	50Hz	MVP to MVPC	Kit Number (UJ 5027)
WL P/N 206-5027	60Hz	MVP to MVPC	Kit Number (UJ 5027)

The MVPC kit contains a completely new MVPC CPU chassis assembly replacing the existing chassis. A new modified motherboard is an integral part of the new assembly. Existing reusable PCBs in the old chassis are removed and installed in the new chassis. New and upgraded PCBs shipped with the kit are installed in the new chassis to complete the board complement for Option C.

The additional number of new and/or updated (PCBs) shipped in the MVPC field kit will fill the PCB complement of each MVPC CPU.

New Factory Orders

Option C will be factory installed on new MVPC systems per customer request prior to shipment to the field. These new systems with the desired peripherals will be shipped to a site for installation. The CE will install the new system including all necessary cabling and initiate turn-on and start-up. The CE will also be responsible for verifying the operation by running the new diagnostics.

Special Tools and Test Equipment

None required other than the standard items provided in the Wang CE tool kit.

FUNCTIONAL DESCRIPTION

Motherboard

A modified motherboard for 2200MVPC systems has additional slots for three more printed circuit boards. These slots will be used for two new Data (user) Memory boards and the new Extended Memory Controller (EMC) board for maximum memory. The motherboard, which is physically mounted on the hardware chassis, has a new part number. Listed below are the new units needed to complement the MVPC systems.

1. MVPC CPU chassis/motherboard assy (Seven I/O slots-60Hz)..270-0465
2. MVPC CPU chassis/motherboard assy (Seven I/O slots-50Hz)..270-0466
3. Extended Memory Controller.....210-7796
4. Instruction Counter (replaces 210-6790).....210-7797

Data Memory

In order to increase the Data (User) Memory from 256K to 512K, another address bit was added. This bit is SL5 which originates on the Logibloc Registers and I/O Board 210-6793-1. This bit is set in register L46, inverted via L39-10 and presented to the motherboard as signal *PA2 at connector pin 19₂. This change (ECO #17388) is transparent to all existing 2200 motherboards.

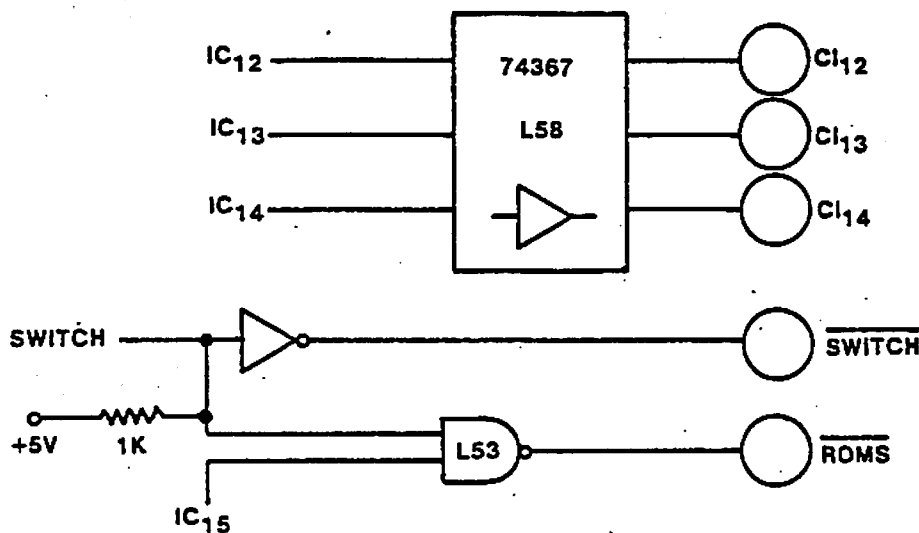
Control Memory

Additional address decoding is also required for the increased size of control memory from 32K to 64K. To accomplish this, the address selection bits *MS1-*MS8 which were on the Instruction Counter (IC) board 210-6790 are now decoded on the new Extended Memory Controller (EMC) board (210-7796).

Instruction Counter

The new Extended Instruction Counter board 210-7797 is similar to the 210-6790 Instruction Counter except that memory select signals *MS1-*MS8 are decoded off the board. To do this, IC12-IC14 Instruction Counter bits are buffered via L58 on the EIC 210-7797 board and brought out as CI12-CI14. In addition, IC15 from register L48 is NANDed with *SWITCH at L53 producing signal *ROMS. See figure below.

These four bits are then decoded by L12 and L4 on the Extended Memory Controller 210-7796 board as Memory Select address bits. The Instruction Counter board will only work on Extended Memory 2200 Systems. All other 2200 Systems require the use of the 210-6790 board.



Extended Memory Controller

The Extended Memory Controller board 210-7796 will perform the memory selection for both the Data and Control memory.

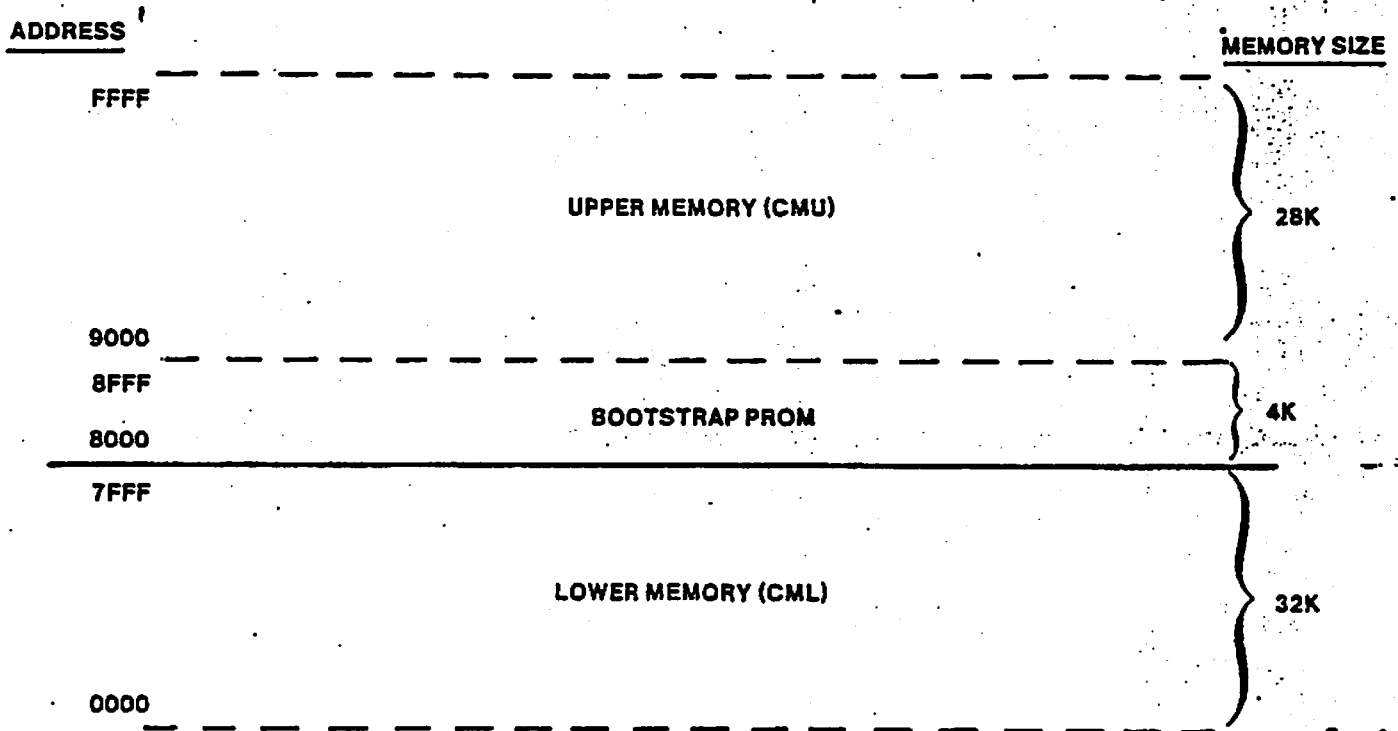
a. Data Memory

512K of Data Memory is structured as four 128K pages (4 separate memory boards) labelled Data Memory DM1, DM2, DM3 and DM4. These pages are selected on the Extended Memory Controller board as follows:

<u>*PA2</u>	<u>*PA1</u>	<u>SELECTION BIT</u>	<u>MEMORY SIZE</u>
0	0	*4PG	128K
0	1	*3PG	256K
1	0	*2PG	384K
1	1	*1PG	512K

The CI12-CI14 bits and *ROMS bit (CI15) from the Instruction Counter board 210-7797 are used to decode either the lower or upper 32K of Control Memory. The lower 32K (labelled CML) is selected by *ROMS being OFF and the upper 32K (labelled CMU) by *ROMS being ON. The first 4K of upper memory is dedicated to the system bootstrap.

The bootstrap section of memory is addressed by having CI12-CI14 OFF and *ROMS (CI15) ON. Memory is configured as shown in following figure.



MVP CHASSIS REMOVAL AND REPLACEMENT

The updated MVPC chassis will be equipped with a power supply (50/60 Hz) minus the regulator board (210-7397). The regulator board removed from the old chassis will be used. Regulator board 210-7397 has replaced the original regulator 210-6797.

Removal of MVP chassis

- a. Set the power toggle switch to the OFF position on the CPU and all peripheral units. Remove the power cable from its receptacle.
- b. Disconnect all cables used for peripherals from the I/O controller boards.
- c. Remove four screws that secure the printed circuit board cover. Set the chassis/motherboard assembly on a table top. Remove all existing boards including the power regulator board 210-7397. Set the old MVP chassis aside.

Replacement of new MVPC chassis

- a. Set the new MVPC chassis with the carrying handle facing up (operating position). Remove the front and rear covers. See figures 1 and 2.

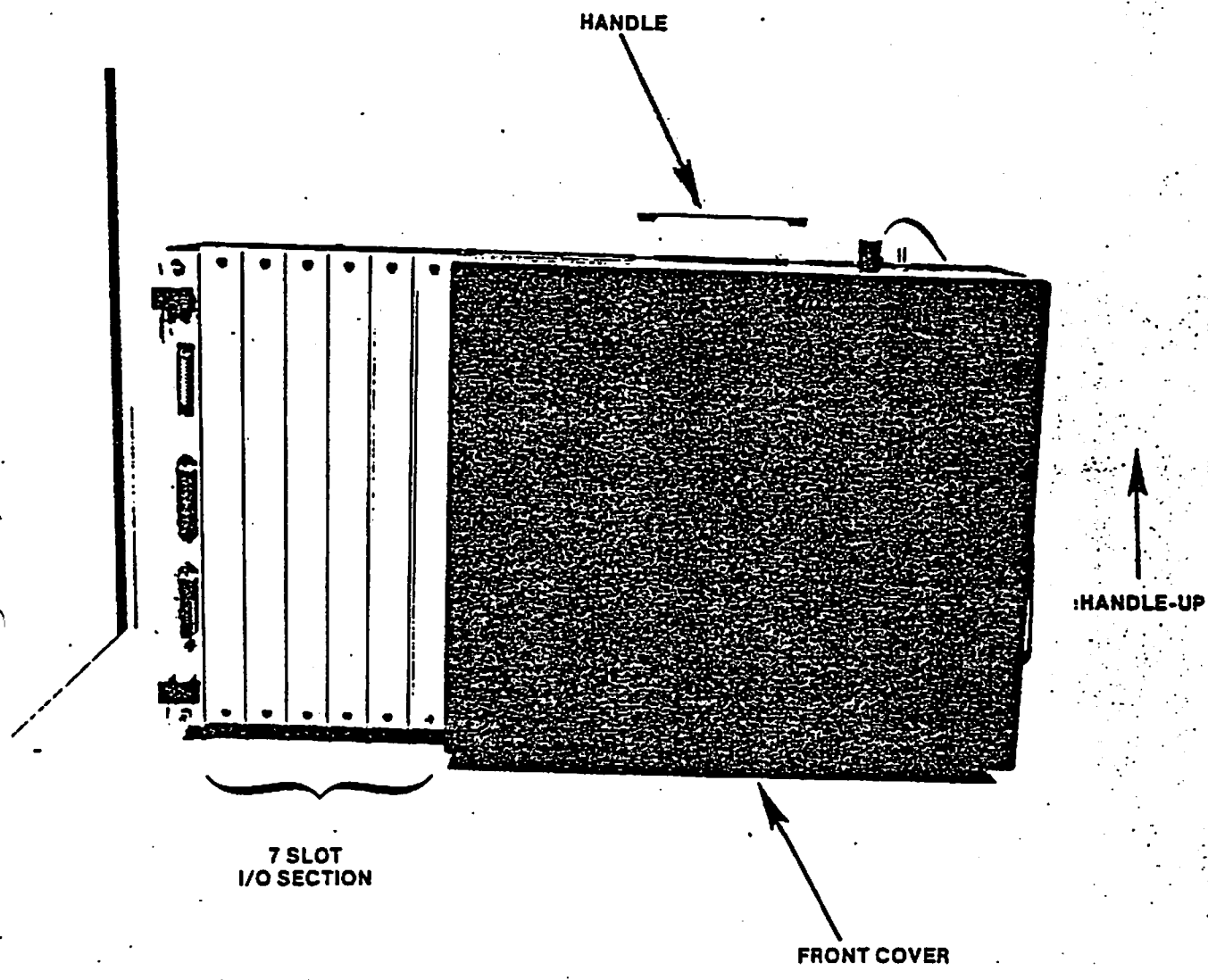


FIGURE 1 MVPC CPU (OPERATING POSITION)

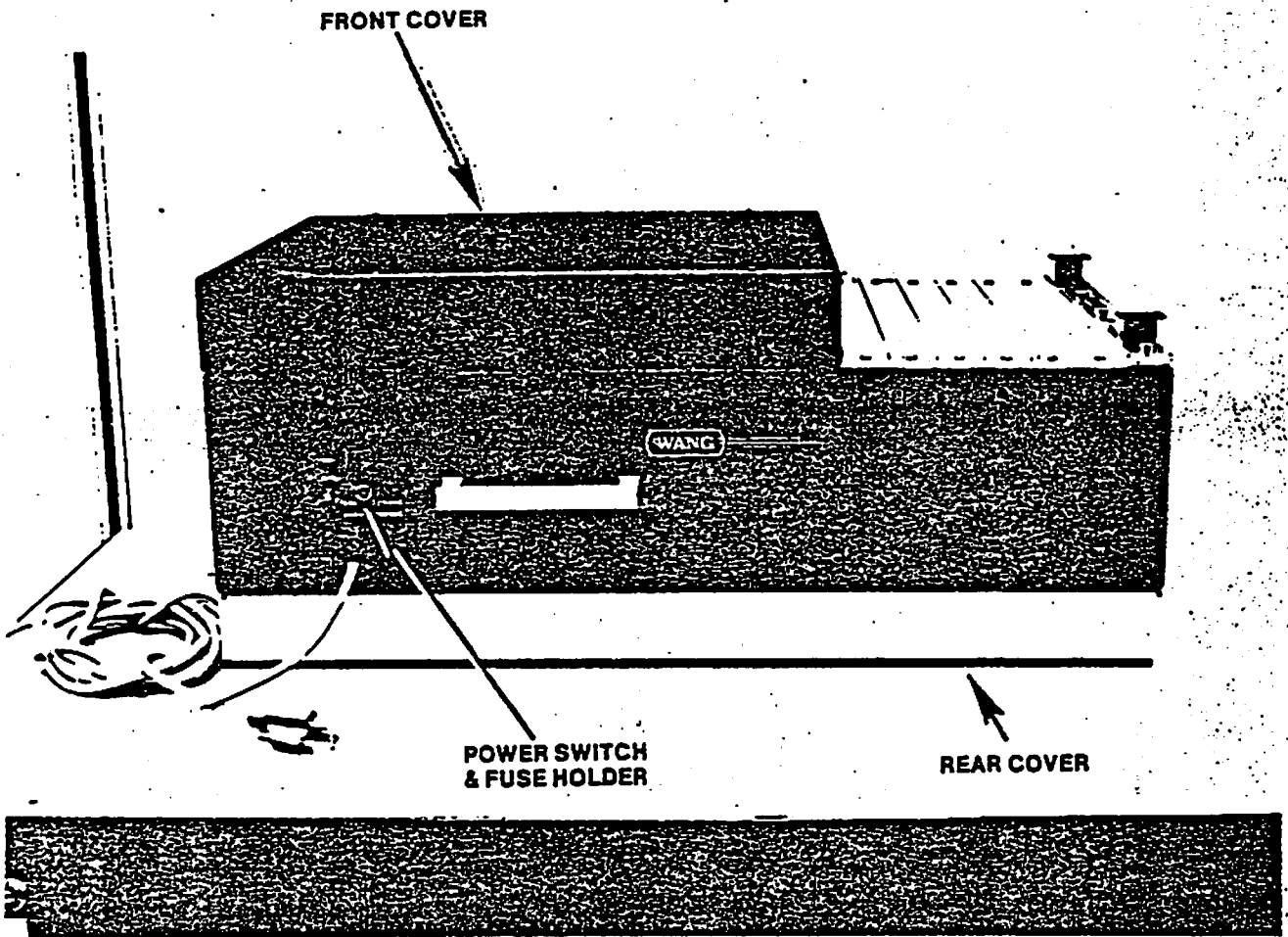


FIGURE 2 MVPC CPU (MAINTENANCE POSITION)

- b. Load the power regulator board 210-7397 from the front into the correct slot on the motherboard. See figure 3.
- c. Plug power cable into power receptacle and turn power ON. Reference the negative lead of a digital Voltmeter to + 0V test point on the regulator board connector on the back of the motherboard. Check all voltages shown on table 1 at the designated pin locations on the motherboard connector to roughly ascertain that all voltages are present prior to loading circuit boards.
- d. If No-Load voltage indications are present, turn power OFF and proceed to install circuit boards (both reuseable and new boards from the kit) except for controller boards into their respective slots on the motherboard.
Use extreme care (double check) when inserting boards to insure that each board is loaded into the proper slot on the new motherboard. Refer to the motherboard layout in figure 4.
- e. Turn power ON and recheck voltages at the same points.

NOTE

Adjust voltages in the order listed for MVPC systems
vs MVP systems within tolerances as indicated in
CPU voltage regulator adjustment table 1

If any of the voltages are missing or do not react to adjustment, prepare to remove all boards and insert boards one at a time until the problem reappears.

- f. If all voltages adjust properly, add one (1) controller board for the 2236DE workstation. Prepare for loading diagnostics and data entry required for checking the operation of the MVPC CPU system.

NOTE

2200 CPU Diagnostics are currently available to the field.
WL# 702-0138 is a single sided diskette, WL# 732-0010 is a
double sided diskette both of which will be used to diag-
nose problems for both MVP and MVPC systems.

- g. Once the system is checked and operating properly, load the remaining I/O boards (Max. quantity of seven (7) into the I/O slots in any arrangement desired. Check and readjust all voltages if necessary.
- h. Cable all peripherals to their respective controller. Replace the board clamp on the new chassis. Replace the front and rear covers which are secured with four screws each.

MVPC SYSTEM CONFIGURATION

CPU boards are inserted into the MVPC CPU as follows:

I/O	6	6	6	7	6	7	7	7	7	7	7	7
I/O	7	7	7	7	7	5	5	7	5	5	5	5
I/O	9	9	9	9	8	8	8	9	8	8	8	8
I/O	3	2	1	7	9	8	8	6	7	7	7	7

FIGURE 4 CPU MOTHERBOARD LAYOUT

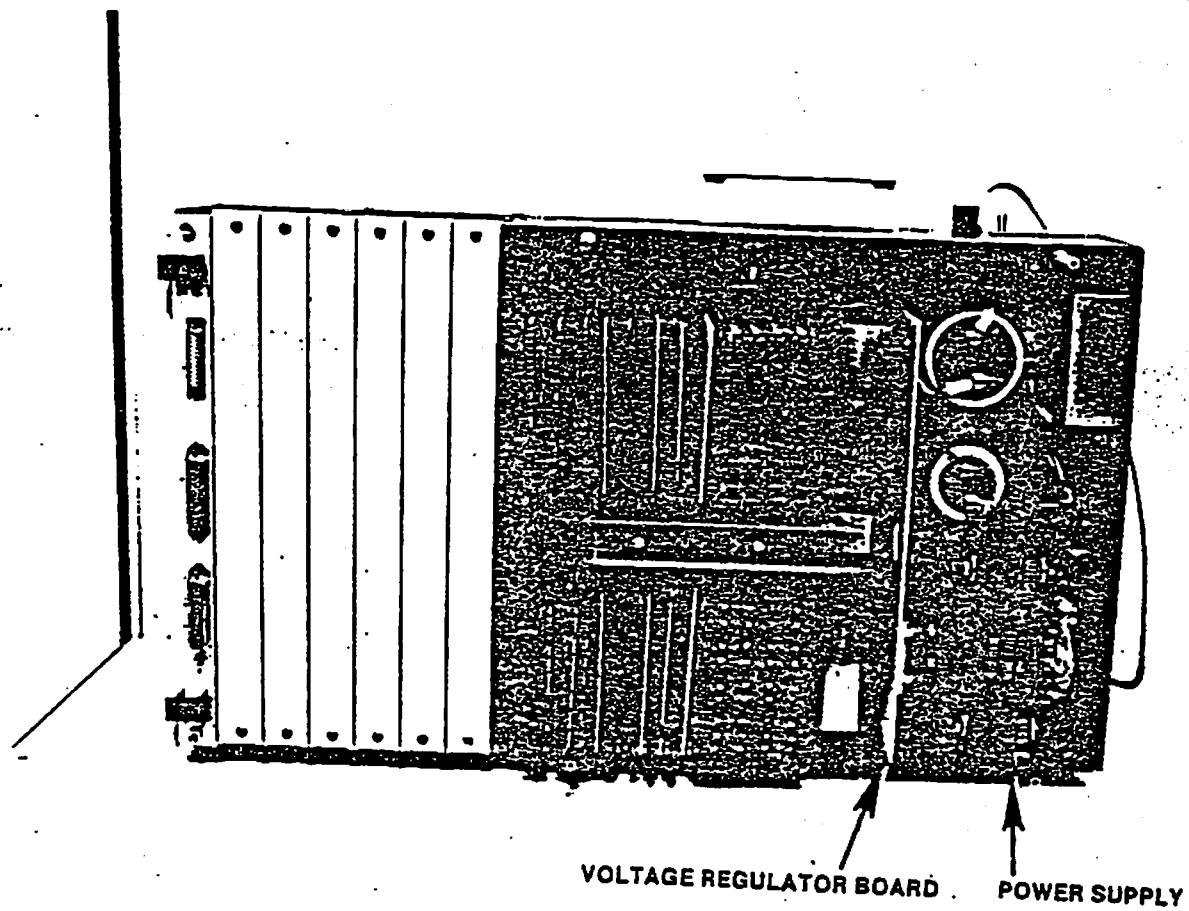


FIGURE 3 MVPC CPU (FRONT COVER REMOVED)

VOLTAGE ADJUSTMENTS--MVP AND MVPC SYSTEMS

The voltage adjustments require that both front and rear covers be removed. The regulator board (210-7397) is used on both the standard MVP and the new MVPC systems. However, there is a difference in the response when adjusting the +5V I/O and +5V Logic potentiometers for each system. Proceed to check and/or adjust these voltages in the order as suggested. Interaction of voltage adjustments will require rechecks for certification of all voltages.

**Standard MVP Voltage Adjustments

-12V -5V +12V +5V Logic +5V I/O

**MVPC Voltage Adjustments

-12V -5V +12V +5V I/O +5V Logic

**(Viewed from the component side of the regulator board, with the edge connectors at the bottom). The adjustments can be made easier with the chassis mounted with the carrying handle in the up position. See figure 3.

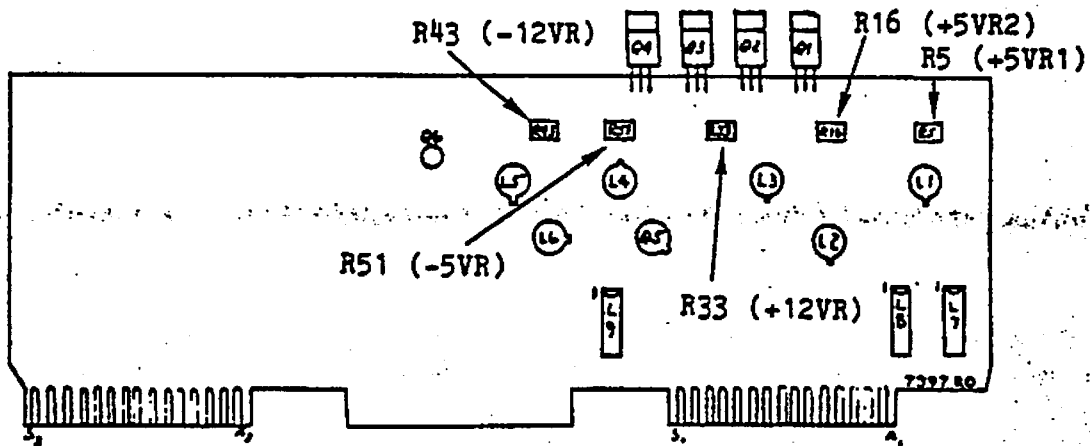


FIGURE 5 7397 REGULATOR BOARD

TABLE 1 CPU VOLTAGE REGULATOR ADJUSTMENTS

LOCATION	VOLTAGE	LIMITS	ADJUST	RIPPLE
			<u>7397</u>	
Pin J ₁	+5VR1	+4.95 vdc to +5.05 vdc	R5	15 mvp-p
Pin L ₁	+5VR2	+4.95 vdc to +5.05 vdc	R16	15 mvp-p
Pin M ₁	+12VR	+11.95 vdc to +12.05 vdc	R33	15 mvp-p
Pin N ₁	-12VR	-11.95 vdc to -12.05 vdc	R43	35 mvp-p
Pin S ₁	-5VR	-4.95 vdc to -5.05 vdc	R51	25 mvp-p

CIRCUIT BOARD COMPLEMENT (MVPC)EXTENDED MEMORY
MVPC (7 I/O Slots)

Register	210-6793-1
ALU	210-6792
Stack Board	210-6791
Ext. Instruction Counter	210-7797
Memory Interface Bd.	210-6789
32K x 24 Bit Cntl. Mem.	210-7588-1
32K x 24 Bit Cntl. Mem.	210-7588-1
Extended Mem. Cntrl.	210-7796
128K x 9 Bit Data Mem.#1	210-7587-3
128K x 9 Bit Data Mem #2	210-7587-3
128K x 9 Bit Data Mem #3	210-7587-3
128K x 9 Bit Data Mem #4	210-7587-3
Power Supply Regulator	210-7397 .

DISPOSITION OF MVP CHASSIS UNITS

Disposition of each original MVP CPU chassis requires an Equipment Transfer form WL# 700-4067B for return of exchanged equipment. The disposition of these units pertains to domestic 2200 systems only.


Return to: WANG SALVAGE OPERATIONS
 51 Middlesex Street
 North Chelmsford, Mass. 01863.

If the serial number sticker is missing on the chassis or cage, return the unit to RDB 6854. If the unit has a sticker serial number return to RDB 6852.

2200LVP card cages replaced outside of the continental limits of U.S. must be coordinated with Wang International for proper disposition.

LIST OF NEW SCHEMATICS FOR 2200MVP OPTION 'C'

1. 210-6793 SCHEMATIC LOGIBLOC REGISTERS & I/O (No. of sheets 1)
Used with 2200MVP
2. 210-7587 128K EXTENDER MEMORY (No. of sheets 4)
Used with 2200MVP
3. 210-7796 EXTENDED MEMORY CONTROLLER (No. of sheets 2)
Used with 2200MVP/LVP Systems
4. 210-7797 EXTENDED INSTRUCTION COUNTER (No. of sheets 4)
Used with 2200MVP/LVP Systems
5. 210-7798 EXTENDED MEMORY MOTHERBOARD (No. of sheets 2)
Used with 2200MVP System

 <p>IMMEDIATE SERVICE NOTICE</p>	NO. 132	DATE: 3/2/77
	CATEGORY	
	2200/2600 #4	
SUBJECT		
2200VP/2600 MICROCODE BUGS		

The following microcode bugs exist on 2200VP Software Release #1.3 diskettes. These problems will all be corrected in Release #1.4. Part number for software diskette is 701-2118.

1. Description: VECM Address

Verify of control memory (RESET, CLEAR) displays wrong address for LRC and CRC errors.

How to Generate Error:

Load system with platter containing invalid checksums. Press RESET and key '15 to branch to BASIC. Then, press RESET again to generate verify error.

2. Description: DATASAVE BA causes PEDM

On VP's with other than 32K or 64K, DATASAVE BA can cause an erroneous PEDM if the length of the value being saved is less than 253 bytes. Non-existent memory is read generating the PEDM.

How to Generate Error:

On a 16K machine.

```
:10 DIM A$(0)1
:20 DATASAVE BAF(0) A$()
:RUN
```

3. Description: ON ERROR GOTO/OVERLAY

ON ERROR GOTO may not work after an overlay. The overlay mode bit is left on after an overlay causing ON ERROR GOTO to resolve the program rather than merely perform the GOTO.

How to Generate Error:

```
:LOAD F"START"  
:LIST  
10 REM START  
20 PRINT "START PROGRAM"  
30 PRINT "LOAD OVERLAY": PRINT : LOAD F"OVERLAY"  
  
:CLEARP  
:LOAD F"OVERLAY"  
:LIST  
10 REM OVERLAY  
20 DIM A$(1)5  
30 PRINT "START OF OVERLAY"  
40 PRINT "REDIM A$": MAT REDIM A$(1)3  
50 PRINT "DIVISION BY 0": X=1/0  
60 ON ERROR E$, L$ GOTO 100  
100 PRINT "ON ERROR ROUTINE"  
110 PRINT "ERROR ";E$,"LINE ";L$  
  
:LOAD RUN  
START PROGRAM  
LOAD OVERLAY  
  
START OF OVERLAY  
REDIM A$  
DIVISION BY 0  
20 DIM A$(1)5  
:ERR P59  
:  
:          EXPECTED RESULT  
:          ERROR 062      LINE 0050
```

4. Description: Default Disk Address

Using a default disk address with low order digit nonzero causes an erroneous syntax error (missing comma) in statements such as VERIFY.

How to Generate Error:

```
:SELECT DISK 321  
:10 VERIFY F  
:          ↑ERR S13
```

5. Description: MOD error for negative values. Modulo function returns incorrect answers for certain negative numbers.

How to Generate Error:

```
:PRINT MOD(-.9 , 1)
```


6. Description: INT (1E15) Changes Constants

Any argument with an exponent of 15, returns a zero, but changes part of 8-bit constants.

How to Generate Error:

```
PRINT INT (1E15) and key Reset
```

7. Description: LIST T

New LIST parameter added.

How to Generate Error:

```
:LIST T "ABC"
```

8. Description: LIST V interfered with by other LIST's

How to Generate Error:

```
:10 I=1  
:20 LIST  
LIST V will not find any variable references.
```

Any of the following program statements suppress execution of LIST V:

LIST, LIST D, LIST #, LIST', LIST I, LIST T.

Note that LIST V and LIST DCF are ok.

9. Description: SF' key/CONTINUE

SF' key subroutine calls from Console Input do not stack the continue information (line number, statement count). Thus, nested STOP's do not work properly. Also, the statement count is not zeroed by SF' key calls; CONTINUE after stop within a DEFFN' subroutine continues at the wrong statement.

How to Generate Error:

```
:10 STOP #  
:20 DEFFN' 0:PRINT "'0":STOP #:PRINT "'0-2":RETURN  
:RUN  
  
STOP 10  
:  
'0
```

```
STOP 20
:CONTINUE
'0-2
```


```
20 DEFFN' 0"PRINT "'0":STOP #:PRINT "'0-2":RETURN
↑ERR P41
```

10. Description: UNPACK ILLEGAL DATA

Unpacking one byte of invalid data to a numeric variable via UNPACK should produce an error; instead the last 8 bytes in the value stack are popped into the numeric variable and an error is not generated.

How to Generate Error:

```
:10 FOR I = 1 2
:20 A$ = HEX('F)
:30 UNPACK (##) A$ TO X
:40 NEXT I
:RUN
40 NEXT I          (should be: UNPACK (##) A$ TO X )
↑ ERR 40          ↑ERR 75
```

 <p>IMMEDIATE SERVICE NOTICE</p>	NO. 135	DATE: 3/30/77
	CATEGORY 2200/2600 #5	
	SUBJECT 6792 ALU BOARD INCORRECT COMPONENT LOADING	

An unknown quantity of 6792 2600 ALU boards were manufactured with incorrect components loaded in IC locations L19 and L20. The incorrect devices loaded are 376-0219 74LS181 ALUs and must be changed to 376-0256 74S181 ALUs.

Any 2600 CPU shipped from Tewksbury before March 21, could have an incorrectly loaded 6792 board in it. Also note that 6792 boards sent out on consignment could have the incorrect devices in them, so it is suggested that all 2600 card kits be checked.



LABORATORIES, INC.

1 INDUSTRIAL AVENUE, LOWELL, MASSACHUSETTS 01851. TEL. (617) 851-4111. TWX 710 343-6769. TELEX 94-7421

WANG

FIELD CHANGE ORDER

FCO NO.
1035

Equipment Affected 2236 MXD I/O Controller (2200 LVP, 2200 MVP)
 Class Problem Only FCO Kit # 728-0046 Page 1 of 4
 Org. Code VI.B.1 (4201) FCO Doc. # 729-1297 Approval Date: **MAY 23 1983**
 Est. Install. Time 30 Minutes Ref. ECO # 26937

1. REASON FOR CHANGE

To prevent intermittent system hangups.

2. DESCRIPTION OF CHANGE

Two capacitors are added to 210-7591 PCB of the 2236 MXD I/O controller.

3. DOCUMENTATION AFFECTED

N/A

4. PREREQUISITE (S)

N/A

5. INSTALLATION PROCEDURE

- A. Ensure power is off.
- B. Remove 2236 MXD I/O controller from 2200 system.
- C. Refer to Figure 1. Solder a 390 pf cap (300-1390) from L6 pin 13 to ground at L6 pin 7 on 210-7591-A PCB assembly.
- D. Add a 30 uf cap (300-3009) from Q2 pin 2 to ground on 210-7591-A PCB assembly.
 - 1. Solder the negative lead of the 30 uf cap (300-3009) to the etch leading to Q2 pin 2 as shown in Figure 1.
 - 2. Solder the positive lead of the 30 uf cap (300-3009) to the negative lead of C4 and to the etch leading to same as shown in Figure 1.
- E. Place E-Rev 1 sticker on 210-7591-A PCB assembly.

Tech Ops <i>Killed Parris</i> 5/20/83	Logistics 5/20/83 <i>Kevin Sanders</i>	Originator <i>Mary Keady</i> 5/20/83	FCO Coordinator <i>John P. Parris</i> 5/20/83
---	--	---	--

- F. Replace 2236 MXD I/O controller in 2200 system.
- G. Perform Check-out procedure described below in Section 6.
- H. Document installation of FCO by completing a Call Report or Activity Report.

ADD A 30UF CAP
(300-3009) FROM
Q2 PIN 2 TO GROUND

ETCH TO
Q2 PIN 2

L6
PIN 13

ADD A 380 PF CAP
(300-1390) FROM
L6 PIN 13 TO GROUND

L6
PIN 7

ETCH TO
C4,OV

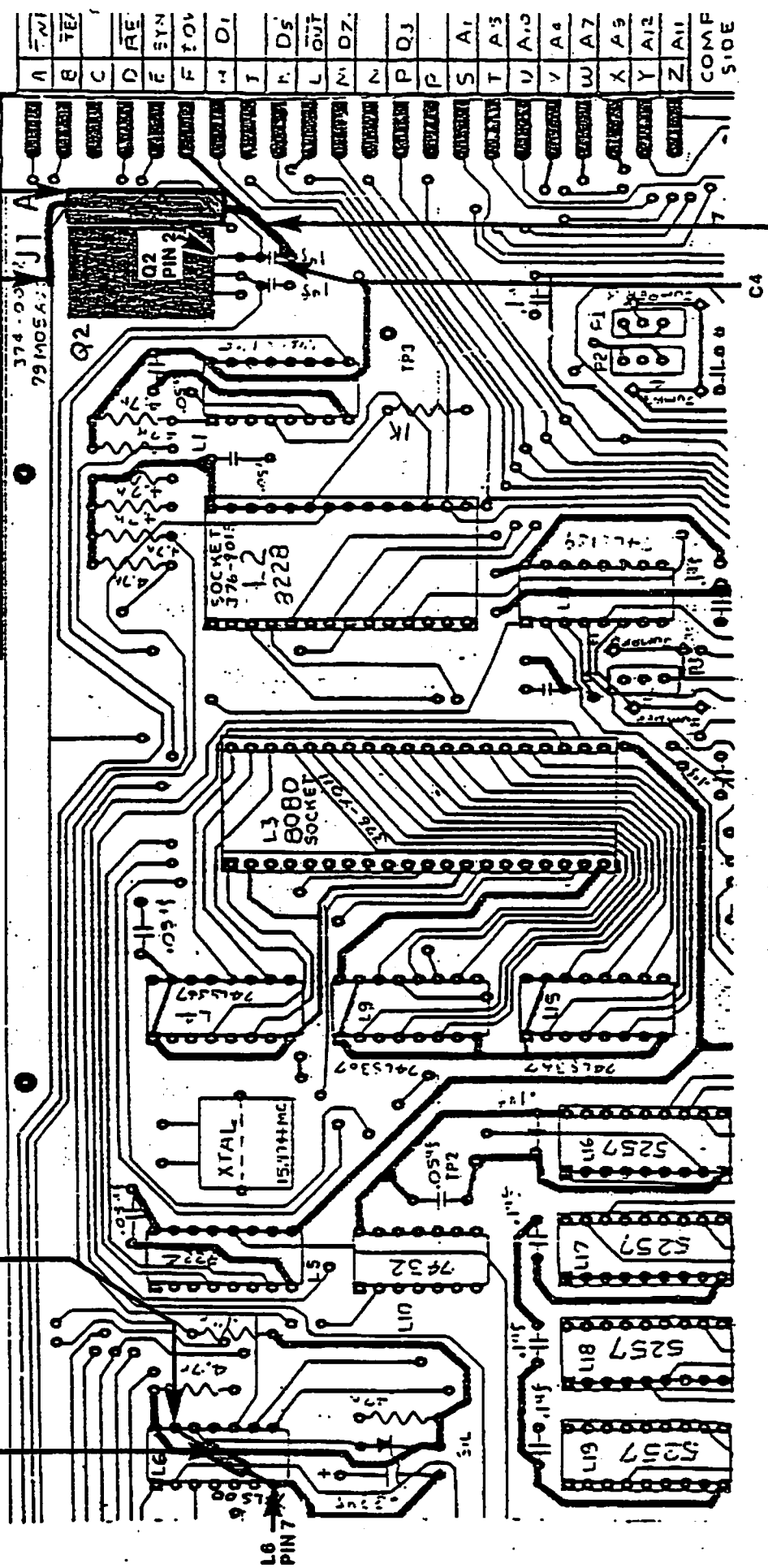


FIGURE 1 210-7591-A PCB ASSY, CAP LOCATIONS

6. CHECK-OUT PROCEDURE

Run the appropriate 2200 system check-out listed below:

<u>System</u>	<u>Diagnostic</u>
LVP	System Exercisor 732-0002B Rev 61B4
MVP	Peripheral Diagnostic 702-0079 Rev 1.0

7. FCO KIT PARTS LISTING

KIT #728-0046

<u>Item</u>	<u>Qty</u>	<u>Item Description</u>
729-1297	1	FCO #1035 Document
300-1390	1	390 pf Cap
300-3009	1	30 uf Cap
615-1283-1	1	E-Rev 1 Sticker

8. FCO KIT AVAILABILITY DATE

FCO Kit #728-0046 will be available June 6, 1983. It can be obtained by placing a routine order through Logistics Order Processing System.

9. REMOVED PARTS DISPOSITION

N/A

10. MISCELLANEOUS

N/A

WANG

ECO

ECO NO. 47774

SHEET 1 OF 17

ORIGINATOR Ariel Betancourt
 WRITTEN BY Arlene Elliott
 PART NO. 209-7587-1/-3
 DWG NO. 7587-1/-3
 MODEL NO. MVP 2200
 CLASS I II III

EXT 2273
 EXT 74313

DATE 01/15/88
 DATE 01/15/88

DOCUMENTS	REVISIONS	
	FROM	TO
HISTORY SH. 510		
HISTORY SH. 210	6	7
ARTWORK		
E-REV.		
ASSY. DWG.		
DRILL DWG.		
SCHEM. DWG.		
MECH. DWG.		
CBL DWG.		
SPI.		
SPECIFICATION		

DESCRIPTION	PEP #	PEP#	HO
128K EXTENDER MEMORY			

DESCRIPTION OF CHANGE

Change assembly drawing, parts list and sample board per attached prints and as follows:

Change BOM 209-7587-1 as follows:

WLI#	DESCRIPTION	UM	EA	COMP TYPE	QTY	TYPE
300-1930	.JUF CAP 50V	EA	108	1	108	1
376-9002	16 PIN SOCKET	EA	54	1	54	1

Change BOM 209-7587-3 as follows:

WLI#	DESCRIPTION	UM	EA	COMP TYPE	QTY	TYPE
376-9002	16 PIN SOCKET	EA	72	1	72	1

MAR 1 1 1988

REASON/SYMPOTM FOR CHANGE

Cost savings of \$7.69 per unit for 209-7587-1 and \$2.17 per unit for 209-7587-3.

COMPANY CONFIDENTIAL

CONFORMING AREA	CF	REMG	DIST	FINAL ASSY AREA	SUB ASSY AREA	NEXT ORDER	INFO ONLY

CONFORMANCE DATE 4-4-88

APPROVALS

ECO CHAIRPERSON	DATE
Paul H. Daniel	3/9/88
DES. ENGRG.	Phil Coyne 1/23/88
CUST. ENGRG.	W. Brown 3/9
MFG.	
MTO	Dave Cappelletto 3/9
PP&M	
F.C.C.	Michael Buntch 2/16/88
PROD. SAFETY	A. Kelley 2/16/88
SECURE SYS.	
ORIGINATOR	Wang
OTHER	

MODEL	309	210	L1-9 L11-19	L20-28 L30-38	L39-47 L49-57	L58-66 L68-76	L10	L29	L48	L67	R27-39 R43-49 R59-60	R34-42 R43-49 R59-60	R43-49 R59-60
2200MVP 32K	7587	7587-A											
2800MVP 64K	7587-1	7587-1A											
2200MVP 96K	7587-2	7587-2A											
2200MVP 128K	7587-3	7587-3A											

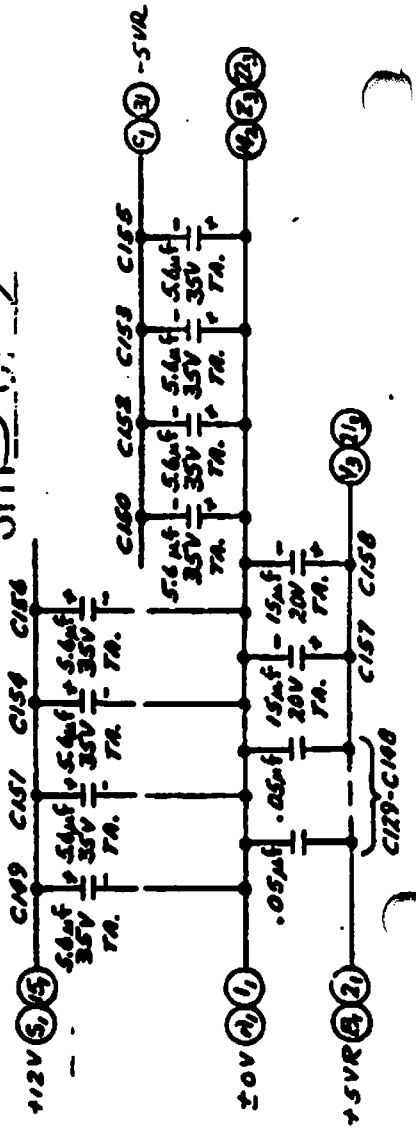
I.C. LOCATION	TYPE	VAL. NO.
L1-9, 11-18, 30-47, 49-66, 68-76	AK4116-N3	SEE CHART
L10, 29, 48, 67	74LS240	SEE CHART
L77, 78, 86	74367	376-0176
L78, 80, 87	8797	376-0189
L81	9321	376-0096
L82	74LS244	376-0288
L83, 90	7408	376-0081
L86, 96	74298	376-0138
L85, 97	74174	376-0098
L88, 98	7404	376-0010
L89	7403	376-0028
L91	74532	376-0205
L92	74537	376-0296
L93	1519-1608	376-8002
L94, 95	74157	376-0082
L1-9, 11-20, 30-47, 49-66, 68-76	16 PIN SKT LOAD PER CHART	376-9002

COMPONENT	TYPE	VAL. NO.
R1-5	2.2K 10% 1/4W	330-3022
R6	390-Ω 10% 1/4W	330-2039
R7-34	180-Ω 10% 1/4W	330-2018
R25	450-Ω 10% 1/4W	330-2045
R26	330-Ω 10% 1/4W	330-3033
R27-74	58-Ω 10% 1/4W	SEE CHART
R75-92	5.6K 10% 1/4W	330-3056
C1-126	.1μf 50V	300-1930
C127, 128	.330pf 50V (C)	300-1830
C129-148	.05μf 12V	300-1900
C149-166	.50μf 35V TA.	300-4017
C157, 158	.15μf 20V TA.	300-6022

MINERONIC	COORDINATE
ZR	168
D10-D117	166
DM00-DM: 1	161
FBI2B	169
F1FB	169
Z8K	1611
MARCLK	1610
PA0-PA1	1F11
PH0-PH7	1D11
PL1-PL7	1C11
RA0-RA6	1C11
RE	1E11
R1W1-R1W2	1G7

ECO NO 47774
SHT 5 OF 7

DELET



LOCATION	TYPE	SPARES
L88	7404	1
L90	7408	2

Bill A, Mike B FYI for C.

WANG FIELD CHANGE ORDER

FCO NO.
1045

Equipment Affected VP, LVP, MVPA, MVPC

Class Problem Only FCO Kit # 728-0063 Page 1 of 7

Org. Code 4103 (IV.A.3) FCO Doc. # 729-1325 Approval Date: DEC 28 1983

Est. Install. Time 20 Minutes Ref. ECO # 27336

1. REASON FOR CHANGE

A thin fan is required in the I/O section of the chassis to accomodate the increased length of the MXE board.

2. DESCRIPTION OF CHANGE

The fan in the I/O section of the chassis is replaced by a thinner fan (400-1029).

3. DOCUMENTATION AFFECTED

N/A

4. PREREQUISITE (S)

This change is required only in units with the longer MXE board.

5. INSTALLATION PROCEDURE

Determine the correct instruction set needed to complete the fan installation by checking the list below:

- Step A Use for VP models
- Step B Use for MVP models
- Step C Use for LVP models
- Steps D-E All models

<p>Tech Ops <i>12/27/83</i></p> <p><i>Michael Wiley</i></p>	<p>Logistics <i>12-28-83</i></p> <p><i>Karen Falvemo</i></p>	<p>Originator <i>12/27/83</i></p> <p><i>Mary Kealey</i></p>	<p>FCO Coordinator</p> <p><i>John Rowley 12/28/83</i></p>
---	--	---	---

A. Refer to Figure 1. Replace the fan in the I/O section of the VP chassis as follows:

1. Power down unit. Remove AC power plug from wall outlet.
2. Remove the I/O controllers from the motherboard and CPU cards as needed.
3. Disconnect fan cord from old fan (400-1009).
4. Remove the old fan from the chassis. Save the four lock nuts to secure the new fan to the chassis in Item 5 below.
5. Install the new fan (400-1029) on the side panel of the chassis. Hold the fan against the inside of the side panel. When properly placed, the air flow indicator on the fan is at the top of the unit. Secure the fan using four new screws (650-3327) and the four lock nuts saved from Item 4 above.

NOTE: The air flow from the fan blows out of the chassis.

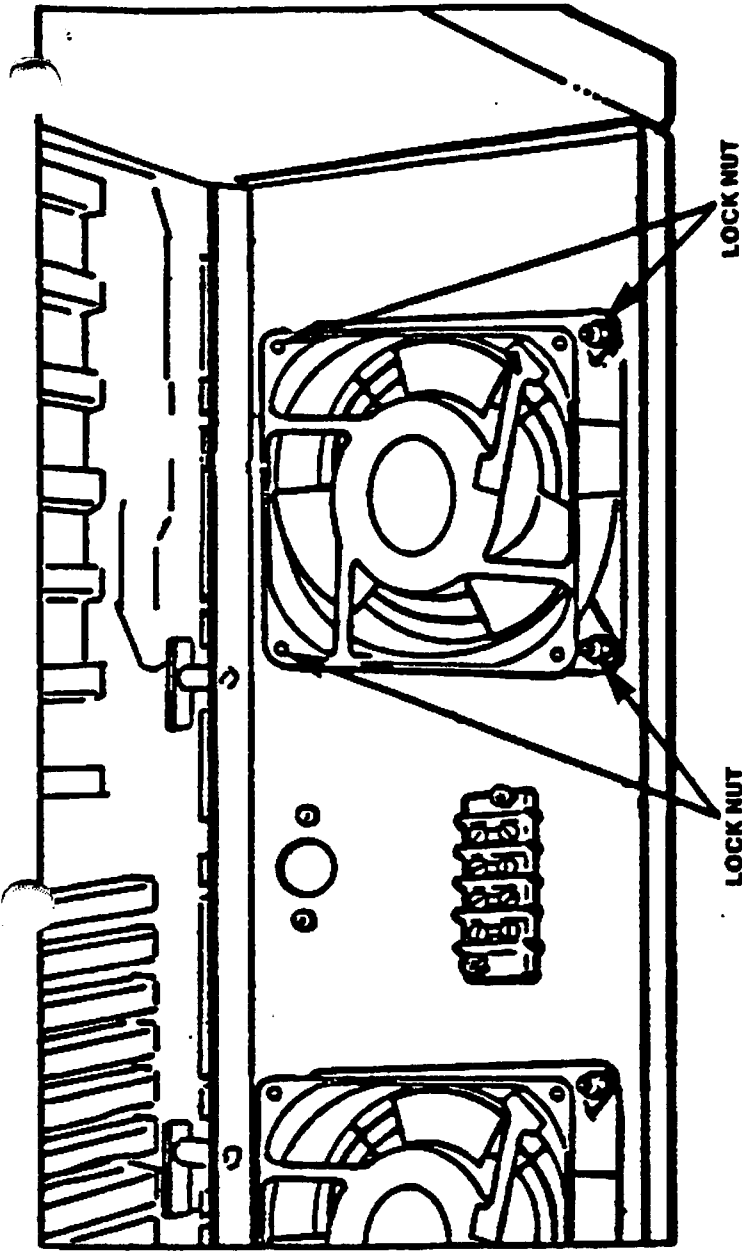
6. Connect the fan cord to the fan.
7. Replace the I/O controllers in the unit and CPU cards if removed. Proceed to Step D below.

B. Refer to Figure 2. Replace the fan in the I/O section of the MVP chassis as follows:

1. Power down unit. Remove AC power plug from wall outlet.
2. Remove the I/O controllers from the motherboard and CPU cards as needed.
3. Disconnect fan cord from old fan.
4. Remove the old fan from the chassis. Save the four lock nuts to secure the new fan in Item 5 below.
5. Install the new fan (400-1029) on the side panel of the chassis. Hold the fan against the inside of the side panel. When properly placed, the air flow indicator on the fan is at the top of the unit. Secure the fan using four new screws (650-3169) and the four lock nuts saved from Item 4 above.

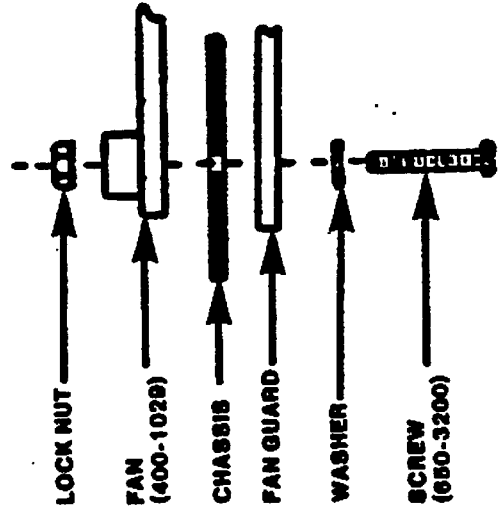
NOTE: The airflow from the fan blows out of the chassis.

6. Connect the fan cord to the new fan.
7. Replace the I/O controllers and CPU cards if removed. Proceed to Step D below.



LOCK NUT

LOCK NUT



LOCK NUT

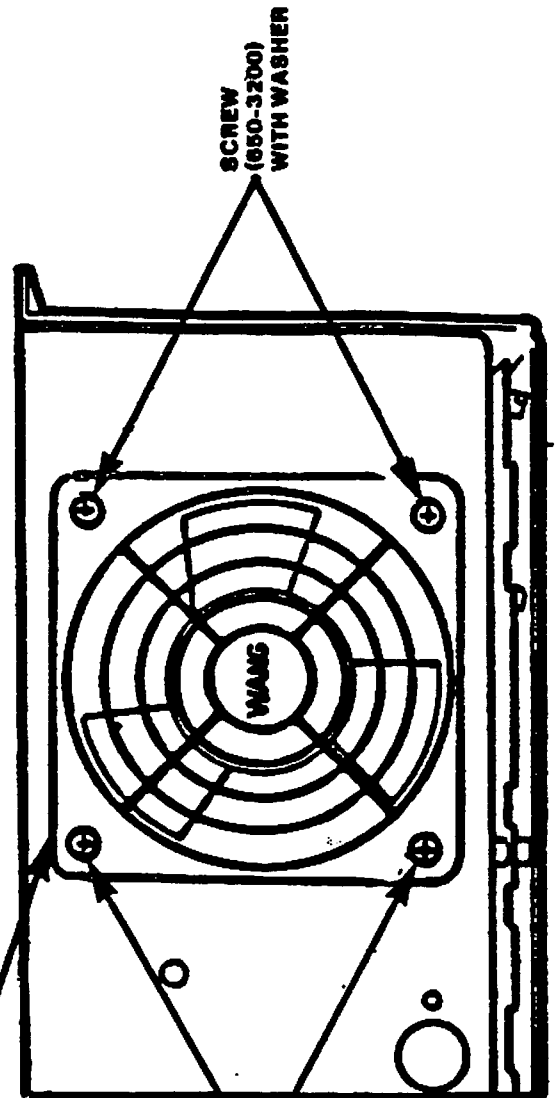
FAN
(400-1028)

CHASSIS

FAN GUARD

WASHER

SCREW
(650-3200)



SCREW
(650-3200)
WITH WASHER

SCREW
(650-3200)
WITH WASHER

FAN GUARD

FIGURE 3 LVP FAN INSTALLATION

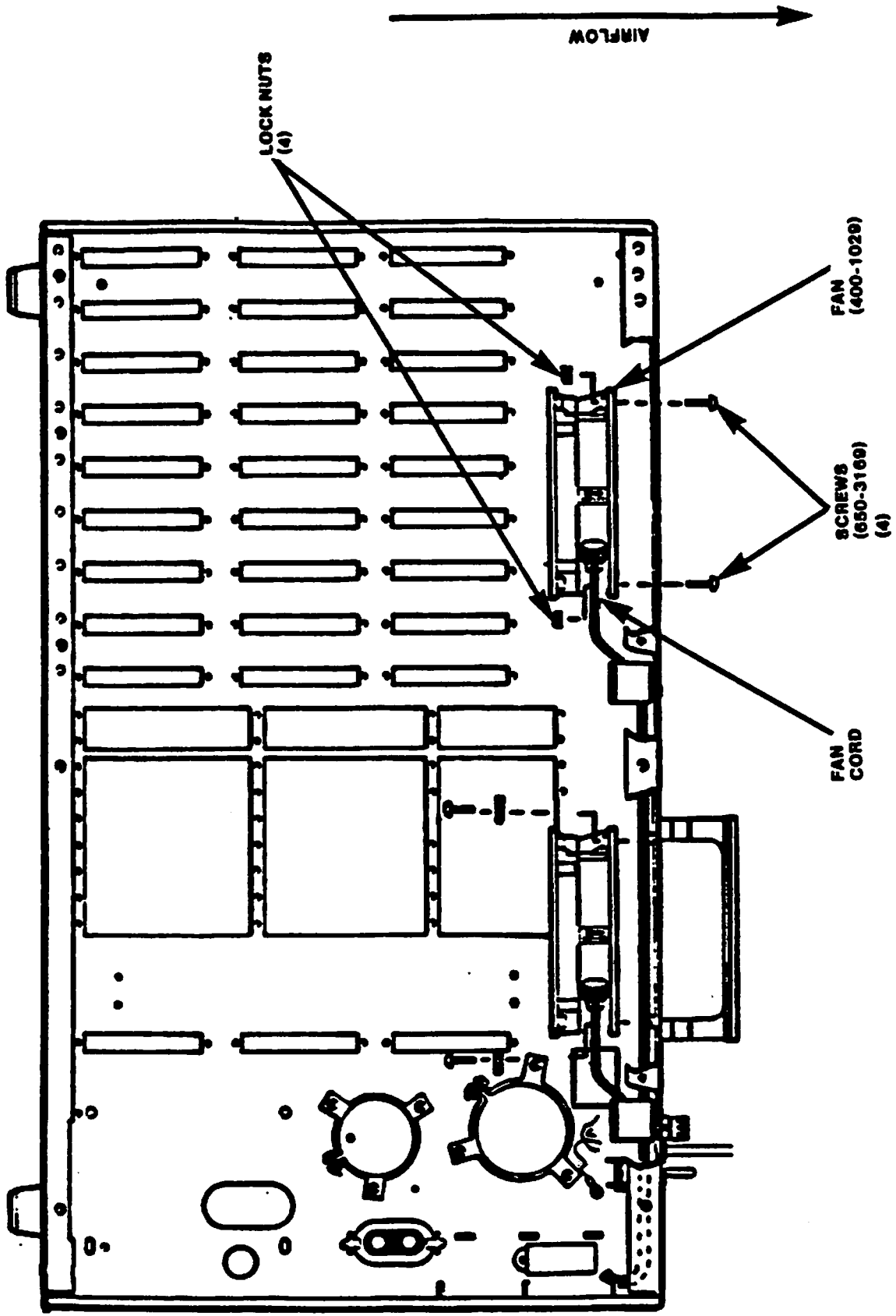


FIGURE 2 MVP FAN INSTALLATION

6. CHECK-OUT PROCEDURE

- A. Power up unit. Observe normal operation of the fan. Air flow blows from the inside to the outside of the chassis.
- B. Run the appropriate Diagnostic or System Exerciser listed below:

<u>System</u>	<u>Part #</u>	<u>Titles</u>	<u>Rev #</u>
VP	702-0138A	2200 CPU Diagnostics	11B4
MVP	702-0138A	2200 CPU Diagnostics	11B4
LVP	732-0002B	LVP/SVP System Exerciser	61B4

7. FCO KIT PARTS LISTING

KIT #728-0063

<u>Item</u>	<u>Qty</u>	<u>Item Description</u>
729-1325	1	FCO Document 1045
400-1029	1	Fan, Tube Axial
650-3327	4	Screw
650-3169	4	Screw
650-3200	4	Screw

8. FCO KIT AVAILABILITY DATE

FCO Kit# 728-0063 will be available January 9, 1984. To obtain the kit, place a routine order through the Logistics Order Processing system.

9. REMOVED PARTS DISPOSITION

Discard the removed fan and unused screws.

10. MISCELLANEOUS

This FCO does not apply to 2200 LVP Short Card Cage (with 3 I/O slots), 279-0572-TW, because the longer MXE board is not an option in this unit.

Service Newsletter

NO. 145

2200/2600 #31

12/18/78

2200MVP SYSTEM-LEVEL DOCUMENTATION

The following list is a corporate-level documentation index for 2200MVP systems. To date, and to the best of our knowledge, no other significant documentation relevant to this system has been published.

THE MVP SYSTEM (Overview Documentation):

2200 MVP Brochure; WL# 700-4587

2200 MVP Technical Information; WL# 700-4656

2200 MVP Introductory Manual; WL# 700-4693

2200 VP/MVP BASIC-2 Lang. Reference Manual; WL# 700-4080, 4080-1, 4080-2

WCS 40/2200MVP Preliminary Service Bulletin #83 (Replaced by 03-0071)

2200MVP Maintenance Manual; CE Div. #03-0071 (Replaced by 03-0071-1)

2200MVP Maintenance Manual; CE Div. #03-0071-1

THE MVP CPU

2200MVP Maintenance Manual; CE Div. #03-0071

Module Repair Guide #'s 4.1A, 4.2A, 4.3A, 4.4A, 4.5

2236D/2236MXD Data Sheet; WL# 700-4807

Module Repair Guide # 3.2

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SYSTEM INTERACTIVE TERMINAL (2236D)

2236D/2236MXD Data Sheet; WL# 700-4807
Model 2236D Interactive Terminal User Manual; WL# 700-4405
Service Bulletins #73, 79, 80, 80A
Module Repair Guide #'s 3 & 3.1
ISN #s 121, 141A, 141B, 149, 173, & 179
SNL #90
CEA #31

OTHER SYSTEM PERIPHERALS

DISKS:

2260 (all versions)

SNL #'s 86.1 (key document)
2260 B Data Sheet; WL# 700-3483
2260C Fixed/Removable Disk Drive Data Sheet
2260B/C Disk Drive Ref. Addenda; WL#700-3159-1,2
2260BC & C Disk Drive Ref. Addendum; WL# 700-4081-2
2200VP/MVP Disk Drive Addendum; WL# 700-4081
Service Bulletin #'s 43, 43.1, 43.2, 43.2A, 72, & 86A
Mass Storage Device Manual; CE Div. #03-0026
Field-Level Maint. Guide: Diablo Series 40 Drives; CE Div. #03-0057
Diablo Series 40 Disk Drive Maintenance Manual
Diablo Series 40 Disk Drive Parts Catalog
Diablo 429 Power Supply Maintenance Manual
Diablo 44B Disk Drive Maintenance Manual
Diablo 44B Disk Drive Parts Catalog
CDC 10 Meg 'Hawk' Maintenance Manual (CE/OEM)
CDC 10 Meg 'Hawk' Training Manual CE Div # 03-0059
CDC Microcircuits Manual (OEM)
Wang 'Hawk' Manual #03-0072
ISN #'s 10, 17, 45, 65, 75.1, 81, 114, 114, 116, 116A, 125, 136,
142, 156, 161A, 164, 170, 171, 174, & 184
SNL #'s 1, 5, 47, 51, 58, 87, 131, & 132

2270A

2270A IBM 3740-Compat. Diskette System Data Sheet; WL #700-4152
Service Bulletin #82
ISN #'s 85, 87, 91, 122, 129A, 154, 154.1
SNL #'s 32, 65, 123

2280 (all versions)

2280 Fixed/Removable Disk Drive Data Sheet; WL# 700-4843
CDC (Phoenix) Cartridge Module Drive Prelim. Hardware Maint. Manual
FLMG: Phoenix Disk Drives; CE Div. Publication (still in prep. stage)

PRINTERS & PLOTTERS:

2201L

2201L Output Writer Data Sheet; WL# 700-4377
2201L Output Writer User Manual; WL# 700-4403

2221W

2221W Line Printer Data Sheet; WL# 700-3620
2221W Line Printer User Manual; WL# 700-3638
Model 72 Matrix Printer (2221W) Manual; CE Div. #03-0027
Matrix printer FLMG #03-0060
ISN #s 83, 96, 102, 108.1, & 176
SNL #s 4, 21, 26, 30, 36, 41, 48, 52, & 100
CEA #s 7 & 32

2231W-1, 2, 3, & 6

2231W Line Printer Data Sheet; WL# 700-3821
2231W Line Printer User Manual; WL# 700-3877
2231W-3 Data Sheet; WL# 700-4375
2231W-3 User Manual; WL# 700-4457
2231W-6 Data Sheet; WL# 700-4677
2231W-6 User Manual; WL# 700-5040
Model 61/62 Matrix Printer (2231W) Manual; CE Div. #03-0077
Matrix printer FLMG #03-0060
Service Bulletin #76
ISN #s 118 & 163
SNL #s 54, 61, 81, 83, & 100
CEA #18

2261W

2261W Data Sheet; WL# 700-4144
2261W Line Printer User Manual; WL# 700-4271
2261W Line Printer User Manual Addendum; WL# 700-4423
Matrix printer FLMG #03-0060
2200VS, Volumes 1, 2, & 3
Model 77 Quad Head (2261W) Printer Manual; CE Div. #03-0061
ISN #s 157, 167, & 176
SNL #s 102, 111, & 119

2263-1,2

2263 Line Printer Data Sheet; WL# 700-4149
2263 Line Printer User Manual; WL# 700-4251
Chaintrain - Logic & Troubleshooting Manual (OEM)
Chaintrain - Maintenance Instructions Manual (OEM)
Chaintrain - Operation Instructions Manual (OEM)
Chaintrain - Principles of Operation Manual (OEM)
Chaintrain - Illustrated Parts Breakdowns (OEM)
ISN #s 162, 168, & 169
SNL #98

2271

2271 Output Writer Data Sheet; WL# 700-4147
2271 Output Writer User Manual; WL# 700-4276

2281

2281 Daisy Printer Data Sheet; WL# 700-4146
Service Bulletin #74
Diablo HY-TYPE II Maintenance Manual
Diablo HY-TYPE II Illustrated Parts Catalog
Module Repair Guide #'s 7 & 9
SNL #s 74, 97, & 128

2281W, WWP

Model 81W/81WWP Prelim. Maintenance Manual; CE Div. Publication

2272

2272 Digital Drum Plotter Data Sheet; WL# 700-3826
2200 Plotter Utilities Manual; WL# 700-3838
2200 Plotter Utilities Manual Addendum; WL# 700-3838-1
2272 Digital Plotter Prelim. Maint. Manual; CE Div. Publication
Module Repair Guide #8

TELECOMMUNICATIONS:

General

Telecom. Self-Teaching Manual; CE Div. Publication #03-0078
Product Service Telecommunications Guide; CE Publication
Service Bulletin #77
Asynchronous I Manual (Marketing Publication); WL# 700-4718
Telecom. Marketing Guide; WL# 700-4412
Telecom. Sales Guide; WL# 700-4703
Telecommunications Support Utilities User Manual; WL# 700-4086
Telecom. Support Utilities User Manual Addendum; WL# 700-4086-1
Teletype Emulator Data Sheet; WL# 700-4704
Burroughs Emulator Data Sheet; WL# 700-4705
2741 Emulator Data Sheet; WL# 700-4706
HASP Multileaving Data Sheet; WL# 700-4707
3741 Software Utilities Data Sheet; WL# 700-4708
2780/3780 Software Utilities Data Sheet; WL# 700-4709

2227B & 2227N

2227B Buffered Async. Telecommunications Data Sheet; WL# 700-3830
2227B Buffered Async. Telecommunications User Manual; WL# 700-4114
Service Bulletin #77

2228B & 2228N

2228B Bisynchronous Telecom. Data Sheet; WL# 700-4143
Service Bulletin #77

TAPE

2209A

2209A 9-Track Tape Drive Data Sheet; WL# 700-4261
2209A 9-Track Tape Drive User Manual; WL# 700-4358
2209A 9-Track Tape Drive Utilities Manual; WL# 700-4325
Kennedy Mod. 9100 Vacuum Column Tape Transport Manual
Kennedy Mod. 9219 Formatter Manual (OEM)
Service Bulletin #87
SNL #s 99, 104, & 107

GENERAL REFERENCE

SNL #s 6, 10, 27, 66, 85, 93, 93A, 93B, 108, & 114

CEA #s 3 & 6

ISN #150

Service Bulletins 33.1 & 85

Standards for IC Symbols #03-0010

Customer Engineering Schematics Manual #03-0019

Technical Procedures Manual #03-0013

Field Price Catalog #03-0022

Standard Tool Kit, Special tool list, & Extender Board
listing #03-0064

Service Newsletter

NO. 80

2200/2600 #14

December 9, 1976

This Newsletter contains the following:

1. INSTALLING THE 2228B CONTROLLER IN THE 2600 CHASSIS
2. SYSTEM 2200 VP (2600) - ECNs ON PERIPHERAL CONTROLLERS

1. INSTALLING THE 2228B CONTROLLER IN THE 2600 CHASSIS

The 2228B controller is slightly larger than other system 2200 controllers. When installing this controller in a 2200 VP, choose an I/O slot away from the fan. It will be seen that the 2228B does not fit next to the fan; it will almost contact the hub. Simply install this controller in any I/O slot away from the fan.

2. SYSTEM 2200 VP (2600) - ECNs ON PERIPHERAL CONTROLLERS

The 2200 VP (2600) CPUs will be shipped to customers very soon. While most of these CPUs are part of new systems, some will be upgrades to existing 2200 systems. If an existing system is upgraded where a customer has peripherals, ECNs must be performed on some of the peripheral controllers. Check to see that the following ECNs have been implemented.

- a. Model 2227B/2228 Telecommunications Controller, PC Board 6723
ECN 6087 should have been performed prior to shipment; if not, make the necessary change.

Cut the run leading from L21 pin 8 and L30 pin 2 to L41 pin 7 and L42 pin 7. An inverter gate must be inserted on this signal line. Wire two short jumpers to pins 3 and 4 of L28. L28 is a hex inverter, and the gate between pins 3 and 4 is currently not being used. Using the jumpers, insert the inverter gate into the signal line as shown on the next page.

WANG

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13-266

BASIC-2 OPERATING SYSTEM RELEASE ANNOUNCEMENT

by 2200 R&D

BASIC-2 Release 2.5

All 2200 VP/SVP single-user systems should be updated to Release 2.5 of the single-user Operating System.

Diskette numbers are: 701-21180 for VP
701-0001C for SVP
701-8068G for minidiskettes
701-8069F "
701-8129B "

Corrected Anomalies

In the editor, a problem relating to pressing the ERASE key at the end of a LINPUT field has been corrected.

In the editor, a problem relating to recalling text lines while in non-edit mode on a 2236DW terminal has been corrected.

A problem with the INPUT statement has been corrected. Attempting to supply a value enclosed by quotes in response to an INPUT request would result in an error X73. Also, not supplying values for all variables in the INPUT statement variable list would occasionally result in an error X75.

Changes and Corrections - Release 2.4 to 2.5

- @DAVFU The documentation displayed at the beginning of the utility has been changed to show the correct loading sequence for all VFU files created by the utility.
- @MOVEFIL All keyboard entries have been made case-insensitive; entering lower case replies will no longer result in an incorrect response from the utility.
- @BACKUP An erroneous message concerning the @BADSCTR file has been corrected.
- @FORMAT The program has been changed to control the occurrence of all disk errors and to erase the 15 second message on the terminal correctly.

Diagnostics

The '@-backslash' file as well as '@A' diagnostic have been updated. They were made to update the field service diagnostic and to fix a problem with the cpu diagnostic.

BASIC-2 Release 2.3

Release 2.3 of the BASIC-2 Multi-Task Operating System has been issued to provide support for the additional memory banks available on the 2200MVPC and 2200LVPC units. Release 2.3 can run on 2200MVP, 2200LVP and 2200SVP as well. Release 2.3 includes the following features and enhancements to earlier versions of the operating system:

The operating system now provides up to 512K bytes of user memory available for 2200MVPC and 2200LVPC systems. The maximum number to terminals remains 13 and maximum number of partitions is still 16.

The Partition Generator (@GENPART) and Partition Status (@PSTAT) System Utilities now support 512K of memory.

Revised system diagnostics for testing control and user memory are provided.

Corrected Anomalies

On earlier versions of the operating system, the DSKIP and DBACKSPACE statements, specifying a number of sectors or BEG could cause Model 2230MXA/MXB Disk Multiplexer to enter "hog" mode, thus locking out other CPU's. These statements have been corrected for Release 2.3 to enable the disk controller only when it is necessary to read the disk.

User's who utilize \$GIO to "hog" and "unhog" the disk are cautioned that a similar problem may occur in their programs if the "unhog" command (CBS 00) is issued without waiting for READY. All user's are encouraged to utilize the \$OPEN and \$CLOSE statements when exclusive control of any device is required.

Changes to the System Platter

The following files have been changed since Release 2.2 . The purpose and operation of each utility remains the same:

@MVP	MVP Operating System and BASIC-2 Language Processor (Release 2.3)
@A	CPU Diagnostic
@B	Control Memory Diagnostic
@C	Data Memory Diagnostic
@-backslash	Field Service Diagnostics Menu
@P	User Diagnostics Menu
@GENPART	Partition Generator Utility
@PSTAT	Partition Status Utility
@INSTALL	System Installation Utility
@SYSFILE	System Configuration File

TECHNICAL SERVICE BULLETIN
SECTION: SoftWare Technical

NUMBER: SWT 6100 REPLACES: _____ DATE: 08/12/86 PAGE 1 OF 2

MATRIX ID. 7615 PRODUCT/RELEASE# 2200 ASYNC I / BISYNC I

TITLE: Duplicate Filename Problem Between 2200 Async I and Bisync I Communications Software

PURPOSE:

To inform the field of a filename duplication in the 2200 Async I and Bisync I communications packages. While these files have the same name and function, they are NOT identical. This makes it necessary to modify the file in question in order run both packages on the same platter.

EXPLANATION:

The file "ASKAEMUL" allows the operator to load the emulator he wishes to run. In Async I, the options are TTY and 2741; in Bisync I, they are HASP, 2780, 3780, 3741, WPS, and 2200 to 2200. Since the files have the same name for both products, they cannot both exist simultaneously on the same platter.

CORRECTIVE ACTION:

In order to work around this, LOAD the ASKAEMUL program from one of the packages into your workspace. Then overlay the ASKAEMUL problem with the second package by performing a LOAD of the ASKAEMUL program from the second package without first clearing your workspace.

Finally, save the new program under the name "ASKAEMUL". The DATA statements and program lines have been numbered to make this newly created program functional for both async and bisync packages.

GROUP: Telecommunications Software Support Group MAIL STOP: 0115A

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TECHNICAL SERVICE BULLETIN
SECTION: Software Technical

NUMBER: SWT 6100 REPLACES: _____ DATE: 08/12/86 PAGE 2 OF 2

MATRIX ID. 7615 PRODUCT/RELEASE# 2200 ASYNC I / BISYNC I

TITLE: Duplicate Filename Problem Between 2200 Async I and Bisync I Communications Software

ADDITIONAL INFORMATION:

If there is any doubt as to if the above procedure has been performed correctly or not, simply list the "ASKAEMUL" program from the Async I, the Bisync I package, and the overlaid version. The programs will be identical except for the data statements at the end. They will appear as follows in the overlaid version:

9010	DATA	"1TTY	ASK?TTY	TELETYPE EMULATOR"
9020	DATA	"2TTT	ASK?2741	IBM 2741 (SELECTRIC)"
9030	DATA	"3HASP	ASK?HASP	MULTILEAVING HASP"
9040	DATA	"42780	ASK?2780	IBM 2780"
9050	DATA	"53780	ASK?3780	IBM 3780"
9060	DATA	"63741	ASK?3741	IBM 3741"
9070	DATA	"72200-2200	ASK?2200	WANG 2200 TO 2200"
9130	DATA	"=WPS MODE	ASK?WPS	2200-WPS MODE"
9500	DATA	" "		

GROUP: Telecommunications Software Support Group MAIL STOP: 0115A

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TECHNICAL SERVICE BULLETIN
SECTION: HardWare Technical

NUMBER: HWT 6152 REPLACES: _____ DATE: 06/18/86 PAGE 1 OF 1

MATRIX ID. 4201 PRODUCT/RELEASE# 2200 all

TITLE: Problems with the 210-7342 Printer/Disk Controller

PURPOSE:

To inform the field of problems associated with the 7342 printer/disk controller and possible circumventions.

EXPLANATION:

When using the 210-7342 printer/disk controller with a Phoenix Disk Drive or a 2275 Disk Unit, I90, I91, I92, and possibly I96 errors may be experienced. The problem could be intermittent or solid dependent on types of chips used on the board and where the board is positioned in the I/O section of the CPU. This is a design problem with the board for which R&D has a fix. Updated boards are being Beta tested at this time. Once the fix is verified an ECO will be issued.

CORRECTIVE ACTION:

There are several circumventions for this problem:

1. Install the 7342 controller in the last I/O slot farthest from the CPU boards. In testing it was found that a board failing solidly when near the CPU boards would run error free in the last slot.
2. Replace the 7342 controller temporarily with a 210-6541-2 single disk controller and a 210-7079 single printer controller.
3. Replace the 7342 controller with the older style 210-7042-2 printer/disk controller if available.
4. Replace the 7342 controller temporarily with the 212-3012 triple controller. See note 1.

Note 1: Although no problems have been reported with the 212-3012 triple controller (term/printer/disk), this board has the same circuit design and could be subject to the same problems. This board will also be updated.

Note 2: A number of newer disk cables (220-0364/0365) have twisted pair wiring. These cables may seem to work fine but should only be used with the Phoenix Mux boards, the 210-7715 and the 7717. The older cables (220-0105-4/0138) should be used if a newer cable with 1 to 1 wiring is not available. Check the cable by disassembling the connector.

GROUP: VS/2200 Hardware Support Group MAIL STOP: 0126

C O M P A N Y C O N F I D E N T I A L

WANG Laboratories, Inc.

WANG

TECHNICAL SERVICE BULLETIN
SECTION: SoftWare General

NUMBER: SWG 5108 REPLACES: _____ DATE: 12/31/85 PAGE 1 OF 1
MATRIX ID. 7605 PRODUCT/RELEASE# 2200 BISYNC/6.00.02
TITLE: New 'SCRATCH DISK' Method

PURPOSE:

PROBE #: F009616

When transmitting a file from a disk scratched with the new 'SCRATCH DISK' method, the emulator cannot find the requested file to send.

EXPLANATION:

The new 'SCRATCH DISK' method sets a flag in the disk index that tells the 2200 operating system to use a new hashing algorithm to determine where in the index to enter a file name. The disk search routines in the emulator software did not support the new hashing algorithm.

CORRECTIVE ACTION:

Modify the disk search routines in the emulator to check if the disk was scratched using the new 'SCRATCH DISK' method and if it was, use the new hashing algorithm to calculate the location in the index of the file name.

ADDITIONAL INFORMATION:

Available in the next maintenance release.

GROUP: Telecommunications Software Support Group MAIL STOP: 0129

COMPANY CONFIDENTIAL

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TECHNICAL SERVICE BULLETIN
SECTION: SoftWare Technical

NUMBER: SWT 5108 REPLACES: _____ DATE: 08/27/85 PAGE 1 OF 1
MATRIX ID. 4306 PRODUCT/RELEASE# 2200 IDEAS2/2.4
TITLE: Elimination of P56 error while running reports in IDEAS2.

PURPOSE:

To correct a problem with IDEAS2 in which an application could fail with a P56 error at line 418 in the IDEAS2 subroutines while running a report.

EXPLANATION:

When an IDEAS2 report finishes running, it first checks the key buffer for each of the files used in the report to make sure that no record has been left protected. If there is a discrepancy between the number of files listed in the application START program, and the number of files actually opened in the application, the P56 will occur when IDEAS2 checks the key buffer.

CORRECTIVE ACTION:

In IDEAS2 module IDS2SUB1, the fourth statement on line 418 is 'FOR V=1 TO LEN(E1\$())/56'. This statement should be changed to 'FOR V=1 TO LEN(STR(F1\$())/LEN(STR(F1\$(1))))'.

NUMBER: SWT 5109 REPLACES: _____ DATE: 08/27/85 PAGE 1 OF 1
MATRIX ID. 4306 PRODUCT/RELEASE# 2200 IDEAS2/2.4
TITLE: Eliminating extraneous STOP statement in IDEAS2 report driver

PURPOSE:

To inform the field about a STOP statement in IDEAS2 that is encountered when running an IDEAS2 report that uses level breaks.

EXPLANATION:

In release 2.4 of IDEAS2 there is a STOP statement that causes reports using level breaks to stop executing. The circumvention is to key 'CONTINUE', then 'RETURN', at which time the report will proceed.

CORRECTIVE ACTION:

Remove the STOP statement from line 1815 in IDEAS2 module IDS2PBX4.

GROUP: VS/2200 Software Support MAIL STOP: 0121A

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TECHNICAL SERVICE BULLETIN
SECTION: SoftWare Technical

NUMBER: SWT 5106 REPLACES: _____ DATE: 08/27/85 PAGE 1 OF 1

MATRIX ID. 4335 PRODUCT/RELEASE# DATAMERGE 2.2

TITLE: 2200 DATAMERGE P56 ERROR CORRECTION

PURPOSE:

To correct a P56 ERROR which occurs in DATAMERGE record selection with some IDEAS 1 files.

EXPLANATION:

With some IDEAS 1 files DATAMERGE 2.2 will abnormally end with a P56 ERROR in line 4270 during record selection. To correct this problem, line number 4460 of the DATAMERGE program "LPIDSUBS" should be changed:

OLD:4460:::::IF D3[=C6 THEN 4480

NEW:4460:::::IF D3[C6 THEN 4480

where [is used to represent the "less than" symbol available in 2200 BASIC 2.

GROUP: VS/2200 Software Support MAIL STOP: 0115

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CUSTOMER ENGINEERING
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NEWSLETTER

#20216

IV.C.4

2200 SYSTEMS-SOFTWARE-UTILITIES/TELECOM INFO.

TOPIC: BASIC-2 OPERATING SYSTEM RELEASE ANNOUNCEMENT

BASIC-2 RELEASE 2.3:

Release 2.3 of the BASIC-2 Multi-User Operating System has been issued to provide support for the additional memory banks available on the 2200MVPC and 2200LVPC units. Release 2.3 can run on 2200MVP, 2200LVP and 2200SVP as well. Release 2.3 includes the following features and enhancements to earlier versions of the operating system:

The Operating System now provides up to 512K bytes of user memory available for 2200MVPC and 2200LVPC systems. The maximum number of terminals remains 13 and maximum number of partitions is still 16.

The Partition Generator (@GENPART) and Partition Status (@PSTAT) System Utilities now support 512K of memory.

Revised system diagnostics for testing Control and User memory are provided.

CHANGES TO THE SYSTEM PLATTER:

The following files have been changed since Release 2.2. The purpose and operation of each utility remains the same:

@MVP	MVP Operating System and BASIC-2 Language Processor (Release 2.3)
@A	CPU Diagnostic
@B	Control Memory Diagnostic
@C	Data Memory Diagnostic
@-backslash	Field Service Diagnostics Menu
@P	User Diagnostics Menu
@GENPART	Partition Generator Utility
@PSTAT	Partition Status Utility
@INSTALL	System Installation Utility
@SYSDFILE	System Configuration File

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NEWSLETTER

#20216

IV.C.4

2200 SYSTEMS-SOFTWARE-UTILITIES/TELECOM INFO.

TOPIC: BASIC-2 OPERATING SYSTEM RELEASE ANNOUNCEMENT (Continued)

CORRECTED ANOMALIES:

On earlier versions of the operating system, the DSKIP and DBACKSPACE statements, specifying a number of sectors of BEG could cause Model 2230MXA/MXB Disk Multiplexer to enter "hog" mode, thus locking out other CPU's. These statements have been corrected for Release 2.3 to enable the disk controller only when it is necessary to read the disk.

Users who utilize ;GID to "hog" and "unhog" the disk are cautioned that a similar problem may occur in their programs. The "unhog" command (CBS 00) is issued without waiting for READY. All users are encouraged to utilize the ;OPEN and ;CLOSE statements when exclusive control of any device is required.

Also please note that the new operating system will automatically do three retries when an LRC error is encountered.

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NEWSLETTER

#20309

IV.A.3

2200 SYSTEMS-MAINFRAMES-VP/MVP/LVP CPU'S.

TOPIC: MEMO ON 2200 OPTION C

Below is a reprint of a memo written by Gary Loper, ATS in the Central Area. The memo deals with information needed to properly install/service the 2200 option "C".

SUMMATION OF LVP OPTION C WITH QUANTUM DRIVES

1. For Data Memory greater than 256K, the 210-6793-1 must have ECO #17388 incorporated, bringing the E-Rev to 4.
2. The 210-6790 is replaced with a 210-7797.
3. A 210-7796 extended memory controller is installed between the Control Memory Boards and the Data Memory Boards..
4. If the Control Memory is not greater than 32K, (only one control memory board), it must be installed in the second slot. If it is installed in slot #1 a PECM 0001 FFFFFFF will result. (CM must be 64K for Cobol and Basic 3).
5. To run the Quantum Drives, ECO #20404D has been done on the LVP motherboard (7799). During installation refer to the TAC Newsletter #10292 for the Quantum shipping clamps and voltage checks.
6. The plus 5V2 volts I/O is now used for the last 4 I/O locations and can be measured at pin B of connector 1 at the I/O location.

Please become familiar with the PSN mentioned as soon as possible because many of these units are being shipped now and numerous other units are being upgraded.

If any questions arise, please don't hesitate to call.

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NEWSLETTER

#20406

IV.C.4

2200 SYSTEMS SOFTWARE RELEASES

TOPIC: 2200 SOFTWARE/HARDWARE BULLETIN #1 (DECEMBER 1, 1981)

PREFACE

The purpose of this Software/Hardware Bulletin is to provide up-to-date documentation for hardware and software enhancements to the 2200 Series until the appropriate manuals are revised.

This bulletin describes the changes and features of Release 2.3 of the 2200 BASIC-2 Multiuser Operating System and discusses the 2200 MVPC, 2200 LVPC and 2200 SVP Central Processing Units (CPUs).

This documentation is intended to be used in conjunction with the following manuals.

BASIC-2 Utilities Reference Manual (700-6855)

Wang BASIC-2 Language Reference Manual (700-40800)

Wang BASIC-2 Disk Reference Manual (700-40816)

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NEWSLETTER

#20406

IV.C.4

2200 SYSTEMS SOFTWARE RELEASES

TOPIC: 2200 SOFTWARE/HARDWARE BULLETIN #1 (DECEMBER 1, 1981)
(Continued)

2200 SYSTEM ENHANCEMENTS

THE 2200MVPC CENTRAL PROCESSING UNIT

The 2200 MVPC Central Processing Unit (CPU) incorporates all the features of the 2200 MVP and supports an increased amount of user memory and control memory. User memory is available in 64K, 128K, 256K, 348K and 512K bytes. User memory can be upgraded in the field. The MVPC chassis contains seven I/O slots; each I/O slot can contain a controller capable of controlling one or more peripherals. The MVPC, like the MVP, supports Release 2.3 of the BASIC-2 Multiuser Operating System.

THE 2200LVPC CENTRAL PROCESSING UNIT

The 2200 LVPC Central Processing Unit (CPU) incorporates all the features of the 2200 LVP and additionally supports an increased amount of disk capacity, user memory and control memory. The Winchester-style disk drive for the LVPC is available in 2, 4, 8, 16, or 32-megabytes storage capacities. User memory is available in 64K, 128K, 256K 348K and 512K bytes. Both user memory and disk capacity can be upgraded in the field. The LVPC chassis contains seven I/O slots; each I/O slot can contain a controller capable of controlling one of more peripherals. The LVPC, like the LVP, supports Release 2.3 of the BASIC-2 Multiuser Operating System.

THE 2200SVP CENTRAL PROCESSING UNIT

Several features have been added to the 2200 SVP Central Processing Unit (CPU), enabling it to function as a multiprogramming system, optionally supporting an expanded memory size and disk storage capacity. The following features are now available on the 2200 SVP.

User memory can be expanded up to 128K bytes.

User memory can be divided into up to 16 partitions, each supporting a separate program or task. The SVP can use the BASIC-2 Multiuser Operating System and the full complement of BASIC-2 Utilities such as @GENPART and @PSTAT.

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NEWSLETTER

#20406

IV.C.4

2200 SYSTEMS SOFTWARE RELEASES

TOPIC: 2200 SOFTWARE/HARDWARE BULLETIN #1 (DECEMBER 17, 1981)
(Continued)

Foreground/background processing is supported.

An optional Winchester fixed disk drive with an 8-megabyte capacity is available.

USER MEMORY

The 2200 SVP, with a standard user memory capacity of 32K bytes, can optionally support up to the 128K bytes of user memory. A standard 2200 SVP can be optionally configured with one or two banks of user memory, each bank consisting of 64K bytes of storage.

MULTIPROGRAMMING FEATURES

The 2200SVP now can simultaneously process up to 16 different tasks. After the operator presses the Special Function key that loads the system programs from the system platter, the operator employs the Partition Generator utility (@GENPART) to distribute system resources. Partition operations can be monitored by means of the Partition Status utility (@PSTAT). Both the Partition Generator utility and the Partition Status utility reside on the system platter.

The 2200 SVP can support up to 16 partitions of varying sizes. The number and size of the partitions are determined by the operator. Within each bank, a fixed amount of the memory is reserved for system overhead and cannot be accessed by the user. The first bank requires 3K bytes and the second bank, 8K bytes. These amounts of memory are fixed for 2200 SVP systems containing one or two banks, regardless of the total memory contained in each bank. The operator can divide the remainder of each bank into a number of partitions of fixed size; a total of 61K bytes in Bank 1 and 56K bytes in Bank 2 are available for user partitions. No partition can overlap banks. In addition, each partition in each bank requires approximately 1K bytes of partition overhead. All remaining memory in a single partition is available for user programs and data.

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#20406

IV.C.4

2200 SYSTEMS SOFTWARE RELEASES

TOPIC: 2200 SOFTWARE/HARDWARE BULLETIN #1 (DECEMBER 1, 1981)
(Continued)

The 2200 SVP user can now execute a variety of special functions and statements that address multiprogramming needs, including global subroutines and variables and a temporary seize/release capacity for programs using shared devices. These functions and statements are briefly explained in the following list; they are discussed in detail in Chapter 16 of the Wang BASIC-2 Language Reference Manual (700-4080D).

The following BASIC-2 functions can now be used on the 2200 SVP.

- #PART - Returns a numeric value equal to the partition number of the originating partition for this job.
- !PSTAT - Returns the current status of the specified partition. The status information includes a user-defined status message, operating system type (VP or MVP), operating system release number, partition size, terminal number, global name, ERR function value and I/O device currently in use.
- #TERM - Returns a numeric value equal to the terminal number of the terminal assigned to the originating partition for this job.

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NEWSLETTER

#20406

IV.C.4

2200 SYSTEMS SOFTWARE RELEASES

TOPIC: 2200 SOFTWARE/HARDWARE BULLETIN #1 (DECEMBER 1, 1981)
(Continued)

The following BASIC-2 statements can now be used on the 2200 SVP.

- ;BREAK - Relinquishes a specified amount of the current partition's execution time for use by other partitions.
- ;CLOSE - Releases one or more hogged devices.
- DEFFN @PART - Defines the current partition as global.
- ;INIT - Passes configuration parameters to the operating system.
- ;MSC - Defines a broadcast message available to all terminals (can be executed only by Terminal 1).
- ;OPEN - Hogs one or more devices.
- ;PSTAT - Sets the user-defined portion of the partition status.
- ;RELEASE PART - Causes ownership of a partition by a terminal to be relinquished.
- ;RELEASE TERMINAL - Detaches the terminal from the current partition.
- SELECT @PART - Selects a specified global partition for subsequent global subroutine and global variable references.

The SVP user can economize on the use of memory by defining one or more global partitions within each memory bank. The variables stored in a global partition are accessible to other partitions within that bank. Though a global partition in Bank 1 cannot be accessed by partitions in Bank 2, and vice versa, a 5K byte area of Bank 1 can be reserved as a universal global partition area. A universal global partition, located entirely within this 5K byte area, can be employed to store control variables used by any partition in either Bank 1 or 2.

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NEWSLETTER

#20406

IV.C.4

2200 SYSTEMS SOFTWARE RELEASES

TOPIC: 2200 SOFTWARE/HARDWARE BULLETIN #1 (DECEMBER 1, 1981)
(Continued)

The 2200 SVP enables a programmer to make common routines and variables accessible to a number of different programs. For instance, if several programs must share a common disk file, all access to the disk file can be controlled by a single routine, contained in a global partition. Whenever a program attempts to access the file, the program branches to the global routine, and the routine actually performs the access. Additionally, global variables can be contained in the same global partition as the routine. Programs running in separate partitions can interrogate and modify global variables, using them as flags to indicate the status of the disk file and to transfer control information. In this way, a central routine controls the use of a resource shared by several programs, oversees the operations of these programs, and resolves potential conflicts among them.

The ;OPEN and ;CLOSE statements enable a program to seize temporary control of a device and subsequently release it. These features are important for operations requiring shared devices that do not lend themselves to interleaved use by several programs, and for special disk operations where one program must have exclusive access to the disk temporarily. For example, a program can temporarily seize a shared printer, complete all necessary printing, and then release the printer so that another partition can use it.

Foreground/Background Operation

Though the terminal can communicate with only one job at a time, it can run up to 16 jobs concurrently, depending upon the partitioning of memory. A terminal can be switched from one partition to another by means of the ;RELEASE TERMINAL statement. The ;RELEASE TERMINAL statement shifts the executing foreground job into the background and a specified background job into the foreground, to permit operator communication with that program.

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NEWSLETTER

#20406

IV.C.4

2200 SYSTEMS SOFTWARE RELEASES

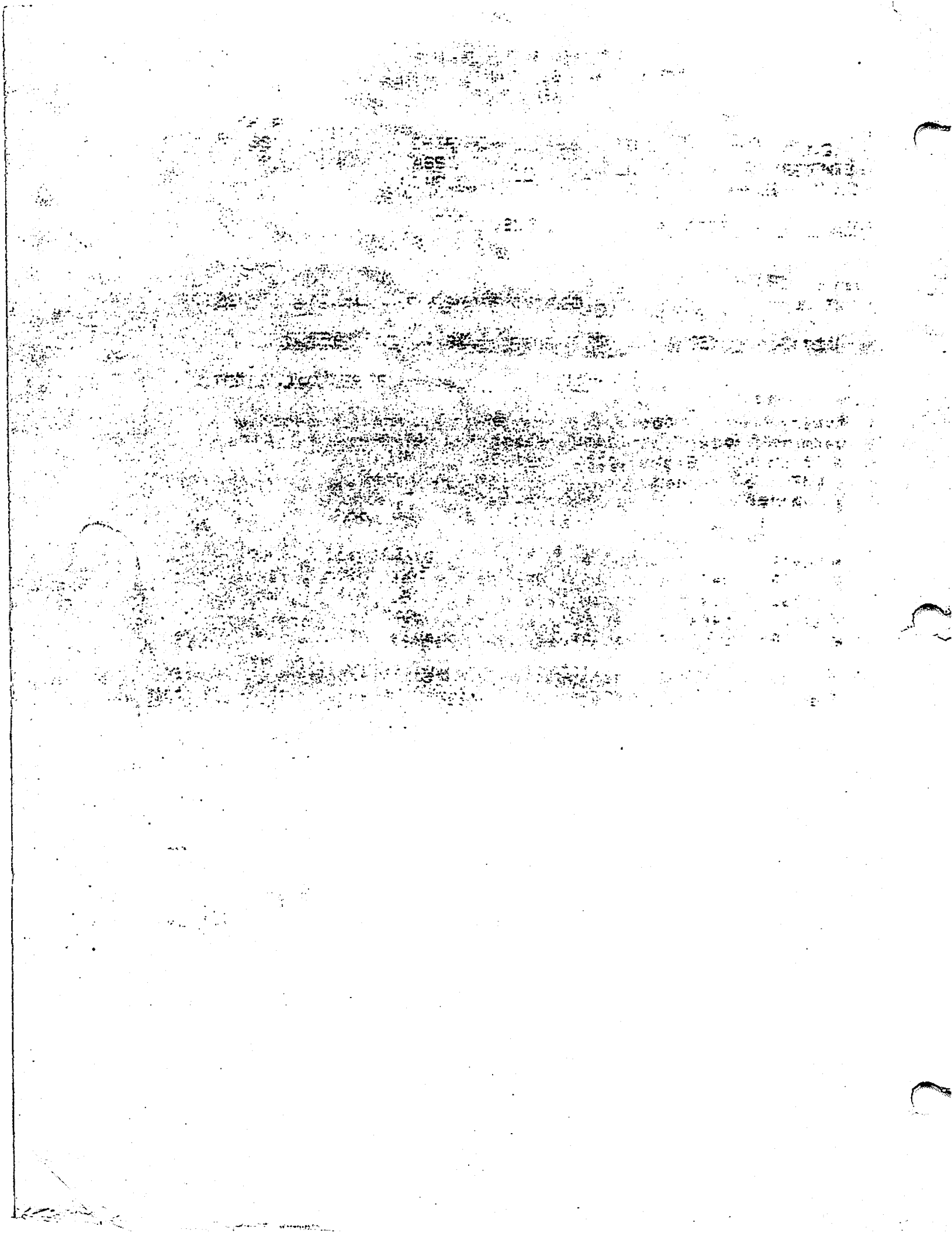
TOPIC: 2200 SOFTWARE/HARDWARE BULLETIN #1 (DECEMBER 1, 1981)

(Continued)

Fixed Disk Drive

The 2200 SVP now supports an 8-megabyte fixed disk drive as a system option. The following list summarizes the disk storage options available for configuration with the 2200 SVP.

- . One dual-sided, double-density (DSDD) diskette drive (standard)
- . Two DSDD diskette drives (dual diskette system)
- . One DSDD diskette drive and a fixed Winchester-style disk drive (optional 2, 4, or 8 megabytes)



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NEWSLETTER

#30215

IV.A.3 (4103)

2200 SYSTEMS-MAINFRAMES-VP/MVP/LVP/SVP CPU'S.

TOPIC: PARITY ERRORS ON 'C' CHASSIS

A problem has been found on the LVP-C and MVP-C where the customer will get intermittent parity errors (PEDM).

The solution to this problem is a new PCA, 210-6791-1 STACK PCA.

All 'C' chassis, both MVP and LVP in the field, should be updated to incorporate the new PCA.

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NEWSLETTER

#21109

IV.B.1

2200 SYSTEMS-INTERFACE-I/O CONTROLLERS.

TOPIC: 22C32 TRIPLE CONTROLLER - REAL TIME CLOCK

To run a real time clock on the triple controller, you must have:

- 210-7816A daughter board.
 - with R1 proms.
 - Minimum E-REV 2.
- MVP 2.4 software.

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NEWSLETTER

#30308

IV.B.1 (4202)

2200 SYSTEMS-INTERFACE-I/O CONTROLLERS.

TOPIC: HANG UP PROBLEM ON 2236 MXD

A legitimate fix has been found for MXD hangups when using a 210-7591 daughter board and R7 proms, refer to TAC newlsetter #20420

The fix involves installing two capacitors on the 210-7591 PCA.

- 1) Add a 390pf capacitor (WLI 300-1390) between L6-pin 13 and plus/minus 0 volts.
- 2) Add a 35uf capacitor (WLI 300-3009) between Q2-pin 2 (-5V output) and plus/minus 0V. (Tie minus end of electrolytic cap to Q2-pin 2).

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NEWSLETTER

#30201

IV.C.3

2200 SYSTEMS-SOFTWARE-UTILITIES/TELECOM INFO.

TOPIC: CONTROL MEMORY FOR COBOL/BASIC-3

Because Wang Laboratories will not be marketing COBOL and BASIC-3 on the 2200 Computer Product Line, 64K of Control Memory is no longer needed. The only requirement for 64K of Control Memory was COBOL and BASIC-3. For all marketed versions of the 2200 Computer Product Line, 32K of Control Memory will suffice. This includes the 'C' models of the MVP and LVP.

In the 'C' models of the MVP and LVP, the active (PCA being used) Control Memory PCA is the one on the right as you face the rear of the LVP chassis, or towards the power supply as in the MVP.

If the customer has already obtained the second Control Memory PCA's, DO NOT remove either PCA or change his configuration in any way as he owns that PCB. Treat the second Control Memory PCA as an extra, unused PCA. All future systems will only have 32K of control memory.

WORD PROCESSING ON THE 2200

There are some known bugs with Word Processing on 2200 which include:

1. Glossary does not work at all
2. If you are not using a TSF with the daisy, the top of form function will not work properly

New prompts, R5, will be coming out along with a 7792 board. WP software is also being revised to help correct these problems.

If you know of any other problems, please let the District Staff know.

The following is a list of error codes for WP on 2200.

ERROR CODES

HEX ERROR CODE

DESCRIPTION

01	Volume Full
02	File or Volume already exists
03	File or Volume does not exist
04	No free device slots
05	Incorrect password
06	Open access type error
07	File not open
08	Illegal file ID
09	Not enough room in File(to reuse scratched file)
10	File mess up
20	EDF reached unexpected (fatal)
22	Destination VAU not valid
23	Buffer variables not valid
24	No VAUS in file
25	Source & VAU # inconsistent
26	Volume unit parameter inconsistent
27	Byte parameter error in replace
28	EOF reached normal (not fatal)
29	Data transfer with greater than 128 VAUs

Number Error Code

Description

80 thru 89	Disk errors (refer to BASIC-2 ref manual)
90-99	I/O errors(refer to BASIC-2 ref manual)

STOP 5070

KNOWN BUG, PROBLEM w/ POINTERS ON DOCUMENT DISK
MESSED UP.

1.5.4 Error Codes

Table 1-3 lists some possible errors that result when using the document access subroutines. The error codes are returned in the variable B1\$.

Table 1-3. Error Codes

<u>Hex Error Code</u>	<u>Description</u>
01	Volume Full
02	File or Volume already exists
03	File or Volume does not exist
04	No free device slots
05	Incorrect password
06	Open access type error - (File is open by another user, or was previously opened by this user)
07	File not open
08	Illegal File ID
09	Not enough room in file (to reuse scratched file)
10	File mess up
20	EOF reached unexpected (fatal)
22	Destination VAU not valid
23	Buffer variables not valid
24	No VAU's in file
25	Source & VAU # inconsistent
26	Volume init parameter inconsistent
27	Byte parameter error in replace
28	EOF reached normal (not fatal)
29	Data transfer with greater than 128 VAU's
A1	Page table full
A2	Last page cannot be deleted
A3	Page does not exist
A4	User defined slot number already assigned
A5	Illegal file name
A6	Library map not found on the selected disk
A7	Library has not been established
A8	Illegal page number
A9	Prototype doesn't exist
B0	Prototype not accessible
B1	Glossary not attached
B2	Glossary not verified
B3	Glossary index exceeds one sector
B4	Glossary entry not found
B5	Wrong numeric type for admin

<u>Numeric Error Code</u>	<u>Description</u>
80 through 89	Disk errors (refer to BASIC-2 manual)
90 through 99	I/O errors (refer to BASIC-2 manual)

** HEX(00) Normal, successful return



TECHNICAL SERVICE BULLETIN
SECTION: SoftWare Technical

NUMBER: SWT 6164 REPLACES: _____ DATE: 12/16/86 PAGE 1 OF 2
MATRIX ID. 4307 PRODUCT/RELEASE# 2200 WP 02.04.00
TITLE: Top Of Form Rules In 2200 WP

PURPOSE:

To inform the field and users that the rules in 2200 WP release 02.04.00 have been changed regarding "Top Of Form".

DESCRIPTION:

With the introduction of 2200 WP release 02.04.00 all printers and CPUs will have new rules for "Top Of Form" when using Word Processing. Very simply the system will call for a "Top Of Form" (TOF) at the beginning of each WP document sent to a printer.

There were many problems with previous releases of 2200 WP regarding this issue. In general, the system would call for TOF at the end of the document, but under certain conditions it could also call for TOF at the beginning or sometimes both at the beginning and the end. This caused problems for people who were running DP applications and WP applications simultaneously. If the DP application did not call for TOF at the end of its report and if the next WP document did not call for a TOF, the WP document would start printing where the DP report left off and thus losing TOF.

The other problem was when WP called for TOF at the beginning and the end of the document. Although this guaranteed TOF, it would also result in extra sheet feeds, which was not acceptable to our users with multicopy preprinted forms (every other sheet would be wasted).

The only logical answer that would accommodate the majority of applications and the current 2200 WP architecture, was a TOF at the beginning of each document and none at the end. This would alleviate the problems with DP vs WP users, because WP would guarantee the TOF. Our users with preprinted forms again would benefit, because they would only see one TOF per document, hence no extra sheet feeds.

GROUP: VS/2200 Software Support

MAIL STOP: 001-150

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TECHNICAL SERVICE BULLETIN
SECTION: SoftWare Technical

WANG

NUMBER: SWT 6164 REPLACES: _____ DATE: 12/16/86 PAGE 2 OF 2

MATRIX ID. 4307 PRODUCT/RELEASE# 2200 WP 02.04.00

TITLE: Top Of Form Rules In 2200 WP

DESCRIPTION (cont'):

The only complaint has been that under the new rules, a document will not automatically clear the printer platen after it has printed. This is because the system does not call for a TOF until the next document. There is an easy circumvention for this problem. The user need only put a page break at the end of the document if they want it to clear automatically. THIS, HOWEVER, WILL CAUSE EXTRA SHEET FEEDS, or they may manually hit the form feed button on the printer.

We feel that this is the best approach to accommodate the majority of users and guarantee TOF for all users.

GROUP: VS/2200 Software Support

MAIL STOP: 001-150

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NEWSLETTER

#30426

4302 (IV.C.4)

2200 SYSTEMS-SOFTWARE-OPERATING SYSTEMS

TOPIC: 2200 WORD PROCESSING RELEASE 2.1 (CONTINUED)

Supervisory Functions

1. Process Print "Queue" has been moved from Background monitor.

9.0 PROBLEMS CORRECTED

1. Various "Print from Archive" problems.
2. Various problems concerned with combinations of special characters in printing on both the DW/22-20 and 2281 printer series.
3. Embedded format line problems in print.
4. Page breaks and indent processing problems in editor.
5. Various "Merge Print" problems.
6. 2200 WP can now safely co-reside with 3270 protocol.
7. Footers and headers now function as they do in the OIS.

10.0 KNOWN ANOMALIES

1. Repagination of existing full pages, of pages with embedded format lines, or during the creation of full pages may potentially create problems, including the possible loss of text. This will be corrected in a later release.
2. When printing on a DW/22-20 and an entire line is underscored and any of the bold print, autoslash or double underscore flags are turned off within that line, the remaining underscores are likely to print at the far left margin. This is suspected to be a microcode peculiarity between the 2281W and the DW/22-20 printers.
3. Dectabs of columnar text which contain embedded blanks are treated somewhat differently than on the OIS, in that alignment is on the first blank space rather than the delimiter character.
4. Underlined keywords printout with underline on summary page.

11.0 REFERENCES

2200 Word Processing Operator's Guide (700-6937A)
2200 Word Processing Supervisor's Manual (700-6864A)
2200 Programmer's Guide to Word Processing (700-6961)

CUSTOMER ENGINEERING
TECHNICAL ASSISTANCE CENTER
NEWSLETTER

#30426

4302 (IV.C.4)

2200 SYSTEMS-SOFTWARE-OPERATING SYSTEMS

TOPIC: 2200 WORD PROCESSING RELEASE 2.1 (CONTINUED)

7.0 RESTRICTIONS AND SPECIAL CONSIDERATIONS

1. A 42k partition is required to use the improved \$GIO editor, Horizontal Scroll, and resident \$GIO delete.
2. A 28k partition is restricted to running 80 column pages, and the original editor.

8.0 ENHANCEMENTS

Editor

1. An improved performance \$GIO editor.
2. Horizontal Scrolling.
3. Resident \$GIO delete.
4. Command "E" - provides escape from document without resaving page.

Printer

1. DW/22-20 printer compatibility.
2. Standard functionality for twin sheet feed (i.e. first sheet from bin one, subsequent sheets from bin two).
3. Printer support of fifteen pitch.

Background Monitor

1. \$ALERT - "Sleep" function.
2. "Process Print Queue" has been moved to Supervisory Functions.

Advanced Functions

These features are resident but will function only if the appropriate Wangwriter software is present.

1. Convert WP document to Wangwriter format.
2. Convert Wangwriter document to 2200 WP format.

CUSTOMER ENGINEERING
TECHNICAL ASSISTANCE CENTER
NEWSLETTER

#30426

4302 (IV.C.4)

2200 SYSTEMS-SOFTWARE-OPERATING SYSTEMS

TOPIC: 2200 WORD PROCESSING RELEASE 2.1 (CONTINUED)

All of these are checked for in PSTAT. Partitions 2-15 are checked sequentially and the first partition for which all three conditions are true will be attached and released to by the directing workstation, leaving the monitor running in the original 28k partition.

Current documentation on background monitor (Process Print Queue) is being updated.

4. 2245 and 2233/35 series printers are considered line printers for purposes of 2200 WP. They will, therefore, not underline, bold print, autoslash, or perform software-controlled form length settings.
5. Pressing FN '29 following a crash or RESET condition is likely to damage the resident WP program file on disk. This condition will be fixed in a later release.
6. Recover archive has not been included in this release.

4.0 DISTRIBUTION INFORMATION

This software will be distributed to all Branch, District and Area Offices and to all customers who have ordered the package. (See Alert #1).

5.0 INSTALLATION INSTRUCTIONS

Refer to the installation procedure in the 2200 Word Processing Supervisor's Manual, page 1-1, section 1.3 "Loading the Software".

Note: If installing from DSDD diskettes, it may be necessary to press EXECUTE to continue after "Mount Diskette" prompt without changing diskettes, as the install may be expecting SSSD diskettes.

6.0 MEDIA CONTENTS

Not listed in this newsletter.

CUSTOMER ENGINEERING
TECHNICAL ASSISTANCE CENTER
NEWSLETTER

#30426

4302 (IV.C.4)

2200 SYSTEMS-SOFTWARE-OPERATING SYSTEMS

TOPIC: 2200 WORD PROCESSING RELEASE 2.1

1.0 RELEASE ABSTRACT

Release 2.1 of 2200 Word Processing software is now available. It contains fixes to release 2.0 as well as numerous functional enhancements.

Part Numbers for DSDD diskettes

731-0067-A
731-0071

2.0 PRE-REQUISITES

2.1 Hardware

2200 VP/SVP/LVP/MVP with a minimum of a 28k partition.

2.2 Software

MVP, SVP (multi-user systems) and LVP CPU's require Release 2.3, or greater, of the operating system.

VP series CPU's require release 2.5, or greater, of the operating system.

3.0 ALERTS

1. Due to problems with interfacing DATAMERGE 2.0 and WP 2.1, this software should only be installed at those sites that do not have DATAMERGE.
2. Column count in the SGIO editor is updated only at crossing lines, crossing white space, and upon use of special control characters (crossing or typing).
3. It should be noted that when releasing a document to background, only three conditions are to be considered:
 1. Attached terminal must be "OO".
 2. Status must be "W".
 3. Global designation must be blank.

SOFTWARE RELEASE



LABORATORIES, INC.

Software Engineering

PRODUCT LINE	2200	SUBJECT	RCM	EFFECTIVE DATE	May 18, 1982
TYPE	Maintenance	RELEASE NO	01.02.00	S.E. PACKAGE NO	0013

RELEASE ABSTRACT

REMOTE CONTROL AND MAINTENANCE SYSTEM

The 2200 Series Remote Control and Maintenance system (RCM) consists of a package of existing and new hardware with existing and new software, to permit a 2200 CPU and interactive terminal to attach to a remote 2200 CPU as a 2236DE OR 2236DW. It permits a 2200 user to execute all programs and diagnostics resident on the remote system. The user may also execute a file transfer program in the remote system, and perform file movement between the systems.

INSTALLATION/UPGRADE POLICY

Obsolesces Release(s): 01 01 00 _____

Prior release supported until: 07/18/82

Installation:

- | | |
|---|--|
| <input type="checkbox"/> At next visit | <input type="checkbox"/> As soon as possible |
| <input type="checkbox"/> New systems | <input checked="" type="checkbox"/> Authorized systems |
| <input type="checkbox"/> Problem correction | <input type="checkbox"/> By: ___/___/___ |
| <input type="checkbox"/> Other _____ | |

Special Installation Instructions:

Scratch previous RCM System version 01.01.00 and replace with RCM System version 01.02.00 on your system disk platter.

	SOFTWARE ENGINEERING <i>[Signature]</i>	DATE 6/5/82
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ALERTS - None

PREREQUISITES

Configuration

Any 2200 Series system.

Hardware/ECO's Required

An asynchronous controller at the "control" system executing the Terminal Emulation Program. (2227B, 2228B, 2228C)

A terminal port at the remote system.

Two async modems supporting 2236DE/DW characteristics.

The SVP requires a switch box (Model 2236LRS) to link the remote 2236DE into the terminal controller instead of the local Interactive Terminal, and to change interface speed from 19.2 KB to 1200 bps or 300 bps.

Software Release Levels

A Terminal Emulation Program (TEP), which executes in the CPU, uses an asynchronous interface, supports a 2236DE/DW Interactive Terminal, and communicates with a remote system as if it were a 2236DE/DW. It also has a file send/receive mode which interacts with the File Transfer Program, providing RCMS operator control of file transfer operations. The TEP's File Transfer Mode displays a full menu of prompts for both File Send and File Receive, as well as a Command Menu.

A File Transfer Program (FTP), which executes in the remote system to exchange files with the Terminal Emulation Program.

There may be more than one system equipped with the Terminal Emulation - there is no reason why every system should not have access to another system's data and facilities, if so desired. The RCM software may also be used to loosely connect several 2200 systems. A user may call a remote CPU, execute a program in that system, perhaps to access a 3270 link, or to fetch a file.

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DELIVERABLES

Media

The RCM System Software is delivered on one diskette.

Remote Control & Maintenance System

Distribution

This product will be mailed to authorized customers and Wang offices as per the data base for 2200 RCM users as compiled by the Software & Literature Control Center.

INSTALLATION INSTRUCTIONS

Scratch previous RCM System Version 01.01.00 and replace RCM System Version 01.02.00 on your system disk platter.

APPLICABLE DOCUMENTATION

Remote Control and Maintenance System Users Manual.
1st Edition - June 1981
700-6848

FEATURES

Enhancements - Error checking has been implemented on the Receive File option of the file transfer.

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MAINTENANCE HISTORY:

Problems Corrected

1. Despooling TC formatted lines in foreground after printing is completed, the menu is reprinted on the screen. When the printer address prompt is printed the error message "UNABLE TO ACCESS SPECIFIED PRINTER" will not appear under the prompt.
2. When loading the terminal emulator program, the program checks the address of the TC controller. If the default address is wrong, the message "cannot access the TC controller. Correct address or key SF'31 to abort." Keying SF'31 now functions accordingly.
3. Timeout/2227B is now fixed.
4. VP Operating System.
5. File Transfer.