CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
A_0							L_1	L_1				L_1	L_1							
A_1							J_1	J_1				J_1	J_1							
A_2							9_1	9_1				9_1	9_1							
A_3							K_1	S_1				K_1	K_1							
A_4							11_1	12_1				11_1		11_1						
A_5							8_1	8_1				8_1		8_1						
A_6							H_1	H_1				H_1		H_1						
A_7							5_1	5_1				5_1		4_1						
A_8							6_1	6_1				6_1		S_1						
A_9							7_1	7_1				7_1		K_1						
A_{10}							10_1	P_1				10_1		F_1						
A_{11}							7_3	J_3				8_3		J_1						
A_{12}							E_1	E_1				E_1	E_1							
A_{13}							13_1	13_1				13_1	13_1							
A_{14}							M_1	A_2				M_1	M_1							
A_{15}							F_1	F_1				F_1	F_1							
$\overline{A_0}$	L_1	L_1	L_1	L_1	L_1	L_1	B_2													
$\overline{A_1}$	J_1	J_1	J_1	J_1	J_1	J_1	5_2													
$\overline{A_2}$	9_1	9_1	9_1	9_1	9_1	9_1	2_2													
$\overline{A_3}$	K_1	K_1	K_1	K_1	K_1	K_1	12													

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
$\overline{A_4}$	11,	11,	11,	11,	11,	11,	4,													
$\overline{A_5}$	8,	8,	8,	8,	8,	8,	12,													
$\overline{A_6}$	H,	H,	H,	H,	H,	H,	S_2													
$\overline{A_7}$	5,	5,	5,	5,	5,	5,	R_1													
$\overline{A_8}$	6,	6,	6,	6,	6,	6,	N_1													
$\overline{A_9}$	7,	7,	7,	7,	7,	7,	J_3													
$\overline{A_{10}}$	10,	10,	10,	10,	10,	10,	15,													
$\overline{A_{11}}$	13,	13,	13,	13,	13,	13,	P_1													
A							8_3						D_1							
$\overline{ABS}$														M_1	J_1	J_1	J_1	J_1	J_1	J_1
$\overline{AB1}$														D_1	D_1	D_1	D_1	D_1	D_1	D_1
$\overline{AB2}$														5_1	5_1	5_1	5_1	5_1	5_1	5_1
$\overline{AB3}$														6_1	6_1	6_1	6_1	6_1	6_1	6_1
$\overline{AB4}$														E_1	E_1	E_1	E_1	E_1	E_1	E_1
$\overline{AB5}$														J_3	F_1	F_1	F_1	F_1	F_1	F_1
$\overline{AB6}$														L_3						
$\overline{AB7}$														M_3						
$\overline{AB8}$														15_3						

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CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
AT1							S_3					9_2		14_2						
AT2												1_2		1_2						
AT3												A_2		A_2						
AT4												2_2		2_2						
B							K_3						D_2							
b-1													A_1	A_1						
b-2													7_1	7_1						
b-4													1_1	1_1						
BI1													1_2	6_2						
BI2													C_2	5_2						
BI4													2_2	15_2						
BI8													5_2	P_1						
$\overline{BRH}$												H_3	H_3							
$\overline{BRL}$												6_3	6_3							
$\overline{CBS}$														5_3	5_3	5_3	5_3	5_3	5_3	5_3
$\overline{CG}$												R_1	R_1	R_1						

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
CH1							9_2	9_2					6_1							
CH2							14_2	14_2					8_1							
CH4							N_2	N_2					11_1							
CH8							7_2	7_2					A_2							
$\overline{CIO}$													10_2	10_2						
CL1							10_2	L_2					5_1							
CL2							H_2	H_2					H_1							
CL4							8_2	J_2					10_1							
CL8							6_2	F_2					N_1							
$\overline{CPB}$														S_2	4_3	4_3	4_3	4_3	4_3	4_3
$\overline{CTA}$												14_1	14_1							
$\overline{CS}$	P_1	P_1	P_1	P_1	P_1	P_1	12_3													
$\overline{DI}$								4_2				B_2	B_2	B_2						
$\overline{D2}$								5_2				8_2	8_2	8_2						
$\overline{D4}$								C_2				4_2	4_2	4_2						
$\overline{D8}$								B_2				3_2	3_2	3_2						
$\overline{DAST}$	R_1	R_1	R_1	R_1	R_1	R_1	R_3													

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
$\overline{DC}$												6_2	6_2							
DIN	12_1	12_1	12_1	12_1	12_1	12_1	15_3	15_3	J_3	J_3	J_3									
DI 0,4,8,12	2_3 N_2 7_2 2_2	2_3 N_2 7_2 2_2	2_3 N_2 7_2 2_2	2_3 N_2 7_2 2_2	2_3 N_2 7_2 2_2	2_3 N_2 7_2 2_2								12_3						
DI 1,5,9,13	1_3 10_2 6_2 1_2	1_3 10_2 6_2 1_2	1_3 10_2 6_2 1_2	1_3 10_2 6_2 1_2	1_3 10_2 6_2 1_2	1_3 10_2 6_2 1_2								11_3						
DI 2,6,10,14	R_2 9_2 5_2 15_1	R_2 9_2 5_2 15_1	R_2 9_2 5_2 15_1	R_2 9_2 5_2 15_1	R_2 9_2 5_2 15_1	R_2 9_2 5_2 15_1								10_3						
DI 3,7,11,15	15_2 8_2 H_2 B_2	15_2 8_2 H_2 B_2	15_2 8_2 H_2 B_2	15_2 8_2 H_2 B_2	15_2 8_2 H_2 B_2	15_2 8_2 H_2 B_2								4_3						
$\overline{DO0}$	5_0	5_3	5_3	5_3	5_3	5_3	3_3													
$\overline{DO1}$	4_3	4_3	4_3	4_3	4_3	4_3	2_3													
$\overline{DO2}$	3_3	3_3	3_3	3_3	3_3	3_3	1_3													
$\overline{DO3}$	P_2	P_2	P_2	P_2	P_2	P_2	P_2													
$\overline{DO4}$	12_2	12_2	12_2	12_2	12_2	12_2	12_2													
$\overline{DO5}$	11_2	11_2	11_2	11_2	11_2	11_2	11_2													
$\overline{DO6}$	M_2	M_2	M_2	M_2	M_2	M_2	M_2													
$\overline{DO7}$	L_2	L_2	L_2	L_2	L_2	L_2	L_2													
$\overline{DO8}$	K_2	K_2	K_2	K_2	K_2	K_2	K_2													
$\overline{DO9}$	J_2	J_2	J_2	J_2	J_2	J_2	J_2													
$\overline{DO10}$	4_2	4_2	4_2	4_2	4_2	4_2	4_2													
$\overline{DO11}$	3_2	3_2	3_2	3_2	3_2	3_2	3_2													
$\overline{DO12}$	D_2	D_2	D_2	D_2	D_2	D_2	D_2													

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
$\overline{DO13}$	C_2	C_2	C_2	C_2	C_2	C_2	C_2													
$\overline{DO14}$	A_2	A_2	A_2	A_2	A_2	A_2	A_2													
$\overline{DO15}$	S_1	S_1	S_1	S_1	S_1	S_1	S_1													
$\overline{ERG}$													10_3	9_3						
$\overline{HALT}$														3_3	K_1	K_1	K_1	K_1	K_1	K_1
$\overline{IC}$												7_2	7_2							
$\overline{IA1}$								8_3	8_3	8_3	8_3	12_3								
$\overline{IA2}$								L_3	L_3	L_3	L_3	N_3								
$\overline{IA4}$								K_3	K_3	K_3	K_3	11_3								
$\overline{IA8}$								N_3	N_3	N_3	N_3	E_3								
$\overline{IB1}$								M_3	M_3	M_3	M_3	M_3								
$\overline{IB2}$								11_3	11_3	11_3	11_3	10_3								
$\overline{IB4}$								9_3	9_3	9_3	9_3	L_3								
$\overline{IB8}$								12_3	12_3	12_3	12_3	S_3								
$\overline{IC1}$								10_3	10_3	10_3	10_3	9_3								
$\overline{IC2}$								3_2	3_2	3_2	3_2	K_3								
$\overline{IC4}$								2_2	2_2	2_2	2_2	J_3								
$\overline{IC8}$								1_2	1_2	1_2	1_2	7_3								
$\overline{ID1}$								6_3	6_3	6_3	6_3	P_3								

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
$\overline{ID2}$								C_3				4_3								
$\overline{ID4}$								P_2				C_3								
$\overline{ID8}$								F_3				15_3								
$\overline{IBS}$														S_3	1_3	1_3	1_3	1_3	1_3	1_3
$\overline{IB1}$														J_2	15_1	15_1	15_1	15_1	15_1	15_1
$\overline{IB2}$														9_2	S_1	S_1	S_1	S_1	S_1	S_1
$\overline{IB3}$														13_2	14_1	14_1	14_1	14_1	14_1	14_1
$\overline{IB4}$														7_2	R_1	R_1	R_1	R_1	R_1	R_1
$\overline{IB5}$														M_2	N_1	N_1	N_1	N_1	N_1	N_1
$\overline{IB6}$														E_2	P_1	P_1	P_1	P_1	P_1	P_1
$\overline{IB7}$														K_2	L_1	L_1	L_1	L_1	L_1	L_1
$\overline{IB8}$														C_2	M_1	M_1	M_1	M_1	M_1	M_1
$\overline{IB9}$														N_1	2_3	2_3	2_3	2_3	2_3	2_3
L0									C_3	C_3	C_3									
L1									3_3	3_3	3_3									
L2									2_3	2_3	2_3									
L3									F_3	F_3	F_3									
L4									P_1	P_1	P_1									

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
L5									13_1	13_1	13_1									
L6									S_1	S_1	S_1									
L7									A_2	A_2	A_2									
L8									12_1	12_1	12_1									
L9									8_1	8_1	8_1									
L10									9_1	9_1	9_1									
L11									L_1	L_1	L_1									
L12									13_2	13_2	13_2									
L13									14_2	14_2	14_2									
L14									12_2	12_2	12_2									
L15									S_2	S_2	S_2									
L16									4_2	4_2	4_2									
L17									5_2	5_2	5_2									
L18									7_2	7_2	7_2									
L19									9_2	9_2	9_2									
$\overline{\text{MER}}$							11_3					5_3	2_3	2_3						
$\overline{\text{MERO}}$							F_3					D_2		D_2						
MNC														14_1						
MNO														13_1						
$\overline{\text{MOT}}$							6_3						14_2							

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
$\overline{MS1}$						14_1	E_3													
$\overline{MS2}$					14_1		D_3													
$\overline{MS3}$				14_1			4_3													
$\overline{MS4}$			14_1				14_1													
$\overline{MTF}$							L_3						13_2							
$\overline{MXS}$							M_3						5_3							
$\overline{OBS}$														L_1	H_1	H_1	H_1	H_1	H_1	H_1
$\overline{OB1}$								12_2						A_3	A_3	A_3	A_3	A_3	A_3	A_3
$\overline{OB2}$								D_2						B_3	B_3	B_3	B_3	B_3	B_3	B_3
$\overline{OB3}$								E_2						C_3	C_3	C_3	C_3	C_3	C_3	C_3
$\overline{OB4}$								13_2						D_3	D_3	D_3	D_3	D_3	D_3	D_3
$\overline{OB5}$								4_1						7_3	J_3	J_3	J_3	J_3	J_3	J_3
$\overline{OB6}$								D_3						H_3	H_3	H_3	H_3	H_3	H_3	H_3
$\overline{OB7}$								3_3						F_3	F_3	F_3	F_3	F_3	F_3	F_3
$\overline{OB8}$								E_3						E_3	E_3	E_3	E_3	E_3	E_3	E_3
1																				
PCG													L_2	L_2						
PNC														9_1						
PNO														10_1						

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
$\overline{P_{RMS}}$														11_2	3_3	3_3	3_3	3_3	3_3	3_3
$\overline{Q_1}$	B_3	B_3	B_3	B_3	B_3	B_3	A_3													
$\overline{Q_2}$	C_3	C_3	C_3	C_3	C_3	C_3	B_3													
$\overline{RESET}$	A_3	A_3	A_3	A_3	A_3	A_3	5_3													
$\overline{RB}$														K_3	K_3	K_3	K_3	K_3	K_3	K_3
$\overline{RTT}$												F_3		12_1						
$\overline{REF}$	N_1	N_1	N_1	N_1	N_1	N_1	9_3													
R_0								4_3	4_3	4_3	4_3	12_2	12_2	12_2						
R1								5_3	5_3	5_3	5_3	1_3	1_3	1_3						
R2								7_3	7_3	7_3	7_3	10_2	K_2	R_2						
R3								H_3	H_3	H_3	H_3	M_2	M_2	N_2						
R4								14_1	14_1	14_1	14_1	15_2	15_2	P_3						
R5								R_1	R_1	R_1	R_1	B_3	B_3	6_3						
R6								15_1	15_1	15_1	15_1	H_2	H_2	H_2						
R7								K_1	K_1	K_1	K_1	P_2	P_2	P_2						
R8							1_1	10_1	10_1	10_1	10_1	14_2								
R9							2_1	11_1	11_1	11_1	11_1	2_3								
R10								M_1	M_1	M_1	M_1	J_2	J_2							
R11								N_1	N_1	N_1	N_1	N_2	11_2							

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
R12								R_2	R_2	R_2	R_2	S_2	S_2							
R13								15_2	15_2	15_2	15_2	3_3	3_3							
R14								A_3	A_3	A_3	A_3	F_2	F_2	F_2						
R15								13	13	13	13	R_2	R_2							
R16								6_2	6_2	6_2	6_2		9_3							
R17								8_2	8_2	8_2	8_2		F_3							
R18								10_2	10_2	10_2	10_2		M_3							
R19							A_1	11_2	11_2	11_2	11_2		C_3							
$\overline{REL}$	M_1	M_1	M_1	M_1	M_1	M_1	N_3													
$\overline{SB}$												C_2	12_3							
$\overline{SR}$												E_2	E_2							
$\overline{STIT}$													J_3	8_3						
STI-0								2_3					N_3	N_3						
STI-3							10_3	S_3						3_1						
ST3-3							3_1	D_1						2_1						
TFF							15_2	S_2												
$\overline{TIP}$												S_1	S_1							
$\overline{TMP}$												P_1	P_1							
$\overline{TPI}$												N_1	N_2							

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
$\overline{TRAP}$												15_1	15_1	15_1						
TRP-1												13_2								
TRP-2												A_3								
TRP-4												L_2								
TRP-8												11_2								
$\overline{UDC}$							H_3					5_2								
$\overline{WW}$												12_1	12_1							
$\overline{WTEN\ 1}$	14_2	14_2	14_2	14_2	14_2	14_2	R_2													
$\overline{WTEN\ 2}$	13_2	13_2	13_2	13_2	13_2	13_2	13_2													
$\overline{WTEN\ 3}$	E_2	E_2	E_2	E_2	E_2	E_2	E_2													
$\overline{WTEN\ 4}$	F_2	F_2	F_2	F_2	F_2	F_2	F_2													
$\overline{STEP}$							C_3	B_3												

CARD LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Signals	8 - Bit ROM's		8 - Bit RAMS 6307				Mem-C 6308	TEST	20 - Bit ROM's (6321)			Regs. (6309)	ALU 6310	I/O Con 6311	I/O COMMON BUS					
+5VR Logic							B_1 14_3					2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3
+5VR MEM	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3			2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3	2_1 B_1 14_3 R_3									
+8VR	E_1	E_1	E_1	E_1	E_1	E_1														
+12VR															S_3 15_3	S_3 15_3	S_3 15_3	S_3 15_3	S_3 15_3	S_3 15_3
-12VR							D_1		A_1 1_1	A_1 1_1	A_1 1_1				N_3 12_3	N_3 12_3	N_3 12_3	N_3 12_3	N_3 12_3	N_3 12_3
+15VR																				
-15VR	A_1 1_1 S_3 15_3	A_1 1_1 S_3 15_3	A_1 1_1 S_3 15_3	A_1 1_1 S_3 15_3	A_1 1_1 S_3 15_3	A_1 1_1 S_3 15_3														
± 0	C_1 3_1 D_1 4_1	C_1 3_1 D_1 4_1	C_1 3_1 D_1 4_1	C_1 3_1 D_1 4_1	C_1 3_1 D_1 4_1	C_1 3_1 D_1 4_1	C_1	C_1 3_1	C_1 3_1	C_1 3_1	C_1 3_1	C_1 3_1	C_1 3_1	C_1	C_1 3_1	C_1 3_1	C_1 3_1	C_1 3_1	C_1 3_1	C_1 3_1
± 0	P_3 13_3 N_3 12_3	P_3 13_3 N_3 12_3	P_3 13_3 N_3 12_3	P_3 13_3 N_3 12_3	P_3 13_3 N_3 12_3	P_3 13_3 N_3 12_3	P_3 13_3	P_3 13_3	P_3 13_3	P_3 13_3	P_3 13_3	P_3 13_3	P_3 13_3	13_3	P_3 13_3	P_3 13_3	P_3 13_3	P_3 13_3	P_3 13_3	P_3 12_3
± 0	M_3 11_3 L_3 10_3 K_3 9_3	M_3 11_3 L_3 10_3 K_3 9_3	M_3 11_3 L_3 10_3 K_3 9_3	M_3 11_3 L_3 10_3 K_3 9_3	M_3 11_3 L_3 10_3 K_3 9_3	M_3 11_3 L_3 10_3 K_3 9_3														
+9VU															A_1 1_1	A_1 1_1	A_1 1_1	A_1 1_1	A_1 1_1	A_1 1_1
+15VU															9_3	9_3	9_3	9_3	9_3	9_3
-15VU															10_3	10_3	10_3	10_3	10_3	10_3
CHASSIS GND.															M_3 11_3	M_3 11_3	M_3 11_3	M_3 11_3	M_3 11_3	M_3 11_3