2336 DW

BASIC THEORY OF OPERATIONS

HM-69

Peter LaFauci
March 31, 1983

PL/lg
0019y

TABLE OF CONTENTS

1. THE Z80 CPU

Clock Frequency - 2.175 MHZ; T cycle - 460 ns

Interrupts - Vectored (Z80 mode 2)
- Priority

1. Receiver Ready
2. Transmitter Ready
3. CTC CH 2
4. CTC CH 3
5. Keyboard Character Available
6. Printer Acknowledge

2. MEMORY

Workstation main memory is divided into three basic sections:

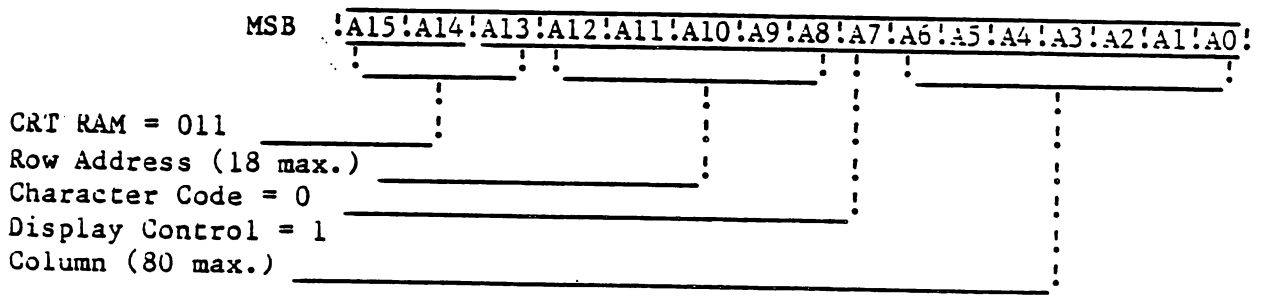
PROM, 8K bytes
RAM, 2K bytes
CRT RAM, 4K bytes

CRT RAM is further divided into two sections:

Character Code (2K bytes)
Display & Forms Control (2K bytes)

CRT RAM is addressed by the Z80 as two separate sections, but when operating with the CRT display it is merged into one section of 2K words by 16 bits.

The CRT RAM is mapped to the display screen, i.e., a character is addressed according to its row and column position on the display screen. Address assignment is as follows:



Memory Address Table

Function	From	TO	Bytes	(MSB)A15	A14	A13	A12	A11	A10	A7
PROM	0000	1FFF	8K	0	0	0	X	X	X	X
RAM	4000	47FF	2K	0	1	0	X	X	X	X
CRT Character RAM	6X00	7X4F	2K*	0	1	1	X	X	X	0
CRT Display Control RAM	6X80	7X6F	2K*	0	1	1	X	X	X	1

X = '0' or '1' as appropriate

* Character Row & Column Addresses are mapped into 2K bytes. Memory addressing is organized as even pages (128 bytes/page) for the Character Code rows, and the odd pages for the Display Control rows.

3. CRT CONTROL

This section controls the presentation of video data, stored in CRT RAM, to the CRT Monitor. The RAM is organized as 2K words of 16 bits.

The lower byte is the CRT character code portion and has the following bit assignment:

MSB D7 D6 D5 D4 D3 D2 D1 D0 LSB

Underscore/Upper PROM ____
Character Code _____

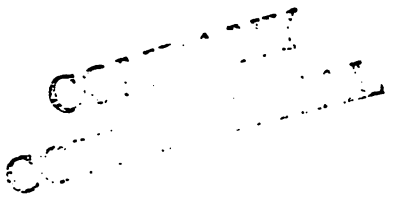
Note: The D7 bit will normally cause the character to be displayed with an underline. If a jumper is loaded on the board this bit will select the upper character set PROM.

The upper byte is the CRT Display & Forms Control portion and has the following bit assignments:

MSB D7 D6 D5 D4 D3 D2 D1 D0

Character Set Graphics ____
Inverse Video _____
Blink _____
HI Intensity _____
Upper Character Set _____

Left Horizontal _____
Vertical Line _____
Right Horizontal Line _____



Note: The 25th line on the display can only display a left and/or right horizontal line, no character can be displayed.

Underscore is used to underline a character; it should not be used as part of the box graphics.

Upper Character Set is used to indicate that the character code should be decoded as the upper 128 character set. This set is optional and is used for special characters and/or extended box graphics.

Note: Character Set Graphics is used to indicate to the hardware that the displayed character is graphic and it must fill in the dots between characters.

The heart of the CRT Control Circuitry is the CRT Video Time-Controller (VTAC) integrated circuit. The VTAC contains the major portion of the logic required to generate the timing signals necessary to present video data on the CRT monitor.

The VTAC must, however, be initialized after power on and before anything is displayed. The following output commands must be executed to initialize the VTAC:

I/O Address	Output Data (Hex)	Function
'40'	'63'	Horizontal Character Count (=100)
'41'	'26'	Mode (non-interlaced) Hor. Sync Width (=4) Hor. Sync Delay (=6)
'42'	'55'	Scans/Data Row (=11) (1) Character/Data Row (=80)
'43'	'97'	Skew bits (=1) Data/Row Frame (=24) (3
'44'	'11'	Scans/Frame (=290) (2)
'45'	'19'	Vertical Data Start (=25)
'46'	'17'	Last Displayed Data Row (=24) (3)

Note: All the above parameters can be changed at any time during operation. To insure a 'clean' display, a 'blank screen' command (see next paragraph) should first be executed.

1. Output Data = '5D' for 50 HZ operation (Scans/Data Row = 12)
2. Output Data = '2B' for 50 HZ operation (Scans/Frame = 342)
3. When 25 lines are required, I/O address '43' should have a date value of 98 and address '46' a value of 18.

The VTAC provides the following I/O Commands:

Address	CPU I/O	Function	
'48'	Input	Read Cursor Row Address	Cursor address is placed on Data bus LSB justified
'49'	Input	Read Cursor Column Address	
'4A'	Output	Blank Screen Reset VTAC	
'4B'	Output	Up Scroll (see next paragraph)	
'4C'	Output	Load Cursor Column Address	Cursor address is read from Data Bus LSB justified
'4D'	Output	Load Cursor Row Address	
'4E'	Output	Unblank Screen	

Scrolling without the need to shift the entire CRT RAM is provided by the 'Up Scroll' and 'Last Displayed Data Row' commands. When scrolling, software must maintain a last displayed data row count as a memory pointer. Upward scrolling is accomplished by issuing an 'up scroll' command, or loading the incremented data row count, then changing the data of the last displayed data row. When downward scrolling, the decremented data row count is loaded, then the previous last displayed data row data is changed. The data row count must be modulo 24 when using this scrolling method. Therefore, the horizontal line graphics in the 25th row cannot be used.

4. COMMUNICATIONS

The workstation communicates with the MVP CPU via the standard 2236 async protocol. The terminal may be located up to 2000 ft. away from the MXD terminal controller. The data is transferred to the UART chip via an OUT '7X' (the low value address lines do not play a role in the chip select). The incoming data is input from the UART chip via an IN '7X'. The UART chip supplies the Z80 CPU with the following status information:

STATUS	LOCATION	ACTIVE
TRANSMITTER REGISTER EMPTY	STATUS REG D4	1
UART ERROR (Framing, parity, or overrun)	STATUS REG D0	0
RECEIVER READY	STATUS REG D5	0
TRANSMITTER BUFFER READY	STATUS REG D7	0

Receiver ready and transmitter buffer ready also go to channels 0 and 1 of the CTC so that they can cause interrupts when they become active (both go active low.)

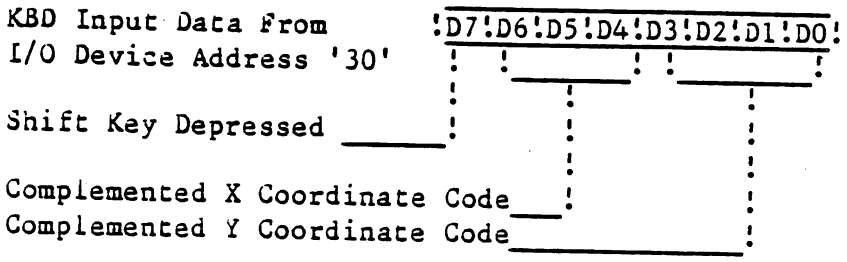
There is a five switch, switch bank that also provides control to the communications logic. The low order three switches determine the baud rate selected (they are status bits D3, D2, and D1.) The fourth switch selects the word length (0 indicates seven data bits, 1 indicates eight data bits), the switch is readable as bit D5 of the PIO channel B. The fifth switch controls even or odd parity (on is odd parity, off is even).

The request to send signal is equal to the value in bit D7 of the PIO channel B, also the PIO channel B bit D4 is used to enable or disable parity checking/generation at the UART (1 enables parity.)

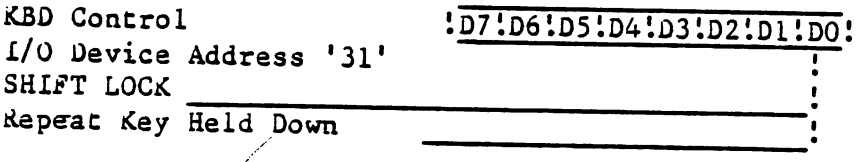
5. KEYBOARD

Keyboard data is input thru the Z80-PIO chip port A; I/O device address '30'.

The key code is presented in complemented binary coded X and Y coordinates as follows;



Keyboard control is handled thru the I/O Control Port (Z80-PIO port B), I/O device address '31', as follows:



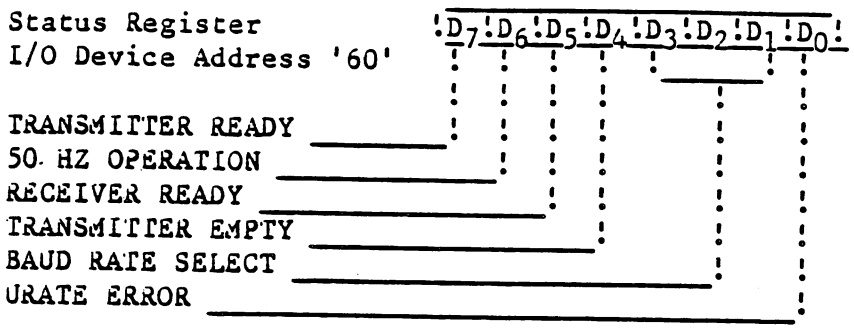
Repeat Key held down indicates an auto repeat key is depressed. Keyboard clicker is activated by OUT '2X' with D0 on.

Repeat key timing is controlled by the Z80-CTC channel 3, I/O device address '13'.

When a repeat key is detected, a time constant of 19 is loaded (304 ms, each interval = 16 ms). CTC Channel 3 is set to counter mode (negative edge decrement, interrupt vector already loaded). When the interrupt occurs, the 'Repeat Key held Down' input bit is tested, and if '1' the KeyCode is read from port A again. The time constant is now set to 8 (128 ms) for each successive character until the 'Repeat Key Held Down' input bit is returned to '0'.

6. STATUS REGISTER

The status register, I/O device address '60' is used to detect the following workstation status bits:



D7 will be zero if the transmitter buffer is empty and the data set is ready and the clear to send signal at the modem interface is active.

D6 will be zero if the unit is to operate at 50 HZ.

D5 will be zero if the receiver buffer is full.

D4 will be one if the transmitter register is empty.

D3-D1 will represent the baud rate selected by the baud rate switches. The following table describes their meaning.

D3 C	D2 B	D1 A	Baud Rate
0	0	0	300
0	0	1	600
0	1	0	1200
0	1	1	2400
1	0	0	4800
1	0	1	9600
1	1	0	19200
1	1	1	[19200] Burn In Self Test Position

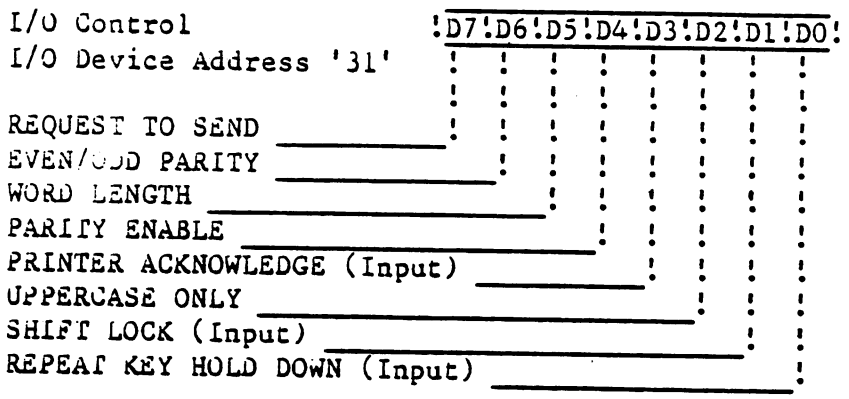
D0 will be zero if there is an UART error (parity error, overrun error, or framing error).

7. ERROR ALARM

The error alarm is activated by OUT '2X' with D1 on.

8. I/O CONTROL

This section reviews the bit assignments presented in previous sections for the I/O Control Port (Z80-PIO port B), I/O device address '31'.



Note: D5 will be a one if 8-bit data is selected, a zero for 7 bit data.
D6 will be a one if even parity is selected.

Before I/O operations can begin, PIO port B must be initialized. The following information is output to the port B control, address '33'.

Set interrupt vector
Set mode to control (mode 3)
Set bits D7 and D4 to outputs and set D6, D5, D3, D2, and D0 to inputs.
Set for high state interrupt (Interrupt Control Word)
Set Interrupt Mask to allow the Printer Acknowledge interrupt (bit D3 = '0', all others = '1').

9. PRINTER

Print data is output to a 1 byte buffer register, I/O device address '50'. Each time a byte is loaded, the hardware generates a data strobe to the printer.

Printer Acknowledge is returned from the printer each time it receives a character. The I/O control port (Z80-PIO port B) detects the acknowledge and generates a vectored interrupt (see section 10).

10. CONTROLS REGISTER

There is one control register that is used to control some terminal I/O functions. The register is write only and its bit meanings are described below.

BIT	MEANING
D0	Sound the Keyboard Clicker
D1	Sound the Audio Alarm
D2	Stop Cursor from Blinking
D3	Start Cursor Blinking
D4	Allow CRT Writes Only on Horizontal Retrace
D5	Allow CRT Writes at any Time

The data value is entered into the control register by an OUT '2X'.

I/O Address Table

FUNCTION	DEVICE	HEX ADDRESS (MSBA7-LSBA0)
Receiver Ready	Z80-CTC Channel 0	'10'
Transmitter Ready	Z80-CTC Channel 1	'11'
Counter/Timer	Z80-CTC Channel 2	'12'
Counter/Timer	Z80-CTC Channel 3	'13'
Control Register	Special I/O	'2X'
I/O Control	Z80-PIO Data Port B	'31'
	Z80-PIO Port Control Port B	'33'
Keyboard Data	Z80-PIO Data Port A	'30'
	Z80-PIO Port Control Port A	'32'
CRT Control	VTAC	'4X'
Printer Data	Output Register	'50'
Status	Input Register	'60'

2200 Terminal Protocol -

Terminal sends FE every 5 secs to CPU.
Terminal and Slave (204) Printer sends FBF9 every 5secs to CPU

Terminal sends FA as flow control Stop, F8 to resume
Terminal sends FB as flow control Stop w/Slave Prt, F9 to resume.

Reset = DC2 or Hex 12

SF'0 = FD 00
SF'1 = FD 01
SF'2 = FD 02
SF'3 = FD 03
SF'4 = FD 04
5 FD 05
6 FD 06
7 FD 07
8 FD 03
9 FD 09
10 FD 0A
11 FD 0B
12 FD 0C
13 FD 0D
14 FD 0E
15 FD 0F
16 FD 10
17 FD 11
18 FD 12
19 FD 13
20 FD 14
21 FD 15
22 FD 16
23 FD 17
24 FD 18
25 FD 19
26 FD 1A
27 FD 1B
28 FD 1C
29 FD 1D
30 FD 1E
31 FD 1F

Erase = E5
CPU gives us 05 in return

Edit = BD
CPU gives FB FC or FB F8 in return

Halt = 13

Clear = FD81

Load = FDA1

Run = FD82

Continue = FD84

FN = FD7E