THIS ISN REPLACES ISN 179.

This ISN presents additional information concerning the boards in the 2236 MXD system (7290-1, 7291, 7292-1). Section 1 is a reprint of ISN 179 with additions pertaining strictly to ISN #179. Section 2 explains the ECN's that are applicable to each of the three boards.

SECTION 1. ISN #179

Recently, hardware changes were made to the 210-7290-1 and 210-7292-1 boards which allow the 2236 MXD system to operate at a baud rate of 19.2K only when both changes are incorporated. This ISN will explain the changes to both boards, in order that existing 2236 MXD systems may by converted to 19.2K baud. Read this ISN completely before making any changes.

1. 210-7290-1 (ECN 9447)
   A. Isolate L19 pin 11 from the etch that connects it to the baud rate switches.
   B. Tie L19 pin 13 to the etch that was connected to L19 pin 11.
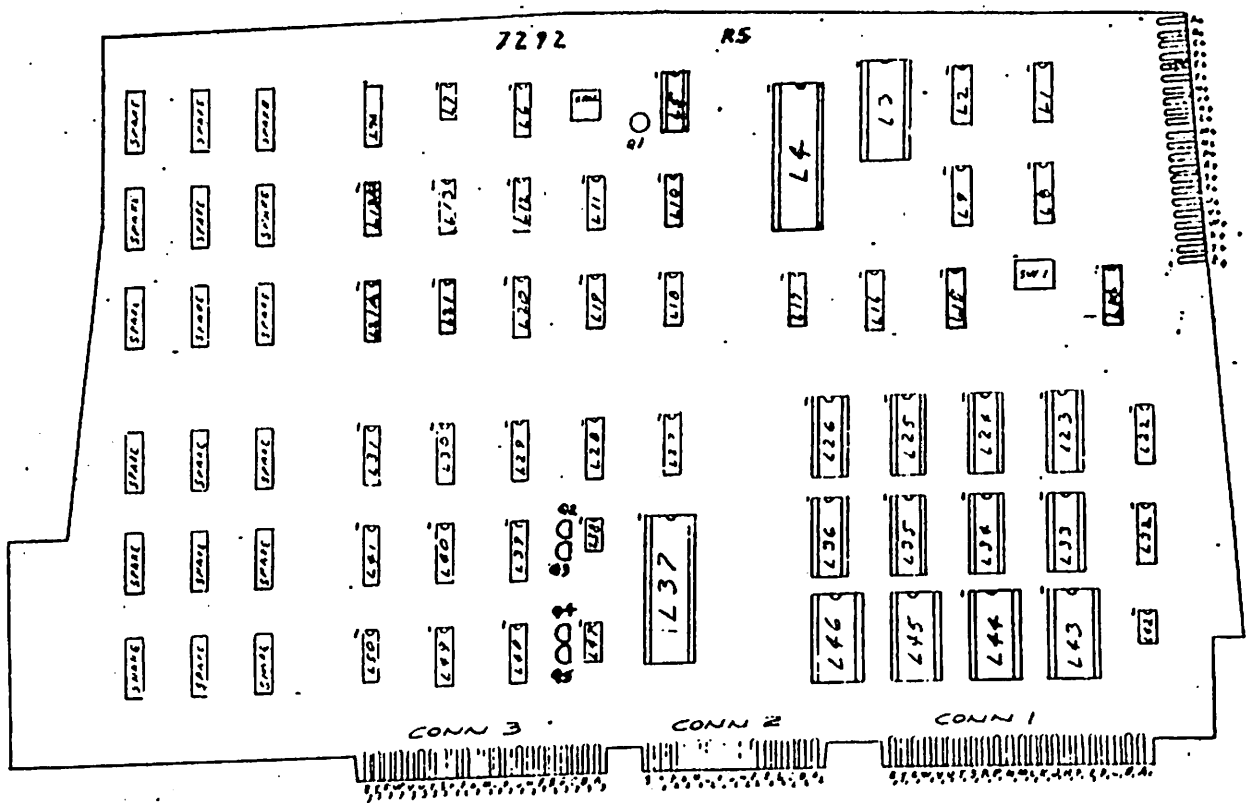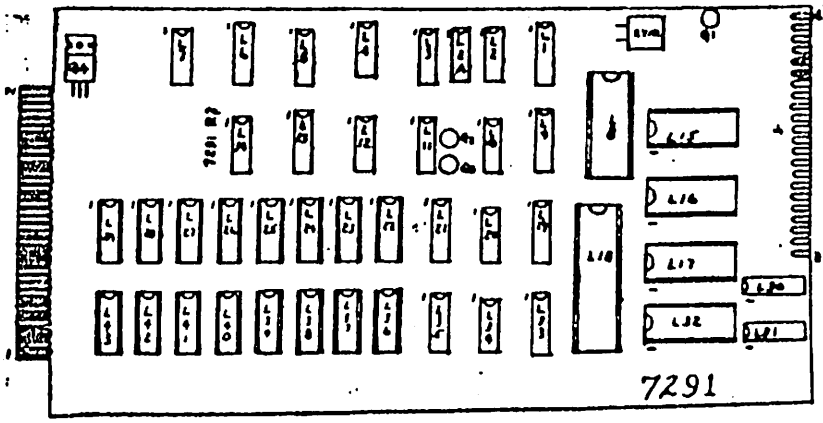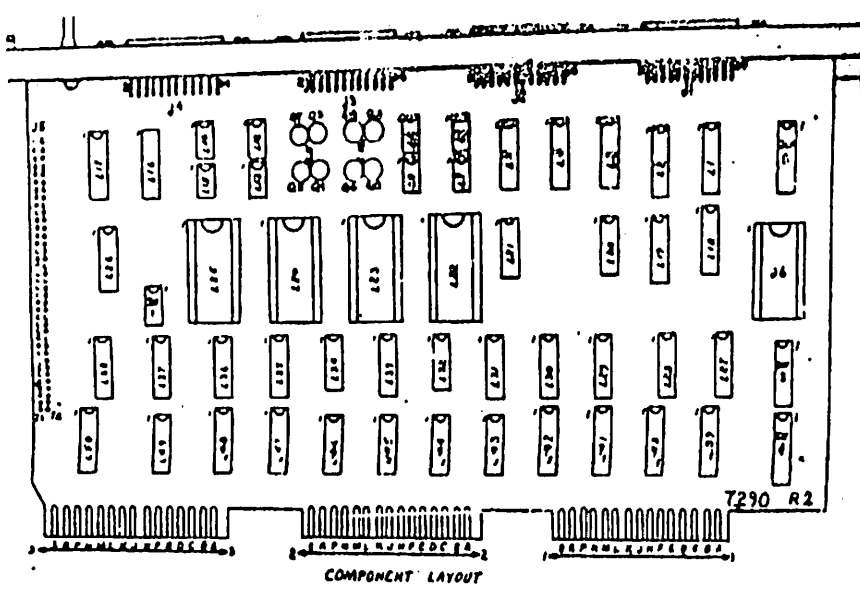   C. Change E-REV from 0 to 1.
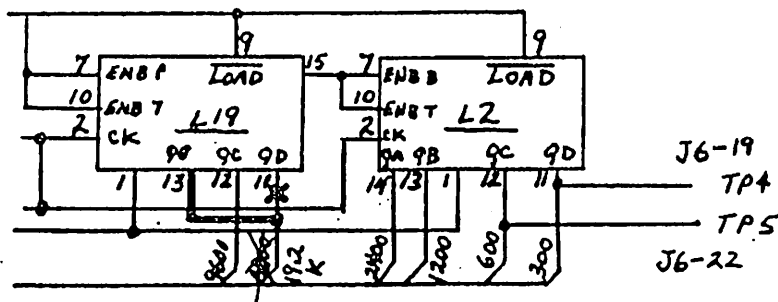
COMPONENT LAYOUT

7290 R2

7291

7292 R5

CONN 3   CONN 2   CONN 1

2

NOTE:

    1.   This prevents the controller from operating
        at 4800 baud.

    2.   On new production boards a jumper has been
        installed between L18 and L19 to facilitate
        the change from 4800 to 19.2K or vice versa.
        The three plate-throughs for the jumper are
        layed out vertically with the common point
        in the center. The top plate-through is for
        19.2K and the bottom for 4800.

    3.   Since 19.2K takes the place of 4800, the baud
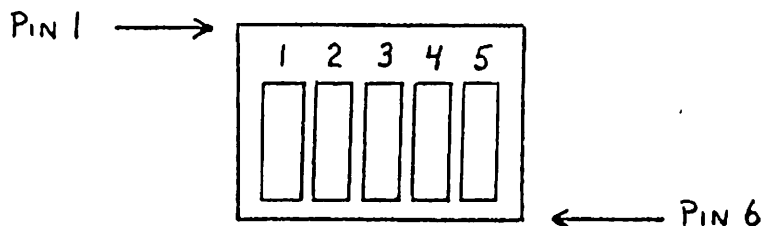   rate switches must be set for 4800 to allow
        19.2K operation.

2.   210-7292-1 (ECN 9210)

    A.   Cut etch connecting L12 pin 9 to L11 pin 11.
    B.   Add the circuitry shown below, using a 7451 I.C. (376-0012).
    C.   Change E-REV from 3 to 4.
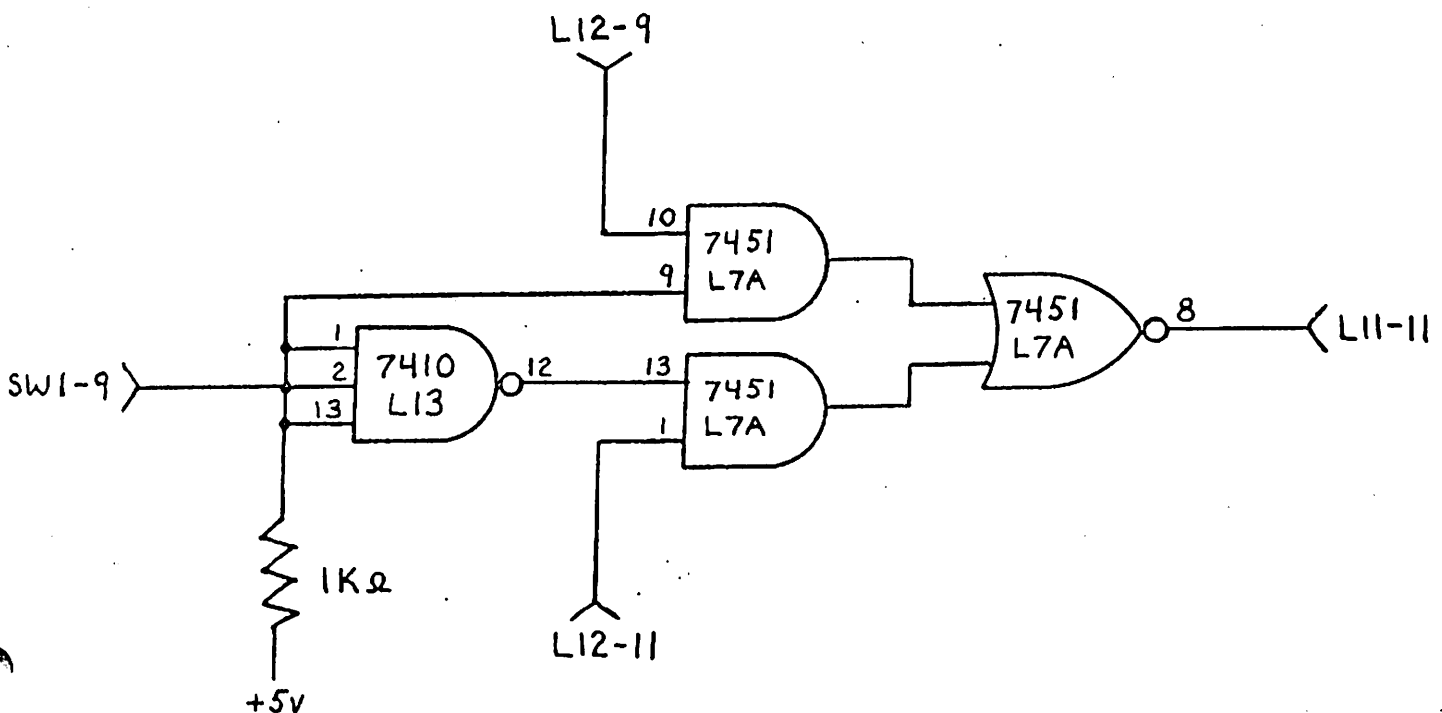
NOTE:

1. If location 7A is occupied by a 74175, return the board to the Home Office.

2. The square plate through designating pin 1 of SW 1 is actually pin 6.

PIN 1 ⟶

| 1 2 3 4 5 |

⟵ PIN 6

SW 1 pin labeling on old schematics is wrong.

3. If pin 9 of SW 1 is occupied by Parity Inhibit (PI), move the wire that is connected to SW 1 pin 9 to SW 1 pin 10. With Parity Inhibit tied to pin 10 of SW1, the board will conform to the new schematics.

4. For 19.2K baud, the switch (SW1) must be set as follows:

SWITCH #	STATE
1	ON (to allow parity errors)
2	ON
3	ON
4	OFF
5	ON

A.   210-7290-1, E-REV 1

ECN #9447, which enables the 7290-1 to operate at 19.2K
baud, is the only ECN applicable to the board.

B.   210-7292-1, E-REV 4

ECN #8056, E-REV 0

This ECN modifies the 7292 to create a 7292-1 board.

ECN #8056A, E-REV 1

1.   Disconnect the collector of transistors Q2, Q3, Q4
     and Q5 from +12V.

2.   Tie each collector of Q2-Q5 to +12V through a 120
     ohm 1/2W resistor (331-2012).

3.   Change the E REV level from 0 to 1.

NOTE:

This change was actually part of ECN #8056,
but production sample boards did not have
the resistors on it; therefore, some boards
were released without resistors. When the
resistors are installed on the board, increment
the E REV level to 1.

ECN #8232, E-REV 2

1.   Insert a 74175 (WLI #376-0119) into location L21A.
     Pin 1 should be located toward the top of the
     board. Connect pin 8 to +0V and pin 16 to +5V.

2.   JUMPER   From   To

|	From	To
	L5-6	L10-11
	L4-19	L13A-1
	L10-10	L13A-2
	L13A-3	L21A-9
	L21A-1	L21-4
	L21A-3	Conn. 7_4
	L21A-6	Conn. L_4
	L21A-11	Conn. N_4
	L4-9	L21A-4
	L4-3	L21A-5
	L4-5	L21A-12

3.   Add a 1K resistor (330-3010) from L21A-1 to +5V.

4.   Increment the E REV level from 1 to 2.

NOTE:.

1.   Some boards may have this ECN
     incorporated, but with the 74175
     located at L7A. If this is
     the case, the board should be
     returned to the Home Office.

2.   Change Module Repair Guide No. 3.1
     to coincide with the description of
   ECN #8232 as stated above.
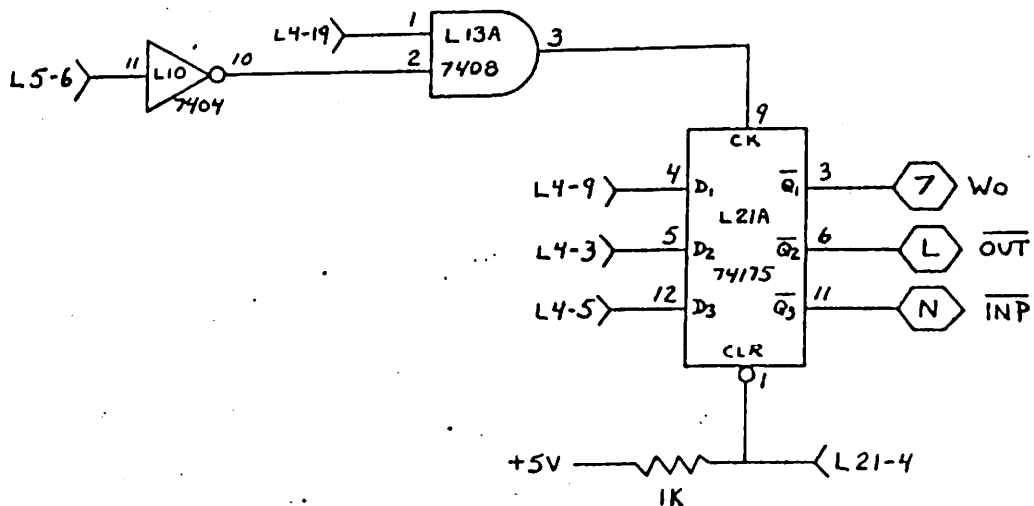
1. Remove the wire connecting L15 pin 9 to L14 pin 5.

2. Remove the wire connecting L15 pin 10 to switch 1 pin 9 (Switch #2).

3. Remove the 1K resistor connected between switch 1 pin 9 and +5V (switch #2).

NOTE:

When this ECN was performed in production, switch #1 of switch bank 1 (pins 1 and 10) was the Parity Inhibit line for the UART. At some unspecified time, production decided to attach the Parity Inhibit line to the now vacant switch #2 (steps 1-3 above). Ensure that the Parity Inhibit line (L31-35) is attached to pin 10 of switch bank 1 (SW. #1). SW. #2 is to be used for 19.2K baud selection in ECN #9210.

4. Cut the etch between L6-6 and L12-3.

Add the following circuity:

L6-6 >———1 [L 13A 7408] 3 ———< L12-3
L5-5 >———2
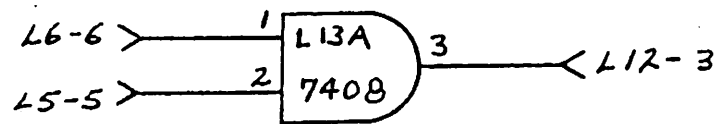
5. Change the E REV level to 3.

BULLETIN

(WANG) LABORATORIES, INC.

DATE: 3/27/79   ADMINISTRATIVE _____   TECHNICAL X   NUMBER 75

ORIGINATOR: Bill Melvin   REVIEWED BY: James Dean _____   _____

DISTRIBUTION: ATS X   DTS X   DM _____   ATOM X'

ALL OFFICES X   HOME OFFICE X   EACH EMPLOYEE _____

SUBJECT: 2236MXD (210-7292-1 ECN 9210)
REF. ISN #179A _____   PAGE 1 OF 2

Recently it has been determined that a few 210-7292-1 PCB's presently released to the field from the Home Office have been updated incorrectly. Referring to ISN #179A – Section 1 and Figure A below, the error involves ECN #9210 and is as follows:

The wire connected from L12 pin 9 may be found connected to L7A pin 1. This wire should be connected to L7A pin 10.

Similarly, the wire connected from L12 pin 11 may be connected to L7A pin 10. This wire should be connected to L7A pin 1.

As per ISN #179A and Figure A below, the following remains valid:

L12 pin 9 is connected to L7A pin 10

L12 pin 11 is connected to L7A pin 1
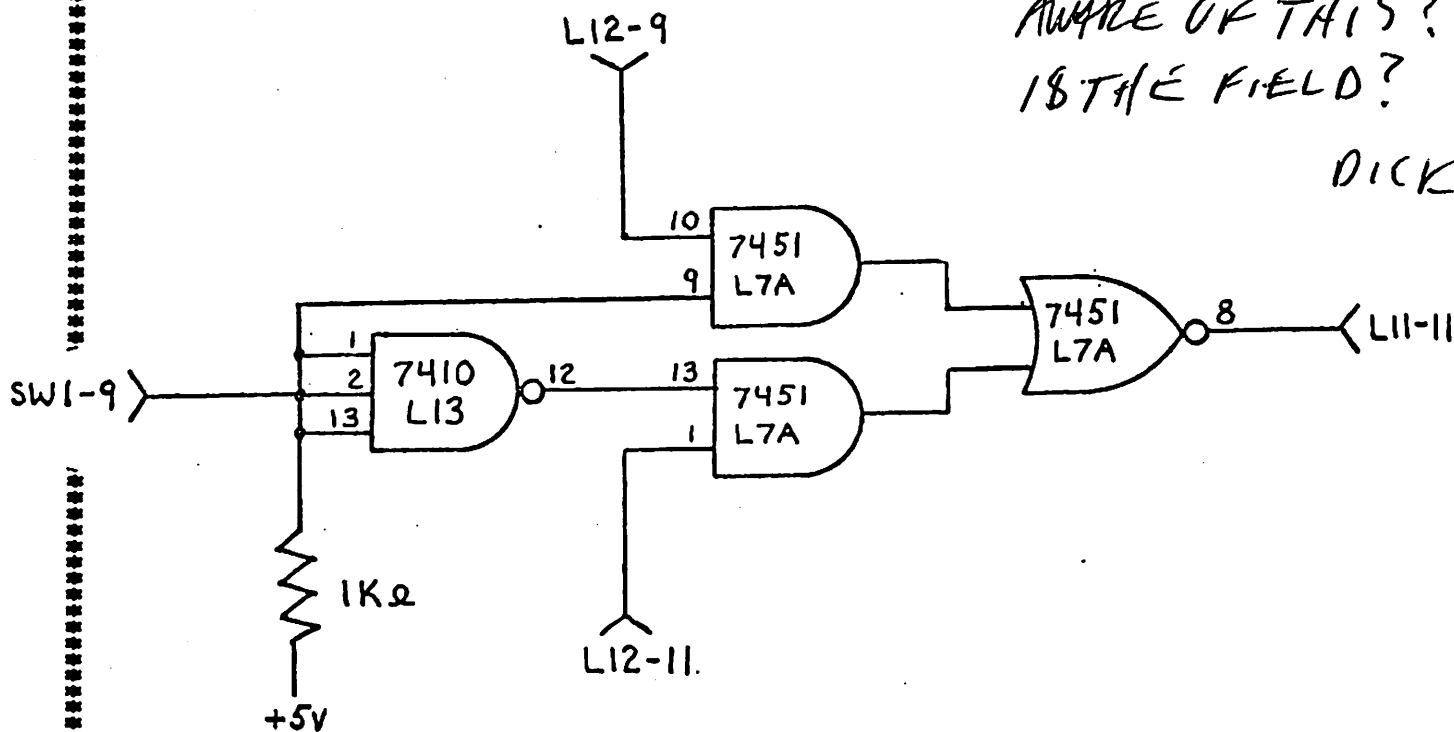
KEITH,
'WERE YOU AWARE OF THIS?
IS THE FIELD?
DICK

Figure A: Added Circuitry of ECN 9210 for the 210-7292-1

With this wiring error, a baud rate of 19.2K cannot be obtained as illustrated by the SW 1 switch settings in Note 4, Section 1 of ISN #179A. Therefore, it is important that this ECN be checked when installing a 7292-1 PCB from the Home Office. This error is only applicable to those 7292-1 PCB's with an E-REV of four (4) or greater.

It should be noted that the documentation of ISN #179A IS CORRECT.