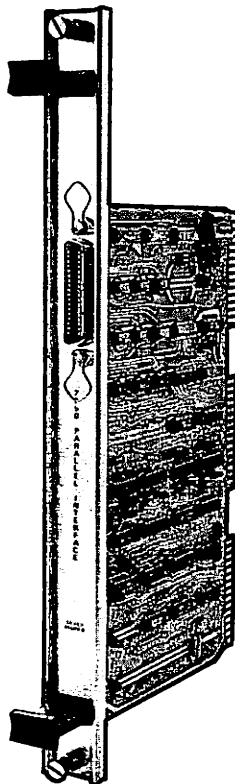


EDITED BY CUSTOMER ENGINEERING DIVISION

## MODEL 2250 INPUT/OUTPUT INTERFACE



THIS BULLETIN DESCRIBES THE FUNCTIONS OF THE 2250, AS USED WITH THE 2200B SYSTEM. (NO GENERAL I/O). USE OF THE 2250 IN A 2200B SYSTEM *WITH* THE GENERAL I/O OPTION WILL BE DOCUMENTED IN A SEPARATE PUBLICATION

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MODEL 2250  
(6394 PC)  
PARALLEL INPUT/OUTPUT INTERFACE

TABLE OF CONTENTS

1. DESCRIPTION	3
1.1 General	3
1.2 2250 Input/Output Connector Pin Diagram	5
1.3 I/O Connector Signals	6
1.4 Code Format	9
1.5 Address Switch	9
2. INSTALLATION	9
3. OPERATIONS	10
3.1 Overall I/O Sequence	10
3.2 2250 Enable Logic	10
3.3 Input/Output Selection	10
3.4 Input Operations	11
3.5 Signal Sequence	12
3.5.1 Standard INPUT Statement (2200A, 2200B)	12
3.5.2 DATALOAD BT Statement (2200B)	13
3.5.3 KEYIN Statement (2200B)	15
3.6 General Output Characteristic	16
3.6.1 Normal Output Sequence	17
3.6.2 Acknowledged Output Sequence For Longer Output Strobes (Assuming DORB On Pin 28 Tied To RBI On Pin 19)	19
4. 2250 CIRCUIT DESCRIPTION	19
4.1 Reset/Enable Circuitry	19
4.2 Address Circuitry	20
4.3 Character Input	22
4.3.1 INPUT Statement Circuit Action	22
4.3.2 DATALOAD BT/DATALOAD BTR Statements Circuit Action	26
4.3.3 KEYIN Statement Circuit Action	27
4.3.4 Use Of The End I Bit	28
4.4 Character Output	29
5. 2250 DIAGNOSTIC TEST	33
6. APPENDIX A - TROUBLESHOOTING	36
7. APPENDIX B - INTERFACE WIRING	39

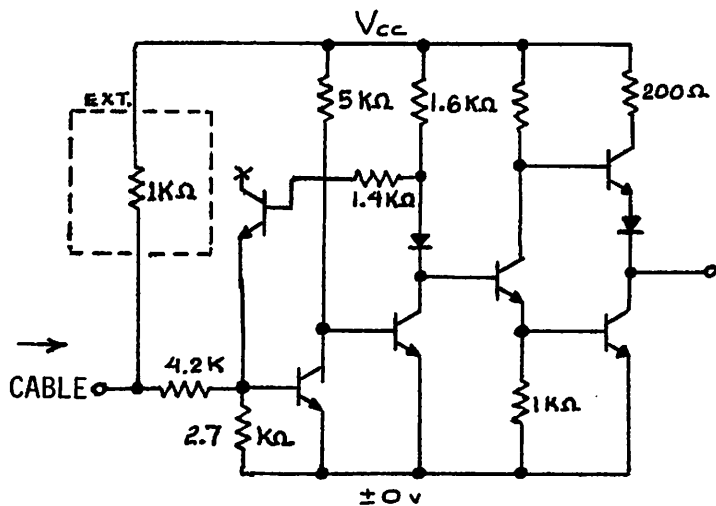
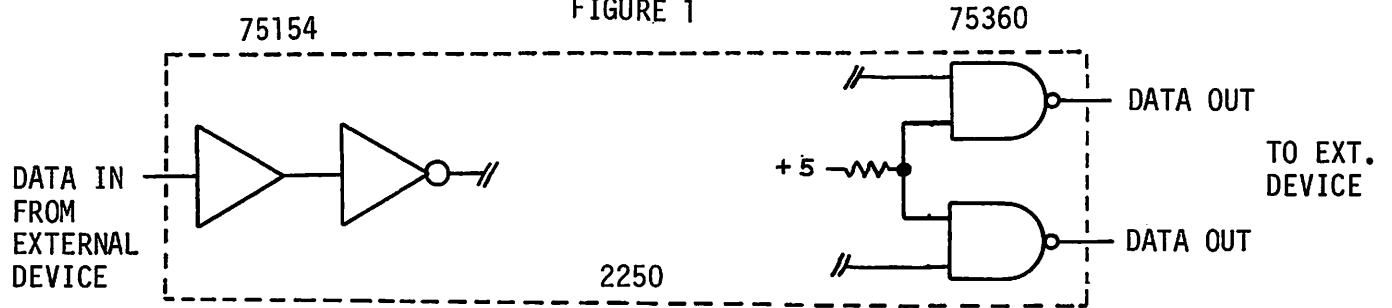
# 1. DESCRIPTION

## 1.1 GENERAL

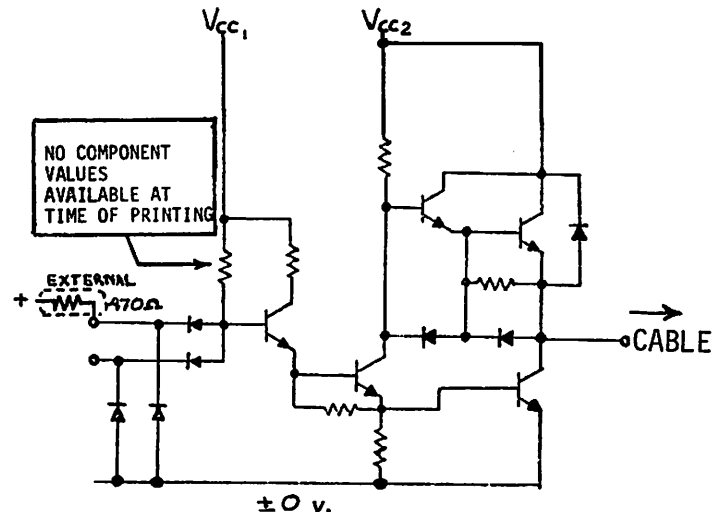
The 2250 PARALLEL INPUT/OUTPUT INTERFACE option allows external equipment to be interfaced directly to a 2200 Series Advanced Programmable Calculator. The option consists of an interface controller card which can be plugged directly into one of the I/O slots in the 2200 CPU chassis or a 2219 Extended I/O chassis. A 36 pin female Amphenol connector is mounted on this controller card to facilitate connection to external devices. Via this connector, sequential characters of parallel 8 bit data can be transmitted from or received by the 2200 under program control. Either an input device, an output device, or an input/output device can be interfaced with the 2250. It is also possible to transmit and receive 2200 Basic programs in ASCII character format.

Data transfer rates of up to 10,000 characters per second can be handled, under certain conditions. The 2250 can be used with either the 2200A or 2200B.

FIGURE 1



INPUT CIRCUIT - (DEVICE TO 2250)



OUTPUT CIRCUIT - (2250 TO DEVICE)

*Output Specifications:*

The output devices are 75360 or 75361 ICs (TTL-to-MOS drivers). These devices are generally capable of driving high capacitance loads; the output of one cannot be wire OR'd with the output of another due to totem pole output structure (see Figure 1).

NOTE:

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate output transient overshoot. The optimum value of damping resistor to use depends on the load characteristics and switching speed. A typical value would be between  $10\Omega$  and  $30\Omega$  (Figure 2).

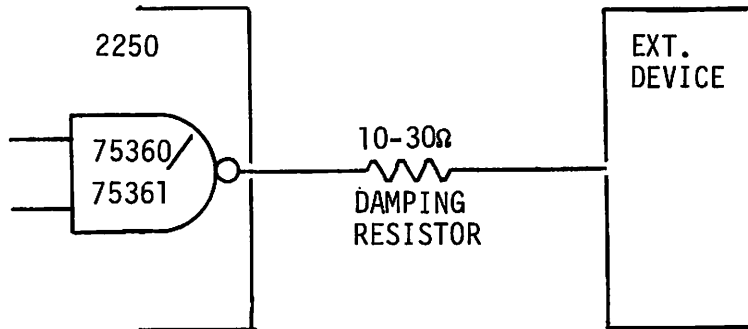


FIGURE 2


*Input Specifications:*

Input/Output circuitry is DTL/TTL compatible.


High level input threshold: +2.5 volts }  $\geq 2.5V = \text{"HIGH"}$   
 Low level input threshold: +0.4 volts }  $\leq 0.4V = \text{"LOW"}$

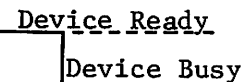
Resistive pull-up to +5 volts provided at each input ( $1K\Omega$  - See Fig. 1).

$\overline{IB1-8}_I$  must be active low signals, present prior to  $\overline{IBS}_I$ .

$\overline{IBS}_I$  must be active low, 5-20  $\mu s$  .

$\overline{RBI}$  must be active low during external device busy time.

$\overline{ACK}$  (if used) must be an active low pulse .



## 1.2 2250 INPUT/OUTPUT CONNECTOR PIN DIAGRAM

The following signals are present at the 2250 I/O connector:

NAME	PIN NO.	REMARKS	NAME	PIN NO.	REMARKS
		INPUT DATA FROM EXTERNAL DEVICE (Buffered)			DATA OUTPUT (Buffered)
$\overline{IB5}_I$	1	10 HEX CODE	$\overline{OB1}_O$	20	1 HEX CODE
$\overline{IB6}_I$	2	20	$\overline{OB2}_O$	21	2
$\overline{IB7}_I$	3	40	$\overline{OB3}_O$	22	4
$\overline{IB8}_I$	4	80	$\overline{OB4}_O$	23	8
$\overline{IB1}_I$	5	1	$\overline{OB5}_O$	24	10
$\overline{IB2}_I$	6	2	$\overline{OB6}_O$	25	20
$\overline{IB3}_I$	7	4	$\overline{OB7}_O$	26	40
$\overline{IB4}_I$	8	8	$\overline{OB8}_O$	27	80
$\overline{IBS}_I$	9	INPUT STROBE FROM EXTERNAL DEVICE	$\overline{DORB}$	28	DATA OUTPUT BUFFER READY/BUSY LEVEL
$\overline{PRMS}$	10	PRIME OUTPUT		29	SPARE
$\overline{ENDI}$	11	END OF INPUT CONTROL LEVEL		30	SPARE
$\overline{COB}_1$	12	1 HEX CODE	$\overline{OBS}_O$	31	OUTPUT DATA STROBE
$\overline{COB}_2$	13	2	$\overline{CPB}_O$	32	CPU Ready/Busy
$\overline{COB}_4$	14	4	+0V	33	Common
$\overline{COB}_8$	15	8	+0V	34	Common
$\overline{CBS}_O$	16	CONTROL OUTPUT STROBE	+0V	35	Common
$\overline{IRB}$	17	INPUT BUFFER READY/BUSY	Chassis	36	Chassis Ground
$\overline{ACK}$	18	OUTPUT DEVICE ACKNOWLEDGE			
$\overline{RBI}$	19	OUTPUT DEVICE READY/BUSY			

\*These signals are used only with Option 2 (General I/O), which will be documented in a separate publication.

### 1.3 I/O CONNECTOR SIGNALS

<u>PINS</u>	<u>NAME</u>	
1-8	$\overline{IB}_1$ thru $\overline{IB}_8$	Buffered Input Data From External Device. Active low data levels from an external device are supplied to these pins for input to the 2200 via the 2250.
9	$\overline{IBS}_I$	Input Strobe From External Device. When a 5-20 $\mu$ s active low is made available on this pin from an external device, the 8 input data levels (pins 1-8) are strobed into an 8 bit buffer on the 2250 interface. The data in the input buffer will be strobed into the CPU when the 2250 card is selected and when $\overline{CPB}$ (CPU Ready/Busy) at pin 4 <sub>3</sub> of the 2250 is set to a high logic level (Ready) by the 2200.
10	$\overline{PRMS}$	Prime Output. This active low output is produced when the reset button on the 2200 is depressed. This is generally used to reset and initialize the 2200 system and all peripherals.
11	$\overline{ENDI}$	The active END I bit (low at J1 pin 11), occurring during CPU ready (CPB=HIGH;2250 selected) causes control to be transferred to the CPU, and a branch to a subroutine (special function) is automatically executed, thus "ending input" (hence:END I)
12-15	$\overline{COB}_1$ thru $\overline{COB}_8$	Not Used (Reserved for General I/O Option)
16	$\overline{CBS}_0$	Control Buffer Output Strobe. An additional 5 $\mu$ sec active low pulse that can be generated by the 2200B DATALOAD BT statement, and is used as a "request for input" strobe.
17	$\overline{IRB}$	Input Buffer Empty/Full. When the 2250 input buffer contains a character, $\overline{IRB}$ is set to a low level (input buffer full).

$\overline{\text{IRB}}$  can be used to control input from external device. (It is undesirable to override a character in cases where the 2200 is not immediately available to receive a new character such as when scanning several input devices.)  $\overline{\text{IRB}}$  is reset to a high logic level when the current character is strobed into the 2200 CPU at  $\overline{\text{IBS}}$  time.

18       $\overline{\text{ACK}}$

Output Device Acknowledge. This pin can be used by an output device to acknowledge each character received from the 2250. This active low input pulse will reset the Data Output Buffer Ready/Busy (pin 28) and RBI (pin 19), back to a high logic level ( $\overline{\text{DORB}}$  tied to  $\overline{\text{RBI}}$ ).

19       $\overline{\text{RBI}}$

Output Device Ready/Busy. This is a pin available for a Ready/Busy signal from the External Output device (High = Device Ready; Low = Device Busy). The 2250 logic makes this signal available to the 2200 for test purposes via pin  $K_3$  ( $\overline{\text{RB}}$ ) when the 2250 interface is enabled by the 2200 with an output address (low order address bit  $\overline{\text{AB}}_1$  at pin  $D_1$  of the 2250 is set to a low logic level ODD address). The 2200 can be programmed to check  $\overline{\text{RB}}$  (pin  $K_3$ ) for an external device ready/busy indication.

20-27     $\overline{\text{OB}}_7$  thru  $\overline{\text{OB}}_0$

Data Output (Buffered). These 8 data levels reflect the contents of the Data Output Buffer on the 2250 Interface. During output operations, the Data Output Buffer is loaded with data strobed from the 2200 CPU. The Data Output Buffer Ready/Busy level, pin 28, is set to a low logic level (output buffer full). After a short delay, a 5  $\mu\text{sec}$  Data

Output strobe becomes available on pin 31 ( $\overline{\text{OBS}}_0$ ). When the character has been received, the output device indicates ready for next character ( $\overline{\text{RBI}} = \text{high}$ ); the 2200 generates the next output character after sensing this condition via  $\overline{\text{RB}}$  from the 2250.

28  $\overline{\text{DORB}}$

Data Output Buffer Ready/Busy. This pin can be used for a longer output strobe (instead of a  $5 \mu\text{s}$   $\overline{\text{OBS}}_0$ ) from the 2250. When the 2200 strobes data into the 2250 output buffer, this pin is set to a low logic level (indicating output buffer is full). The external device can then reset this level either by sending an acknowledge strobe to the 2250 via pin 18 or by resetting  $\overline{\text{RBI}}$  high.

29 Spare

30 Spare

31  $\overline{\text{OBS}}_0$

Output Data Strobe. This pin provides a  $5 \mu\text{sec}$  output strobe when 8 bits of 2200 data are available from the 2250 Data Output Buffer. This is the standard method of outputting from the 2200/2250. For outputs requiring longer strobes, the Data Output Buffer Ready/Busy level, pin 28, can be used in place of  $\overline{\text{OBS}}_0$ . See  $\overline{\text{DORB}}$ , above.

32  $\overline{\text{CPB}}_0$

CPU/2250 Ready/Busy. Used to indicate to the external device whether the 2200/2250 is ready for I/O operations. This signal indicates when high that both the 2200 is ready and the 2250 interface card has been enabled (selected) for either input (even address) or output (odd address).



33	<u>+0V</u>	Common
34	<u>+0V</u>	Common
35	<u>+0V</u>	Common
36		Chassis Ground

#### 1.4 CODE FORMAT

The normal code format in which data is transmitted and received is 7-bit ASCII code with the 8th bit set to 0. Because BASIC language is flexible, it is possible to convert data by programming to and from any code format and number format. Therefore, data can be transmitted or received in any single or packed 8-bit code format, EIA, 2 BCD digits, etc.

#### 1.5 ADDRESS SWITCH

Standard settings for the address *switch* are as follows: 3A, 3C, 3E.

When *addressing* the unit, the following will select the 2250/external device: 23A, 23C, 23E for INPUT; 23B, 23D, 23F for OUTPUT.

EXPLANATION: If the address switch is set to 3A, use address 23A for input and 23B for output. If the switch is set to 3C, use 23C (INPUT) and 23D (OUTPUT). If the switch is set to 3E, use 23E (INPUT) and 23F (OUTPUT).

## 2. INSTALLATION

- 1) Run diagnostic tests, described on pages 33-35.
- 2) If diagnostic passes, turn off 2200 power supply, remove 2250 from CPU, set 2250 address switches to 3A, 3C, or 3E per customer requirement, remove diagnostic connectors, replace 2250 into CPU, connect customer's cable to 2250, and turn 2200 system on.

### 3. OPERATIONS - See operators manual for programming (WL# 700-3156A)

#### 3.1 OVERALL I/O SEQUENCE

A single Basic I/O statement in the 2200 is designed to complete an entire input or output operation sequence including enabling the controller for an external device, transmitting/receiving data and then disabling the controller at the end of the operation.

#### 3.2 2250 ENABLE LOGIC

Seven switches are used to set a device address on this interface card (the eighth, lowest order address switch, is not connected). The program language provides the ability to *specify* a device address within an I/O statement, or *select* the address by means of the SELECT statement or #N file designators. When the I/O statement is executed, the device address is strobed internally from the 2200 CPU to enable the 2250. When the I/O operation is complete, the 2200 disables the 2250. This is done automatically and does not require device interaction or programming control. When the 2250 is enabled, signal levels and strobes are gated between the 2200 I/O bus and the 2250 connector. When the 2250 is not enabled these levels and strobes are inhibited or ignored. Thus, the 2200 and the connected I/O device are protected from other device interaction and noise. For Input Devices, a CPU Ready/Busy signal is available on pin 32 of the I/O connector ( $\overline{CPB}_0$ ). When a high logic level is available on this pin, it indicates that the 2200 is waiting to receive data and the 2250 is enabled.

#### 3.3 INPUT/OUTPUT SELECTION

The 2250 can be enabled for either Input or Output operations by utilizing the low order bit of the device address used in the BASIC program. When the low order bit  $\overline{AB}_1$  is set to a high logic level, the card is enabled for *input* (EVEN address). When the low order bit is set to a low logic level, the card is enabled for *output* (ODD address).

### 3.4 INPUT OPERATIONS

There are three basic modes of input operation:

1) *Consecutive Character Input (2200A, 2200B)*

On execution of a standard INPUT statement, consecutive characters are sent from the currently selected input device to the 2200 via 2250, until the termination code HEX 0D (carriage return) is read. When input terminates, the next program step is executed.

2) *Requested Consecutive Character Input (2200B)*

On execution of a DATALOAD BT statement, the input device currently selected can be initialized with an  $\overline{OBS}_0$  plus HEX 00 or HEX 01 from  $\overline{OBI}_0$ - $\overline{OB}_8$ , then  $\overline{CBS}_0$  begins "requesting" individual characters (one character per  $\overline{CBS}_0$ ). Each  $\overline{CBS}_0$  sent to the external device causes a single  $\overline{IBS}_I$  and new character to be strobed into the selected 2250 input buffer. Consecutive characters are requested and read into the 2200 via the 2250 until one of the following conditions occur:

- (a) A predesignated number of characters has been read; the exact number is specified within the DATALOAD BT statement.
- (b) A stop character code is read; this character is also specified within the DATALOAD BT statement.
- (c) Variable (Array) has been filled.

When input terminates, the next program step is executed.

3) *Single Character (Scanned) Input (2200B)*

The 2200B offers this input method whereby the BASIC program might scan several devices for single character inputs or for applications where the 2200 scans one device for slow or irregular input. On

execution of a KEYIN statement, the currently selected 2250 input buffer is checked (scanned) for an empty/full condition. If the input buffer contains a character (full), the CPU becomes ready, and that character is sent to the 2200 CPU; the program branches to the statement number specified in the KEYIN statement. If the input buffer is empty (no character), the CPU remains busy, and the next statement is executed.

More detailed explanations of the three input modes described above follow:

### 3.5 SIGNAL SEQUENCE

#### 3.5.1 Standard INPUT Statement (2200A, 2200B)

##### 1) Enable 2250 for input:

A SELECT INPUT statement is executed; then, on execution of an INPUT statement, Address Bus signals  $\overline{AB}_{2-8}$  from the CPU match the 2250 device address switch settings. The logical state of the low order Address Bus signal  $\overline{AB}_1$  will be high at  $\overline{ABS}$  time to enable the 2250 for an input operation.

##### 2) 2200 indicates READY for input:

The CPU sends a ready level ( $\overline{CPB}$  = high) to the 2250, which in turn indicates to the external input device via  $\overline{CPB}_0$  (= high) that one 8 bit character on  $\overline{IB1}_1$  thru  $\overline{IB8}_1$  accompanied by  $\overline{IBS}_1$  may be clocked into the empty input buffer of the selected 2250.

##### 3) External device sends input strobe:

When  $\overline{CPB}$  from the CPU goes high,  $\overline{CPB}_0$  from the 2250 also goes high, flagging the external device to send an input strobe ( $\overline{IBS}_1$ ) to clock

the data on  $\overline{IB1}_I$  thru  $\overline{IB8}_I$  from the external device into the 2250 input buffer. The CPU becomes busy ( $\overline{CPB}$ ,  $\overline{CPB}_0 = \text{low}$ ) and remains so until ready to accept a new character.

4) Input remaining characters:

Steps 2 and 3 are repeated for all characters to be read. Up to 190 characters plus 1 HEX 0D (carriage return) may be entered from a single INPUT statement, without producing an error 45.

5) Terminate input:

An ASCII carriage return, HEX 0D, strobed in by  $\overline{IBS}_I$  will terminate input from the external device. The next program statement is executed, and the 2250 remains selected (in the CPU) for proceeding INPUT statements until a *different* device is selected for input with SELECT INPUT and INPUT statements.

### 3.5.2 DATALOAD BT Statement (2200B)

1) Enable 2250 for output:

When the DATALOAD BT instruction is executed, Address Bus signals  $\overline{AB}_{2-8}$  from the CPU match the 2250 device address switch. The logical state of the low order Address Bus signal  $\overline{AB}_1$  will be low at  $\overline{ABS}$  time (ODD address) to enable the 2250 with an output address.

2) 2200 senses 2250 ready for output:

With the 2250 enabled by an *output* address, and with external device ready ( $\overline{RBI} = \text{high}$ ), signal  $\overline{RB}$  from the 2250 to the CPU will be low, indicating that the 2250 output buffer is empty and the external device is ready to accept a character.

3) 2200 initializes external device:

With the 2250 enabled by an output address, the CPU receives the low from the 2250  $\overline{RB}$  line and a HEX 00 (or HEX 01 for DATALOAD BTR) is sent back to the 2250 output buffer via  $\overline{OB}_{1-8}$ , accompanied by a 5  $\mu$ s  $\overline{OBS}$ , all from the CPU.  $\overline{OBS}$  from the CPU becomes  $\overline{OBS}_0$  to the external device, and the HEX 00 (or HEX 01) is strobed out of the 2250 output buffer and into the external device via  $\overline{OB1}_0$ - $\overline{OB8}_0$ .

4) 2250 indicates ready:

From the time of the HEX 00 (or HEX 01) code is loaded into the 2250 output buffer, the Data Output Ready/Busy ( $\overline{DORB}$ ) signal from the 2250 indicates that the 2250 output buffer is full ( $\overline{DORB} = \text{low}$ ).  $\overline{RBI} = \text{high}$  indicates external device ready via  $\overline{RB}$  (pin  $K_3$ ), since 2250 is enabled with an output address.

5) 2200 senses ready for input:

$\overline{CPB}$  from the CPU goes high (CPU ready for input). The corresponding output to the external device ( $\overline{CPB}_0 = \text{high}$ ) indicates that the 2200/2250 is ready for input.

6) CPU sends "request for input" strobe:

A  $\overline{CBS}$  pulse is sent from the CPU to the 2250 and there becomes  $\overline{CBS}_0$  (5  $\mu$ s active low - pin 32) from the 2250 to the external device. This 5  $\mu$ s data request strobe can be used to trigger an input strobe ( $\overline{IBS}_I$ ).

7) External device sends input strobe plus data:

Execution of steps 5) and 6) generates an input strobe ( $\overline{IBS}_I$ ) in order to strobe data into the 2250 input buffer. Since  $\overline{CPB}$  from the CPU is already high at this time, the input character is immediately read into the CPU. The CPU ready/busy line then goes busy ( $\overline{CPB}$ ,  $\overline{CPB}_0 = \text{low}$ ) and remains so until the CPU is ready to accept a new character.

8) Input remaining characters:

Steps 5) or 6) and 7) are repeated for all characters to be read until one of the conditions stated in paragraph 3.4(2) (page 11) occur.

9) Terminate input:

As stated above, one of the three conditions in paragraph 3.4(2) will terminate input. When input terminates, the next program step is executed.

### 3.5.3 KEYIN Statement (2200B)

- 1) External Device Sends Input Strobe - Since in this procedure, the CPU does not have to be ready, the input device can send  $\overline{IBS}_I$  plus data at any time. The data is stored in the 2250 input buffer.
- 2) Enable 2250 For Input - A KEYIN statement for inputting is executed. The 2200 first enables the 2250 controller card. It does not, however, set a level ( $\overline{CPB} = \text{high}$ ) which indicates that the 2200 is ready for input.
- 3) 2200 Senses Character In 2250 Input Buffer - The 2200 then tests for Ready/Busy. In this case, when the 2250 card is selected with an input address, it will test the input buffer for a Full/Empty condition in the 2250 (i.e., the level available on pin  $K_3$ ,  $\overline{RB}$ ). If the 2200 sees an "Empty" condition ( $\overline{RB} = \text{high}$ ), the 2250 will be disabled, and processing will continue at the next sequential statement. If the

2200 sees a "Full" condition ( $\overline{RB} = \text{low}$ ), the CPU will set a level indicating to the 2250 that it is awaiting data ( $\overline{CPB} = \text{high}$ ). This will cause the contents of the 2250 input buffer to be strobed into the 2200 and will reset the input buffer Empty/Full indicator,  $\overline{IRB}$  on pin 17 to the external device.

- 4) Terminate Input - For the KEYIN command, which inputs one character, the 2200 will disable the 2250 at this point and continue processing at the specified statement number.

### 3.6 GENERAL OUTPUT CHARACTERISTIC

The 2250 contains an output buffer which holds the 8 bits of data output ( $\overline{OB}_{1-8}$ ) from the 2200. Data levels from this buffer are available on pins 20 through 27 of the 2250 I/O connector ( $\overline{OB}_{10}-\overline{OB}_{80}$ ).

When a 2200 Basic output statement is executed, the 2200 enables the 2250 with an output address, and output characters obtained from variables, expressions, or literals in the argument list are sequentially output on an external device ready basis (when  $\overline{RBI} = \text{high}$ ). When all characters have been sent, the 2200 then disables the 2250 controller card and continues processing.

The 2250 provides two general means of outputting, depending upon the output strobe length required. These methods apply for PRINT, PRINTUSING, HEXPRINT, and DATASAVE BT statements, which provide the means of outputting formatted or unformatted data to an external output device.

By standard method, characters are strobed from the 2200 to the 2250 data output buffer, where the data levels are provided on pins 20 through 27 along with a 5  $\mu\text{sec}$  output strobe on pin 31,  $\overline{OBS}_0$ . When the output device receives the data output strobe, it must set the  $\overline{RBI}$  signal to busy (low logic level), within 5 microseconds of the leading edge of the output strobe  $\overline{OBS}_0$ , and hold  $\overline{RBI}$  low until the external device is ready to receive another character from the 2250/2200.



An alternative method of output response is available when a longer output strobe is required by the external device, or where a Ready/Busy D.C. level response is not available from the output device. In this method the output device Ready/Busy signal,  $\overline{\text{RBI}}$ , can be supplied from the 2250 by tying the DATA OUTPUT BUFFER READY/BUSY signal on pin 28 ( $\overline{\text{DORB}}$ ) to pin 19. When a character is sent to the output buffer on the 2250,  $\overline{\text{OBS}}$  from the CPU causes the Output Buffer Ready/Busy level available on pin 28 to be set to a low logic level (output buffer full). An output device may use this as a strobe, instead of  $\overline{\text{OBS}}_0$  on pin 28. When the output has had sufficient time to receive the data, it will send an acknowledge input strobe back to the 2250 on pin 18,  $\overline{\text{ACK}}$ . This active low input strobe will reset Data Output Buffer Ready/Busy back to a high logic level (output buffer empty); the 2200 CPU will sense this via  $\overline{\text{RB}}$  pin  $\text{K}_3$  as a 2250 READY indication and will send another character.

Typical output sequences are described below:

3.6.1 Normal Output Sequence - (5  $\mu\text{sec}$  Output Strobe, Device Ready/Busy Level Response)

- 1) Enable - A 2200 Basic Output Statement (PRINT, PRINTUSING, HEX PRINT, DATASAVE BT) is executed; the 2200 first enables the 2250 interface controller by strobing the address for that particular output device.
- 2) Test Ready - When the 2250 is enabled with an output address, ( $\overline{\text{AB}}_1 = \text{low}$ ) the level on pin 19,  $\overline{\text{RBI}}$ , will be sensed by the 2200 via  $\overline{\text{RB}}$  (Pin  $\text{K}_3$ ) to test output device ready. The 2200 will test the 2250 for ready ( $\overline{\text{RBI}}$ , pin 19 = high;  $\overline{\text{RB}}$ , Pin  $\text{K}_3$  = low); when ready, the CPU will output a character to the 2250 output buffer.
- 3) Character Output - The 2200 will strobe an 8-bit data character into the 2250 output buffer. This will cause the data levels to be available on pins 20 through 27, and a 5  $\mu\text{sec}$  output strobe to be available on pin 31 ( $\overline{\text{OBS}}_0$ ). The Data Output Buffer Empty/Full condition ( $\overline{\text{DORB}}$ ) on pin 28 is set to a low logic level (Full), but this signal is not generally used in the normal output sequence.

- 4) Output Device Busy Until Character Processed - When the output device receives the  $\overline{\text{OBS}}_0$  strobe, it sets  $\overline{\text{RBI}}$  on pin 19 to a low logic level until it has processed the character. The external device then resets  $\overline{\text{RBI}}$  to a high logic level when READY for next output character.
- 5) Repeat For All Characters - For successive characters, the 2200 will continue testing the device Ready/Busy, which is set immediately after the 5  $\mu\text{sec}$  output strobe, and steps 2, 3 and 4 are repeated for all remaining characters to be output. A ready test is not made after the final character.
- 6) Disable - The 2200 will then strobe out an address to disable the 2250 and will continue processing.

3.6.2 *Acknowledged Output Sequence; For Longer Output Strokes (Assuming DORB on pin 28 tied to RBI on pin 19)*

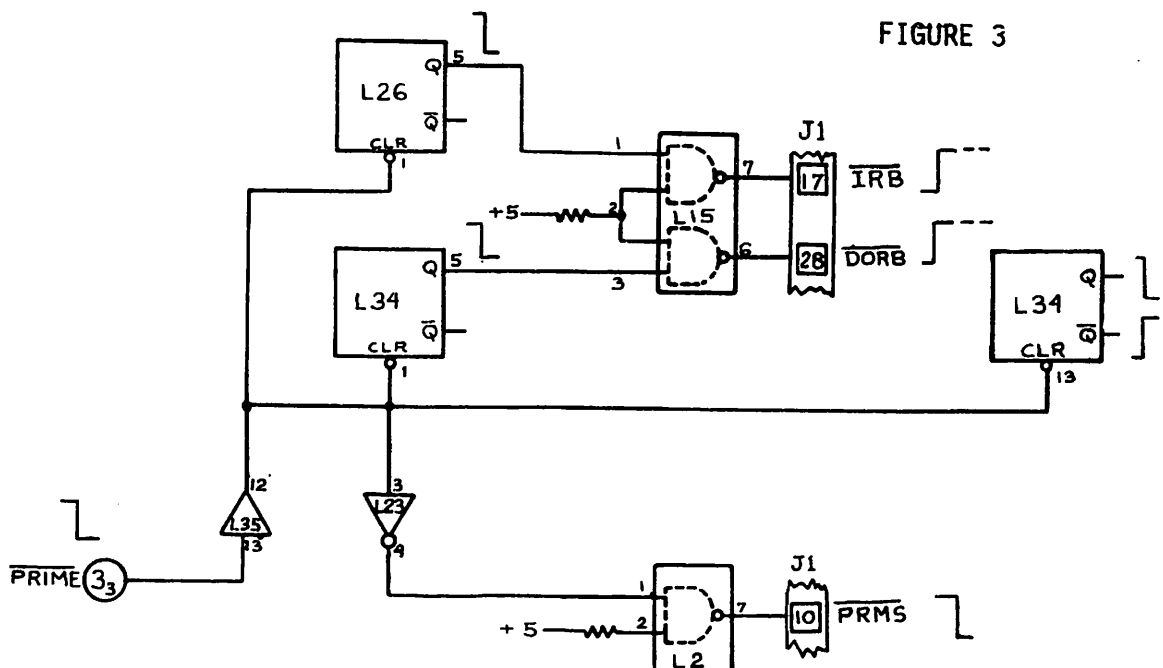
- 1) Enable - The 2200 enables the 2250 with an output address.
- 2) Test For Ready - The 2200 tests device Ready/Busy ( $\overline{\text{RBI}}$ ) level via RB (Pin  $K_3$ ) of the 2250. When external device ready ( $\overline{\text{RBI}} = \text{high}$ ), a low logic level at  $\overline{\text{RB}}$  (Pin  $K_3$ ) is sensed, and the 2200 outputs the first character. In this case,  $\overline{\text{RBI}} = \overline{\text{DORB}}$ .
- 3) Output A Character - The 2200 strobos a character into the 2250 Output Buffer, pins 20 through 27 and provides a 5 microsecond strobe on  $\overline{\text{OBS}}$ .  $\overline{\text{OBS}}$  causes  $\overline{\text{DORB}}$ , Data Output Buffer Empty/Full to be preset to low logic level (Buffer Full). This level can be used for longer output strobe instead of  $\overline{\text{OBS}}_0$ .  $\overline{\text{DORB}}$  (tied to  $\overline{\text{RBI}}$ ) remains set low and the data levels remain available until an input acknowledgment pulse is received from the device.
- 4) Output Device Acknowledges - The output device sends an acknowledgment pulse on pin 18 ( $\overline{\text{ACK}}$ ). This will reset the Data Output Buffer Ready/Busy on pin 28 and the Device Ready/Busy  $\overline{\text{RBI}}$  on pin 19 back to a high logic level; this will be sensed by the 2200 via  $\overline{\text{RB}}$  (= low), pin  $K_3$ , and the next character will be loaded into the 2250 output buffer.

- 5) Repeat For All Characters - Steps 2, 3, and 4 are repeated for data in the argument list. (A ready test is not made following the last character.)
- 6) Disable - The 2200 strobes an address to disable the 2250 and processing continues.

#### 4. 2250 CIRCUIT DESCRIPTION

##### 4.1 RESET/ENABLE CIRCUITRY

In order to manually initialize the 2250, key RESET on the 2215 keyboard. This will cause a  $\overline{\text{PRIME}}$  signal to be sent to all controller boards (from the keyboard controller). At the 2250,  $\overline{\text{PRIME}}$  (coordinates C,9) clears the following latches: L26-5 (coordinates 8,D&E), L34-5 (coordinates 8,D), and L34-8 (coordinates 6,D). Clearing L26-5 sets  $\overline{\text{IRB}}$  high (coordinates 8,E); clearing L34-5 sets  $\overline{\text{DORB}}$  high (coordinates 8,E); clearing L34-8 sets L36-4 high.  $\overline{\text{PRIME}}$  also resets the external device via  $\overline{\text{PRMS}}$  which is active low, (coordinates 8,C).



Since the 2250 is not yet selected for output or input, L8-9 and L36-5 (coordinates 5,D) will be low thus causing  $\overline{RB}$  to be high.

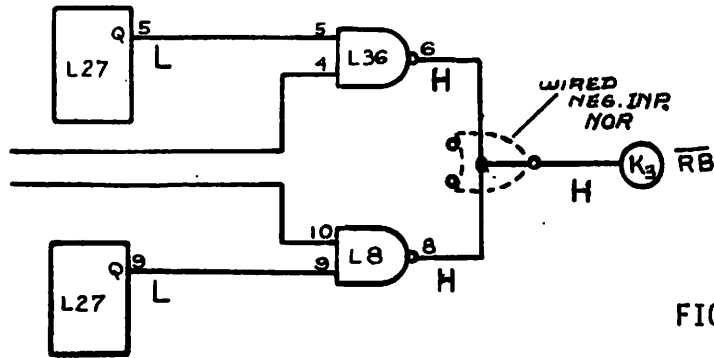


FIGURE 4

#### 4.2 ADDRESS CIRCUITRY

The 2250 INPUT/OUTPUT controller has one bank of eight rocker switches (only 7 are used: 2,4,8,10,20,40,80) for setting the address of the 2250 and a peripheral unit. The state of the low order 1 address bit ( $\overline{AB}_1$ ) from the CPU enables the 2250 for either input or output at  $\overline{ABS}$  (address bus strobe) time.

Refer to 6394 PC schematic, at coordinates 7/8, A/B. Address bits  $\overline{AB}_{2-8}$  (from the CPU) are compared to the settings of address switches 2, 4, 8, 10, 20, 40 and 80 via comparators L29 and L30.

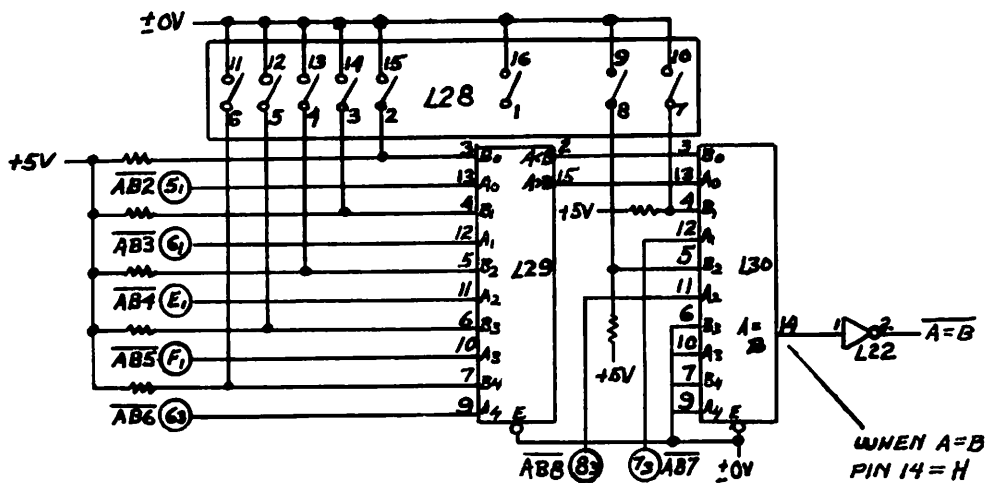


FIGURE 5

When the Address Bus signals match the address switch settings, pin 14 of L30 will be active high (A=B), which will provide a low logic level at L18 pins 6 and 9 via inverter L22, pins 1 and 2.

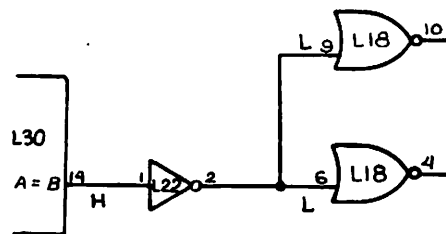


FIGURE 6

If  $\overline{AB}_1$  is low at  $\overline{ABS}$  time, L27 pin 5 (latch) will be clocked into a set condition (high); L27 pin 9 (latch) will be clocked into a reset condition (low). If  $\overline{AB}_1$  is high at  $\overline{ABS}$  time, L27 pin 9 will be clocked into a set condition (high); L27 pin 5 will be clocked into a reset condition (low).

L27 pin 5 is the output enable latch; L27 pin 9 is the input enable latch. Thus, if  $\overline{AB}_1$  is low at  $\overline{ABS}$  time (ODD address), the 2250 is selected for output from CPU to peripheral via 2250; if  $\overline{AB}_1$  is high at  $\overline{ABS}$  time (EVEN address), the 2250 is selected for input from peripheral to CPU via 2250.

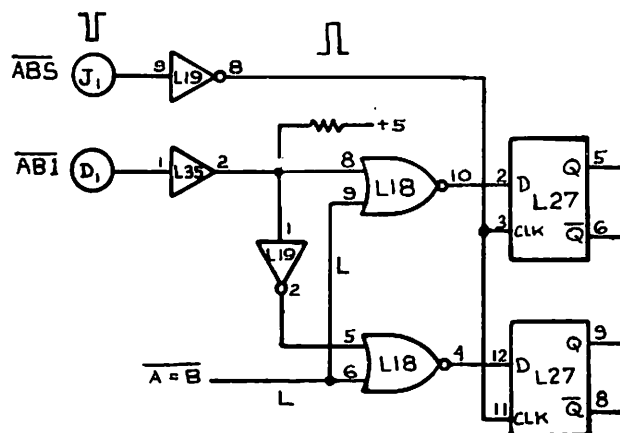


FIGURE 7



With the 2250 ready, the peripheral device sends  $\overline{IBS}_I$  (pin 9), the input strobe, which performs several functions:

- 1)  $\overline{IBS}_I$  (active low, 5-20  $\mu$ s) triggers one shot L33 pin 12 (coordinates 9,G). The trailing edge of the pulse from L33 pin 12 clocks the first input character into the input buffer ICs (L31 and L32: coordinates 8/9, F/G).

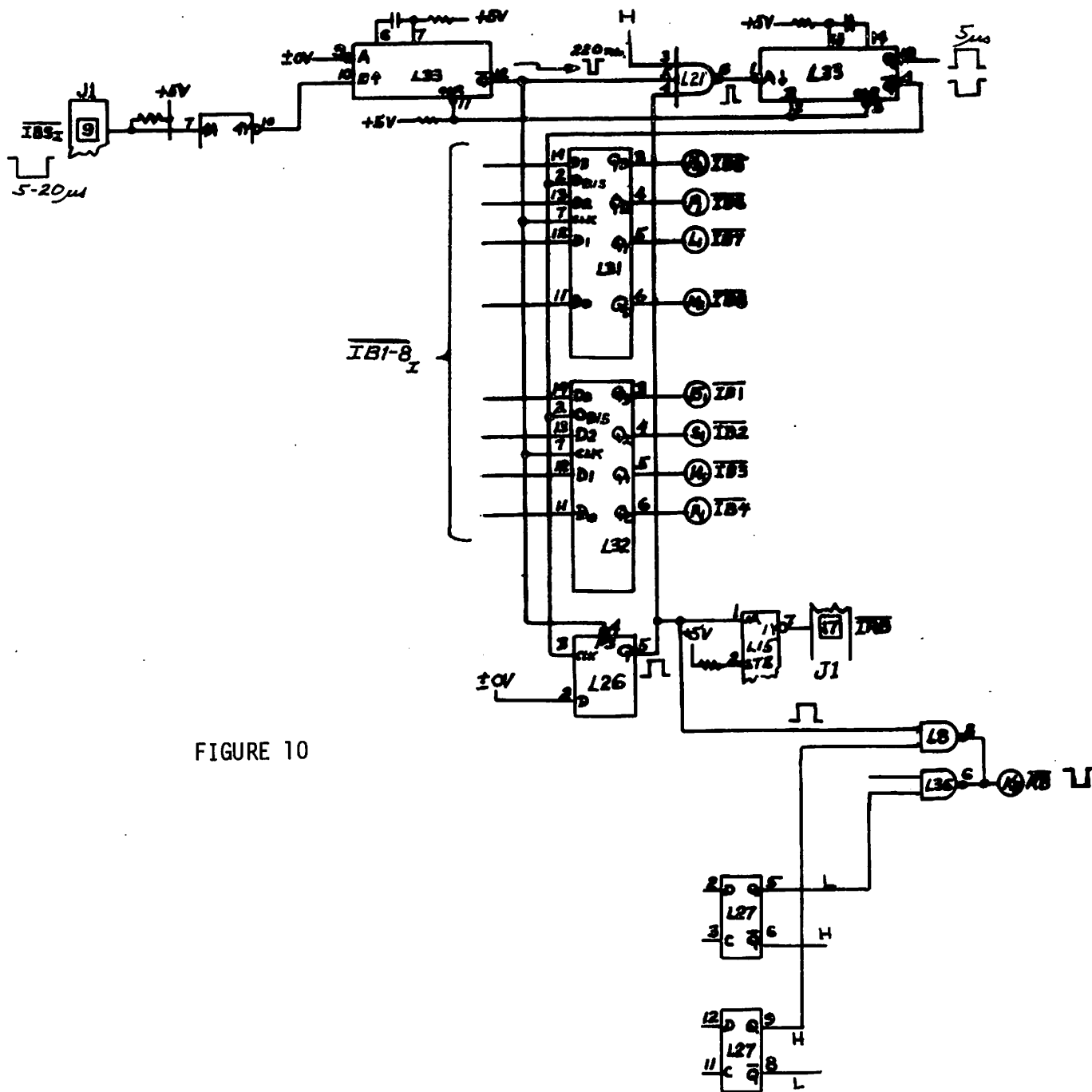


FIGURE 10

- 2) The leading edge of the pulse from L33-12 also presets latch 26 pin 5 (coordinates 8/9, D/E). Presetting L26 pin 5 results in a low at  $\overline{IRB}$ , indicating to the peripheral device that the 2250 input buffer is now





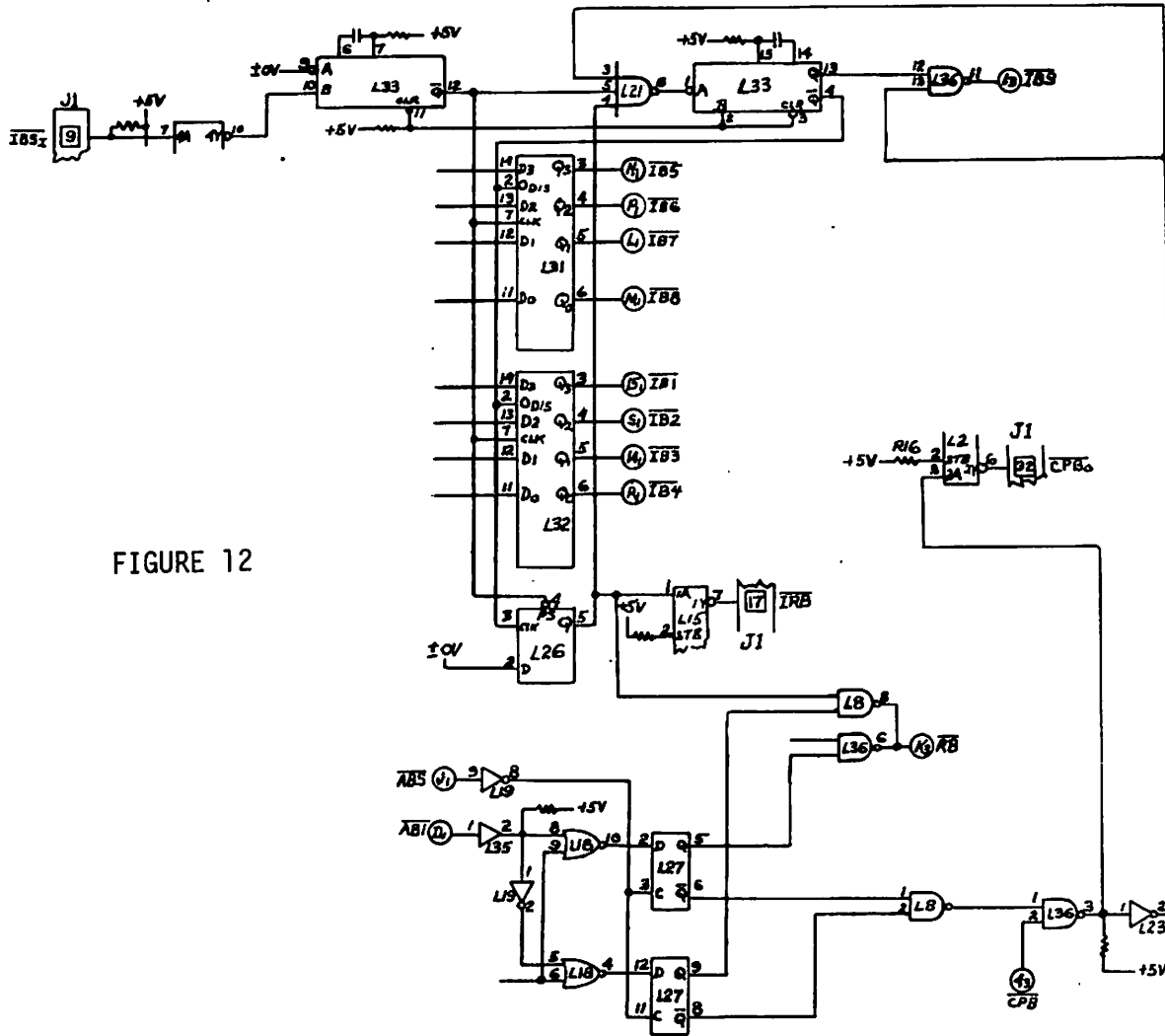


FIGURE 12

Whenever the peripheral issues an  $\overline{IBS}_I$  strobe to the 2250 input buffer, a new character on  $\overline{IB}_{1-8}$  overrides the previous character in L31 and L32. As a precaution, a busy signal such as  $\overline{IRB}$  indicates to the peripheral when it may not send another  $\overline{IBS}_I$ .

When  $\overline{CPB}$  returns high (ready)  $\overline{CPB}_0$  will also go high, and the input sequence repeats for all remaining data until the 2250 is deselected by the CPU, on receipt of a HEX OD termination character.



### 4.3.3 KEYIN STATEMENT CIRCUIT ACTION

To accomplish input via KEYIN, the external device need not wait for the 2250 to be selected and ready.  $\overline{IBS}_I$  plus one input character can be sent from the external device whenever available. The character will be strobed into the input buffer and  $\overline{IRB}$  will go low, indicating an input buffer full condition, as explained in paragraph 4.3.1.

On execution of a KEYIN statement, the 2250 is selected for input (EVEN address) as in paragraph 4.3.1. Next, the CPU (still not ready) checks the level at pin  $K_3$  ( $\overline{RB}$ ) of the 2250. If  $\overline{RB}$  is low (resulting from L26-5 being preset high) the CPU becomes ready ( $\overline{CPB}$  = high) and the contents of the input buffer (L31,32) is strobed into the CPU when L33-13,4 is triggered by L21-6.

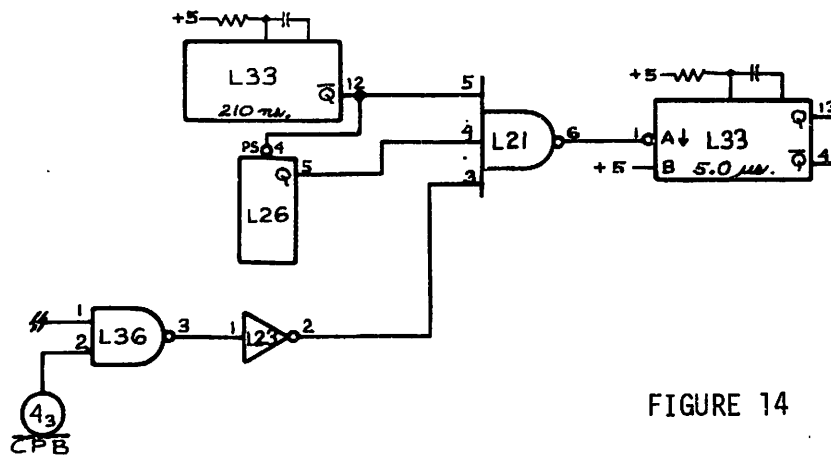


FIGURE 14

After inputting a single character, the 2250 is deselected and a branch is made to a statement number specified within the KEYIN statement.

If  $\overline{RB}$  had been high when being checked by the CPU (L26-5 = low - input buffer empty) the CPU would not become ready and processing would simply continue at the next statement.

#### NOTE:

It is important to remember that the 2250 must be enabled with an input address (EVEN); otherwise, the condition being checked at  $\overline{RB}$  (pin  $K_3$ ) will be external device ready/busy, instead of 2250 input buffer full/empty.



#### 4.4 CHARACTER OUTPUT

On execution of a statement for data output (PRINT, PRINTUSING, HEX PRINT, DATASAVE BT), low order address bit  $\overline{AB}_1$  = low at  $\overline{ABS}$  time (output address - ODD); L27 pin 5 (output enable latch) will be clocked into a set condition (high) at  $\overline{ABS}$  time via L19-9,8.

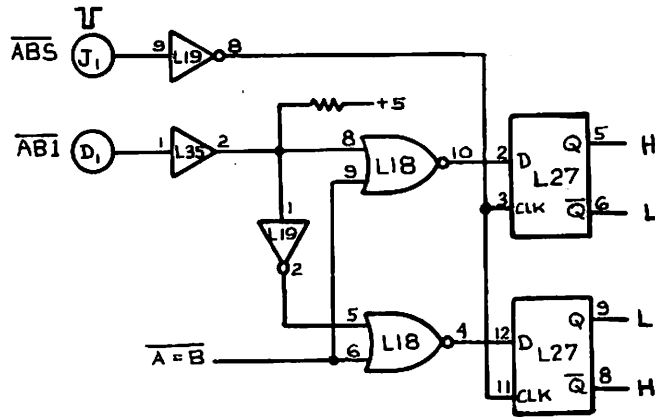


FIGURE 16

Since L34 pin 8 (coordinates 6,D) is in a clear condition, L36 pin 4 will be high.\*

Since L27 pin 5 has been clocked into a set condition, L36 pin 5 will also be high. With both input pins (4 and 5) to L36 high, L36 pin 6 ( $\overline{RB}$ ) will be low, indicating to the CPU that peripheral is ready and that the 2250 is selected and ready to receive an output bus strobe ( $\overline{OBS}$ ) from the CPU at L7-8. Since L8 pin 1 (5,B) detects that the 2250 is selected for output, L8 pin 3 issues a high to L19 pin 11 (6,B). L19 pin 10 then enables L7 with a low at pins 9 and 11.

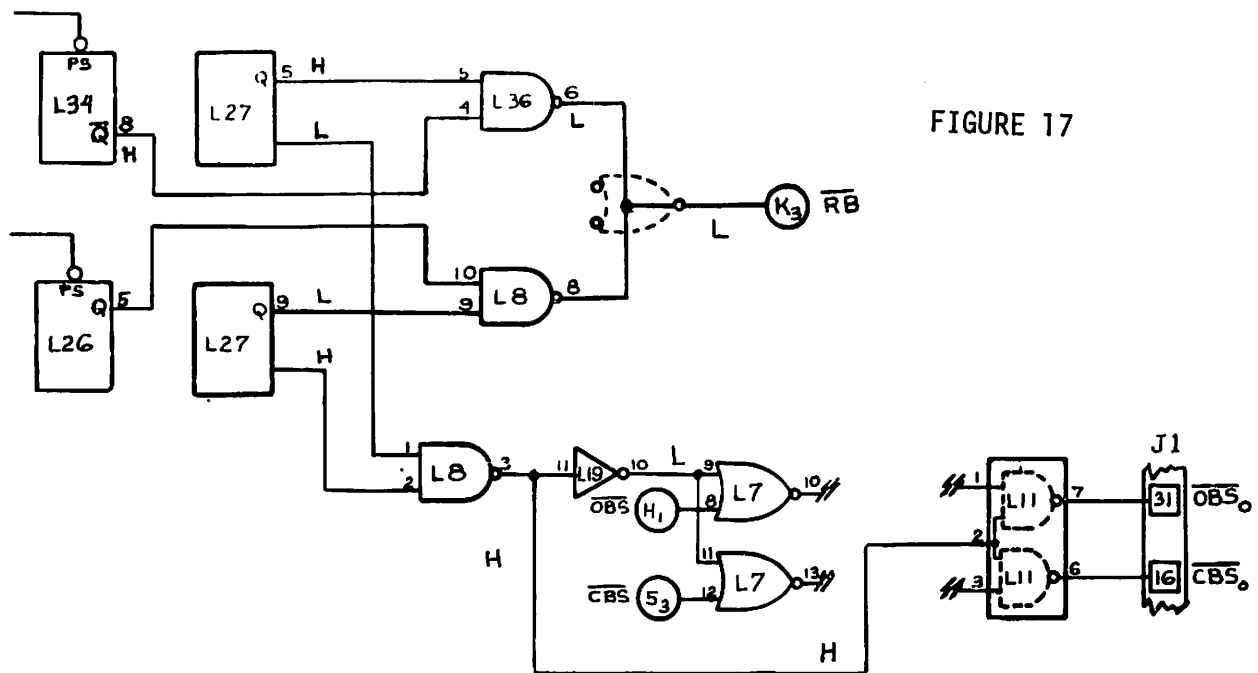


FIGURE 17

NOTE:

If the peripheral is not ready,  $\overline{RBI}$  from the peripheral is low, and L34 pin 8 will be preset via L20 pins 5 and 12, and L19 pins 5 and 6. If L34 pin 8 is preset (low),  $\overline{RB}$  will be high, indicating to the CPU that the 2250 and the external device cannot accept any CPU output data at this time (peripheral busy).

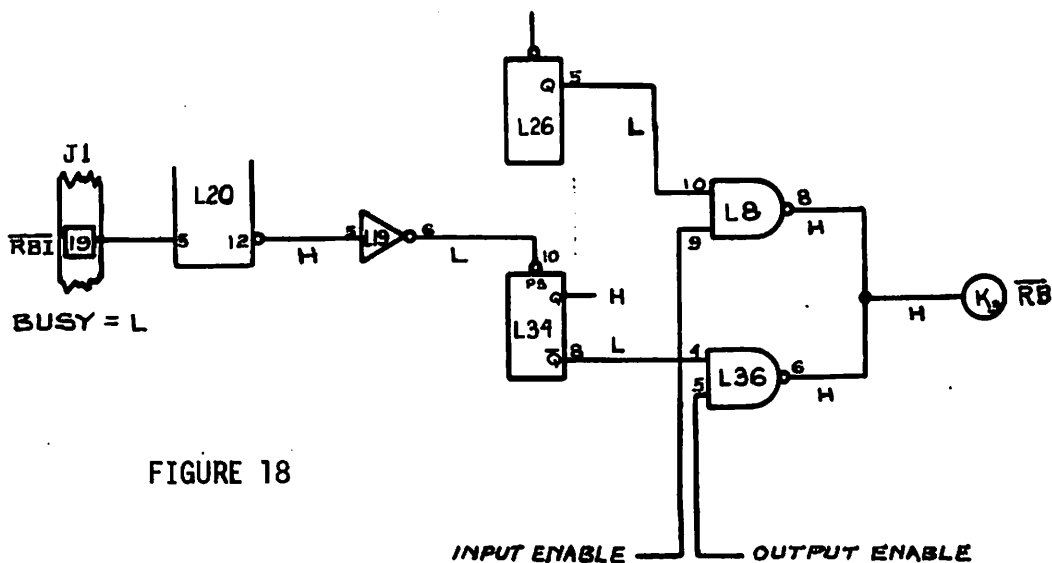


FIGURE 18

When  $\overline{OBS}$  arrives from the CPU at L7 pin 8 as an active low, (coordinates 11,E) a number of actions occur simultaneously:

- (a) The high on L7-10 resulting from  $\overline{OBS}$  causes L18 pin 13 (coordinates 10,D) to send a low to L34 pin 4, L7 pin 6, and L19 pin 13 (coordinates 9-D, 7-C, and 7-F respectively).

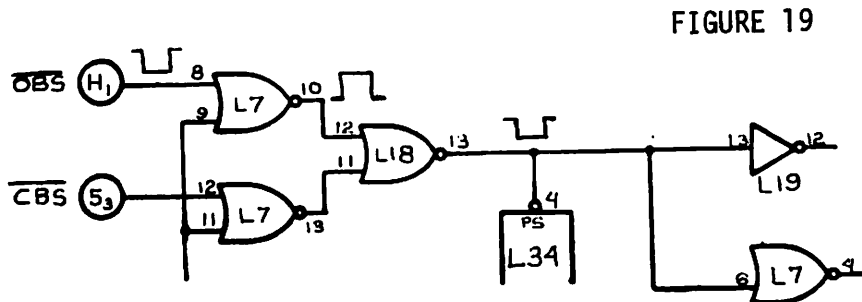


FIGURE 19

- (b) The low at L19 pin 13 is inverted at L19 pin 12 and clocks output data  $\overline{OB}_{1-8}$  from the CPU into the 2250 output buffer (L17 and L25, coordinates 5, E/F).

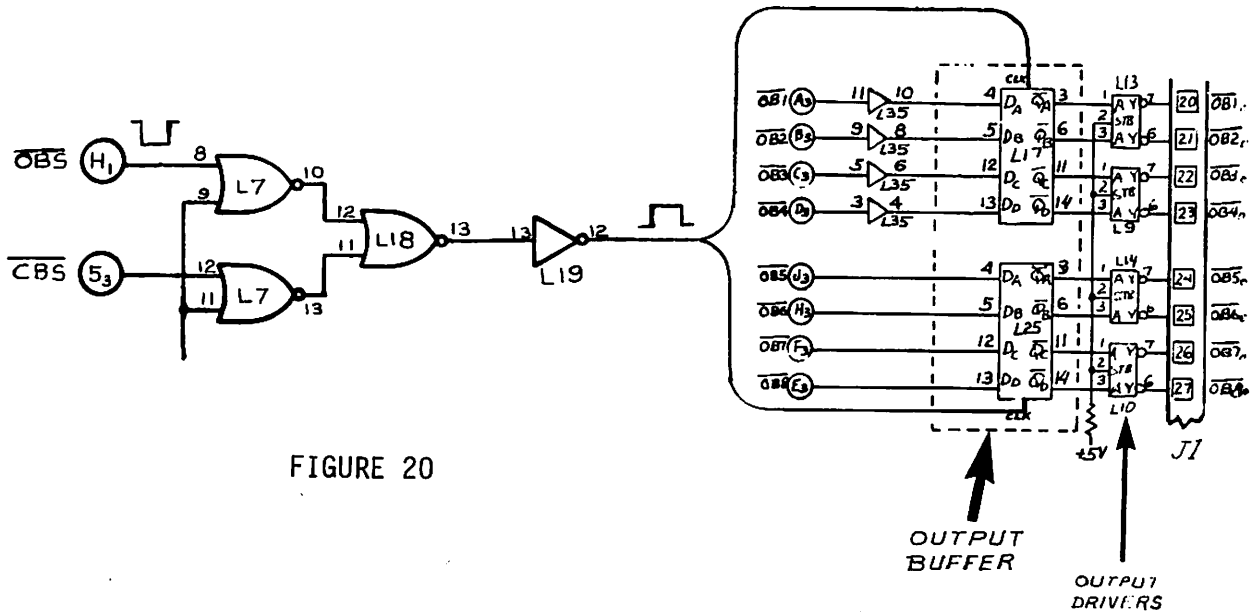


FIGURE 20

- (c) The low at L34 pin 4 presets L34 pin 5 (coordinates 8/9,D), which in turn sets  $\overline{DORB}$  low (coordinates 8,E).

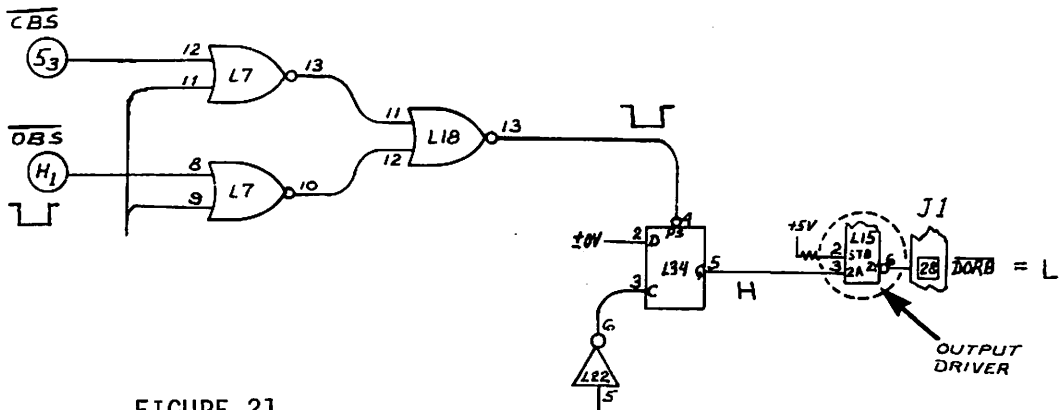


FIGURE 21

- (d) The low at L7 pin 6 (coordinates 7/8,C) along with the low from L19 pin 4 at L7 pin 5 causes one shot L5 pin 4 (coordinates 7,C) to trigger one shot L5 pin 5 (coordinates 6,C), which in turn, sends  $\overline{OBS}_0$  (5  $\mu$ s) to the external device via L11 pin 7 (coordinates 5,C; active low). Thus,  $\overline{OBS}_0$  strobes the contents of the 2250 output buffer into the peripheral device via  $\overline{OB}_{1-8}$ .

Thus,  $\overline{OBS}_0$  strobes the contents of the 2250 output buffer into the peripheral device via  $\overline{OBI-8}_0$ .

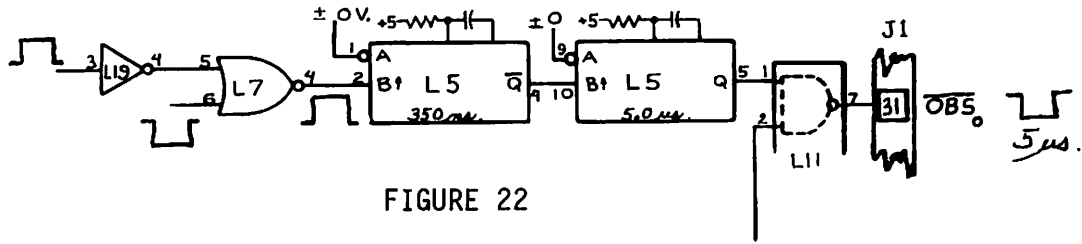
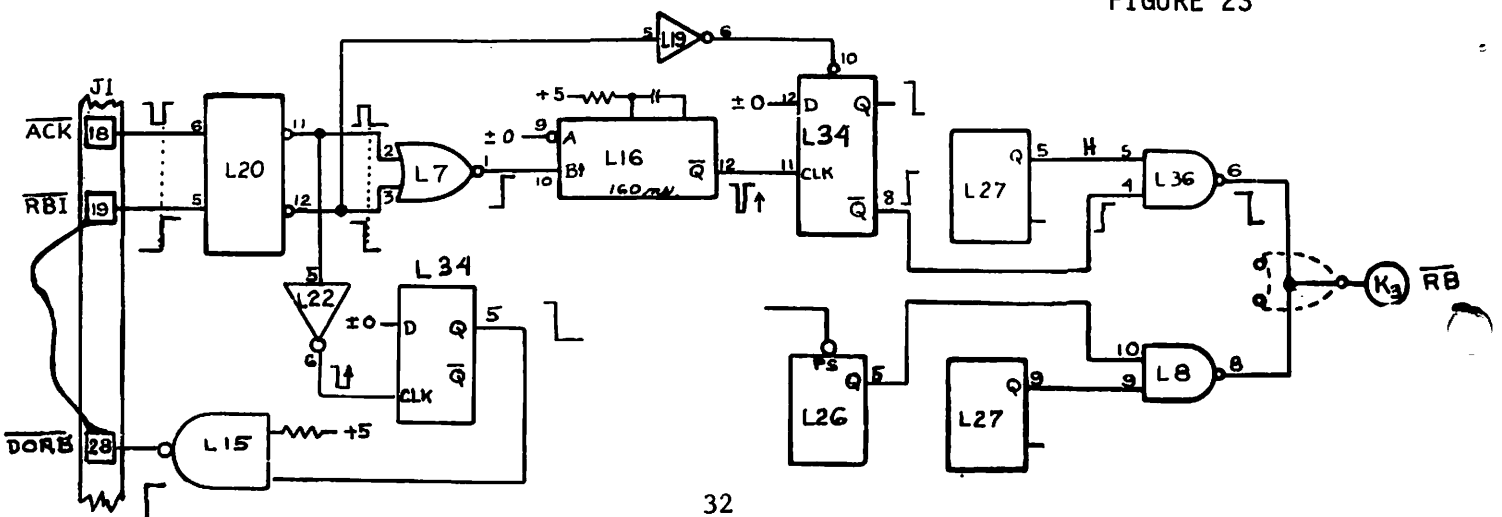


FIGURE 22

To verify that the peripheral has received the output data from  $\overline{OBI-8}_0$ , an ACKNOWLEDGE ( $\overline{ACK}$ ) pulse can be sent to the 2250 ( $\overline{DORB}$  tied to  $\overline{RBI}$ ). When  $\overline{ACK}$  is received at J1 pin 18 (active low; coordinates 11,E) the following events occur:

- 1) L20 pin 11 (coordinates 10,E) issues a high pulse ( $\square$ ) which is inverted at L22 pin 6 (coordinates 9,E). The trailing edge of the resulting low pulse ( $\sqcap$ , from L22 pin 6) clocks L34 pin 5 back to a reset condition. When L34 pin 5 goes low,  $\overline{DORB}$  is reset high. If  $\overline{DORB}$  is tied to  $\overline{RBI}$ ,  $\overline{RBI}$  is also reset high.
- 2) The trailing edge of the high pulse from L20 pin 11 and  $\overline{DORB}/\overline{RBI}$  returning high causes L7 pin 1 to trigger one shot L16 pin 12 (coordinates 7,D), which in turn clocks L34 pin 8 to a reset condition ( $\overline{Q} = \text{high}$ ). Since a high from L27 pin 5 and a high from L34 pin 8 are now present at L36, L36's output pin 6 goes low ( $\overline{RB}$ ) indicating to the CPU that the external device is ready (2250 is ready to accept next output code on  $\overline{OB}_{1-8}$  from CPU at next  $\overline{OBS}$  time). Character output terminates on conditions presented by the particular output statement.

FIGURE 23





If no acknowledge pulse is supplied to the 2250 from the external device, the device can reset  $\overline{RBI}$  from a low (busy condition) to a high (ready condition). This L→H transition from the device will result in L34-8 being clocked L→H, so that  $\overline{RB}$  goes low (L36-5 enabled high) indicating to the CPU that the device is ready.

## 5. 2250 DIAGNOSTIC TEST

### Minimum Equipment Needed:

- (a) Diagnostic Test Tape
  - (b) Two Diagnostic Connectors (See pages 34,35)
  - (c) 2200/2250 System
- 1) Before inserting 2250 into the CPU, set 2250 address switch to HEX 3E.
  - 2) Turn 2200 system off and insert 2250 into CPU I/O slot. (DO NOT FORCE PC BOARD).
  - 3) Turn 2200 system on.

The 2250 diagnostic test occupies one block of a multiblock system diagnostic tape, and is run as follows:

- 4) LOAD, EXECUTE
- 5) RUN, EXECUTE
- 6) KEY SPECIAL FUNCTION 14

At this point the 2250 test will be loaded:

```
THERE ARE TWO CONNECTORS FOR 2250 DIAG.  
BOTH DIAGNOSTICS MUST BE RUN  
*****  
KEY SPECIAL FUNCTION KEY 00 FOR CONN. #1  
KEY SPECIAL FUNCTION KEY 01 FOR CONN. #2  
JUMP L7 PINS 8 AND 12 FOR CONN. #2 DIAG.  
-----  
KEY RESET TO STOP TEST  
*****  
* SET SWITCHES TO 3E FOR THESE DIAGNOSTICS  
*****
```

A good diagnostic run appears as follows:

```
PASS #           XX
                                     Pass Count
```

A failure appears as:

```
                                     ERROR-TEST FAILED
STOP
:_
```

The test connectors are constructed as follows:

**PARTS REQUIRED:**

36 Pin amphenol connector (male). WL #350-2049 or 350-2051.

**CONNECTOR #1**

Put jumpers between Pin # (output) and Pin # (input) as listed below for Amphenol connector.

OUTPUT SIGNAL TERM	PIN # OUTPUT	PIN # INPUT	INPUT SIGNAL TERM
$\overline{OB}_0$	31	9,18,19	$\overline{IBS}, \overline{ACK}, \overline{RBI}$
$\overline{OB}_1$	20	5	$\overline{IB}_1$
$\overline{OB}_2$	21	6	$\overline{IB}_2$
$\overline{OB}_3$	22	7	$\overline{IB}_3$
$\overline{OB}_4$	23	8	$\overline{IB}_4$
$\overline{OB}_5$	24	1	$\overline{IB}_5$
$\overline{OB}_6$	25	2	$\overline{IB}_6$
$\overline{OB}_7$	26	3	$\overline{IB}_7$
$\overline{OB}_8$	27	4	$\overline{IB}_8$

**USE:**

Attach this connector to 2250 controller card and run 2250 diagnostic for connector #1.

CONNECTOR #2

OUTPUT SIGNAL TERM	PIN # OUTPUT	PIN # INPUT	INPUT SIGNAL TERM
$\overline{\text{CBS}}_0$	16	9,18,19	$\overline{\text{IBS}}, \overline{\text{ACK}}, \overline{\text{RBI}}$
$\overline{\text{COB}}_1$	12	5	$\overline{\text{IB1}}_I$
$\overline{\text{COB}}_2$	13	6	$\overline{\text{IB2}}_I$
$\overline{\text{COB}}_4$	14	7	$\overline{\text{IB3}}_I$
$\overline{\text{COB}}_8$	15	8	$\overline{\text{IB4}}_I$
$\overline{\text{CPB}}_0$	32	1	$\overline{\text{IB5}}_I$
$\overline{\text{PRMS}}_0$	10	2	$\overline{\text{IB6}}_I$
$\overline{\text{IRB}}$	17	3	$\overline{\text{IB7}}_I$
$\overline{\text{DORB}}$	28	4	$\overline{\text{IB8}}_I$
OV	34	11	$\overline{\text{ENDI}}$

USE:

Attach this connector to 2250 controller card and run 2250 diagnostic for connector #2.

## APPENDIX A


### TROUBLESHOOTING:

The following items can be checked if the 2250 will not function with an external device or if the 2250 diagnostic test fails.

- 1) Check address switch setting.
- 2) Perform the following steps for signal checks:

- (a) Disconnect external device.
- (b) Insert program steps in 2200:

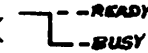

```
10 SELECT PRINT 23B (address switches on 23A)
20 PRINT "A"
30 GO TO 10
RUN, EXECUTE
```

- (c) On pin 31 check  $\overline{\text{OBS}}_0$   (5  $\mu$ s).
- (d) On pin 32 check  $\overline{\text{CPB}}_0$
- (e) On pin 28 check  $\overline{\text{DORB}}$ . The signal will go low at first loop execution and will stay low.
- (f) On pin 18 ground momentarily,  $\overline{\text{ACK}}$  signal,  $\overline{\text{DORB}}$  must be reset (high) momentarily and then will go low again with program running.
- (g) Check output lines for A1 = HEX(41).









- 3) CLEAR, EXECUTE.

- 4) Put following program in 2200B:

```
10 SELECT INPUT 23A
20 KEYIN A$, 40, 40
30 GO TO 20
40 SELECT PRINT 005
50 HEXPRINT A$
60 GO TO 20
```


- 5) Connect two wires to a microswitch, common end of microswitch is to be connected to pins 33, 34, and 35 on a 36 pin male Amphenol connector (WL #350-2049 or 350-2051). The normally open end of microswitch is to be connected to pin 9 of the test connector.  $\overline{IBS}_1$  can be generated by pressing this switch.
- 6) Check the following signals for input sequence: (RUN, EXECUTE)
  - (a)  $\overline{RB}$  on pin  $K_3$
  - (b)  $\overline{CPB}_0$  on pin 32 (  --READY CPU busy signal busy).
  - (c)  $\overline{IRB}$  on pin 17
  - (d)  $\overline{IBS}$  on pin  $l_3$  (  - 5  $\mu$ s).

Input will be displayed on 2200 CRT as 002020202020202020202020202020.

- 7) RESET, CLEAR, EXECUTE.
- 8) Enter: 10 DATALOAD BT/63B,A\$. RUN, EXECUTE. Key microswitch for each entry and check  $\overline{CBS}_0$  (  - 5  $\mu$ s)
- 9) Key RESET, RUN, EXECUTE. Check L27-5 (  after input terminates).
- 10) Check ABS at L27-3,11  .
- 11) Check L30-14 (  ) for A=B condition.
- 12) Check L5-4 (330 ns  ).
- 13) Check L5-5 (5  $\mu$ s  ).
- 14) Check L33-12 (225 ns  ).
- 15) Check L33-13 (  5  $\mu$ s).
- 16) If  $\overline{IRB}$  is never set low or never set high, check L26-5 (D latch).

17) If  $\overline{\text{DORB}}$  is not set low or never reset high, check L34-5 (D latch).

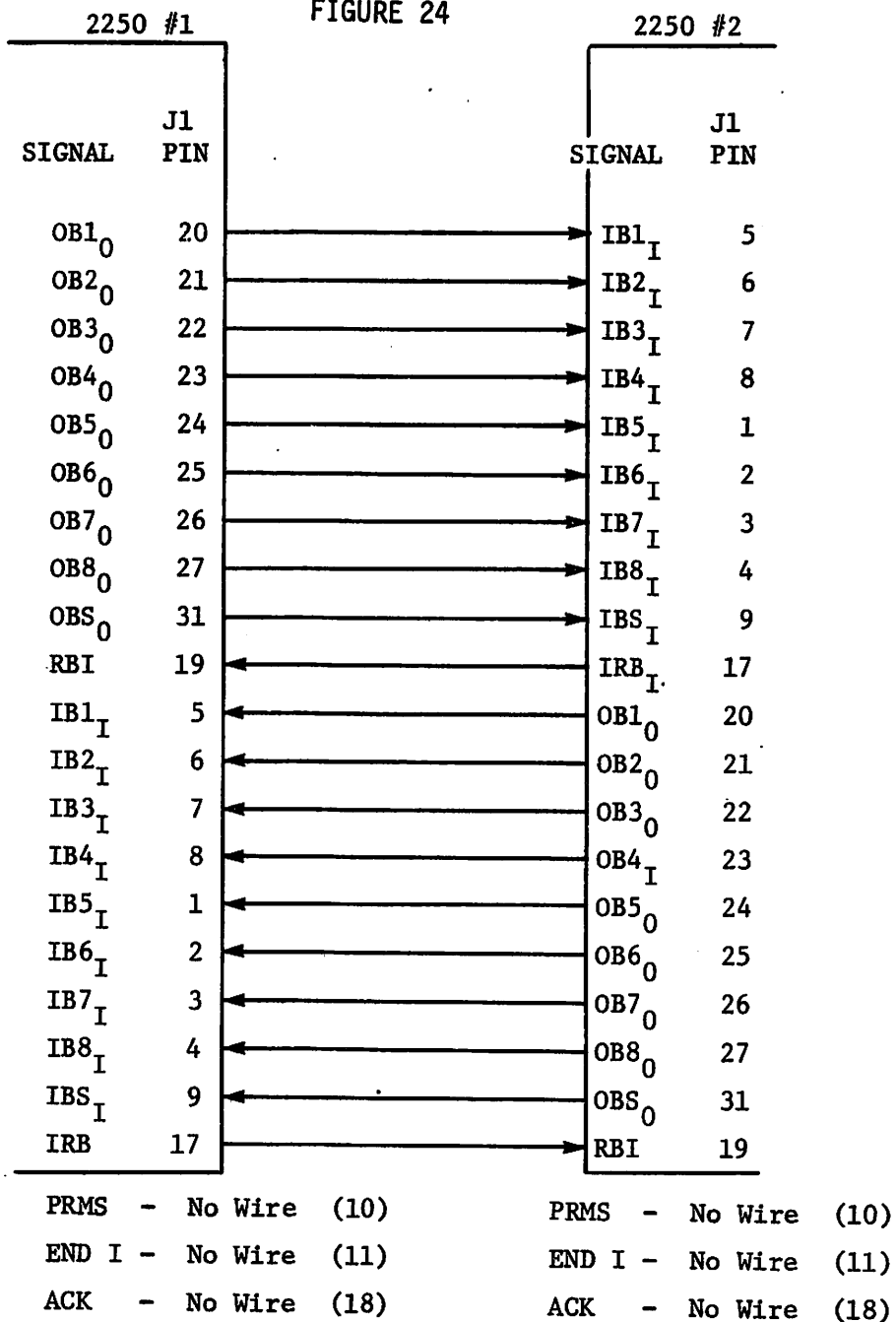
18) If all the above items are verified *good*, make sure that:

- (a) Customer's equipment is supplying the  $\overline{\text{IBS}}_I$ ,  5-20  $\mu\text{s}$  signal going low, and check  $\overline{\text{RBI}}$ , external device Ready - H, external device Busy - L.
- (b) The customer's 2200 program is correct for the specific application.
- (c) The external device supplies the correct last character (to terminate input), depending on the input statement used.

APPENDIX B - INTERFACE WIRING

LINK 2200 TO 2200 VIA 2250'S:

FIGURE 24



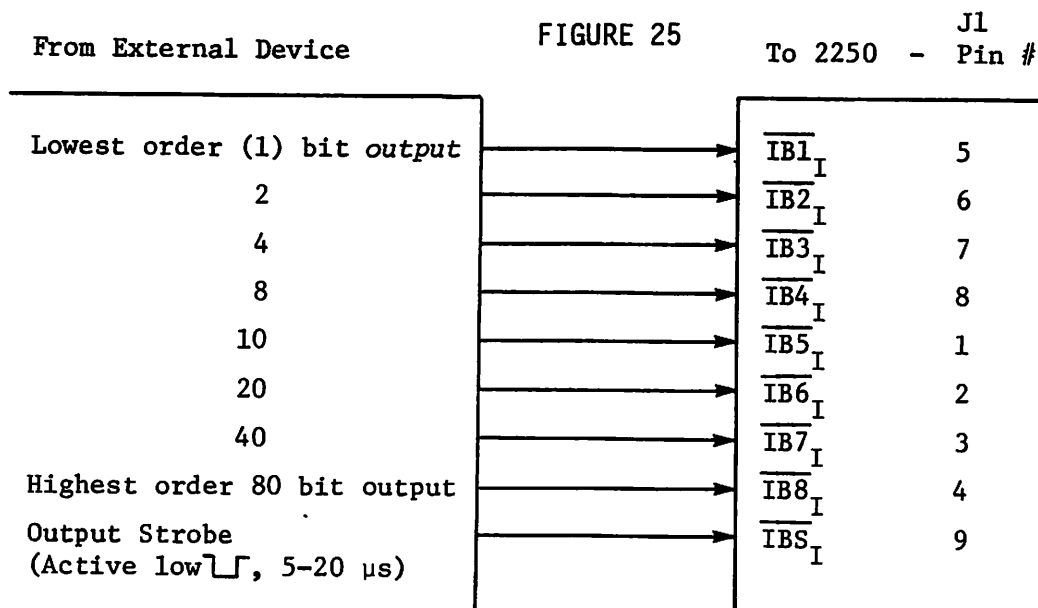
Communicating from 2200 to 2200 can be accomplished via INPUT, DATALOAD BT(R), KEYIN, PRINT, PRINTUSING, and HEX PRINT statements.

The receiving 2200 must first be selected for input and set into a receive mode via either an INPUT statement or a DATALOAD BT statement. On execution of the input statement (excluding KEYIN), the receiving 2200 will await input from the sending 2200. At that time, the sending 2200 should be selected for output. On execution of a PRINT, PRINTUSING or HEXPRINT statement, the sending 2200 senses that the input buffer of the receiving 2200 is empty and ready to accept a character ( $\overline{IRB}$  = high). The first character is strobed into the input buffer at the receiving end ( $\overline{OBS}_0$  from the sending 2200 becomes  $\overline{IBS}$ ). Since the receiving 2200 was awaiting input, the character is immediately sent to the CPU. At the end of the actual input strobe ( $\overline{IBS}$ ) to the CPU,  $\overline{IRB}$  is reset, giving an indication to the sending 2200 that the input buffer of the receiving 2200 is again empty; send next character. Input will terminate as explained on page 11.

## 2. STANDARD INPUT

The diagram below shows standard wiring of the eight data input lines plus the data input strobe line from external device to 2250 connector (J1). This wiring should be performed for all input applications; wiring of one or more additional input control signals will be performed as follows based on individual external device requirements.

Input Signals (Standard/Required Minimum)





There are two basic data input modes using the 2250 input/output interface:

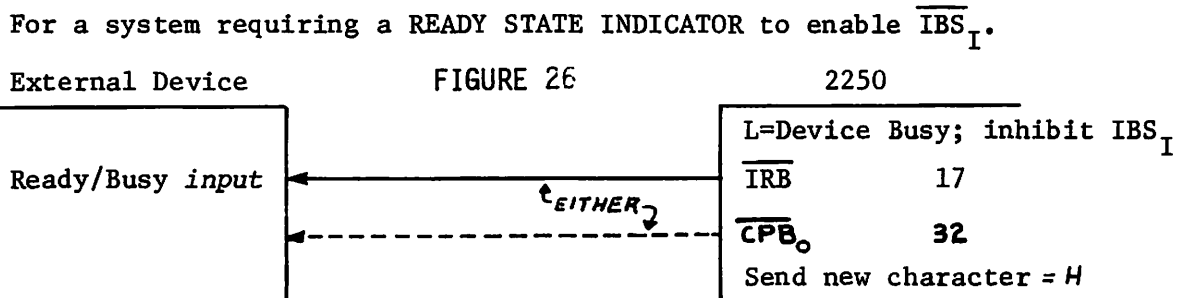
- I. Consecutive character input                      8 bits parallel
- II. Single character input                              per character

I. Consecutive character input may be accomplished by one of two standard techniques (depending on the external device requirements). One character may be input to the 2250 from the external device each time either a *ready state indicator* or a *request for input* strobe is sent to the external device. Terminate consecutive character input under one of the following conditions:

- 1) Device sends "stop" character.
- OR 2) The total number of characters to be read, specified in the BASIC program, has been read.
- OR 3) The variable accepting input data has been satisfied.

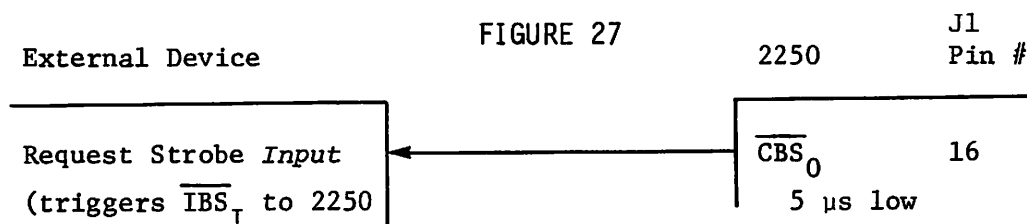
Input control signal wiring:

METHOD A - Consecutive Character Input

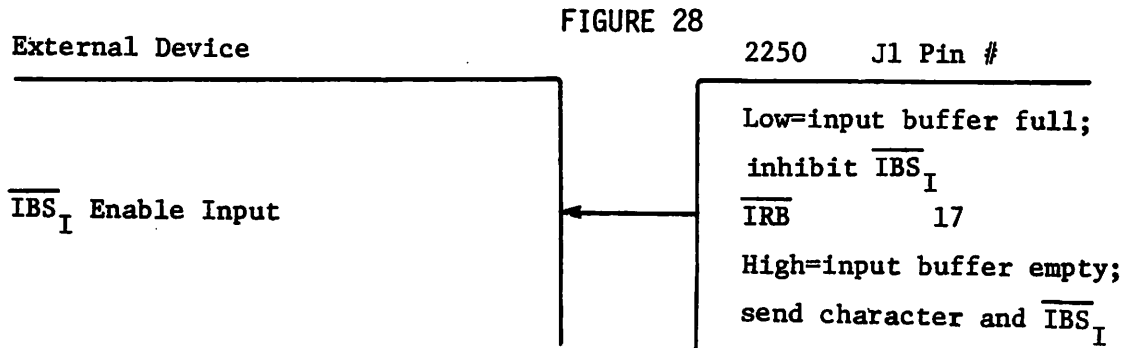


METHOD B - Consecutive Character Input

For a system requiring a "request" strobe (in order to trigger  $\overline{IBS}_I$ ):



- II. Single character input applies to systems with irregular or slow input to the 2250: (allowing  $\overline{IBS}_I$  to be sent at any time by the external device after an enabling signal is received from the 2250). Using this method a character may be transferred to the 2250 input buffer even if the 2250 is not currently selected by the 2200.



## 2. STANDARD OUTPUT

One of two output strobes may be used to strobe a character out to the external device via  $\overline{OBI-8}_0$ .

- a)  $\overline{OBS}_0$  - 5  $\mu$ s, active low.
- b)  $\overline{DORB}$  - High when output buffer and external device are ready awaiting a character from the 2200 CPU. As soon as the 2250 output buffer is loaded by the CPU,  $\overline{DORB}$  goes to a low logic level (active strobe time = low).  $\overline{DORB}$  is reset high on the trailing edge of an acknowledge pulse ( $\overline{ACK}$ , active low  $\lrcorner$ ) from the external output device, signifying that the character has been received.

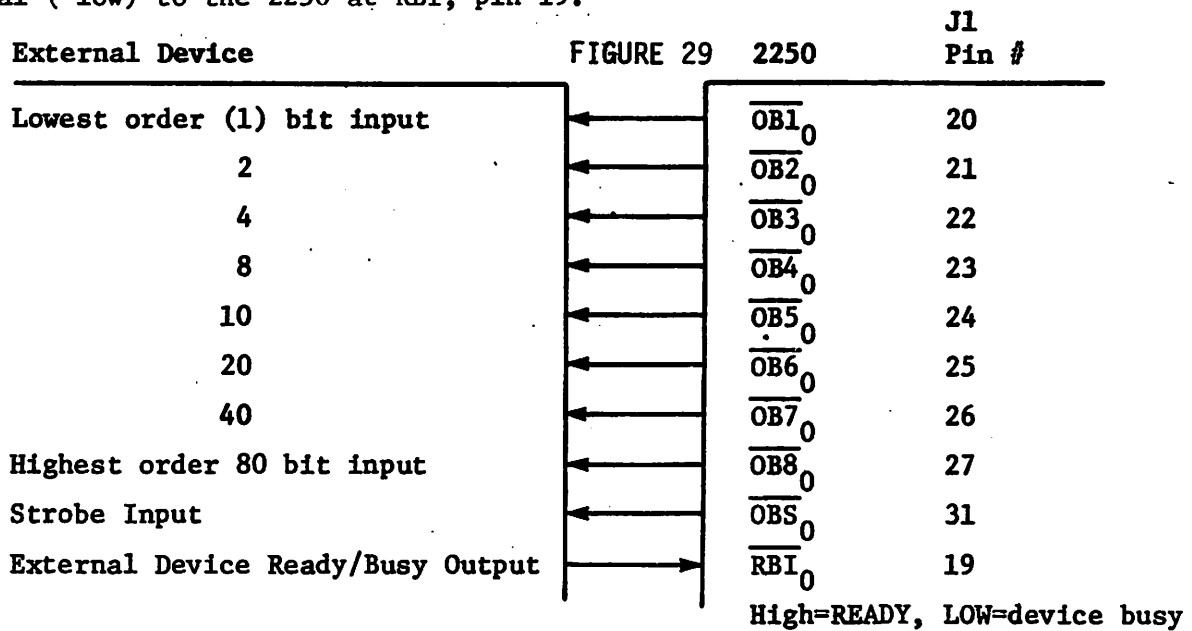
An external device ready/busy signal is normally provided by either the external device, or by the 2250 itself:

- a) A busy signal ( $\overline{RBI}$ =low) supplied by the external device will inhibit new characters from being sent to the external device, until this device is again ready to accept a new character ( $\overline{RBI}$ =high).
- b) Tying  $\overline{DORB}$  to  $\overline{RBI}$  will provide the 2250 with its own busy indication ( $\overline{RBI}=\overline{DORB}$ =low) until  $\overline{DORB}$  (and  $\overline{RBI}$ ) is reset by an  $\overline{ACK}$  ( $\lrcorner$ ) pulse from the external device.

Techniques used to output data from the 2250 may be categorized as follows:

- a) Standard output interface - No acknowledge response from external device. Device supplies ready/busy level to 2250.

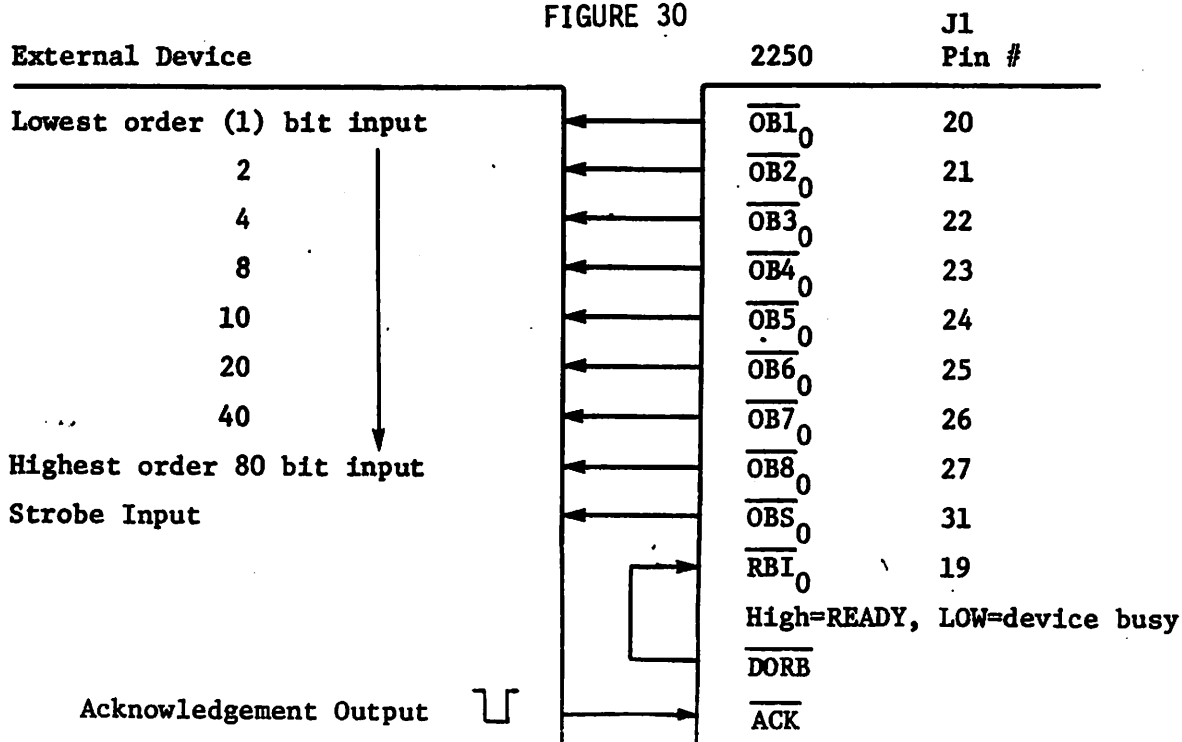
External device receives a 5  $\mu$ s strobe,  $\overline{OBS}_0$ , from the 2250; within 5  $\mu$ s of the leading edge of the output strobe the device sends a busy signal (=low) to the 2250 at  $\overline{RBI}$ , pin 19.



- b) Acknowledged output and/or longer output strobe.

Using this technique, the 2250 supplies its own ready/busy line by tying  $\overline{DORB}$  to  $\overline{RBI}$ . The busy (active low) from  $\overline{DORB}$  to  $\overline{RBI}$  is reset high on receipt of an  $\overline{ACK}$  pulse from the external output device. The PRINT and PRINTUSING statements are satisfactorily used with this wiring application. During the time  $\overline{RBI}$  is low, the output device will not receive any new characters. See page 18 for signal sequence.

FIGURE 30



With the 2250 selected for output, a PRINT, PRINTUSING, HEXPRINT, or DATASAVE BT statement will cause the sequences described on pages 16-19.

Other output applications are possible using Option 2 General I/O Commands. Option 2 will be documented in a separate publication.

