

PERFORMANCE SPECIFICATIONS AND DESIGN NOTES ON THE

2200 MVP 5 1/4" DISK POWER SUPPLY

HM- 75

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TABLE OF CONTENTS

|                                      | <u>Page</u> |
|--------------------------------------|-------------|
| Section 1. Performace Specifications | 3           |
| Section 2. Specification Definitions | 4           |
| Section 3. Design Notes              | 9           |
| Section 4. Temperature Measurements  | 12          |

(1). PERFORMANCE SPECIFICATIONS

+5V SUPPLY

|                            |  |
|----------------------------|--|
| Load regulation            | .8% or less (measured at logic bd.)          |
| Load regulation            | .015% or less (measured at power supply bd.) |
| Line regulation            | less than .002%                              |
| Ripple and noise           | less than 4 mV peak to peak.                 |
| Load transient response    | less than 40 usec.                           |
| Minimum adjustment range   | .65 V.                                       |
| Worst case adj. ranges     | refer to pg. 6                               |
| Max. cont. output current* | 8.5 amps.                                    |
| Current limiting           | 10A to 12.25A                                |
| Typical A.C. dropout       | 93 Vac                                       |
| +12V crosstalk             | 20 mV peak to peak                           |
| Over-voltage protection    | none   |

+12V SUPPLY

|                             |  |
|-----------------------------|--|
| Load regulation             | .5% or less (measured at furthest drive) |
| Load regulation             | .015% (measured at power supply bd.)     |
| Line regulation             | less than .002%                          |
| Ripple and noise            | less than 6 mV peak to peak.             |
| Load transient response     | less than 40 usec.                       |
| Minimum adjustment range    | 1.5V                                     |
| Worst case adj. ranges      | refer to pg. 6                           |
| Max cont. output current*   | 4.25A                                    |
| Current lim. 0 to 6 secs.   | 10.6 to 13.15A refer to pg. 7            |
| Current lim. 6 to 15 secs.  | 7.15 to 8.8A "                           |
| Current lim. after 15 secs. | 5.25 to 6.4A "                           |
| Typical A.C. dropout        | 93 Vac                                   |
| +5V crosstalk               | 20 mV peak to peak V                     |
| Over voltage protection     | none                                     |

+16V UNREGULATED SUPPLY

Max. cont. current (average) .65A  
Nominal output voltage at 115 Vac; with both supplies fully loaded: 20 Vdc

-16V UNREGULATED SUPPLY

Max. cont. current (average) .65A  
Nominal output voltage at 115 Vac; with both supplies fully loaded: 18 Vdc

A.C. INPUT

|                |                  |                    |
|----------------|------------------|--------------------|
| 115V Operation | 98Vac to 128Vac  | 2.0A max @ 128 Vac |
| 230V operation | 196Vac to 256Vac | 1.0A max @ 256 Vac |

OPERATING AMBIENT TEMPERATURE RANGE 50' F to 120' F ( supply is equipped with a thermal protection switch )

\* Requires forced air cooling.

## (2). SPECIFICATION DEFINITIONS

This section outlines the proper test procedures to be taken to determine the performance characteristics of the 8397. To meet the specifications as stated in section 1 these measurement procedures must be adhered to. Additionally, the specifications presented are based on the actual system configuration. Any alteration of component placement or wiring may affect certain parameters.

Only the maximum current drain is defined for the +16V and -16V supplies, because these supplies are unregulated.

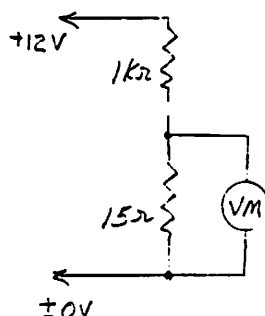
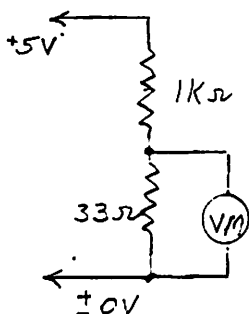
LOAD REGULATION : The following formula shall be used to determine load regulation.

$$\text{LD. REQ.} = \frac{\text{no load voltage} - \text{full load voltage}}{\text{full load voltage}} * 100\%$$

Due to the small differences between no load and full load voltages, a resistor voltage divider network had to be utilized in order to obtain more accurate measurements. The measuring instrument used was a 4 1/2 digit digital voltmeter set on the 200 mv. range. The voltage dividers required are illustrated below.

Note that all voltage readings should be taken quickly to minimize thermal effects.

Additionally, all specifications listed in section 1 are based on using new connectors which have not had more than 10 insertion cycles.



Load regulation was tested at two different locations for both the +5V supply and the +12V supply. The measurement points for the +5V supply were at the back side of the connector on the main logic board and at the back side of the output connector on the 8397 regulator board. Typical regulation figures as measured at the logic board are approximately .65%; the supply is specified at .8% or less. The load change used was from 0 amp to 4.25 amps. Typical regulation figures as measured at the regulator board are approximately .01%; the supply is specified at .015% or less. The load change used was from 0 amp to 8.5 amps.

The measurement points for the +12V supply were at the back side of the power connector on the disc drive located furthest from the regulator board, and at the back side of the output connector on the 8397 regulator board. Typical regulation figures as measured at the disc drive are approximately .4%; the supply is specified at .5% or less. The load change used was from 0 amp to 2.25 amps. Typical regulation figures as measured at the regulator board are approximately .01%; the supply is specified at .015% or less. The load change used was from 0 amp to 4.0 amps.

## (2). SPECIFICATIONS DEFINITIONS

LINE REGULATION : Line regulation is to be calculated based on the following formula:

$$\text{Line Reg.} = \frac{\text{change in D.C. output voltage}}{\text{change in A.C. input voltage}} * 100\%$$

The A.C. voltage is to be changed from 98 Vac to 128 Vac as measured at the A.C. plug that inserts into the VARIAC. Both of the supplies are to be continuously loaded, the +12V supply should have a load of 4 amps and the +5V supply should have a load of 8.5 amps.

Again, due to the small voltage variations, the voltage dividers as outlined in the load regulation section must be used.

Typical line regulation figures for both the +12V and +5V supplies are approximately .0002%; the supply is specified at .002% or less.

RIPPLE AND NOISE : Ripple and noise is to be measured following the conditions listed below:

1. Both the +12V and +5V supplies are to be continuously loaded using the following loads; +12V with a 4.0 amp load, +5V with a 8.5 amp load.
2. A 75 MHZ. or faster scope with a 'times' 1 probe is to be used to take measurements.
3. Measurement locations are the back side of the output connector on the regulator board.
4. A nominal line voltage of 115Vac is to be used.
5. The scope's ground connection is to be disconnected from the wall outlet and the ground connection shall be made via the ground connection at the probe end using a ground wire which is not more than 4 inches in length. To maintain adequate safety precautions the scope case should be grounded to the supplies ground via a separate wire incorporating a series resistor of 10 ohms.

LOAD TRANSIENT RESPONSE AND CROSSTALK : The typical response time for both supplies is approximately 20 micro-seconds; the supply is specified at 40 micro-seconds or less. The load step change for the +5V supply is from 5 amps to 8.5 amps while the step change for the +12V supply is from 2 amps to 4 amps.

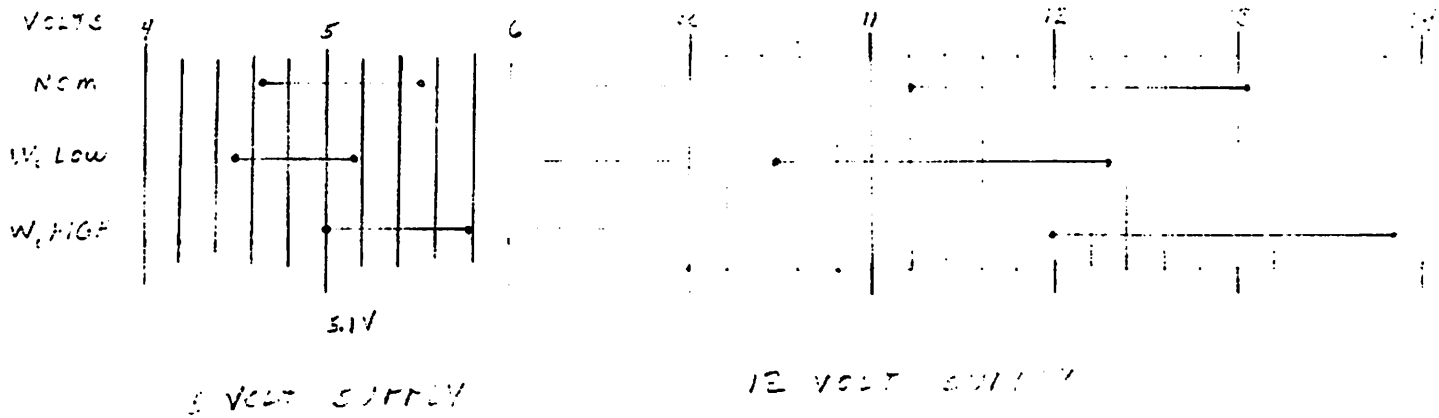
Only one supply at a time is to be tested while the other supply has a continuous maximum load as specified in section 1.

The response time is to be measured from the moment the supplies output voltage changes to the time the output voltage reaches 5% of its new steady state voltage. All measurement points are to be taken at the back side of the output connector on the 8397 board.

While one supply is being tested for transient response, the other supply can be monitored for the amount of induced crosstalk. The crosstalk figures indicated in section 1 do not include the normal ripple and noise voltage associated with the particular supply. Therefore, the total noise is the summation of the crosstalk and the ripple & noise voltage.

## (2). SPECIFICATION DEFINITIONS

WORST CASE ADJUSTMENT RANGES : The following graphs best describe all possible worst case adjustment conditions which could exist regarding the supplies adjustment. From the graphs it can be deduced that the worst case range for the +5V supply will be at least .65V, while for the +12V supply it will be 1.5V.



MAXIMUM CONTINUOUS OUTPUT CURRENT : The maximum load specifications as stated in section 1 are based on forced air cooling conditions. The supply can be operated continuously at these loads with an input voltage of 128Vac, and at an ambient temperature of 120' F as long as the fan is functioning properly. In the event the fan becomes defective, the supply will shut down automatically once the internally equipped thermal switch reaches a temperature of 95 C +4 C.

After the thermal switch cools down to approximately 65 C the unit will power back up, assuming of course that the power switch is still in the on position.

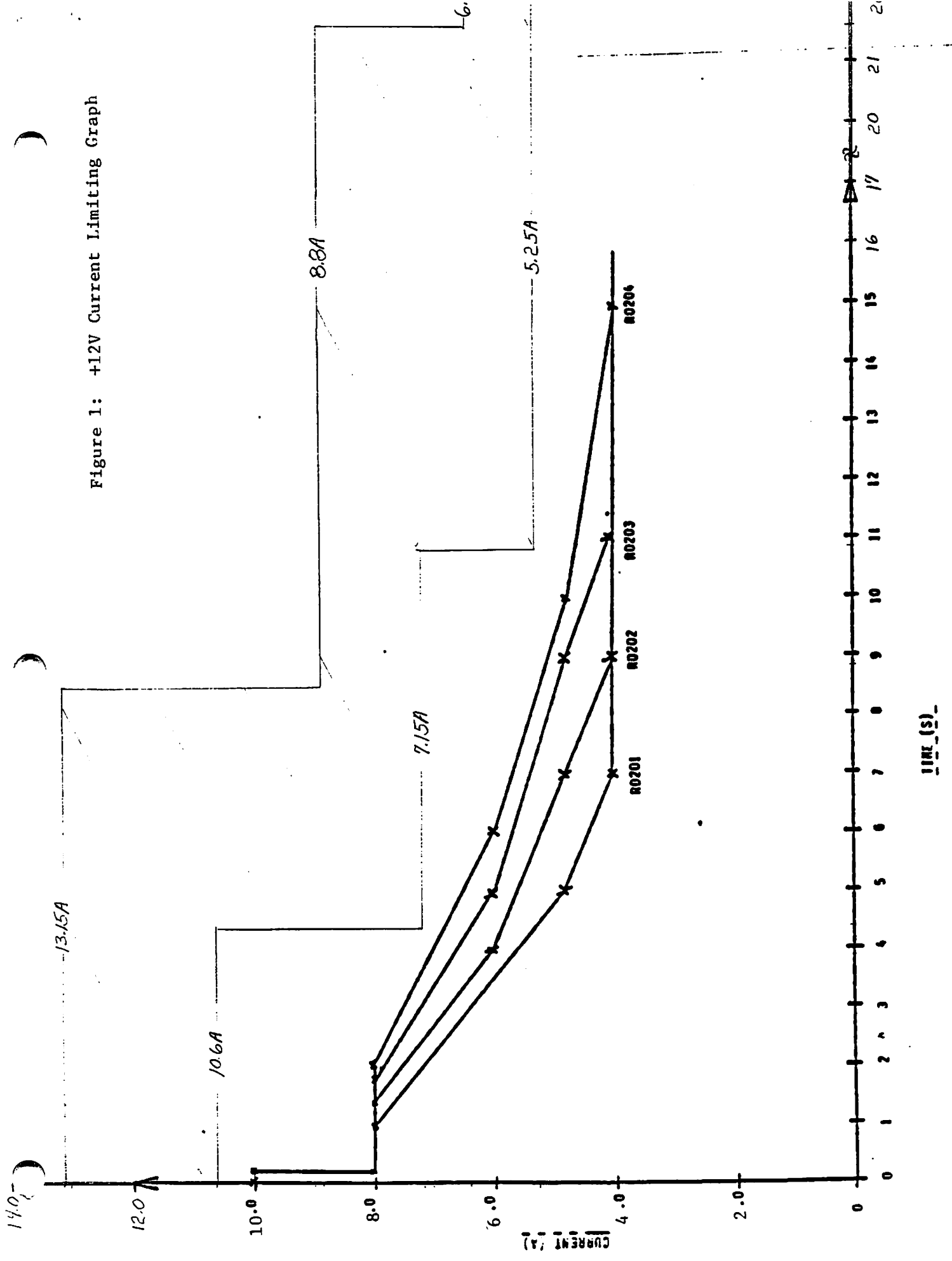
If the fan is defective the unit will stay powered on for approximately 5 to 15 minutes before shutting down. The input line voltage, the ambient temperature, the system configuration ( which manufacturer drives are installed ), and the placement and orientation of the system all effect how long the unit will remain powered on should the fan die.

CURRENT LIMITING : The current limit specifications as outlined in section 1 describe the load where the output voltage just begins to decrease, this point is more commonly referred to as the foldback knee. The +5V supply has a knee point of somewhere between 10 amps to 12.25 amps.

The +12V supply however is not so easily described, instead, a graph will be provided (on next page ) which will yield a clearer picture of the foldback characteristics. Actually, the supply cannot provide good regulation at the stated current level for the first initial six seconds, the current limiting is only set this high to allow for the high initial surge during start-up caused by the drives. The worst case condition occurs when two Rodime fixed drives ( model R0204 ) are used.

It's very important to realize that to meet these specifications as outlined in section 1; R2, and R3 must be properly mounted as illustrated in figure 2 (pg. 8). Don't be deceived, these resistors have very low resistance, and consequently the leads themselves contribute to the overall resistance.

Figure 1: +12V Current Limiting Graph



(2). SPECIFICATION DEFINITIONS

TYPICAL A.C. DROPOUT VOLTAGE : This is the input voltage at which the supplies output voltage has a total of 10 mv. ( peak to peak ) of ripple and noise. Both supplies are to be loaded at the respective maximum currents as defined in section 1. The typical dropout point for a new supply is approximately 93Vac. Even after 5 years the dropout voltage should not exceed 98Vac.

All A.C. voltage measurements are taken at the wall outlet.

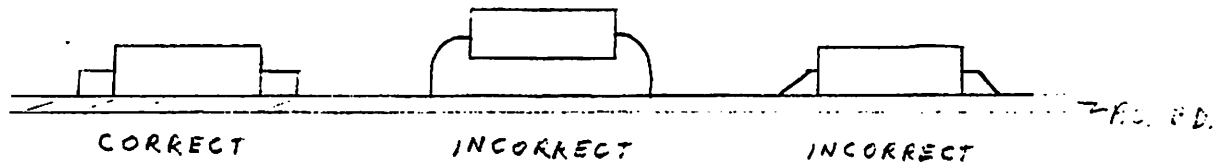


Figure 1 : Proper and improper mounting arrangements for resistors R2 and R3.



### (3). DESIGN NOTES

The 8397 regulator board has many similarities to the 7770 regulator board. Therefore, to eliminate a duplication of effort reference should be made to hardware manual #56 ( H.M. 56 ). This manual provides ample information concerning component selection and alternative circuits.

Topics to be discussed in this particular manual will be restricted to significant differences between the 7770 and 8397 regulator boards or items which are unique only to the 8397 board.

#### +5V SUPPLY DESIGN NOTES

The +5V circuit incorporated on the 8397 board is virtually an exact duplicate of the one used on the 7770 board.

Significant differences include:

1. The addition of a 16K ohm resistor ( R16 ) across R13. The purpose is to increase the output voltage by approximately .05V to compensate for the losses due to the power distribution cable. Recall that the 7770 board sensed the voltage at the load, in contrast to the 8397 board sensing the voltage at the power output connector.

2. The addition of a 470 ohm resistor ( R10A ) from L1 pin 3 to ground. This helps prevent hysteresis during current limiting foldback.

A hysteresis loop is when the external load must be significantly reduced beyond the point where foldback began in order for the supply to resume normal operation.

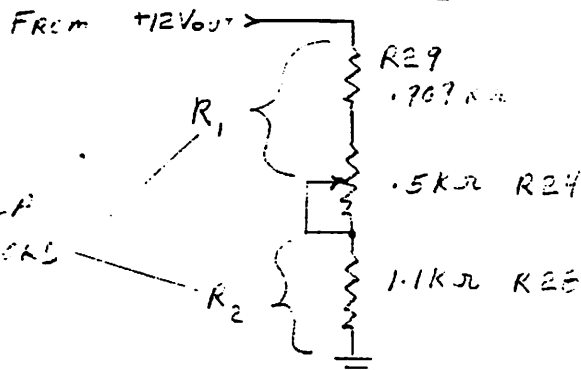
3. Instead of using a single 2210 ohm resistor from L1 pin 5 to ground; two resistors were utilized to form a voltage divider network to be used by the +12V foldback circuitry. The two resistors are 1.1K ohm ( R14 ) and 1.21K ohm ( R15 ). The +12V foldback circuitry will be more fully discussed at a later time.

#### +12V SUPPLY DESIGN NOTES

The configuration of the +12V supply is basically similar to the +5V supply. One major difference is the voltage divider network comprising R24, R28, and R29; instead of being connected to the non-inverting input of the 723 regulator the network is connected to the inverting input of the 723. This is necessary because the desired output voltage of +12V exceeds the 723's internal reference voltage ( approx. 7.15V ).

The formula for determining  $V_{out}$  and the actual resistor values used are indicated below:

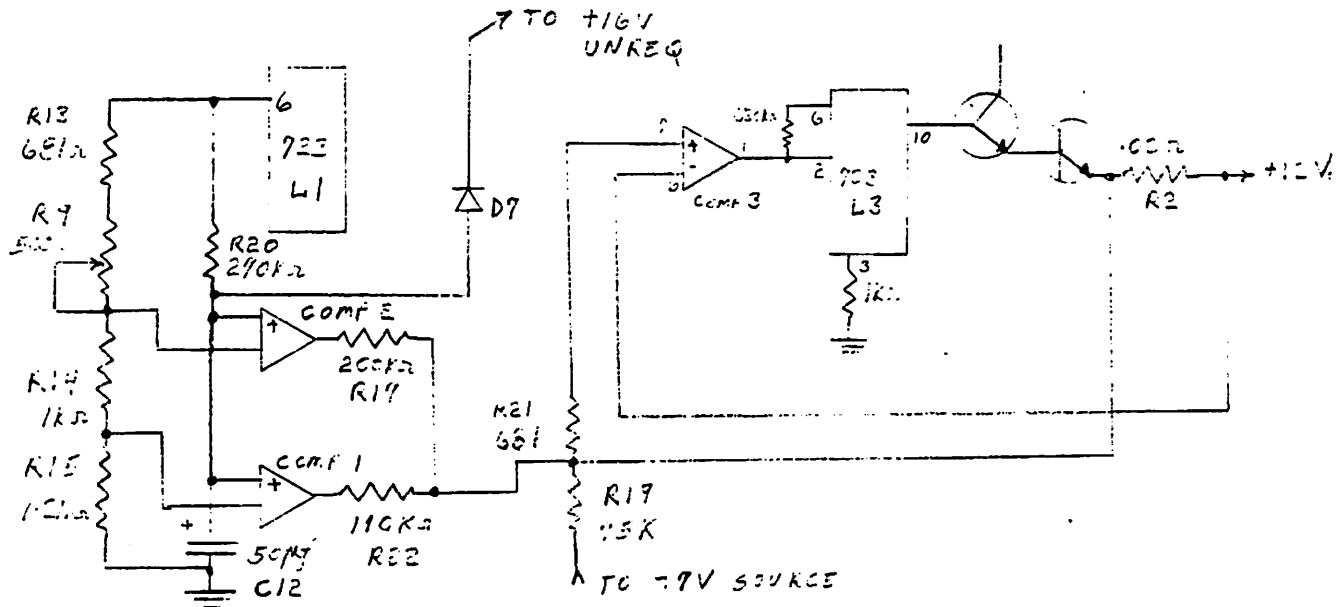
$$V_{out} = \frac{R_1 + R_2}{R_2} * V_{ref}$$



### (3). DESIGN NOTES

A second major difference between the +12V circuit arrangement and the +5V circuit is the fashion in which Q4 and L3 obtain their power. Since the required current is relatively low; typically about 45 ma, it was derived from a half-wave rectifier circuit operating at a higher voltage than that required for Q1. Consequently, the supply's efficiency was increased.

A third major difference is the unusual aspect of the +12V supply current limiting foldback circuitry. The circuitry involved is indicated below.



At initial power-on, the voltage across C12 will be approximately zero volts and consequently both Comp1 and Comp2 outputs will be low ( approx.  $-0.3V$  ). This effectively places R17, R19, and R22 in parallel and permits a higher current limiting value. The graph on page 7 best describes the foldback characteristics. The shaded portion indicates the area that the foldback knee may exist at any particular time.

It should be noted that the supply does not have the capability of providing a clean, regulated output voltage in excess of 10 amps. Should the current drain exceed this value during the first 6 seconds after power-on the output voltage will contain increased amounts of ripple. This is due to Q1's collector voltage being too low.

R20 and C12 comprise a timer circuit and after roughly 6 seconds, the voltage at L2 pin 9 will be approximately 2.75 volts. The other input to the comparator is obtain from the +5V regulator voltage divider network, which incorporates R14 and R15. When the +5V supply is adjusted for an output voltage of 5.05 volts, the voltage at pin 8 of L2 will be 2.75 volts.

At any rate, when the voltage at pin 9 exceeds that at pin 8 the comparator's output will switch to a high impedance state.

After about 6 seconds only R17 and R19 will be in parallel and thus yields the intermediate current limiting value between 7.15A to 8.8A.

After about 15 seconds the voltage at L2 pin 11 will exceed the 5.05 volts present at pin 10. As a result, the comparator's output ( pin 13 ) will go to the high impedance state and thus only R19 now controls the final current limiting value between 5.25A to 6.4A.

### (3). DESIGN NOTES

Diode D7 is used to discharge C12 during power down so that the same current limiting curve can be obtain within a few seconds after powering down. The reason for stepping down the current limiting in this fashion was to reduce the cost, and weight of the supply while maintaining adequate protection for the supply should the output be shorted to ground. This was an alternative to designing a supply capable of providing a continuous 10 amps, which would require a much larger transformer and a corresponding heavier rectifier.

During initial power-on the fixed disk drive(s) exhibit high current surges, this can be seen on the graph on page 7, which illustrates the current versus time characteristics of two Rodime drives. This should fully explain the necessity of altering the current limiting value with respect to time.

#### AN ALTERNATIVE TO FUTURE DESIGNS

There are basically two major disadvantages of linear supplies as compared to switching supplies. The first disadvantage is the greater weight and the second disadvantage is the lower efficiency. Unfortunately, at the present time there is little that can be done to reduce the size of the linear transformer; which is the component contributing the most to the overall weight of the supply.

The efficiency can be improved by utilizing pass transistors which have very low saturation voltage, which was exactly what was done on the 7770 and 8397 boards. However, a future alternative might be to use a monolithic regulator being offered by National; part number LM-196-5. Besides being a single package device, this regulator requires only a 1 volt differential voltage. A definite plus in order to obtain the maximum efficiency possible.

Supposedly this part was to be released over a year ago, but as of 2/83 the part was still not available. Apparently, National encountered design problems, but nevertheless, it may prove valuable in future designs.

(4). TEMPERATURE MEASUREMENTS

The following indicated temperatures are based on the conditions outlined below.

1. The +5V supply is connected to an 8.5 amp load, and the +12V supply is connected to a 4.25 amp load. Both of these loads are to be located externally from the system cabinet.

2. All A.C. voltages are to be measured at the output of the Variac.

3. The thermal sensors are to be applied to the 2N5301 transistors using Eastman's 910 glue or equivalent. While the glue is drying, pressure is to be applied to the sensor to insure a good thermal connection with the transistor case; a small bladed screwdriver is a suitable tool for applying pressure. An accelerator can be used to reduce the drying time.

The sensors are to be located on the top side of the transistor base just in front of the mounting screw that is furthest from the fan.

4. The PAC10 thermal sensor is to be secured between the washer and the rectifier module with the retaining nut tightened to 10 in. lbs.

5. The FE16C thermal sensor is to be located between the rectifier's case and the flat rectangular washer.

6. The thermal switch sensor is to be located between the heatsink and the switch housing.

7. All temperatures are based on an enclosed unit standing vertically with the fan at the highest elevation. The back of the unit is to be located 6 inches from a vertical wall.

| Ambient temp.= 75 F    | (A) | (B) All temperatures in Fahrenheit |
|------------------------|-----|------------------------------------|
| +12V 2N5301 transistor | tba | 187                                |
| +5V 2n5301 transistor  | tba | 179                                |
| PAC10 rectifier module | tba | 140                                |
| Thermal switch         | tba | 141                                |
| FE16C rectifier module | tba | 175                                |
| P.C. bd. under Q1      | tba | 145                                |
| P.C. bd. under Q2      | tba | 147                                |

(A) 115 Vac input

(B) 128 Vac input

Harvey,

FYI

Wayne 12/2/83

TO: Dan Messuri  
Ken Samel  
Whom it May Concern

FROM: Don Logan  
Hardware Technical Writing

DATE: November 29, 1983

SUBJ: Review draft of theory of operation manual for the 2200 MVP  
2275 5-1/4" Winchester Floppy Disks Controller

Since it appears that this document is going to be much longer than I had originally expected, I am giving you 50 pages of text to review now, rather than waiting until the entire document is written. This should reduce the likelihood of you falling asleep while trying to review the manual. Those of you who are using this document for technical information should bear in mind that this is a review draft, and, as always, is subject to changes and corrections at the whim of the engineer.

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## Table of Contents

|          |  |      |
|----------|--|------|
| 2        | DPU Bus Architecture, Memory, and I/O.....   | 2-1  |
| 2.1      | Bus Overview.....  | 2-1  |
| 2.2      | Memory.....  | 2-5  |
| 2.2.1    | ROM and Memory Mapped Status Port.....   | 2-5  |
| 2.2.2    | Dynamic RAM.....   | 2-6  |
| 2.2.2.1  | Generating /RAS.....   | 2-7  |
| 2.2.2.2  | Generating Read and Write Enable Signals.....  | 2-11 |
| 2.2.2.3  | Memory Timing Logic and Memory Timing.....   | 2-13 |
| 2.2.2.4  | Cache Data Parity Generator/Checker.....   | 2-17 |
| 2.3      | Input/Output Ports.....  | 2-21 |
| 2.3.1    | DPU Status Ports and Z80A Command Ports.....   | 2-21 |
| 2.3.1.1  | Winchester Interface Status Port<br>(Input Port 00).....                                     | 2-21 |
| 2.3.1.2  | Winchester Interface Command Register 1<br>(Output Port 10).....                             | 2-23 |
| 2.3.1.3  | Winchester Interface Command Register 2<br>(Output Port 20).....                             | 2-25 |
| 2.3.1.4  | Set Controller Ready Port (Output Port 40)<br>Set Controller Busy Port (Output Port 50)..... | 2-26 |
| 2.3.1.5  | 2200 Data Input Register (Input Port 60).....  | 2-28 |
| 2.3.1.6  | 2200 Data Output Register (Output Port 70).....  | 2-29 |
| 2.3.1.7  | Floppy Interface Command Register<br>(Output Port C0).....                                   | 2-31 |
| 2.3.1.8  | Floppy Controller Reset Port<br>(Output Port D0).....  | 2-32 |
| 2.3.1.9  | DPU System Status and Options Port<br>(Input Port E0).....                                   | 2-33 |
| 2.3.1.10 | Issue Floppy Terminal Count Port<br>(Output Port F0).....                                    | 2-34 |
| 2.3.2    | Programmable I/O Devices.....  | 2-35 |
| 2.3.2.1  | 9517-4 DMA Controller.....   | 2-35 |
| 2.3.2.2  | Z80 Counter Timer Chips.....   | 2-44 |

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| <u>List of Figures</u> |   | <u>Page</u> |
|------------------------|---|-------------|
| 2-1                    | Block Diagram of the DPU Bus Structure..... | 2-2         |
| 2-2                    | Generating /RAS.....                        | 2-8         |
| 2-3                    | Generating RDEN.....                        | 2-12        |
| 2-4                    | Write-Enabling the Cache.....               | 2-12        |
| 2-5                    | Memory Timing Logic.....                    | 2-14        |
| 2-6                    | Z80A Memory Timing.....                     | 2-16        |
| 2-7                    | Winchester Memory Timing.....               | 2-18        |
| 2-8                    | Cache Data Parity Generator/Checker.....    | 2-19        |

| <u>List of Tables</u> |   | <u>Page</u> |
|-----------------------|---|-------------|
| 2-1                   | How the Z80A interprets input from the<br>Winchester Interface Status Port.....   | 2-22        |
| 2-2                   | Effects of Z80A output to Winchester<br>Interface Command Register 1.....   | 2-24        |
| 2-3                   | Effects of Z80A output to Winchester<br>Interface Command Register 2.....   | 2-26        |
| 2-4                   | Effects of Z80A output to the Floppy<br>Interface Command Register.....   | 2-32        |
| 2-5                   | How the Z80A interprets the BD0-BD4 inputs<br>from the DPU System Status and Options Port.....                          | 2-33        |
| 2-6                   | How the Z80A interprets the BD5-BD7 inputs<br>from the DPU System Status and Options Port.....                          | 2-34        |
| 2-7                   | Addressing the DMA Controller's Base and<br>Current Address Registers and Base and<br>Current Word Count Registers..... | 2-40        |
| 2-8                   | Programming the DMA Controller Command Register.....  | 2-40        |
| 2-9                   | Programming the DMA Controller Mask Register.....   | 2-41        |
| 2-10                  | Programming the DMA Controller Mode Registers.....  | 2-42        |
| 2-11                  | DMA Controller Master Clear and Write All<br>Mask Register Bits commands.....   | 2-43        |
| 2-12                  | DMA Controller ports addressable by<br>firmware but not used.....   | 2-44        |
| 2-13                  | Addressing and programming the Z80<br>Counter Timer Chips.....  | 2-45        |

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## 2. DPU Bus Architecture, Memory, and I/O

Before looking at how each of the subunits of the DPU functions, it is necessary to look at how information is transferred between these subunits and to look at how these transfers are controlled. This chapter examines the bus architecture of the DPU and discusses the DPU subunits that connect directly to the buses, focusing mainly on memory and I/O.

### 2.1 Bus Overview

Fig 2-1 is a block diagram of the DPU bus structure. While this diagram shows most of the hardware that is connected to the buses, it does not show all of it. Hardware not shown is discussed at the end of this section. The Main Data Bus, DB0-7, and the Main Address Bus, AB0-15, are controlled by the Z80A CPU (2I13) and, under the direction of the Z80A, by the 9517A DMA controller (2I7). Because the DMA controller has only eight address outputs, it must use the DMA Controller High-Order Address Latch (2J10) to form a 16-bit address. The DMA controller writes the high-order byte of the address into the latch, whose outputs are connected to the high-order address bus, and then uses its own eight address outputs to form the low-order byte.

Information flow on the main data and address buses is controlled by the Z80A and the DMA controller. The Z80A operates under the direction of the firmware stored so lovingly in the 8K X 8 ROM (2H10) by that brilliant software engineer, Ken Samel. The DMA controller operates under the direction of the Z80A. The data cache, a 64K X 9 dynamic RAM (3J2-3J99), may be addressed by either the Z80A or the DMA controller through the DMA pointer (3G12-3K12). This pointer is transparent to both the Z80A and the DMA controller and is used by the microsequencer to address the cache during Winchester operations. The DMA pointer and the microsequencer are discussed in



detail in the section on Winchester disk read operations. The row address is gated to the cache from the low-order address bus through the Row Address RAM Driver, L42 (3I11), and the column address is gated to the cache from the high-order address bus through the column address RAM driver, L44 (3G11). This hardware is discussed in more detail in the next section.

When the Z80A or the DMA controller address the data cache, data is transferred over the Main Data Bus and the Memory Data Bus through the Main/Memory Data Bus Transceiver, L63 (3G9). The Memory Data Bus is also used by the Winchester control logic to transfer data to or from the cache during read, write, and format operations using a DMA operation. Winchester disk data is transferred to and from memory over the Disk Data Bus and the Memory Data Bus through the Memory/Disk Data Bus Transceiver, L80 (3G7). Because the memory data bus is used by both the Z80A and the Winchester control logic, and since a large portion of the Winchester operations are controlled by the microsequencer while the Z80A marks time, great care has been taken to ensure that the Z80A cannot perform a memory operation when the Winchester control logic is using the cache.

The Z80A controls the Winchester disk drive (or drives) through a pair of I/O ports called the Winchester Interface Command Registers (3D4 and 4H13). Winchester drive status is available to the Z80A at the Winchester Interface Status Port (4I12). I/O ports are selected by a pair of address decoders (not shown), and are discussed in greater detail in the section on I/O ports. The Z80A also addresses the DMA controller and both Z80 CTCs (2C13-2E13) as I/O ports. In addition to performing timing functions for the Z80A, the CTCs function as programmable interrupt prioritizers.

Four DPU system status signals and four options status signals are available to the Z80A through the DPU System Status and Options Port (2E8). Firmware instructs the Z80A to read this port in order to determine what types of disk drives are connected to the DPU. Four switches are connected to this port, and these switches are set to

indicate to the firmware what type of devices it is controlling.

If the removable drive is a mini-floppy, the DPU board will contain a floppy disk controller chip (6H7). This chip is addressed by the Z80A and the DMA controller as an I/O port. It is programmed by the Z80A over the Main Data Bus. Floppy disk data is transferred between the cache and the floppy controller by the DMA controller over the Main Data bus and the Memory Data Bus. Floppy control lines that are not manipulated directly by the floppy controller chip are handled by the Z80A through the Floppy Interface Command Register, L56 (6J4).

The two I/O ports in the bottom right-hand corner of Fig 2-1 allow the Z80A and the DMA controller to communicate with the 2200. The bus nomenclature used here can lead to some confusion. Note that data comes onto the Main Data Bus through the 2200 Data Input Register (3D12) over the Buffered 2200 Output Data Bus. The 2200 buses are named from the 2200's perspective, while ports on the DPU board are named from the DPU's perspective. Thus, the 2200 output bus is connected to a DPU input register, and the 2200 input bus is connected to a DPU output register.

Commands bytes from the 2200 are read and echoed by the Z80A, while block data transfers to and from the 2200 are handled by the DMA controller. The DPU is interfaced to the 2200 through either a Triple Controller Board or a single-connector Disk Interface Board and therefore does not need to decode address information on the 2200 address bus. The controller or interface board handles address decoding, and generates signals to let the DPU know when its services are being requested.

Not shown in Fig 2-1 is the Address Mark Status Port. This memory mapped I/O port, when addressed by the Z80A, places two bits of information on the main data bus: address mark status and header check status. These signals are discussed in the section on Winchester disk read operations. Also not shown is the data cache parity generator/checker, L29 (2E3), which is connected to the memory data

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bus. This circuit adds a ninth, parity bit to each byte of data as it is written into the cache, and checks the parity of each byte as data is read from the cache. A non-maskable interrupt is generated when a parity error is detected.

Winchester header data is checked by an 8-bit comparator, L82 (4G8). Header information stored in the data cache by the Z80A is presented to the comparator over the Memory Data Bus, and header information read from the disk is presented to the comparator from the outputs of the serial/parallel converter over the D' data bus. The output of the comparator is used by the Winchester control logic to determine if the head is over the desired sector.

One final piece of hardware connected to the Disk Data Bus but not shown in Fig 2-1 is the 4E/00 bus driver, L75 (4E2). This driver, when enabled by the microsequencer, places a byte of either 4EH or 00H onto the disk data bus. These bytes are routed over the Disk Data Bus to the parallel/serial converter and written onto the disk, where they provide the 4EH filler bytes and the 00H phase locked oscillator synchronization fields. Memory space is saved and execution time is shortened by not requiring the Z80A to write these bytes into the data cache and then have them transferred to the disk.

## 2.2 Memory

DPU memory consists of 8K-bytes of UV-erasable PROM, 64K-bytes of dynamic RAM, and one memory mapped status port. This section looks at how and when each of these segments of memory are accessed.

### 2.2.1 ROM and Memory Mapped Status Port

Z80A firmware is stored in a 2764-2 8K X 8 EPROM that occupies memory locations 0000H through 1FDFH (8,160 bytes). The last 32 bytes of ROM are not used and are not addressable. When the Z80A outputs an

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address between 000H and 1FDFH, the 1Y2 output of decoder L47 (2J3) is forced low, asserting /PROMSEL and bringing the ROM /CE input low. The ROM output is enabled when the Z80A brings its /MREQ output low. Note that when ROM is being addressed, the pin 9 input of NAND gate L81 is forced low and /RAMSEL is forced high, ensuring that ROM and RAM cannot be addressed simultaneously. ROM is only addressed by the Z80A, and only during an instruction fetch cycle.

The memory mapped status port occupies memory location 1FE0H. When the Z80A performs a read of this address, the 1Y0 output of decoder L47 goes low, asserting /AMST. Since /RD is also low, the pin 8 output of OR gate L8A is forced low, asserting /AMSTEN. /AMSTEN enables the pin 6 and pin 11 outputs of buffer L60 (4E6 and 5B6), placing the status of the header check circuit on Main Data Bus line DB2 and the status of the address mark detection circuit on DB1. These signals are used during Winchester operations and are described in more detail in the section on Winchester disk read operations. When the Z80A writes to this address (1FE0H) with bit DB7 set, the rising edge of /WR clocks a one into the 2D input of flipflop L144 (2E3). The Z80A always reads from RAM immediately after setting this flipflop, forcing ZDISABLE to be asserted and cutting the Z80A off from dynamic memory. ZDISABLE is discussed in more detail in the next section.

### 2.2.2 Dynamic RAM

The disk data cache consists of nine, parallel 4864 64K X 1 DRAMs. Data is stored in L17 through L10, with the least significant bit stored in L17, and L9 stores parity information. The largest block of memory is divided into eight, 16-sector Winchester data caches and an 18-sector floppy data cache. Other blocks of memory are reserved for storage of data to be written to a disk, storage of read-after-write data, and as work space for the ECC correction routine. Additionally, certain blocks are reserved as scratchpad memory for the Z80A. Memory allocation is covered in detail in the

chapter on firmware.

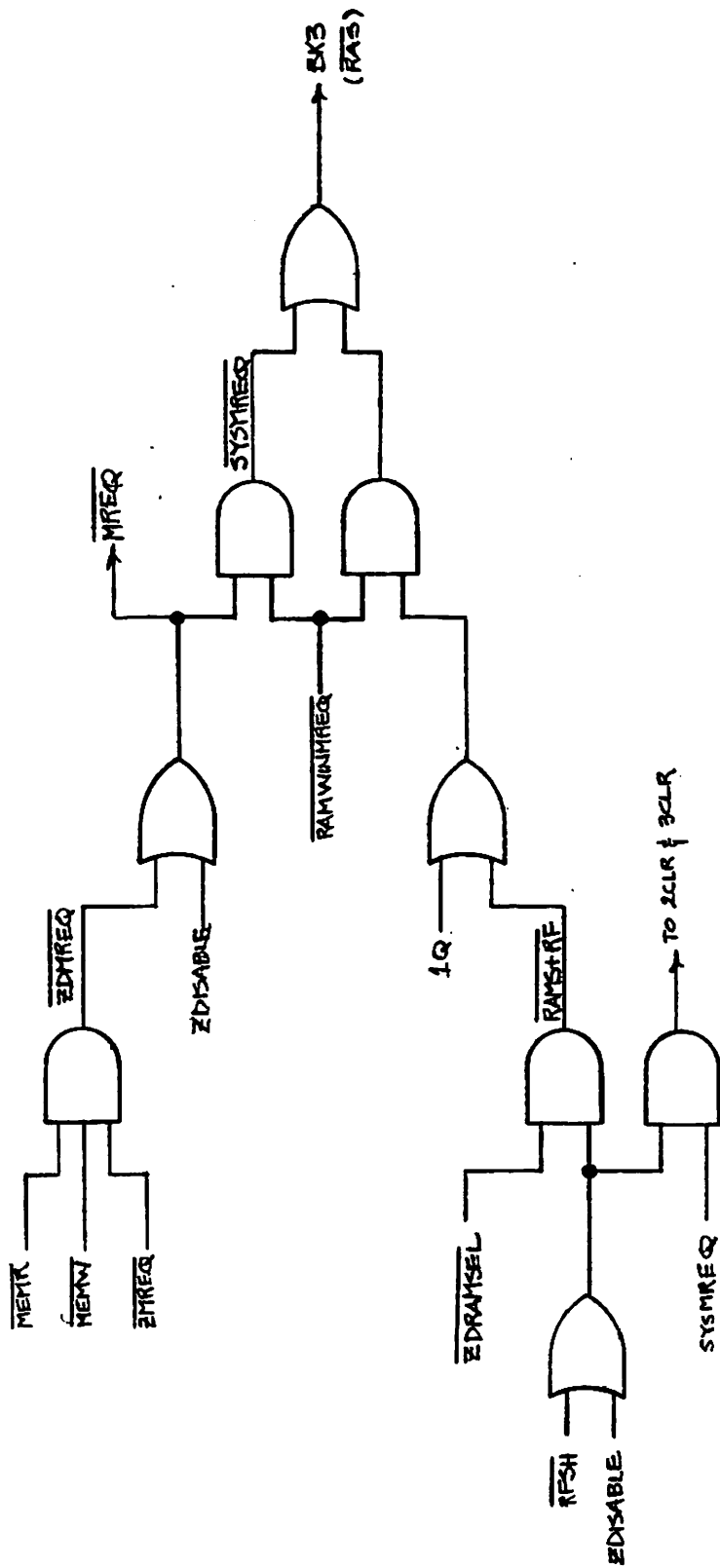
This section looks at the logic that generates the memory timing signals used to control addressing and data transfers. Because of the large number of logic gates and flipflops used to perform these control tasks, it is difficult to see by inspection exactly how memory is controlled. Therefore, the memory control logic has been broken down into several subunits. Each of these subunits is discussed in detail before turning to the general subject of memory timing.

Sixteen address bits are required to directly address 64K-bytes of memory; however, the 4864 DRAMS have only eight address inputs. These inputs are multiplexed to allow two 8-bit addresses to be gated into the chip to form, internally, a 16-bit address. The two 8-bit address segments are gated into the DRAMs by a pair of memory control signals: /RAS and /CAS. The falling edge of the active-low Row Address Strobe signal, /RAS, gates an 8-bit row address into each DRAM. This address is analogous to the low-order address byte in a static RAM. The falling edge of the Column Address Strobe signal, /CAS, gates an 8-bit column address into each DRAM. This address is analogous to the high-order address byte in a static RAM.

#### 2.2.2.1 Generating /RAS

Fig 2-2 shows a schematic of the gates used to generate the /RAS control signal. /RAS is asserted any time that either the Z80A or the DMA controller reads from or writes to the cache. The Winchester control logic also asserts /RAS when taking data from the cache and storing it on a disk or when storing data read from the disk in the cache. Additionally, the Z80A generates /RAS during what is called the '/RAS-only' refresh cycle. /RAS logic also ensures that the Z80A cannot generate /RAS or turn off /CAS when the Winchester control logic is reading from or writing to the cache.

During periods when no device is accessing memory and no



Winchester operation is in progress, /MEMR and /MEMW (from the DMA controller), /ZMREQ, /RFSH, and /ZDRAMSEL (from the Z80A), and /RAMWINMREQ (from the Winchester control circuitry) are all in the inactive high states. The input marked lQ, which comes from the Q output of flipflop L64, is at logic zero. (This signal will be looked at in detail in the section on timing logic). ZDISABLE, which is used to shut the Z80A off from dynamic memory, is in the inactive low state. /ZDMREQ is therefore in the inactive high state, forcing /MREQ, and /SYSMREQ to be in the inactive high states. Note that since /SYSMREQ is high, SYSMREQ is low and the CLR inputs to both flipflops in L31 are held low. Finally, /RAMS+RF is in the inactive high state and, therefore, /RAS is in the inactive high state.

When the Z80A performs a cache read or write operation, both /ZMREQ and /ZDRAMSEL are forced low, in turn asserting /ZDMREQ, /MREQ, /SYSMREQ, /RAMSEL+RF, and /RAS. At the end of the memory cycle, /ZMREQ returns high, lQ is forced high, and /RAS is forced to return high. A short time later, /ZDRAMSEL returns high, lQ again goes low, and the /RAS generator circuit returns to the inactive state. /RAS is generated in essentially the same manner when the DMA controller performs a cache read or write operation. Instead of asserting /ZMREQ, however, the DMA controller pulls either /MEMR or /MEMW low.

Each time the Winchester control logic is ready to read a byte from the cache or write a byte into the cache, it pulls /RAMWINMREQ low, in turn asserting /SYSMREQ and /RAS. Since ZDISABLE is in the active high state when Winchester operations are in progress, the state of /ZDMREQ has no effect on /RAS. In general, neither the Z80A nor the DMA controller can access the cache during Winchester operations. (As always, there is an exception to the rule, and it is discussed in the section on formatting the Winchester).

Before discussing how /RAS is generated during a refresh cycle, a brief review of 'RAS only' refresh is presented. Those who are thoroughly familiar with dynamic memory may wish to skip this paragraph and the next two paragraphs (except Dan, since he has to

review them). The value of a bit of information stored in a dynamic memory cell is indicated by the presence or absence of a charge stored in the capacitance between a transistor gate and the substrate. Because of charge leakage, each cell must be refreshed, or recharged, periodically to avoid losing information. Only those capacitances that are currently holding a charge are recharged, the rest remain discharged.

Memory on a single chip is arranged in 128 rows of data cells. Each row has 512 data cells, or columns, for a total of  $128 \times 512 = 65,536$  data cells. Columns can be further divided into two, 256-cell groups that may be thought of as a right and a left bank. To address a single cell within a chip, an 8-bit row address and then an 8-bit column address are gated into the chip. When a row address is strobed into the chip, the seven least significant bits are decoded to select one of the 128 rows. The eighth and most significant bit is not looked at until the column address is strobed into the chip. At this time, the eighth bit is used to select either the left or the right bank of data cells, and the column address is decoded to select one of the 256 columns in that bank. Also, at this time, the chip's data output is enabled, provided that the write enable input is not active.

Each time a row is addressed, all 256 data cells in that row are refreshed. Since memory access is random, there is no guarantee that every row will be addressed within the 2-msec time limit. The CPU therefore sequentially addresses each row at least once every 2-msec. In practice, each row is addressed far more often than this. To perform a refresh, the Z80A outputs a refresh address on its A0-A6 outputs in conjunction with /RFSH and /MREQ. This 7-bit address is decoded by the each memory chip, refreshing all 512 cells in the addressed row. The Z80A automatically performs a refresh cycle after every opcode fetch. One reason for arranging data cells as 128 rows by 512 columns rather than 256 rows by 256 columns is that the former requires only 128 refresh cycles every two msec while the latter requires 256.

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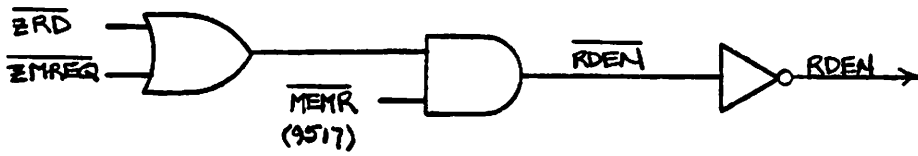


During refresh, memory timing logic is prevented from generating /CAS, since no column address is provided and no data output is needed. The write enable input is also held at the inactive high level. /RAS is generated in the same manner for refresh as it is for a normal Z80A read or write from the cache. The only difference is that when /RFSH is asserted, the CLR inputs of both flipflops in L31 are held low, and /CAS is not generated. Since the timing logic is held cleared, lQ remains low, and /RAS is not deactivated until both /ZMREQ and /ZDRAMSEL return high. Note that /RFSH is ORed with ZDISABLE to prevent the Z80A from shutting down the memory timing logic when the Winchester logic is active.

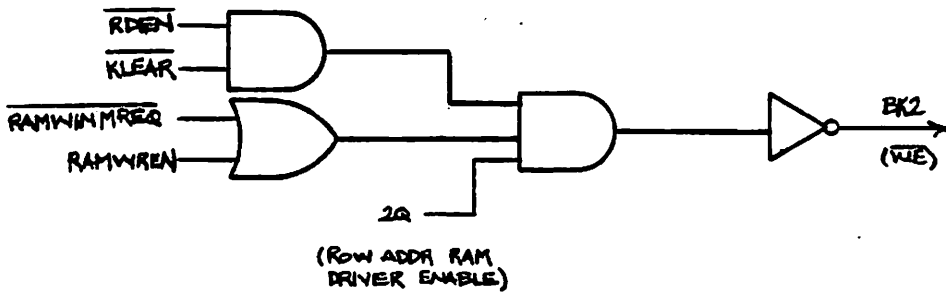
#### 2.2.2.2 Generating Read and Write Enable Signals

The RDEN signal is generated by the circuit shown in Fig 2-3. This signal, or its complement, is used to control the direction of information flow between the Main and Memory Data Buses, to aid in developing the write enable signal, and to let the cache data parity generator/checker know whether it should be generating parity or checking it. When RDEN is false (low), a write operation is in progress and data flows from the Memory Data Bus to the Main Data Bus. Data can then be gated from the Main Data Bus into either the Z80A or the DMA controller.

When RDEN is true, data flows out of either the Z80A or the DMA controller onto the Main Data Bus, and from there onto the Memory Data Bus and into the cache. Note that the status of RDEN is irrelevant if either /ZDRAMSEL or /MREQ is high, since the Main/Memory Data Bus Transceiver is then disabled. RDEN is only active when the Z80A or the DMA controller is attempting to read data from the cache. In this case, either /ZRD and /ZMREQ will both be low or /MEMR will be low. When data is being written into the cache, or when no operations are being performed on the cache by the Z80A or DMA controller, RDEN is in the inactive low state.



2-3 Generating RDEN



2-4 Write-Enabling the Cache

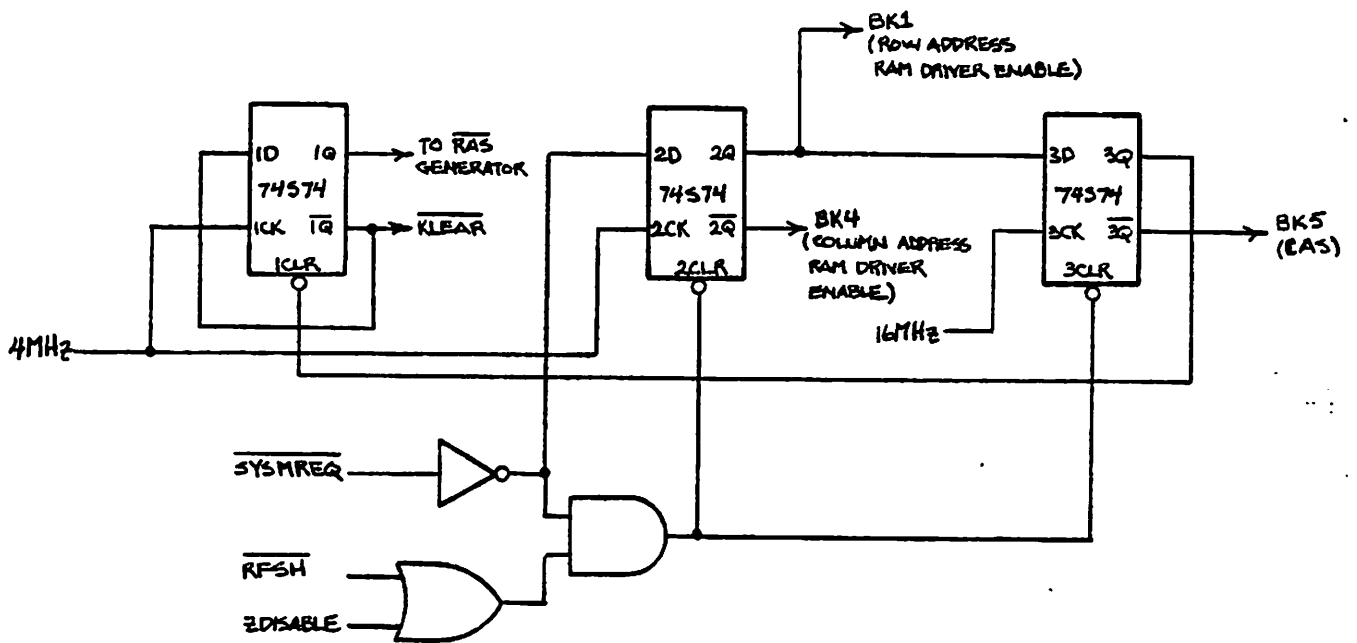
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Signals and gates used to write-enable the cache are shown in Fig 2-4. When any of the inputs to the 3-input AND gate are low, /WE is in the inactive high state. When the Z80A or DMA controller is writing data into memory, /RAMWINMREQ remains high and holds the middle input at logic 1. Since a write operation is in progress, /RDEN is in the inactive high state. /KLEAR, as the section on memory timing will show, is in the inactive high state until the end of a write operation, and the top input is therefore at a logic one. The 2Q signal is therefore responsible for asserting /WE. 2Q is part of the timing control logic, and goes high to enable the gating of the column address into the DRAMS. /WE is asserted roughly 125 nsec after /RAS and roughly 125 nsec before /CAS.

When the Winchester control logic is transferring information from a disk drive to the cache, RAMWREN is active high. As with a Z80A write operation, the 2Q signal is responsible for generating /WE. The timing is equivalent to a Z80A write operation. If the Winchester logic is reading information from the cache and storing it on a disk, RAMWREN will be inactive. When the Winchester logic signals a memory operation by bringing /RAMWINMREQ low, the middle input of the 3-input AND gate will be forced low and /WE will not be asserted. The /KLEAR input is responsible for deactivating the /WE signal at the proper time for all memory write operations. /KLEAR returns low when /RDEN returns low, in the case of a Z80A or DMA memory write, or when /RAMWINMREQ returns high, in the case of a Winchester memory write.

#### 2.2.2.3 Memory Timing Logic and Memory Timing

Memory timing is controlled by three flipflops, shown in Fig 2-5. Two of these flipflops are driven by a 4 MHz clock while the third is driven by a 16 MHz clock. These flipflops are shown in the figure in the same order as they are shown on the engineering prints (bottom center of page 2). For convenience, the leftmost flipflop will be designated flipflop 1 in this discussion, followed by



2-5 Memory Timing Logic

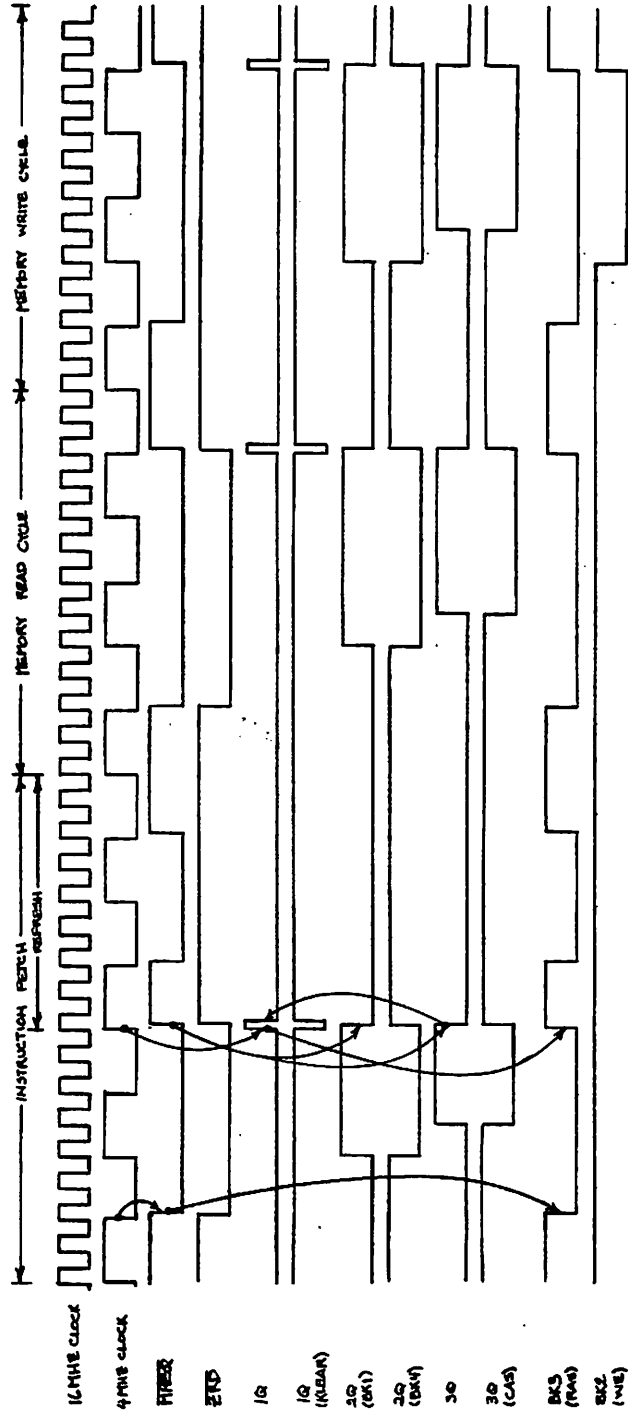
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flipflops 2 and 3. The Q output of flipflop 1, 1Q, is the source of the 1Q signal described in the section on generating /RAS. Similarly, the Q output of flipflop 2, 2Q, is the source of the 2Q signal mentioned in the previous section.

Prior to a cache read or write operation, the 2CLR and 3CLR inputs are held at logic zero. The 3Q output, in turn, holds the 1CLR input at logic zero. Fig 2-6 shows how these flipflops control the generation of memory timing signals for various Z80A memory operations. At the start of an instruction fetch cycle, the Z80A asserts /MREQ and /RD on the falling edge of the 4 MHz clock, forcing the /RAS generating logic to assert /RAS. Four gate delays later, the 2CLR and 3CLR inputs are raised to logic one, enabling flipflops 2 and 3. 2Q is connected to the enable input of Row Address RAM Driver L42, allowing the row address to be gated from the Main Address Bus to the inputs of the DRAMS. The falling edge of /RAS strobes the row address into the DRAMS. Note that the /2Q output holds the Column Address RAM Driver, L44, in the disabled state.

At the same time that the 2CLR and 3CLR inputs are raised to logic one, a logic one is presented to the 2D input of flipflop 2. The next rising edge of the 4 MHz clock clocks a one into the 2D input, forcing the 2Q and /2Q outputs to toggle. Row Address RAM Driver L42 is then disabled and Column Address RAM Driver L44 is enabled. The column address is then presented to the inputs of the DRAMS and given approximately 70 nsec to stabilize. Since 2Q is now at a logic one, the next rising edge of the 16 MHz clock forces the 3Q and /3Q outputs to toggle, asserting /CAS. 3Q raise the 1CLR input to a logic one, enabling flipflop 1. The next rising edge of the 4 MHz clock forces the 1Q and /1Q outputs to toggle, and 1Q immediately turns off /RAS. In the case of a write operation, /1Q, the source of /KLEAR, immediately turns off /WE. A short time after the rising edge of the 4 MHz clock, /MREQ and /RD return high, forcing the 2CLR and 3CLR inputs to clear flipflops 2 and 3. 3Q in turn clears flipflop 1, and the memory control circuits are all returned to their inactive states.

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2-6 Z80A Memory Timing

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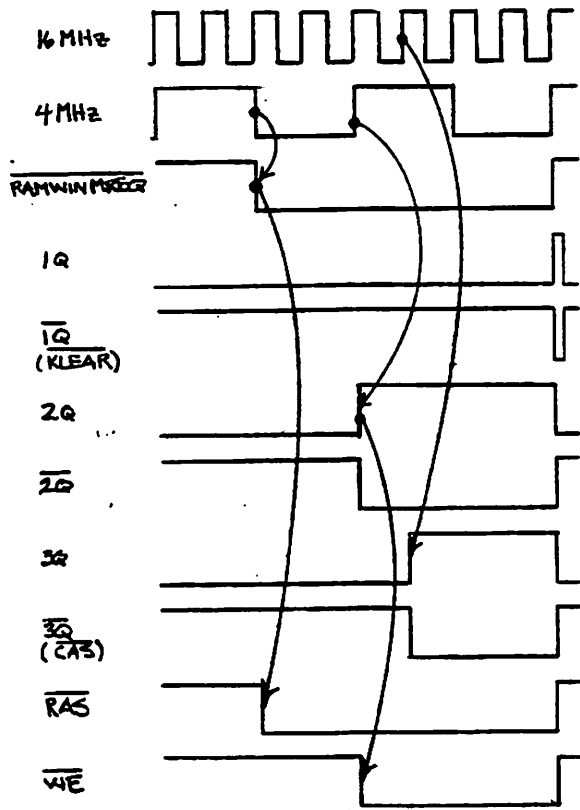
All instruction fetch operations are immediately followed by a /RAS only refresh cycle. It is here that the lQ signal plays an important role. According to the manufacturer's specs for the 4864 DRAMS, /RAS must remain high for a minimum of 100 nsec between memory operations. The /MREQ signal does not always return high after the instruction fetch cycle soon enough to meet this timing requirement. lQ is therefore used to turn /RAS off on the rising edge of the 4 MHz clock to allow for the 100 nsec /RAS precharge requirement. As the timing diagram shows, this timing problem only occurs between an instruction fetch and a refresh cycle.

During a refresh cycle, /RFSH goes low in conjunction with /MREQ and holds flipflops 1, 2, and 3 in the cleared state. /CAS cannot be asserted and the data outputs of the DRAMS are not enabled. /RAS simply follows /MREQ. Memory read and memory write cycles are similar to the instruction fetch cycle, but /RAS and /CAS are stretched out an extra 125 nsec. Winchester memory timing, shown in Fig 2-7, is identical to the instruction fetch operation just described, except that /RAMWINMREQ sets the ball rolling rather than /MREQ. Finally, memory timing under the direction of the DMA controller is identical to the timing of the memory read and write cycles for the Z80A, and is not shown.

#### 2.2.2.4 Cache Data Parity Generator/Checker

The circuit responsible for automatically generating and checking the parity of data stored in the cache is shown in Fig 2-8. The easiest way to see how this circuit works is to step through an example. Assume that a byte of 01H is to be written into the cache. Since /RDEN is high for a write operation, the signal named 'A' in Fig 2-8 will be at logic 1. During normal operation, REVP is in the inactive low state. (REVP is only activated during powerup diagnostics to check the operation of the parity circuit). The EXCLUSIVE OR of A (1) and REVP (0) is therefore true, and a logic 1 is presented to the I input of the parity generator chip.

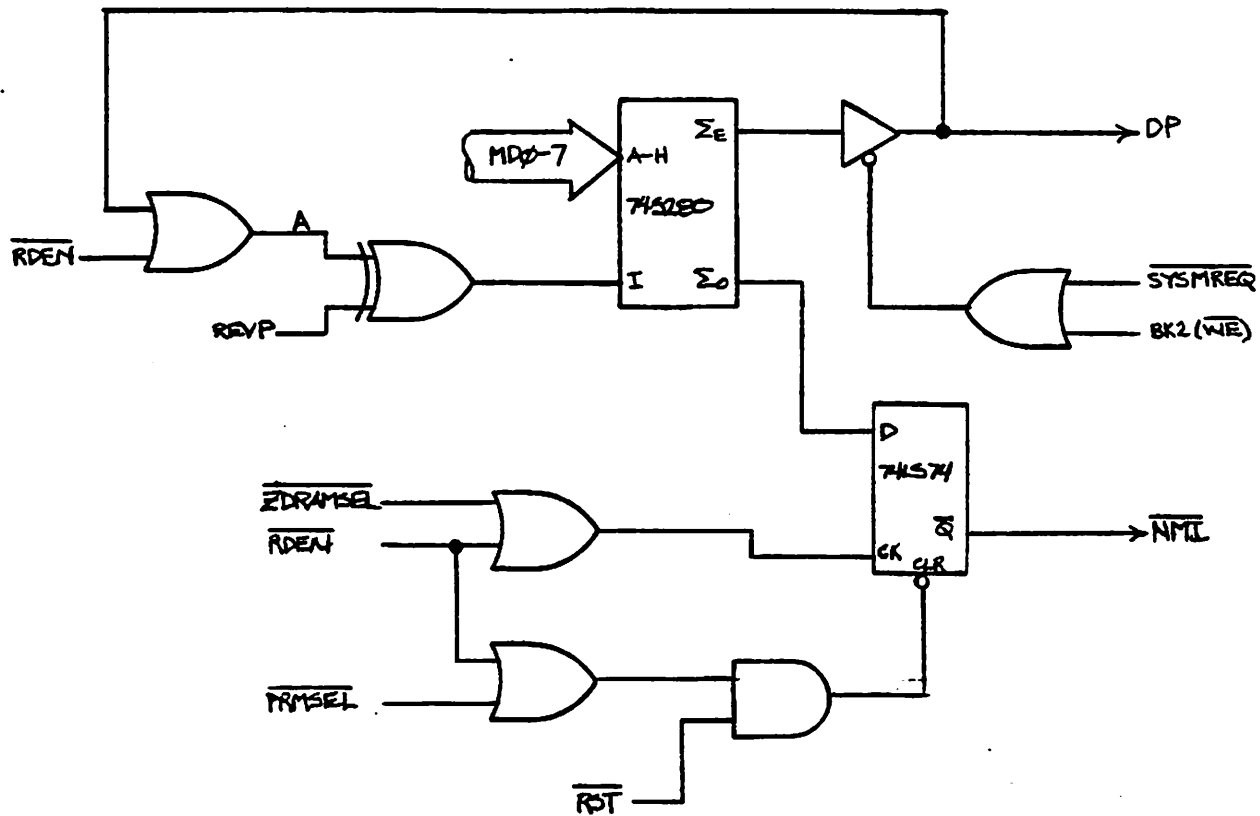
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2-7 Winchester Memory Timing

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2-8 Cache Data Parity Generator/Checker

Since the data byte has a single one, and since the I input is at logic 1, the EVEN output of the parity generator will be a logic 1. (The EVEN output is at logic 1 if an even number of inputs are at logic 1, and the ODD output is at logic 1 if an odd number of the inputs are ODD). During a write operation, both /SYSMREQ and /WE will go low, enabling the output of the parity buffer. The EVEN output of the parity generator is then connected to the data input of the parity DRAM. In this example, the parity bit is a logic 1.

When this byte is read from memory, /RDEN goes low, and the 'A' signal is forced to reflect the state of the parity bit. The EXCLUSIVE OR of the parity bit (1) and REVP (0) is a logic 1, and the EVEN output from the parity generator is again a logic 1. The ODD output from the parity generator is a logic 0. At the end of the read operation when /RDEN returns to the inactive high state, this zero is clocked into the D input of the flipflop. The /Q output remains high, and /NMI is not asserted.

If one of the DRAMS had failed, resulting in no ones in the data field instead of a single one, the ODD parity output would have been a logic 1. When the logic 1 was clocked into the flipflop, the /Q output would have gone low and /NMI would have been asserted. A parity error is defined as a fatal error. If a parity error is detected during the normal course of events, the board puts the cat out for the night and goes into an idle state.

During powerup diagnostics, the operation of the parity generator/checker is tested by writing data with reverse parity and then reading it back with normal parity. In the example used in this section, the EXCLUSIVE OR of 'A' and REVP during write with reverse parity would be a logic 0, since both 'A' and REVP are at logic 1. Because only one data bit is at logic 1 and the I input is at logic 0, the EVEN output would be logic 0. This zero would be stored in the parity DRAM as the parity bit. On read-back with normal parity, 'A' would be logic 0 and REVP would be logic 0, forcing the I input to the parity generator to be a logic 0. The ODD output from the parity

generator would therefore go high forcing a non-maskable interrupt. If a parity error does not occur during this test, the Z80A knows something is really hosed up. /NMI can be cleared either by a reset or a Z80A read from ROM. The interrupt is automatically cleared when the Z80A attempts to read the first instruction in the service routine (the interrupt vector), since /PRMSEL is necessarily asserted.

## 2.3 Input/Output Ports

I/O ports on the DPU board can be divided into two general categories: those that provide the Z80A with direct input of DPU status signals or allow the Z80A to directly manipulate DPU control signals, and those that interface the Z80A with programmable controllers, counters, and timers. This section examines each of these ports in detail.

### 2.3.1 DPU Status Ports and Z80A Command Ports

The Z80A monitors the DPU board through three input ports. These ports provide information ranging from the status of individual signals that allow the Z80A to make control decisions, to the statuses of groups of signals that allow firmware to determine what type of removable disk drive is currently plugged into the board. The Z80A outputs commands to non-programmable circuits on the board by writing to one of eight output ports. These ports provide the Z80A with a way to directly manipulate control signals. This section describes each of these eleven ports in detail.

#### 2.3.1.1 Winchester Interface Status Port (Input Port 00)

Five status signals from the Winchester drive (or drives) are made available to the Z80A at this port. If a removable Winchester disk drive is plugged into the board, it must share this port with the

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fixed Winchester drive. Only the selected drive will make status information available; outputs from a de-selected drive are floated by circuits in the drive. This port informs the Z80A whether or not the heads are over cylinder 0, alerts the Z80A to any conditions on the drive that might cause data to be written improperly, informs it when the drive is ready and when the heads are over the desired cylinder, and lets it know which drive is supplying the information to ensure that the correct disk drive is responding.

When the Z80A reads this port by outputting xx00 on the Main Address Bus and asserting /IORQ, the Y0 output of decoder L57 (2H2) is forced low and /WININ is asserted. /WININ pulls the enable inputs of driver L115 (4I12) low, placing Winchester status information on the Main Data Bus. The Z80A then latches the information into an internal register and decodes it. Data obtained from this port is interpreted as shown in Table 2-1. Note that signals from the disk drive are inverted by the driver. The logic values shown in the 'State' column of Table 2-1 reflect the values the Z80A sees. The state of the signals coming from the disk drive are actually the inverse of the logic values shown in the 'State' column.

| Bit Number | State | Interpretation  |
|------------|-------|---|
| DB0        | 0     | /TRACK0 is at logic 1. Heads are not over track 0.  |
|            | 1     | /TRACK0 is at logic 0. Heads are over track 0.  |
| DB1        | 0     | /WRFLT is at logic 1. Disk drive is OK.   |
|            | 1     | /WRFLT is at logic 0. A write fault condition exists. May cause data to be written improperly. All write operations are inhibited until condition is corrected. |
| DB2        | 0     | /READY is at logic 1. The drive is not ready. Generally this means that the motor is not up to speed yet.   |
|            | 1     | /READY is at logic 0. The drive is ready. When true in conjunction with /SKCOMP, data can be read from or written to the disk.                                  |

Table 2-1. How the Z80A interprets input from the Winchester Interface Status Port.

|            |   |  |
|------------|---|--|
| DB3        | 0 | /SKCOMP is at logic 1. Seek is not complete. Heads are not over the desired cylinder.    |
|            | 1 | /SKCOMP is at logic 0. Seek is complete. Heads are positioned over the desired cylinder. |
| DB4        | 0 | /DRS0 is at logic 1. The fixed drive is not selected.                                    |
|            | 1 | /DRS0 is at logic 0. The fixed drive is selected. (DB5 had better be 0).                 |
| DB5        | 0 | /DRS1 is at logic 1. The removable drive is not selected.                                |
|            | 1 | /DRS1 is at logic 0. The removable drive is selected. (DB4 had better be 0).             |
| DB6<br>DB7 |   | Spare. Not looked at by firmware.<br>Spare. Not looked at by firmware.                   |

Table 2-1 (continued). How the Z80A interprets input from the Winchester Interface Status Port.

#### 2.3.1.2 Winchester Interface Command Register 1 (Output Port 10)

Four of the signals originating at the outputs of this register are sent to the disk drive. Three of them are combined at the drive to select one of the heads, while the fourth is used to reduce the amount of current passed through the heads when data is being written onto one of the dense inner tracks. The latter output, along with the three of the remaining register outputs, are used either individually or in pairs to generate control signals that enable and disable circuits in the Winchester control logic. These signals allow the Z80A to initiate and halt Winchester read, write, and format operations.

When the Z80A outputs xx10 on the Main Address Bus and asserts /IORQ, the Y1 output of decoder L57 is forced low and /WINOUT1 is asserted. At the end of the write cycle, the Z80A deactivates /IORQ, causing /WINOUT1 to return high. The rising edge of /WINOUT1 clocks data from the main data bus into Winchester Interface Command Register 1, L112 (3D4), forcing the outputs to reflect the commands from the Z80A. The effects of writing to this port, based on the state of each

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bit, are shown in Table 2-2. Note that signals sent to the disk drive are inverted before leaving the board.

| Bit Number | State | Effect on Control Signals  |
|------------|-------|--|
| DB0        | 0     | /HDSELO is set to logic 1. /HDSELO-3 are combined at the drive to form a binary number that is used to select a head.  |
|            | 1     | /HDSELO is cleared to logic 0.   |
| DB1        | 0     | /HDSEL1 is set to logic 1.   |
|            | 1     | /HDSEL1 is cleared to logic 0.   |
| DB2        | 0     | /HDSEL2 is set to logic 1.   |
|            | 1     | /HDSEL2 is cleared to logic 0.   |
| DB3        | 0     | RWC and /RWC are forced to logic 0 and 1 respectively. Normal write current is passed through the heads, and write precompensation logic on the MFM generator is not activated.                                    |
|            | 1     | RWC and /RWC are forced to logic 1 and 0 respectively. Current flowing in the write head is reduced, the write precompensation logic on the MFM generator is activated.  |
| DB4        | 0     | TEND is cleared to logic 0. The microsequencer will not execute the format-track-end firmware.   |
|            | 1     | TEND is set to logic 1. The microsequencer will execute the format-track-end firmware.   |
| DB5        |       | Not connected. Has no effect.  |
| DB6        | 0     | READ is cleared to logic 0, turning off the read control hardware of the Winchester logic. Brought to this state temporarily during a READ operation to clear a header error condition. /FORMAT is set to logic 1. |
|            | 1     | READ and RW are set to logic 1. Initiates a read operation. If WRITE is asserted simultaneously, /FORMAT will be asserted and a format operation will be performed.  |
| DB7        | 0     | WRITE is cleared to logic 0, turning off the write control hardware of the Winchester logic. /FORMAT is set to logic 1.  |
|            | 1     | WRITE and RW are set to logic 1. Initiates a write operation. If READ is asserted simultaneously, /FORMAT will be asserted and a format operation will be performed.   |

Table 2-2. Effects of Z80A output to Winchester Interface Command Register 1.

### 2.3.1.3 Winchester Interface Command Register 2 (Output Port 20)

Signals from the outputs of this register are used to select a Winchester disk drive, step the heads, and define the direction in which the heads are to be stepped. When the 2200 commands the Z80A to perform a Winchester operation, the Z80A first figures out which Winchester the 2200 is asking for (even if there is only one), and then writes to this port to select the appropriate drive. If the heads are not over the desired cylinder, they must be moved. After determining which cylinder the heads are currently over, which direction they need to be stepped in, and how many steps need to be made to place the heads over the correct cylinder, the Z80A checks to see if /DIRCT is in the appropriate state. If /DIRCT is indicating a step in the wrong direction, the Z80A writes to this port and changes the step direction.

To step the heads, the Z80A pulses the /STEP signal low for 6.75 usec. /STEP is pulsed by writing to this port twice: once to force /STEP low and once to return it high. If the heads are to be stepped more than one cylinder, the Z80A continues to pulse /STEP every 22.5 usec until a /STEP pulse has occurred for every cylinder the heads are to be moved over. The heads move in or out one cylinder for each pulse of the /STEP line. At the disk drive, the /STEP pulses are counted, and when the drive determines that it has received all the step pulses it is going to get, it moves the heads over the appropriate number of cylinders in one smooth motion. The process of counting the step pulses before moving the heads is known as a buffered seek.

When the Z80A writes to this port by placing xx20 on the Main Address Bus and bringing /IORQ low, the Y2 output of decoder L57 (2H2) is forced low, and /WINOUT2 is asserted. At the end of the write cycle when /IORQ is returned high, the Y2 output of L57 also returns high and the rising edge of /WINOUT2 clocks data from the main data bus into Winchester Interface Command Register 2, L113 (4H13). Table 2-3 shows what actions are forced when this port is written to, based

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on the state of the individual bits. Note that signals sent to the disk drive are inverted before leaving the board.

| Bit Number | State | Effect on Control Signals   |
|------------|-------|---|
| DB0        | 0     | /DRVSELO is cleared to logic 0. Fixed Winchester is de-selected.                              |
|            | 1     | /DRVSELO is set to logic 1. Fixed Winchester is selected.                                     |
| DB1        | 0     | /DRVSEL1 is cleared to logic 0. Removable Winchester is de-selected.                          |
|            | 1     | /DRVSEL1 is set to logic 1. Removable Winchester is selected.                                 |
| DB2        | 0     | /STEP is deactivated by setting to logic 1.   |
|            | 1     | /STEP is activated by clearing to logic 0.  |
| DB3        | 0     | /DIRCT is forced to logic 1. Direction of step will be out (toward the center of the disk).   |
|            | 1     | /DIRCT is forced to logic 0. Direction of step will be in (away from the center of the disk). |
| DB4        |       | Not connected. Has no effect.   |
| DB5        |       | Not connected. Has no effect.   |
| DB6        |       | Not connected. Has no effect.   |
| DB7        |       | Not connected. Has no effect.   |

Table 2-3. Effects of Z80A output to Winchester Interface Command Register 2.

#### 2.3.1.4 Set Controller Ready Port (Output Port 40) and Set Controller Busy Port (Output Port 50)

Before the 2200 attempts to send a command byte to the DPU, it must check the DPU's ready/busy status to ensure that the DPU is ready. Similarly, before attempting to read data from the DPU's 2200 Data Output Register, the 2200 must ensure that the DPU is ready. The 2200 must always wait until the DPU is ready before attempting to send or receive data. On Friday afternoons, the DPU gets incredibly drunk (like its designer) and doesn't raise the ready flag until sometime late Saturday afternoon. In the board-busy state the /2Q output of flipflop L83 (3B10) is at logic 0; in the board-ready state L83 is in

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the cleared state and the /2Q output is at logic 1. This signal is inverted by driver L130 (3A9) before it is routed to the 2200.

The DPU board can be placed in the busy state in any one of four ways. A busy state is automatically entered during both power-on and hardwired resets. When /RST is brought low, the 2PR input of L83 is forced low, and the ready/busy flag is set to the busy state. The board is also automatically placed in the busy state when the DMA controller completes a data transfer from the DPU to the 2200. In this case, the DMA controller simultaneously outputs both /EOP and /DACK2 low, forcing the 2PR input of L83 low.

A third condition also automatically places the controller in the busy state. When the 2200 writes a command byte into the DPU's 2200 Data Input Register, the falling edge of /BOBS (which is inverted by line driver L130) clocks a high into the 2D input of L83, placing the board in the busy state. The Z80A may place the board in the busy state at any time by writing arbitrary data to the Set Controller Busy Port (output port 50). When the Z80A addresses this port by placing xx50 on the Main Address Bus and bringing /IORQ low, the Y5 output of decoder L57 (2H2) is forced low and /SETBSY is asserted. /SETBSY forces the pin 12 output of AND gate L128 low, in turn forcing the 2PR input of L83 low, placing the board in the busy state.

If the board is in the busy state and firmware determines that the board is no longer busy, the Z80A sets the board in the ready state by writing arbitrary data to the Set Controller Ready Port (output port 40). When the Z80A places xx50 on the Main Address Bus and brings /IORQ low, the Y4 output of decoder L57 is forced low and /SETRDY is asserted. /SETRDY forces the pin 6 output of AND gate L61 low, in turn bringing the 2CLR input of flipflop L83 low, placing the board in the ready state.

During DMA transfers from the 2200 to the DPU, as mentioned, the board is automatically placed in the busy state. When the DMA controller reads the 2200 Data Input Register by bringing /RD low, the

pin 6 output of AND gate L61 is forced low (since /DACK1 is also low). The 2CLR input of L83 is brought low, and the board is placed in the ready state. Thus, the board is automatically placed in the busy state when the 2200 sends a byte of data, and automatically placed in the ready state when the DMA controller reads the byte.

#### 2.3.1.5 2200 Data Input Register (Input Port 60)

All command and data bytes from the 2200 are passed to the DPU through the 2200 Data Input Register, L65 (3D11). The 2200 places a byte of data on its data output bus, /BOB1-8 (3C-E14), and brings the Output Bus Strobe (/BOBS) low. /BOBS is inverted by line driver L130 and is presented to the A input of 1-shot L129, the 2CK input of flipflop L83, and the CK/TR3 input of CTC1. The falling edge of /BOBS clocks a one into the 2D input of L83, placing the board in the busy state, triggers L129, and generates an interrupt request to the Z80A via channel three of CTC1. The /Q output of L129 is pulsed low for 500 nsec. Since the /Q output is tied to the 1-shot's B input, the A input is disabled for the duration of the pulse, preventing noise on the /BOBS input from re-triggering the 1-shot.

Data on the 2200's output bus is inverted by the 2200-DPU Data Input Buffer, L102, and then presented to the D inputs of the 2200 Data Input Register. When the 1-shot times out, the rising edge of its /Q output clocks data from the 2200 into L65, where the data may then be read by either the Z80A or the DMA controller. When the 1-shot is triggered, the Q output from the 1-shot is presented to the 1D input of flipflop L83. The next rising edge of 4CLK sets the flipflop, asserting OBREQ1, which issues a DMA request to the DMA controller at its DREQ1 input. OBREQ1 is synchronized with 4CLK to satisfy a timing requirement of the DMA controller.

Because OBREQ1 is generated even when the 2200 sends a command byte to the Z80A, the DMA controller is programmed to ignore OBREQ1 when command bytes are being sent. CTC1 informs the Z80A when a

command byte has been written into the register, and the Z80A then reads the command byte. Once the Z80A has received all the command bytes from the 2200 and is ready to receive data, CTC1 is programmed to ignore the output bus strobe and the DMA controller is programmed to respond to the interrupt request. The DMA controller then takes over the task of reading data from the 2200. After the DMA controller reads all the data it has been programmed to read, it issues an End of Operation (/EOP) signal that is passed through CTC2 to the Z80A. The Z80A then programs the DMA controller to ignore the DMA request, and continues on to the next step of the operation.

The Z80A reads the 2200 Data Input Register by placing xx60 on the Main Address Bus and bringing /IORQ low, forcing the Y6 output of decoder L57 (2H2) to go low asserting /ZRD2200. /ZRD2200 forces the pin 3 output of AND gate L61 low, forcing the OC input of L65 low, which dumps the data in the input register onto the Main Data Bus. Data is strobed into the Z80A on the rising edge of its /RD output. The DMA controller reads the 2200 Data Input Register by simultaneously bringing /DACK1 and /RD low. /RD is asserted when the DMA controller brings its /IOR output low. Pin 6 of OR gate L116 then goes low, forcing the pin 3 output of AND gate L61 and the OC input of L65 low, placing the data in the input register onto the Main Data Bus. Data is latched into the DMA controller on the rising edge of the DMA controller's /IOR output.

#### 2.3.1.6 2200 Data Output Register (Output Port 70)

All data and operation status bytes sent from the DPU to the 2200 must pass through the 2200 Data Output Register, L117 (3D10). The Z80A uses this register to send operation status information to the 2200 when an operation has been completed, and also to echo command bytes as they are received from the 2200. Data is transferred from the data cache to the 2200 through this register by the DMA controller. Before sending any data to the 2200, both the DMA controller and the Z80A must ensure that the 2200 is not busy. When

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the 2200 is busy, its BCPB signal (3A9) is in the active high state.

When the Z80A desires to send data to the 2200, it polls the DPU System Status and Operation Port until it finds /CPB is in the inactive high state. Having determined that the 2200 is not busy, the Z80A writes a byte of data into the 2200 Data Output Register by placing xx70 on the Main Address Bus and bringing /IORQ low. The Y7 output of decoder L57 (2H2) is forced low, and /ZWR2200 is asserted. /ZWR2200 then forces the pin 6 output of NAND gate L81 high, which in turn forces the ENB input of L117 high. At the end of the write cycle, the rising edge of /ZWR2200 latches the data on the Main Data Bus into the the 2200 Data Output Register.

The rising edge of /ZWR2200 also clocks a one into the 1D input of flipflop L127, causing its 1Q output to assert the 2200 Input Bus Strobe (IBS). IBS is inverted by driver L130, and /BIBS is presented to the 2200. The /1Q output of L127 brings the /1G and /2G inputs of the DPU-2200 Data Output Buffer, L118, low, gating data in the output register onto 2200 Data Input Bus lines BIB1-8. When the 2200 receives an active /BIBS, it knows that the data on the input bus is valid. The Z80A knows that the 2200 received the data when it sees the 2200 enter the busy state. If the 2200 is busy, /CPB holds the 1CLR input of L127 low, ensuring that a fault in the DPU board cannot accidentally cause data to be placed on the 2200 Data Input Bus.

Data read from a disk is sent to the 2200 under the direction of the DMA controller. When the 2200 goes from the busy state to the ready state, a logic one is presented to the 2D input of flipflop L127 (3A6). The first rising edge of 4CLK sets L127, forcing its 2Q output high. The rising edge of the 2Q output clocks a one into the 1D input of flipflop L143, causing IBREQ2 to be asserted at the 1Q output. IBREQ2 issues a DMA request to channel two of the DMA controller.

The DMA controller writes a byte of data into the 2200 Data Output register by simultaneously bringing /DACK2 and /WR low. /WR is forced low when the DMA controller brings its /IOW output low.

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Bringing these two signals low has the same effect as bringing /ZWR2200 low, which has already been covered in detail. In addition, the pin 3 output of AND gate L126 is forced low, clearing L143 and removing the DMA request by forcing /IBREQ2 back to the inactive low state. When the 2200 goes busy to read the data, the 2CLR input of L127 is brought low, clearing the flipflop for the next transfer. Again, /CPB holds the 1CLR input of L127 low, preventing a fault in the controller board from accidentally dumping data onto the 2200 Data Input Bus.

IBREQ2 is also generated when the Z80A is sending status information to the 2200 and echoing command bytes. During these times, the DMA controller is not programmed to respond to the DMA request. When the Z80A is ready to let the DMA controller take over the task of sending data, it programs the DMA controller to respond to the DMA request. After the DMA controller has transferred the number of bytes it was programmed to transfer (generally 257 bytes), it issues an End of Operation (/EOP) signal to the Z80A via channel zero of CTC2. The Z80A then programs the DMA controller to ignore DMA requests on channel two, and continues on to the next phase of the operation.

#### 2.3.1.7 Floppy Interface Command Register (Output Port C0)

The Floppy Interface Command Register, L57 (6J4), allows the Z80A to turn the floppy motor on and off, select and de-select the floppy, clear the floppy door-open flag, and assert REVP during the powerup diagnostics. REVP allows data to be written into the cache with reverse parity so that the operation of the cache data parity generator/checker can be tested.

When the Z80A writes to this port by placing xxC0 on the Main Data Bus and bringing /IORQ low, the Y4 output of decoder L59 (2I2) is forced low, and /FLOUT is asserted. At the end of the write cycle, the rising edge of /FLOUT clocks the data on Main Data Bus lines DB0-5

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into the D inputs of buffer register L56 (6J4). In addition, /FLOUT is connected to the pin 1 input of OR gate L50 (6J13). When /FLOUT goes low, the 2CLR input of flipflop L3 either remains high or goes low, depending on the status of bit DB6. If this bit is a logic 0, the flipflop is cleared and the floppy door-open flag is deactivated. The effects of setting or clearing each bit in this register are shown in Table 2-4.

| Bit Number        | State | Effect on Control Signals   |
|-------------------|-------|---|
| DB0               | 0     | /MTRON is set to logic 1. Turns off the floppy motor.   |
|                   | 1     | /MTRON is cleared to logic 0. Turns on the floppy motor.  |
| DB1               | 0     | /DRVSEL is set to logic 1. The floppy drive is de-selected.   |
|                   | 1     | /DRVSEL is cleared to logic 1. The floppy drive is selected.  |
| DB2               | 0     | REVP is set to logic 0. Data will be written into the cache with normal parity (normal operation).                              |
|                   | 1     | REVP is cleared to logic 1. Data will be written into the cache with reverse parity (powerup diagnostics).                      |
| DB3<br>DB4<br>DB5 |       | Spare. Not connected.<br>Spare. Not connected.<br>Spare. Not connected.   |
| DB6               | 0     | 2CLR input of flipflop L3 is brought low, and the floppy door-open status latch is cleared. Clears the door-open condition.     |
|                   | 1     | 2CLR input of flipflop L3 remains in the inactive high state, and the floppy door-open status latch retains its current status. |
| DB7               |       | Spare. Not connected.   |

Table 2-4. Effects of Z80A output to the Floppy Interface Command Register.

### 2.3.1.8 Floppy Controller Reset Port (Output Port D0)

Before the Z80A attempts to program the floppy controller's

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step rate, head load time, and head unload time, it writes arbitrary data to the Floppy Controller Reset Port to clear the floppy controller chip. All floppy drive control signals from the controller chip are deactivated. When the Z80A places xxD0 on the Main Address Bus and brings /IORQ low, the Y5 output of decoder L59 (2I2) is forced low and /FLOPRST is asserted. /FLOPRST triggers 1-shot L90 (6I10) by bringing the B input low. The Q output of L90 goes high for 15 usec, resetting the controller chip. This output is also routed to the A input to prevent re-triggering while the 1-shot is in the quasi-stable state. If you don't believe it, then the hell with ya.

### 2.3.1.9 DPU System Status and Options Port (Input Port E0)

The DPU System Status and Options Port, L55 (2F9), is read by the Z80A to determine what type of removable drive is plugged into the controller board. It also provides the Z80A with the status of four system signals: /CPB, DROP/CL, /KS, and FLPINDEX. When the Z80A reads this port by placing xxE0 on the main address bus and bringing /IORQ low, the Y6 output of decoder L59 (2I2) is forced low and /STATUS is asserted. /STATUS brings the /1G and /2G inputs to L55 low, placing status and options data on the main data bus. Table 2-5 defines how DB0-4 are interpreted by the Z80A, and Table 2-6 defines how DB5-7 are interpreted.

| Bit Number | State | Interpretation  |
|------------|-------|---|
| DB0        | 0     | /CPB is asserted. The 2200 is busy. Data may not be sent to the 2200.                   |
|            | 1     | /CPB is inactive. The 2200 is ready. Data may be sent to the 2200.                      |
| DB1        | 0     | DROP/CL is inactive. The floppy drive door is closed.                                   |
|            | 1     | DROP/CL is asserted. The floppy drive door is open and the drive motor is getting cold. |

Table 2-5. How the Z80A interprets the BD0-BD4 inputs from the DPU System Status and Options Port.

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|     |   |  |
|-----|---|--|
| DB2 | 0 | /KS is asserted. Data is being written from the 4E/00 Bus Driver, L75, to a Winchester disk.   |
|     | 1 | /KS is inactive. Data is not being written from the 4E/00 Bus Driver to a Winchester. While this signal was probably checked at one time to let the Z80A know when refresh cycles could be performed during a Winchester format operation, it is not used for anything any more. Firmware includes no way to check the status of this signal. Still, it's comforting to know you could check it if you really wanted to. |
| DB3 | 0 | FLPINDEX is inactive. The floppy heads are not over the index mark.  |
|     | 1 | FLPINDEX is asserted. The floppy heads are over the index mark.  |

Table 2-5 (continued). How the Z80A interprets the BD0-BD4 inputs from the DPU System Status and Options Port.

| Switch Settings |              |              |              | Indicated Drive(s) Connected to Board |                      |
|-----------------|--------------|--------------|--------------|---------------------------------------|----------------------|
| DB7<br>(SW4)    | DB6<br>(SW3) | DB5<br>(SW2) | DB4<br>(SW1) | Fixed Drive Type                      | Removable Drive Type |
| 0               | 0            | 0            | 0            | 10 Mbyte Winchester                   | Mini-Floppy          |
| 0               | 0            | 0            | 1            | 30 Mbyte Winchester                   | Mini-Floppy          |
| 1               | 0            | 0            | 0            | 10 Mbyte Winchester                   | 10 Mbyte Winchester  |
| 1               | 0            | 0            | 1            | 30 Mbyte Winchester                   | 10 Mbyte Winchester  |
| 1               | 0            | 1            | 1            | 30 Mbyte Winchester                   | 30 Mbyte Winchester  |

All other combinations are illegal.

Table 2-6. How the Z80A interprets the BD5-BD7 inputs from the DPU System Status and Options Port.

### 2.3.1.10 Issue Floppy Terminal Count Port (Output Port F0)

When data is to be read from or written to a floppy disk, the Z80A tells the DMA controller how many bytes of data to read or write, and tells the floppy controller where to start reading or writing. Since the floppy controller has no way of knowing on its own when to stop reading or writing, the Z80A must write arbitrary data to the Issue Floppy Terminal Count Port to tell it when to stop. When the last byte of data is written or read, the DMA controller issues an End

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of Operation (/EOP) signal to the Z80A via channel zero of CTC2. In response, the Z80A writes to Output Port F0 to issue a terminal count to the floppy controller. A terminal count signal forces the floppy controller to stop reading or writing.

When the Z80A places xxF0 on the main address bus and brings /IORQ low, the Y7 output of decoder L59 (2I2) goes low and asserts /OTC. /OTC is inverted by NAND gate L54 (6G11) and then sent to the TC input of the floppy controller.

### 2.3.2 Programmable I/O Devices

To aid the Z80A in controlling data transfers, monitoring signals on the DPU board, timing and counting events, and controlling floppy disk operations, the Z80A has at its disposal four, programmable I/O devices: a 9517-4 DMA controller, a 765A Floppy Disk Controller (FDC), and two Z80 Counter Timer Chips (CTCs). This section discusses the DMA controller and CTCs in detail, including information on the specific functions they perform and how their internal registers are addressed and programmed. The Floppy Disk Controller is covered in the chapter on floppy disk operations. As is true with most chips that are designed for use in a wide variety of applications, the DMA controller and CTCs have many features that go unused in any specific application. This section describes, for each chip, the features the Z80A makes use of.

#### 2.3.2.1 9517-4 DMA Controller

DMA data transfers, in general, are much faster than programmed I/O transfers because an instruction fetch cycle is not required between each transfer. The 9517-4 DMA controller, L99 (2I7), improves system performance by assuming control of data transfers between the 2200 and the data cache and between the floppy controller and the data cache. Features of the DMA controller include a 64k byte word-count

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capability, a 64k byte addressing capability, and four independent, individually-programmable I/O channels. This chip can juggle, whistle Dixie, bring home the bacon, and fry it up in a pan -- all at the same time.

Only three of the four channels on the DMA controller are actually used by the Z80A. Channel 0 is activated for data transfers from the data cache to the floppy controller and vice versa, channel 1 handles transfers from the 2200 to the data cache, and channel 2 controls transfers from the data cache to the 2200. Channel 3 is not used. After a powerup or a hard-wired reset, firmware programs channels 2 and 3 to ignore DMA requests by masking the DREQ1 and DREQ2 inputs. Channel 0 is not masked, since DMA requests are not issued by the floppy controller unless the floppy controller has been instructed to read or write data.

The DMA controller has two major cycles, referred to as the Idle and Active cycles. In the idle cycle, the controller samples the /CS input every clock cycle to determine if the Z80A is attempting to read from or write to one of its internal registers, and samples the DREQ inputs to determine if a channel is requesting DMA service. Any time the Z80A outputs an address of the form xxAx in conjunction with /IORQ low, the Y2 output of L59 is forced low and /DMACS is asserted. Address lines A0-A3 are inputs to the controller when /DMACS is asserted, and are used to select one of the controller's internal registers. The state of the signals at the /IOR and /IOW inputs determine whether the Z80A is attempting to read from or write to an internal register.

The Z80A initiates a transfer by writing a starting address into a channel's Base Address Register and Current Address Register. It then tells the controller how many bytes are to be transferred by placing a number one less than the actual number of bytes to be transferred into the channel's Base Count Register and Word Count Register. Finally, if the channel's DREQ input is masked, the Z80A unmask the DREQ input. When the controller is in the idle state and

a channel requests a DMA service, the device will output a HREQ to the Z80A and enter the active cycle.

All transfers are made in what is called the Single Transfer Mode. In this mode, a one-byte transfer takes place during each HREQ/BUSAK handshake. When an unmasked DREQ input goes active, the controller responds by outputting HREQ active. After the Z80A responds by driving BUSAK active, a one-byte transfer takes place. HREQ is then deactivated, the word count is decremented, and the address is incremented. When the word count goes to zero, a Terminal Count (TC) causes /EOP to be asserted, informing the Z80A via channel 0 of CTC2 that the transfer is complete.

By convention, a write operation refers to a data transfer from an I/O port to the data cache, and a read operation refers to a data transfer from the cache to an I/O port. The eight, high-order address bits are multiplexed on the data lines. Prior to a transfer, the controller places the high-order address byte on the Main Data Bus and brings the ADSTB output low. ADSTB forces the ENB input of the High-Order Address Latch, L101 (2J10), to go low, and the high-order address byte is gated into the latch. ADSTB is then returned high, and the address is latched into L101. The high-order address byte is updated only when a carry occurs out of the low-order address byte or when a new DMA operation begins.

As an illustration of how the DMA controller operates, assume that data is being transferred from the 2200 to the cache. When the 2200 writes a byte of data into the 2200 Data Input Register, OBREQ1 goes high. Channel 1, which is programmed to perform a write operation, receives the DMA request and forces the controller's HREQ output high. When the Z80A returns an active BUSAK, indicating that it has floated its bus lines, the controller outputs /DACK1 and brings the /IOR output low. The contents of the 2200 Data Input Register are then forced onto the Main Address Bus. This data byte is latched into a temporary register in the controller, and /DACK1 and /IOR are returned to the inactive high state.

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In the second half of the write operation, the controller brings its AEN output high, causing the High-Order Address Latch to place the high-order address byte on the high-order address bus, and the low-order address byte is placed on the low-order address bus at the A0-7 outputs. /MEMW is brought low to indicate that data is to be written to the cache, and the byte of data is placed back on the Main Data Bus from the temporary register. The timing of memory operations from this point on is similar to the timing described for Z80A memory operations in section 2.2.2.

When the byte has been written into the cache, the High-Order Address Latch, A0-A7, and D0-D7 outputs are floated, and HREQ is returned to the inactive low state. The Z80A then resumes control of the bus. Read operations are similar to write operations, except the direction of the transfer is exactly the opposite and the /MEMR and /IOW signals are active rather than the /IOR and /MEMW signals.

Before discussing exactly how the DMA controller is programmed by the Z80A for various transfers, a brief description of some of the internal registers in the 9517-4 is needed. Each channel's Current Address Register contains the memory address to be used during a DMA transfer. The current address is stored in two bytes, a low-order and a high-order byte. When the Z80A writes the low-order byte into this register, the register's First/Last Flipflop is toggled so that the next byte the Z80A sends will be stored in the high-order byte. At the end of a single-byte transfer, the low-order address byte is incremented. If a carry occurs out of the low-order byte, the high-order byte is incremented and the High-Order Address Latch is updated.

Each channel's 16-bit Current Word Count Register is programmed with, and always contains, a value that is one byte less than the actual number of bytes that remain to be transferred. This register is automatically decremented after each transfer. When the word count goes to zero, a TC will be generated and /EOP will be asserted. Similar to the Current Address Register, the Current Word Count

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Register contains a low- and a high-order byte. The first byte written into this register is placed in the low-order register, and the register's First/Last Flipflop is toggled so that the next byte sent will be placed in the high-order register.

Two registers that cannot be read by the Z80A are the Base Address and Base Word Count Registers. These registers are loaded in parallel with the Current Address and Current Word Count Registers, and maintain the values that are loaded into them throughout a transfer operation. If a channel is programmed to autoinitialize, an /EOP at the end of a transfer operation will cause the original values of the Current Address and Current Word Count registers to be restored from the Base Address and Base Word Count registers of that channel. The mask bit of that channel will not automatically be set by the /EOP, and the channel is ready to repeat its service. Firmware makes use of this feature with a slight modification.

When a channel is to transfer more than one block of data, that channel is programmed to autoinitialize after an /EOP. Upon autoinitialization, the Z80A immediately steps in and writes a new starting address into the Base and Current Address Registers, and the channel continues on with the transfer. If a channel is not autoinitialized, its DREQ input is automatically masked by an /EOP, and the Current Address and Word Count Registers are not restored. In order to transfer another block of data on that channel, the entire initialization process must be repeated. The only channel that is not programmed for autoinitialization is channel 2. More information on the operation of specific channels is given in the chapter on firmware.

Although firmware provides the Z80A with the capability to address all of the DMA controller's internal registers, not all of the registers are used. Furthermore, some registers that may be both read from and written to are either only read from or only written to. Tables 2-7 through 2-12 list the addresses of the registers that are used by the Z80A, indicates whether the registers are read from or written to, and shows in detail what effects certain bit patterns have

on the operation of the DMA controller.

|                         |   |
|-------------------------|---|
| <u>Output Port xxA0</u> | Channel 0 Base and Current Address Registers. Written to by the Z80A to load the starting memory address for DMA transfers both to and from memory. The I/O port involved in these transfers is always the Floppy Disk Controller. Although the Current Address register can be read, it never is. See section 2.3.2.1 for more detail on these registers.  |
| <u>Output Port xxA1</u> | Channel 0 Base and Current Word Count Registers. Written to by the Z80A to specify how many bytes are to be transferred in one transfer operation. The value loaded is one less than the number of bytes that will actually be transferred. The I/O port involved in these transfers is always the Floppy Disk Controller. Although the Current Word Count register can be read, it never is. See section 2.3.2.1 for more detail on these registers. |
| <u>Output Port xxA2</u> | Channel 1 Base and Current Address Registers. The I/O port involved in these transfers is always the 2200 Data Input Register. See Output Port xxA0.  |
| <u>Output Port xxA3</u> | Channel 1 Base and Current Word Count Registers. The I/O port involved in these transfers is always the 2200 Data Input Register. See Output Port xxA1.   |
| <u>Output Port xxA4</u> | Channel 2 Base and Current Address Registers. The I/O port involved in these transfers is always the 2200 Data Output Register. See Output Port xxA0.   |
| <u>Output Port xxA5</u> | Channel 2 Base and Current Word Count Registers. The I/O port involved in these transfers is always the 2200 Data Output Register. See Output Port xxA1.  |

Table 2-7. Addressing the DMA Controller's Base and Current Address Registers and Base and Current Word Count Registers.

|                         |   |
|-------------------------|---|
| <u>Output Port xxA8</u> | Command Register<br>Written to by the Z80A to select characteristics that are applied to all four registers. Only written to once, after either a powerup or hardwired reset. Byte written to register = 20H. Effects of this bit pattern are as follows: |
|-------------------------|---|

Table 2-8. Programming the DMA Controller Command Register.

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| Bit # | State | Effect  |
|-------|-------|---|
| BD0   | 0     | Disables memory-to-memory transfer option used to move a block of data from one location in memory to another. This function is not needed by the DPU.  |
| BD1   | 0     | This bit is not looked at because BD1 is logic 0.   |
| BD2   | 0     | Enables the controller.   |
| BD3   | 0     | Selects normal timing (as opposed to compressed timing, which requires a faster access time than is available on the DPU).  |
| BD4   | 0     | Selects fixed priority DMA requests with channel 0 having the highest priority.   |
| BD5   | 1     | Selects extended write cycle. This selection forces the write control line to go low one clock period earlier than it would normally go low, but does not extend the length of the write cycle. Used in order to meet the timing requirements of the DRAMS. |
| BD6   | 0     | Sets the sense of all DREQ inputs active high. A logic 1 at any of the DREQ inputs will be interpreted as a DMA request.  |
| BD7   | 0     | Sets the sense of all DACK outputs active low. A DMA request is acknowledged by bringing the appropriate DACK output low.   |

Table 2-8 (continued). Programming the DMA Controller Command Register.

|  |
|--|
| <p><u>Output Port xxAA</u> Mask Register.</p> <p>Written to by the Z80A to set or clear a channel's mask bit. DMA requests are not acknowledged when the mask bit is set. Bit BD2 determines whether the bit will be set or cleared, and bits BD0 and BD1 select the channel. Only the bytes shown below are written into this register by firmware. No other bit patterns are used.</p> |
|--|

Table 2-9. Programming the DMA Controller Mask Register.

| Byte Sent | DB7-DB3 | BD2 | BD1 | BD0 | Effect   |
|-----------|---------|-----|-----|-----|--|
| 01H       | Ignored | 0   | 0   | 1   | Clear channel 1 mask bit. DMA request is generated when 2200 writes a byte of data into the 2200 Data Input Register.                        |
| 02H       | Ignored | 0   | 1   | 0   | Clear channel 2 mask bit. DMA request is generated when 2200 goes from the busy state to the ready state.                                    |
| 05H       | Ignored | 1   | 0   | 1   | Set channel 1 mask bit. No DMA request is generated when the 2200 writes a byte of data into the 2200 Data Input Register. DREQ1 is ignored. |
| 06H       | Ignored | 1   | 1   | 0   | Set channel 2 mask bit. No DMA request is generated when 2200 goes from the busy state to the ready state. DREQ2 is ignored.                 |

Table 2-9 (continued). Programming the DMA Controller Mask Register.

| <u>Output Port xxAB</u> Mode Register  |  |
|--|--|
| <p>Selects a channel's mode register to provide specific information regarding the type of transfer to be performed. Bits BD1 and BD0 are decoded to determine which channel's mode register is being addressed. Bits BD3 and BD2 determine whether a read or a write transfer is to be performed (10 = read, 01 = write). Bit BD4 is a logic 1 if autoinitialization is allowed, and logic 0 if it is not allowed. Bit BD6 is always zero, specifying that the contents of the Current Address Register should be incremented after each transfer. Bits BD7 and BD6 are always logic 0 and 1 respectively, indicating Single Mode transfers. Only four bit patterns are used for Mode Register programming. These bit patterns and their effects are:</p> |  |
| Byte Sent  | Effects  |
| 4AH  | Selects channel 2, read transfer, no autoinitialization, address increment, single transfer mode. Programs channel 2 to send data to the 2200 through the 2200 Data Output Register. |

Table 2-10. Programming the DMA Controller Mode Registers.

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| Byte Sent | Effects   |
|-----------|---|
| 54H       | Selects channel 0, write transfer, autoinitialization, address increment, single transfer mode. Programs channel 0 to transfer data from the Floppy Disk Controller to the cache. |
| 55H       | Selects channel 1, write transfer, autoinitialization, address increment, single transfer mode. Programs channel 2 to receive data from the 2200 Data Input Register.             |
| 58H       | Selects channel 0, read transfer, autoinitialization, address increment, single transfer mode. Programs channel 0 to transfer data from the cache to the Floppy Disk Controller.  |

Table 2-10 (continued). Programming the DMA Controller Mode Registers.

|  |
|--|
| <p><u>Output Port xxAD</u> Master Clear.</p> <p>Writing arbitrary data to this port has the same effect as a hardware reset. All bits in the Command, Status, Request, and Temporary Registers are cleared, all First/Last flipflops are cleared (first byte written to Current Address or Word Count Registers will be interpreted as a low-order byte), and all DREQ mask bits will be set. Used once during every powerup or hardwired reset sequence to initialize chip.</p> |
| <p><u>Output Port xxAF</u> Write All Mask Register Bits.</p> <p>Writing data to this port allows the Z80A to selectively set or reset all DREQ mask bits in one operation. Only the four least significant bits are decoded. Used once during every powerup or hardwired reset sequence to initialize chip after a Master Clear. Byte sent is 0EH, which clears channel 0's mask and sets the other three channel's masks.</p>   |

Table 2-11. DMA Controller Master Clear and Write All Mask Register Bits commands.

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|             |       |  |
|-------------|-------|--|
| Input Port  | xxA0: | Read channel 0 Current Address Register.     |
| Input Port  | xxA1: | Read channel 0 Current Word Count Register.  |
| Input Port  | xxA2: | Read channel 1 Current Address Register.     |
| Input Port  | xxA3: | Read channel 1 Current Word Count Register.  |
| Input Port  | xxA4: | Read channel 2 Current Address Register.     |
| Input Port  | xxA5: | Read channel 2 Current Word Count Register.  |
| Input Port  | xxA6: | Read channel 3 Current Address Register.     |
| Output Port | xxA6: | Write channel 3 Current Address Register.    |
| Input Port  | xxA7: | Read channel 3 Current Word Count Register.  |
| Output Port | xxA7: | Write channel 3 Current Word Count Register. |
| Input Port  | xxA8: | Read a channel's status register.            |
| Output Port | xxAC: | Write to clear First/Last flipflops.         |
| Input Port  | xxAD: | Read contents of Temporary Register.         |

Table 2-12. DMA Controller Ports addressable by firmware but not used.

### 2.3.2.2 Z80 Counter Timer Chips

Two Z80 CTC's count events, time events, and prioritize interrupts for the Z80A. Channel 0 of CTC1, L124 (2E12), is used to interrupt the Z80A when the microsequencer issues a DONE signal at the end of a Winchester operation. An INDEX signal from a Winchester drive generates an interrupt via channel 1 of CTC1 to indicate either that the heads are over the index mark and a format operation should begin or that the maximum number of rotations has been exceeded during a sector header search. Channel 2 of CTC1 generates an interrupt when the floppy controller issues a FLOPINT signal, indicating that either a floppy operation is complete or the floppy door has been opened. And, when the 2200 writes a byte of data into the 2200 Data Input Register, an interrupt is generated via channel 3 of CTC1 to alert the Z80A that an output bus strobe was asserted by the 2200.

Channel 0 of CTC2, L125, interrupts the Z80A when the DMA controller signals the completion of a data transfer operation by pulling /EOP low. When the 2200 issues a re-initialization sequence by asserting /START, an interrupt is generated via channel 1. Channels 3 and 4 of CTC2 perform timing functions for the Z80A.

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When the Z80A places an address of the form xx8x on the Main Address bus in conjunction with /IOR low, the Y0 output of decoder L59 (2I2) is forced low, and /CTCCS1 is asserted. Address lines AB0 and AB1 are decoded by CTC1 to determine which of the four channels is being addressed. Similarly, when the Z80A places an address of the form xx9x on the Main Address Bus and brings /IOR low, the Y1 output of L59 is forced low and /CTCCS2 is asserted. The Z80A programs a channel when its services are needed. When a channel's services are no longer required, the Z80A disables that channel. Table 2-13 shows exactly how each channel is addressed and programmed by the Z80A.

| <u>Output Port xx80 CTC1 Channel 0</u>   |       |   |
|--|-------|---|
| <p>Channel 0 generates an interrupt that wakes the Z80A up from a halt state during Winchester read, write, and format operations. In addition, the interrupt vector for all four channels of CTC1 is sent through this port. When bit BD0 is a logic 1 the control register is addressed, and when bit BD0 is a logic 0 the interrupt vector register is addressed. The interrupt vector written to this port is 40H, which results in interrupt vectors of 40H for channel 0, 42H for channel 1, 44H for channel 2, and 46H for channel 3. The first byte sent to this address is always D7H, which has the effects described below. Channel 0 is disabled by writing a byte of 03H to this port, which stops any active operation and disables the channel interrupt.</p> |       |   |
| Bit #  | State | Effect  |
| BD0  | 1     | Addresses the control register.   |
| BD1  | 1     | Stops any current operation on this channel.  |
| BD2  | 1     | Indicates that the next byte sent to this address should be interpreted as a time constant for the Down Counter. For read and format operations, the Down Counter is loaded with a count of one, and for format operations the Down Counter is loaded with a count of 31. |
| BD3  | 0     | Don't care, since bit BD6 is a logic 1.   |
| BD4  | 1     | The rising edge of DONE will decrement the down counter.  |

Table 2-13. Addressing and Programming the Z80 Counter Timer Chips.

| Bit # | State | Effect  |
|-------|-------|---|
| BD5   | 0     | Don't care, since bit BD6 is a logic 1.   |
| BD6   | 1     | Selects the counter mode.   |
| BD7   | 1     | Channel interrupts are enabled and will occur when the Down Counter reaches zero. |

Output Port xx81 CTC1 Channel 1

This channel generates an interrupt when the heads of a selected Winchester are over the index mark. During format operations, this interrupt is used to signal that formatting should begin; during read and write operations, index marks are counted and an interrupt is generated when a sector is not located within a predefined maximum number of rotations. The default value for the maximum number of rotations is three. Channel 1 is programmed identically to channel 0, and is also disabled by sending a byte of 03H. The Down counter is loaded with either one or three, depending upon the type of disk operation to be performed.

Output Port xx82 CTC1 Channel 2

Channel 2 generates an interrupt when the NEC floppy controller issues an interrupt to signal the end of a floppy operation or when the floppy drive door is opened. This channel is programmed the same way that channels 1 and 2 are programmed, and the Down Counter is always given a value of one. Once programmed, this channel is not disabled except by a power outage or a hardwired reset.

Output Port xx83 CTC1 Channel 3

An interrupt is generated by this channel when the 2200 writes a command byte into the 2200 Data Input Register. Channel 3 is programmed in the same manner as Channels 0, 1, and 2. After all command bytes are received, the Z80A disables this channel by writing 03H into the control register. The DMA controller is then enabled, and will respond to OBS signals until 257 bytes of data have been received. The DMA controller is then disabled and Channel 3 is re-enabled. Channel 3 then responds to OBS signals until again disabled by the Z80A.

Table 2-13 (continued). Addressing and Programming the Z80 Counter Timer Chips.

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Output Port xx90 CTC2 Channel 0

Channel 0 generates an interrupt that informs the Z80A that a DMA transfer operation has been completed. In addition, the interrupt vector for all four channels of CTC2 is sent through this port. When bit BD0 is a logic 1 the control register is addressed, and when bit BD0 is a logic 0 the interrupt vector register is addressed. The interrupt vector written to this port is 48H, which results in interrupt vectors of 48H for channel 0, 4AH for channel 1, 4CH for channel 2, and 4EH for channel 3. The first byte sent to this address is always C7H, which has the effects described below. Channel 0 is disabled by writing a byte of 03H to this port, which stops any active operation and disables the channel interrupt.

| Bit # | State | Effect   |
|-------|-------|--|
| BD0   | 1     | Addresses the control register.  |
| BD1   | 1     | Stops any current operation on this channel.   |
| BD2   | 1     | Indicates that the next byte sent to this address should be interpreted as a time constant for the Down Counter. The Down Counter is loaded with a count of one. |
| BD3   | 0     | Don't care, since bit BD6 is a logic 1.  |
| BD4   | 0     | The falling edge of /EOP will decrement the down counter.  |
| BD5   | 0     | Don't care, since bit BD6 is a logic 1.  |
| BD6   | 1     | Selects the counter mode.  |
| BD7   | 1     | Channel interrupts are enabled and will occur when the Down Counter reaches zero.  |

Output Port xx91 CTC2 Channel 1

This channel generates an interrupt when the 2200 initiates a reinitialization sequence by asserting /START. Once programmed, this channel remains active until power down or a hardwired reset.

Table 2-13 (continued). Addressing and Programming the Z80 Counter Timer Chips.

Output Port xx92 CTC2 Channel 2

Channel 2 is used with Channel 3 to measure dead time after completion of a disk operation. If four seconds elapse and the floppy is not accessed, this channel causes channel 3 to generate an interrupt to the Z80A, informing the Z80A to shut the floppy drive motor off. The channel is programmed with 37H as shown below, and times out every 16.4 msec (system clock period times the prescaler times the time constant).

| <u>Bit #</u> | <u>State</u> | <u>Effect</u>  |
|--------------|--------------|--|
| BD0          | 1            | Addresses the control register.  |
| BD1          | 1            | Stops any current operation on this channel.   |
| BD2          | 1            | Indicates that the next byte sent to this address should be interpreted as a time constant for the Down Counter. The Down counter is loaded with 00H, which results in a timeout every 256 counts. |
| BD3          | 0            | Causes counting to begin on the rising edge of the clock in the first T2 machine state following the loading of the time constant.   |
| BD4          | 1            | Don't care, since timer is not triggered externally.   |
| BD5          | 1            | Selects 256 for the prescaler. The Down Counter will be decremented every 256 clock cycles.  |
| BD6          | 0            | Selects the timer mode.  |
| BD7          | 1            | Channel interrupts are disabled. No interrupt will be generated when the timer times out.  |

Output Port xx93 CTC2 Channel 3

Channel 3 is used as both a counter and a timer. During Winchester format operations, this channel functions as a timer that informs the Z80A when it is safe to refresh dynamic memory. This channel is also used with Channel 2 to measure dead time after completion of a disk operation. If four seconds elapse and the floppy is not accessed, this channel generates an interrupt informing the Z80A that the floppy drive motor should be turned off (an interrupt is generated when 256, 14.6-msec timeouts have been counted). In the counter mode, the channel 3 control register is programmed

Table 2-13 (continued). Addressing and Programming the Z80 Counter Timer Chips.

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with FFH, and in the timer mode the control register is programmed with 87H, as shown below. Both the timer and the counter can be disabled by writing 03H into the control register.

| COUNTER MODE |       |  |
|--------------|-------|--|
| Bit #        | State | Effect   |
| BD0          | 1     | Addresses the control register.  |
| BD1          | 1     | Stops any current operation on this channel.   |
| BD2          | 1     | Indicates that the next byte sent to this address should be interpreted as a time constant for the Down Counter. The Down Counter is loaded with 00H, causing an interrupt to be generated after a count of 256.   |
| BD3          | 1     | Don't care, since bit BD6 is a logic 1.  |
| BD4          | 1     | The rising edge of Channel 2's Time Out output will decrement the down counter.  |
| BD5          | 1     | Don't care, since bit BD6 is a logic 1.  |
| BD6          | 1     | Selects the counter mode.  |
| BD7          | 1     | Channel interrupts are enabled and will occur when the Down Counter reaches zero.  |
| TIMER MODE   |       |  |
| Bit #        | State | Effect   |
| BD0          | 1     | Addresses the control register.  |
| BD1          | 1     | Stops any current operation on this channel.   |
| BD2          | 1     | Indicates that the next byte sent to this address should be interpreted as a time constant for the Down Counter. Depending on the operation being performed, the Down Counter will be loaded with either 28H, 30H, or 40H, corresponding to times of 160 usec, 192 usec, and 256 usec. |
| BD3          | 0     | Causes counting to begin on the rising edge of the clock in the first T2 machine state following the loading of the time constant.   |

Table 2-13 (continued). Addressing and Programming the Z80 Counter Timer Chips.

| Bit # | State | Effect  |
|-------|-------|---|
| BD4   | 0     | Don't care, since timer is not triggered externally.                                      |
| BD5   | 0     | Selects 16 for the prescaler. The Down Counter will be decremented every 16 clock cycles. |
| BD6   | 0     | Selects the timer mode.   |
| BD7   | 1     | Channel interrupts are enabled. An interrupt will be generated when the timer times out.  |

Table 2-13 (continued). Addressing and Programming the Z80 Counter Timer Chips.

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## CHAPTER 2 THEORY OF OPERATION

### INTRODUCTION

The 2275 Disk Peripheral consists of two OEM Disk Drives, a Disk Processing Unit (Controller), and a linear regulated Power Supply, all mounted in a single case. This section contains the theory of operation of the Power Supply with 8397 Power Supply Regulator Board; and the Disk Processing Unit/8396 Disk Controller Board. OEM Disk Drive theory is beyond the scope of this manual.

### POWER SUPPLY

The power supply for this unit is of straightforward design, incorporating linear voltage regulation and current limiting. It operates from either 115 VAC or 230 VAC power lines, and produces two regulated and two unregulated DC output voltages:

- + 5 VDC Regulated
- + 12 VDC Regulated
- + 16 VDC (Nominal) Unregulated
- 16 VDC (Nominal) Unregulated

Physically, the power supply is divided into two sections. The larger and heavier components are mounted on the chassis rear panel; while the filters, regulators, and most of the rectifiers are on the 8397 Regulator Board.

#### Chassis-Mounted Power Supply Components

The chassis-mounted components include the Power Transformer, the transformer Primary Side Accessories, and the Full-Wave Center-Tap Rectifier for the +5 VDC section.

The transformer Primary Side Accessories include a Line Filter, power ON/OFF Switch, Line Fuse, Transient Suppressors, and a Cooling Fan. Two other accessories operate on the primary side of the power transformer, but they are physically located on the Regulator Board. These are the Thermal Overload Protector, and the Primary Voltage Selector Switch.

The Power Transformer has dual primary windings which can be connected in parallel for 115VAC operation, or connected in series for 230 VAC operation. The Primary Voltage Selector Switch determines whether the windings are connected in series or parallel. The Transformer has two tapped secondary windings. One winding feeds low voltage AC to the +5 VDC rectifiers and regulator; while the other winding feeds higher AC voltages to three rectifiers that produce nominal -16 VDC, +16 VDC, and +24 VDC.

The Rectifier for the +5 VDC section of the power supply is a high-power, encapsulated, and heat-sinked unit of full-wave center-tap configuration. This is the only rectifier that is not mounted on the regulator board.

### 8397 Power Supply Regulator Board

The Power Supply Regulator Board contains four Rectifiers, all of the power supply Filters, a +12 VDC Voltage Regulator, a +5 VDC Voltage Regulator, and a -.7 VDC Clamp. The Voltage Regulator pass transistors and the nominal +16 VDC Rectifier are heavily heat-sinked. A Thermal Overload Protector on one of the heat sinks will open the Power Transformer primary circuit if the heat sink temperature becomes excessive.

The four rectifiers include a half-wave unit that provides the nominal +24 VDC that powers the +12 VDC regulator. A heat-sinked full-wave center-tap rectifier provides both the nominal +16 VDC unregulated and +12 VDC regulated outputs of the power supply. The third rectifier is a low-power full-wave center-tap unit that provides the nominal -16 VDC unregulated output. This same negative voltage source also feeds a low voltage Clamp circuit that provides -.7 VDC for the voltage regulator current limiting circuits. The remaining rectifier is a low-power full-wave center-tap type, and provides the nominal +8.5 VDC that powers the +5 VDC Voltage Regulator.

The power supply filters are all simple capacitor filters, and are mounted on the regulator board.

The +12 VDC and +5 VDC Regulators are of similar design. Each consists of an integrated low-power regulator that controls high-power external pass transistors. Each regulator is adjustable over a small range, and each incorporates fold-back current limiting. The principal differences between the regulators are that the reference and feedback voltages require different handling in each case, and the +12 VDC Regulator has been designed to withstand a power-up current surge that exceeds the normal current limiting level. Regulator details are described below.

#### Voltage Regulator Details

Each of the Voltage Regulators is designed around a standard IC regulator, the LM723. The features of this unit include current limiting, and a stabilized reference voltage source. In operation, the IC regulator receives feedback voltage from the regulated output terminal, reference voltage from the stabilized reference source, and current-sense feedback from a small series resistor in the output line.

The regulator compares the feedback and reference voltages, then adjusts the regulator output until the feedback and reference voltages match. The reference voltage used by the regulator is reduced by a voltage divider to obtain output voltages lower than approximately 7.7 VDC. The feedback voltage used by the regulator is reduced by a voltage divider to obtain output voltages higher than 7.7 VDC.

The current-sense feedback signal is a voltage drop produced across the small series resistor in the output line. This voltage is applied to the current limiting control within the regulator. If the regulator output current exceeds a specified value, the current limiter reduces the regulated output voltage as low as necessary to prevent any further increase in the current.

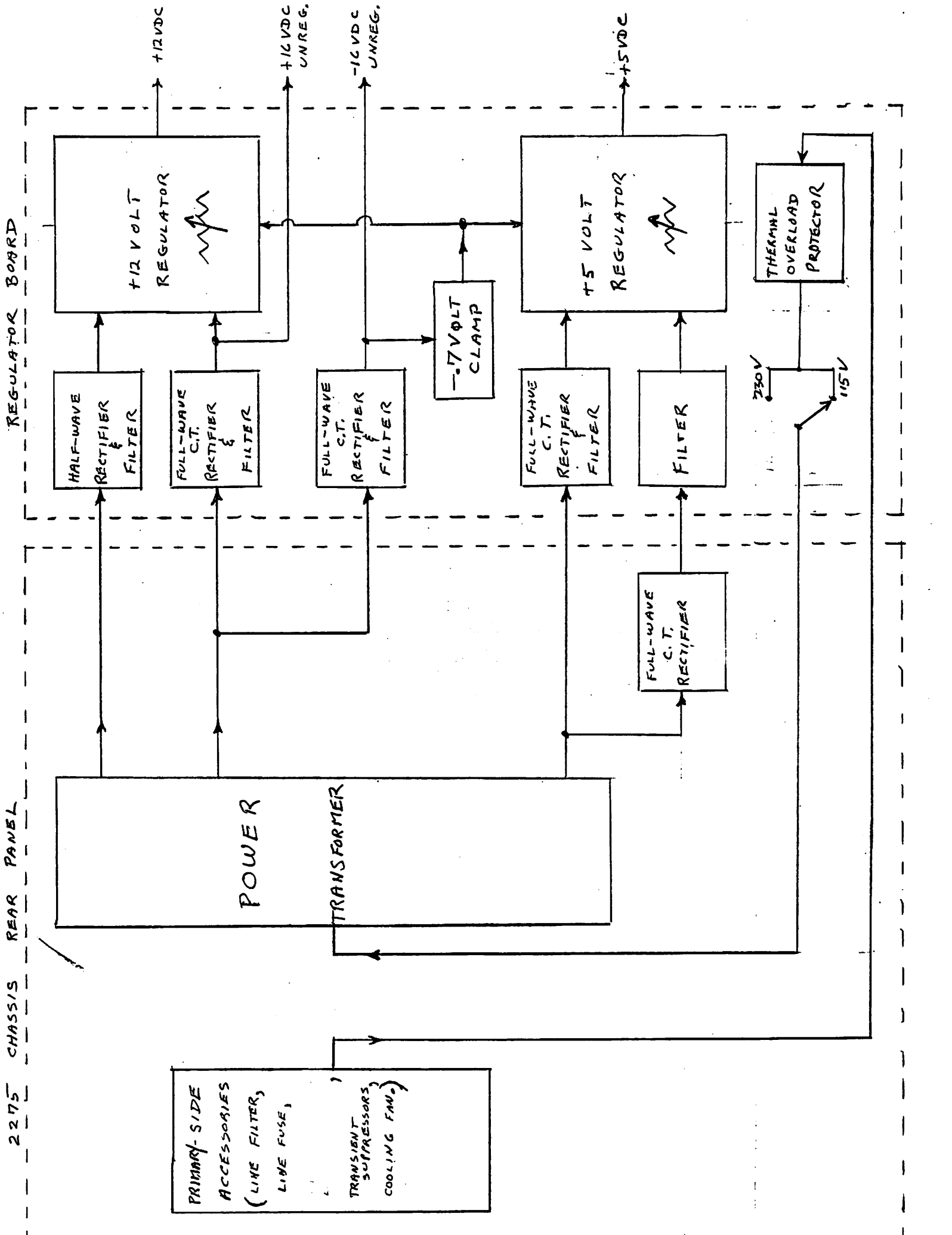
The voltage regulators on the 8397 Power Supply Regulator Board generally operate as described above, except that external pass transistors are used with the IC regulators to allow high current operation. These pass transistors are included in the feedback loops, so the overall results are the same.

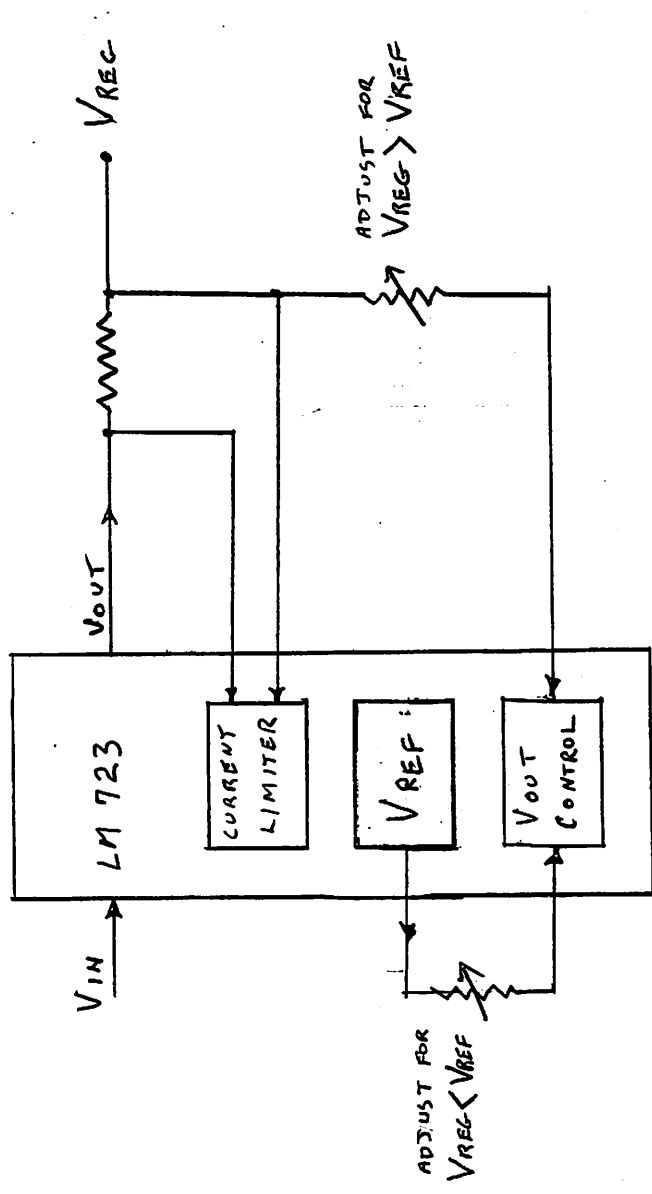
Two additional features have been incorporated into the current-sense feedback loops: Foldback Current Limiting, and Current Surge Compensation. Both regulators use foldback current limiting, but only the +12 VDC regulator uses surge compensation.

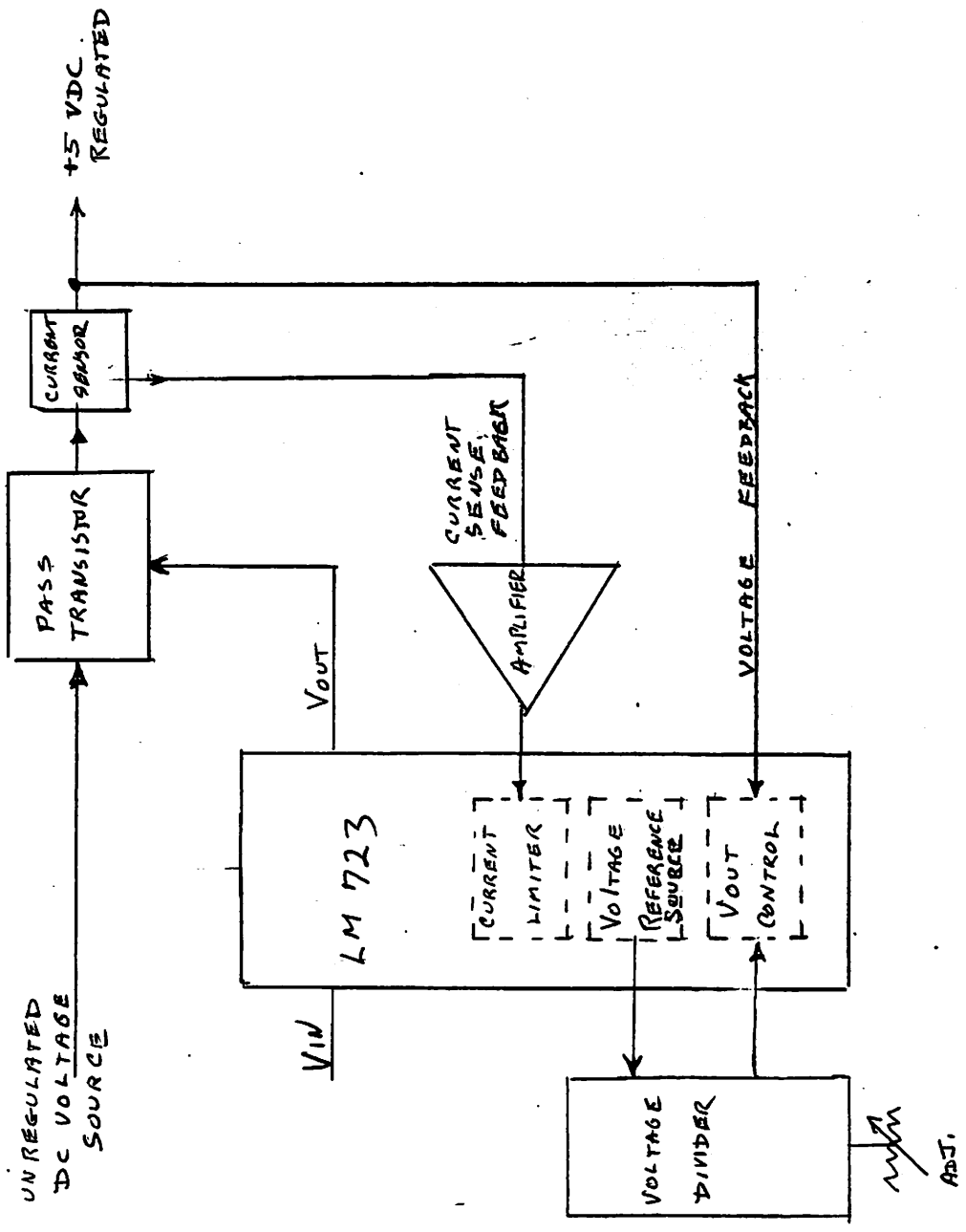
Foldback current limiting prevents excessive pass transistor power dissipation in the event of a short circuit load. In high power regulators such as these, a short circuit load condition can easily cause a power dissipation far beyond the normal level at full load, even though current limiting is used. The reason is that the external pass transistor must handle the full input voltage as well as full load current under short circuit conditions. Under normal full load conditions, the voltage felt by the transistor is far lower.

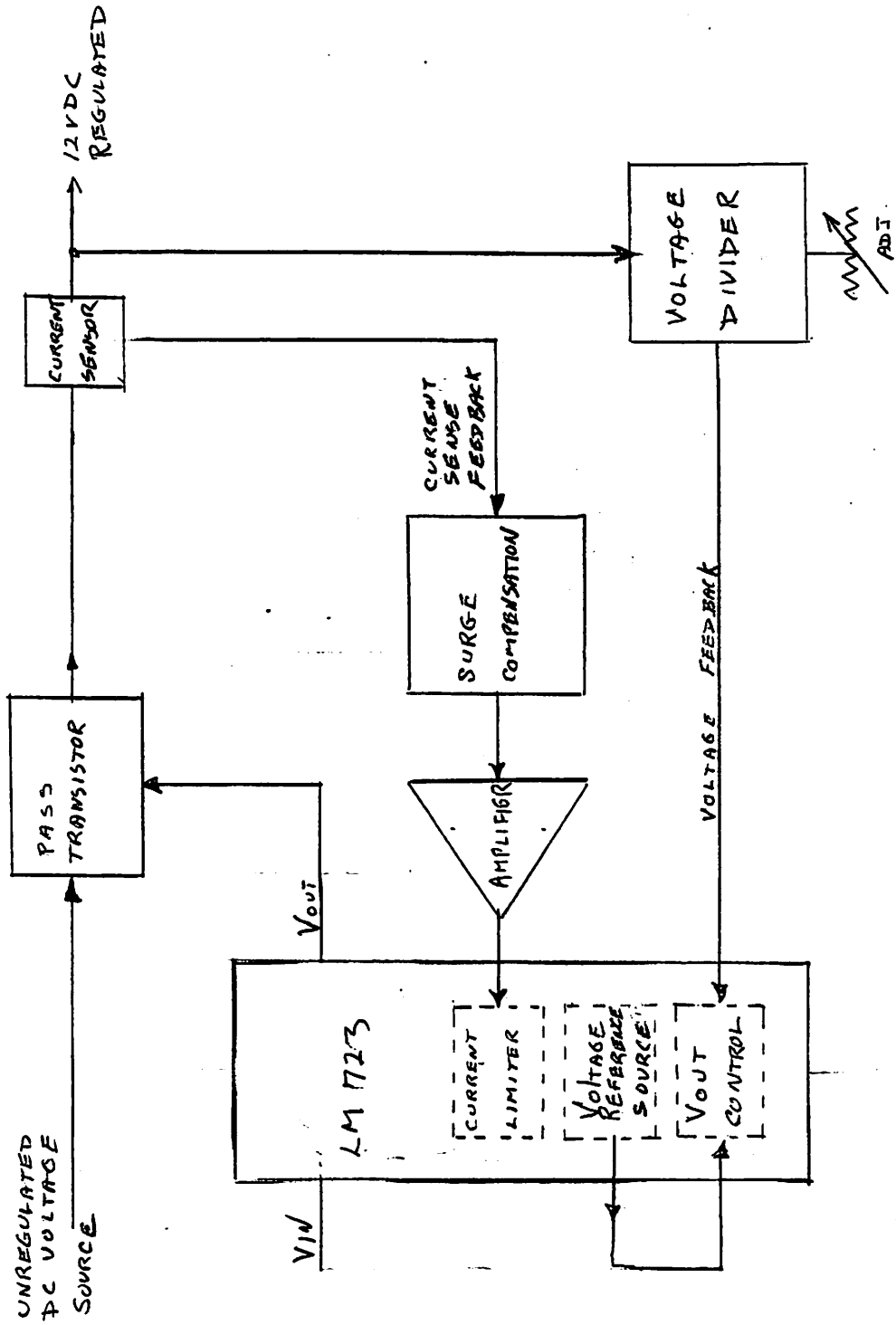
Foldback limiting is effected in this case by the use of a comparator in the current-sense feedback loop. At normal current levels, the comparator is saturated, and no limiting voltage is applied to the IC regulator. As the regulator output current approaches the limiting value, the comparator operates as a feedback amplifier, and current limiting proceeds normally. A short circuit on the regulator output line will drop the output voltage to zero, or nearly so. Under that condition, the comparator quickly cuts off, applies full limiting voltage to the IC, and forces the regulator to reduce the output current to substantially below the full load value.

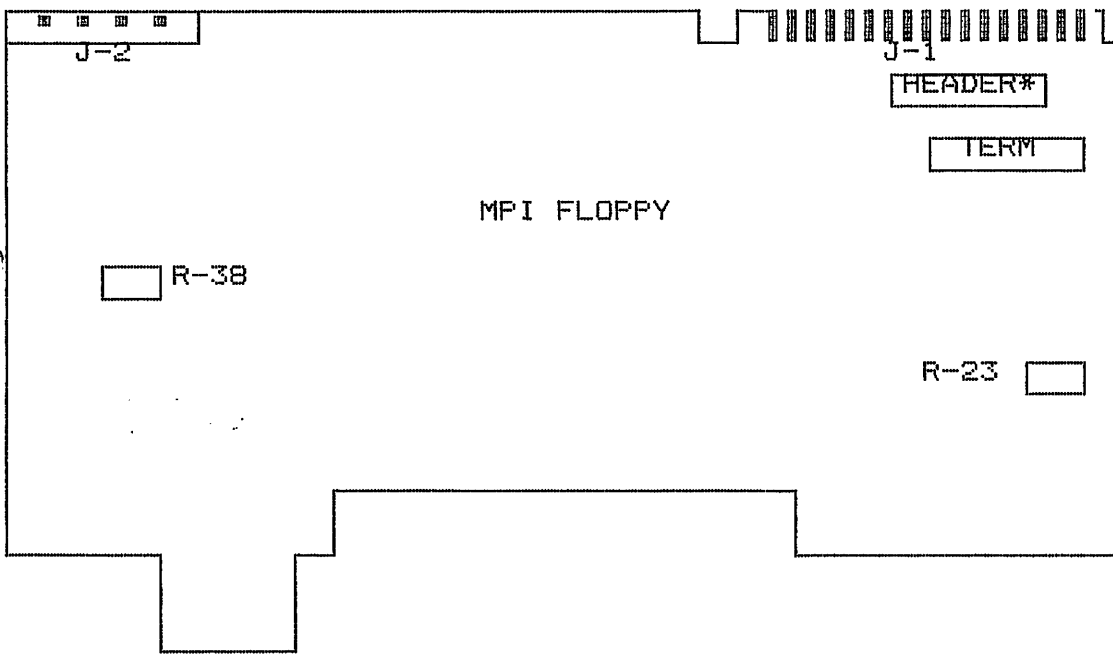
Current Surge Compensation is required by the +12 VDC regulator because it powers the Winchester Drive(s), and is therefore subject to a heavy starting current surge at the time of initial power-up. The surge exceeds the design current limiting level for several seconds. To prevent regulator shut-down during this period, additional circuitry temporarily increases the current limiting level, and then lowers it back to normal in two steps. This process is carried out by a pair of comparators and an RC time delay network. Initially, these comparators act together to reduce the reference voltage of the comparator in the current limiting feedback loop, thus raising the current limiting threshold. The compensating comparators drop out of the circuit sequentially as the capacitor in the time delay network charges.











NOTE:  
ALL CONNECTORS  
ARE KEYED.

\* HEADER  
JUMPER 2-13  
AND 7-8

CR/LF TO  
CONTINUE  
?



FLOPPY  
OR  
WINCHESTER #2

J-2

J-1

SW-1

J-3  
POWER

|   |   |
|---|---|
| 6 | 5 |
| 4 | 3 |
| 2 | 1 |

R  
E  
A  
R

F  
R  
O  
N  
T

L-100  
FROM R-2  
379-2000

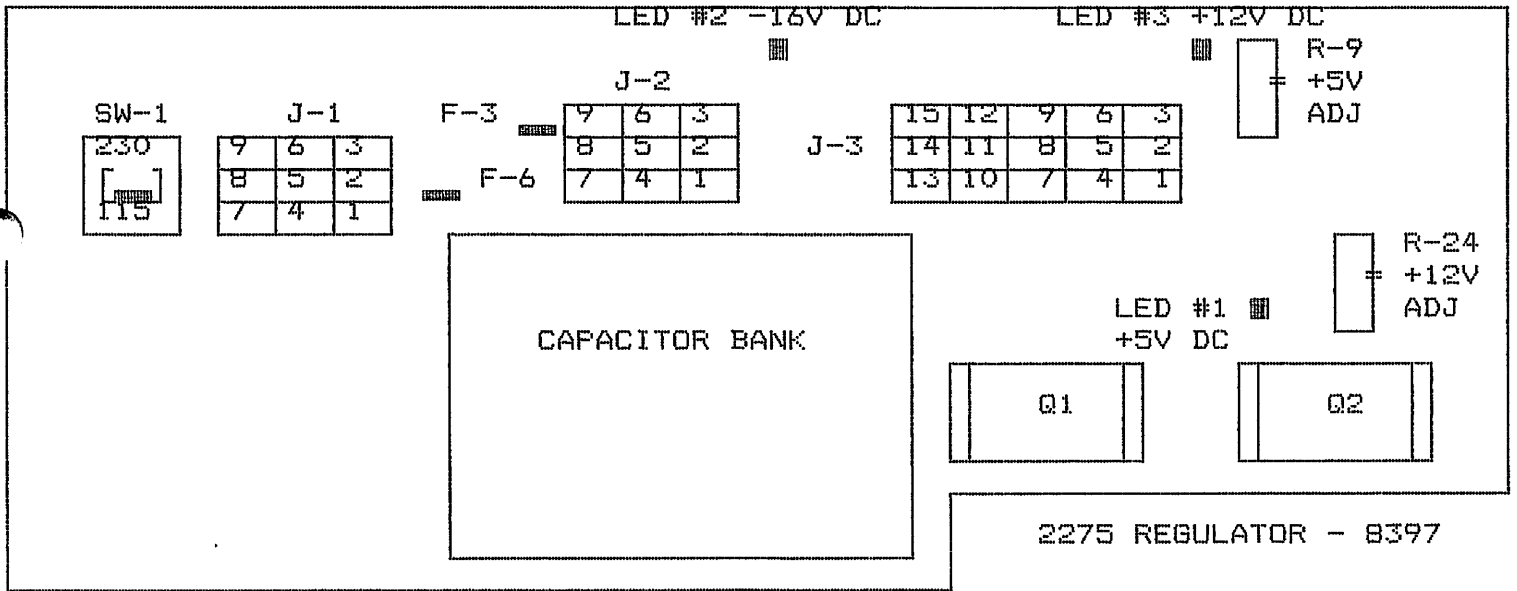
WINCHESTER #1

J-5

J-4

2275-10720730760  
8396 REV 1

CR/LF TO CONTINUE?



CR/LF TO CONTINUE?

8397 REGULATOR  
CONNECTOR J-1

|   |     |                                   |
|---|-----|-----------------------------------|
| 1 | --- | AC IN FROM FUSE AND LINE SWITCH * |
| 2 | --- | NOT USED                          |
| 3 | --- | 110/220VAC                        |
| 4 | --- | 110/220VAC                        |
| 5 | --- | AC IN FROM LINE SWITCH            |
| 6 | --- | 110/220VAC                        |
| 7 | --- | 110/220VAC                        |
| 8 | --- | AC TO FAN                         |
| 9 | --- | AC TO FAN                         |

\* NOTE:

PIN #1 GOES TO THERMAL CIRCUIT BREAKER ON  
HEATSINK OF Q1 THEN RETURNS TO SWITCH S-1

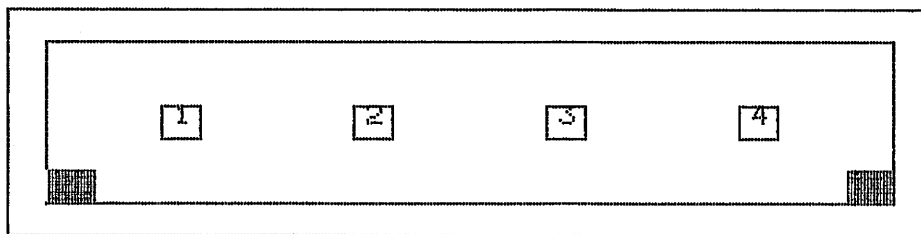
CR/LF TO CONTINUE?

8397 REGULATOR  
CONNECTOR J-2

|   |     |            |
|---|-----|------------|
| 1 | --- | 0 VOLTS DC |
| 2 | --- | AC 1       |
| 3 | --- | AC 2       |
| 4 | --- | 0 VOLTS DC |
| 5 | --- | 0 VOLTS DC |
| 6 | --- | NOT USED   |
| 7 | --- | AC 4       |
| 8 | --- | AC 5       |
| 9 | --- | AC 3       |

CR/LF TO CONTINUE?

J-3 VOLTAGE CONNECTOR



PIN #1 = +12V DC

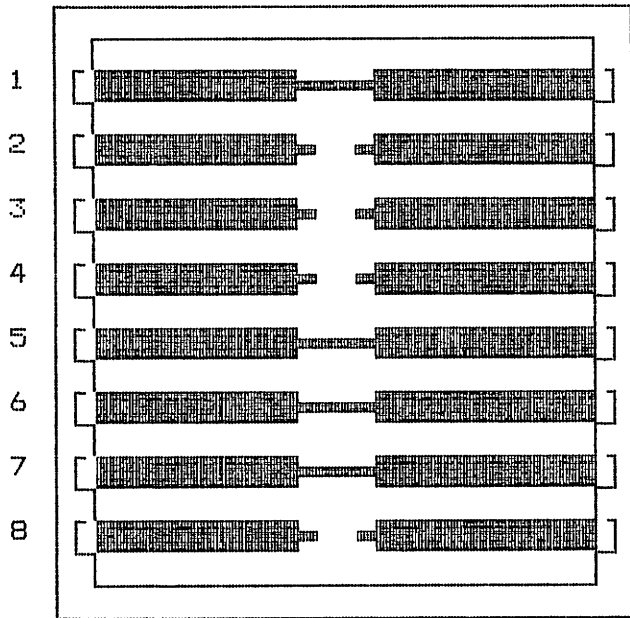
PIN #2 = +12V RETURN

PIN #3 = +5V RETURN

PIN #4 = +5V DC

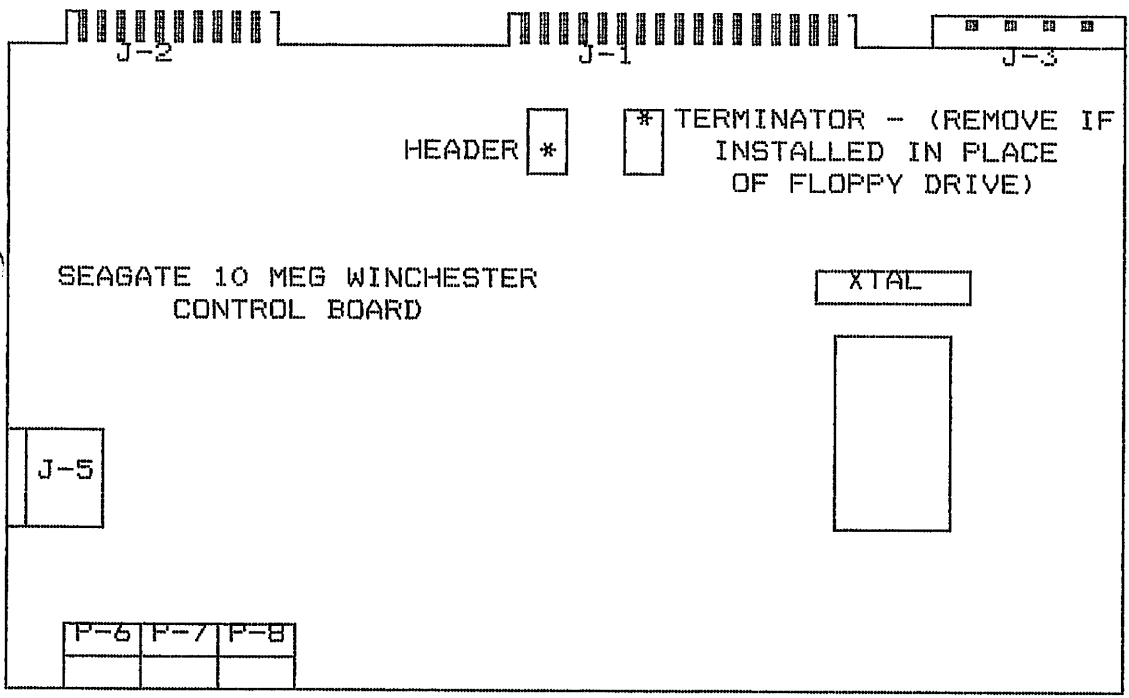
CR/LF TO CONTINUE?

HEADER FOR SEAGATE WINCHESTER



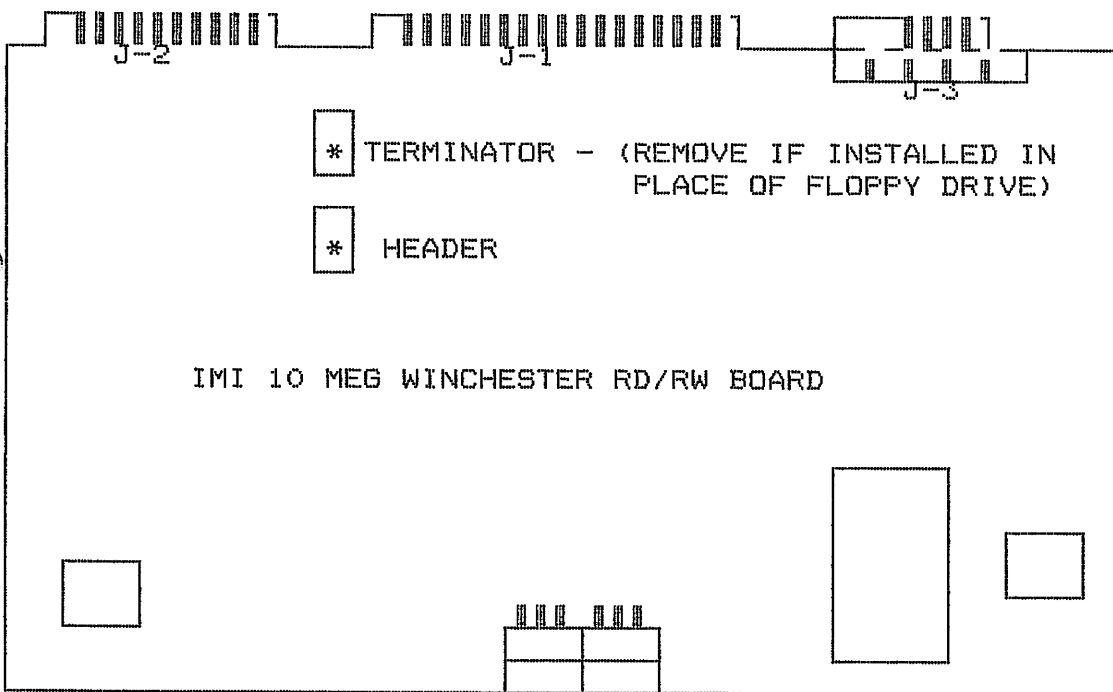
- 16 \*\* DRIVE SELECT #1
- 15 \*\* DRIVE SELECT #2
- 14 \*\* DRIVE SELECT #3
- 13 \*\* DRIVE SELECT #4
- 12 \*\* GROUND - NO CONNECTION
- 11 \*\* GROUND - NO CONNECTION
- 10 \*\* GROUND - NO CONNECTION
- 9 \*\* DRIVE ALWAYS SELECTED

FN/TAB TO RETURN TO MENU



NOTE:  
ALL CONNECTORS  
ARE KEYED.

CR/LF TO  
CONTINUE  
?

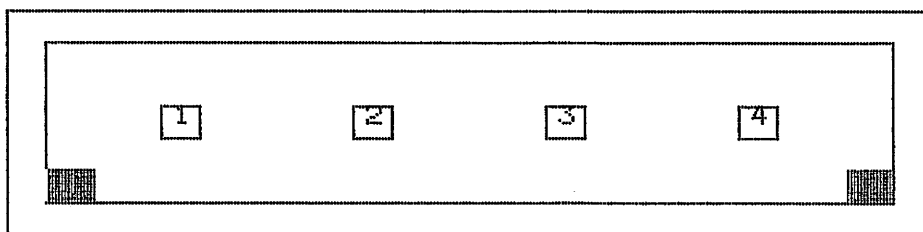


NOTE:  
ALL CONNECTORS  
ARE KEYED.

CR/LF TO  
CONTINUE  
?



J-3 VOLTAGE CONNECTOR



PIN #1 = +12V DC

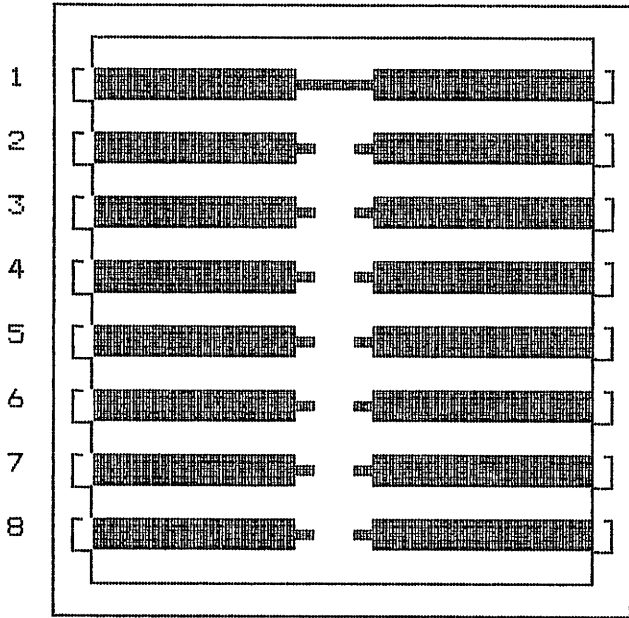
PIN #2 = +12V RETURN

PIN #3 = +5V RETURN

PIN #4 = +5V DC

CR/LF TO CONTINUE?

HEADER FOR IMI WINCHESTER



- 16 \*\* DRIVE SELECT #1
- 15 \*\* DRIVE SELECT #2
- 14 \*\* DRIVE SELECT #3
- 13 \*\* DRIVE SELECT #4
- 12 \*\* OPTIONAL RESET
- 11 \*\* SIZE SELECT 0
- 10 \*\* SIZE SELECT 1
- 9 \*\* DRIVE ALWAYS SELECTED

FN/TAB TO RETURN TO MENUE

?

2275 FUSE LIST

MAIN LINE FUSE - 115 VOLTS AC = 2.3 AMPS  
" " " 220 VOLTS AC = 1.6 AMPS  
FUSE #1 - JUMPER - NEXT TO J-2  
FUSE #2 - JUMPER - NEXT TO J-2  
FUSE #3 - 24 VOLTS = 4A \* NO FUSE ON R-0 BOARDS  
FUSE #3 - 24 VOLTS = 4A \* FUSE ON R-2 BOARDS  
FUSE #4 - JUMPER - NEXT TO J-2  
FUSE #5 - JUMPER - NEXT TO J-2  
FUSE #6 - 8.5 VOLTS = 4A \* NO FUSE ON R-0 BOARDS  
FUSE #6 - 8.5 VOLTS = 4A \* FUSE ON R-2 BOARDS

FN/TAB TO RETURN TO MENUE?

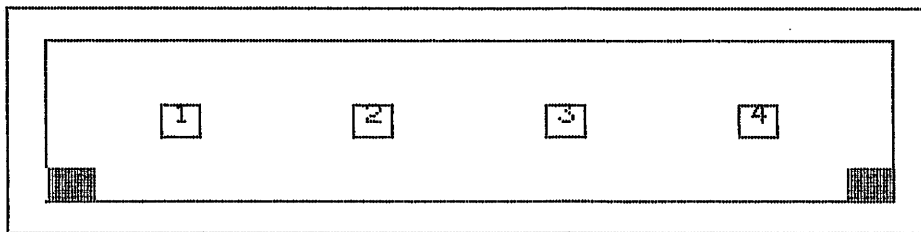
| 2275     | SWITCH CONFIGURATION |      |      |      |
|----------|----------------------|------|------|------|
| - XX     | 8396 BOARD           |      |      |      |
| - 10     | ON                   | ON   | ON   | ON   |
| - 30     | ON                   | ON   | ON   | OFF  |
| - XX     | ON                   | ON   | OFF  | ON   |
| - 20     | OFF                  | ON   | ON   | ON   |
| - 40     | OFF                  | ON   | ON   | OFF  |
| - XX     | OFF                  | ON   | OFF  | ON   |
| - 60     | OFF                  | ON   | OFF  | OFF  |
| SWITCH # | SW-4                 | SW-3 | SW-2 | SW-1 |

SWITCH ON = SWITCH CLOSED

FN/TAB TO RETURN TO MENU

?

J-2 VOLTAGE CONNECTOR



PIN #1 = +12V DC

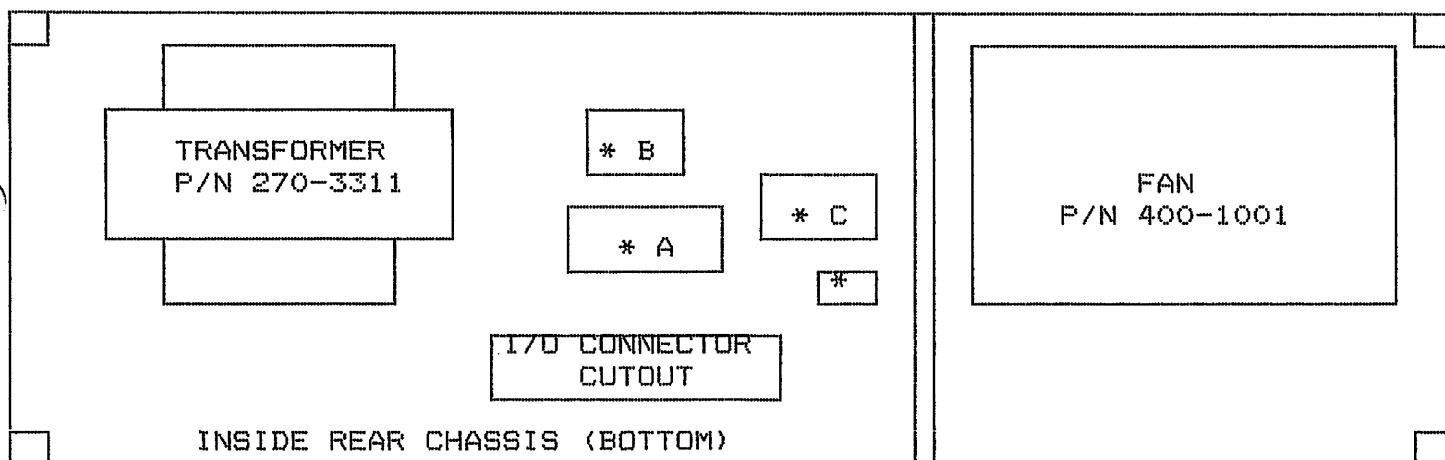
PIN #2 = +12V RETURN

PIN #3 = +5V RETURN

PIN #4 = +5V DC

CR/LF TO CONTINUE?

2275 POWER SUPPLY AND CHASSIS ASSEMBLY P/N 270-0870



\* = FUSE HOLDER P/N 360-0018

\*A = LINE FILTER P/N 410-2024

\*B = LINE SWITCH P/N 325-0059

\*C = RECTIFIER P/N 380-4005

NOTE: - IF ANY COMPONENT IS DEFECTIVE ORDER COMPLETE CHASSIS ASSEMBLY

FN/TAB TO RETURN TO MENUE - CR/LF TO RESTART?

8397 REGULATOR  
CONNECTOR J-3

|    |     |                       |
|----|-----|-----------------------|
| 1  | --- | +12 VOLTS OUT         |
| 2  | --- | +5 VOLTS OUT          |
| 3  | --- | +5 VOLTS OUT          |
| 4  | --- | +12 VOLTS OUT         |
| 5  | --- | +5 VOLTS OUT          |
| 6  | --- | +5 VOLTS OUT          |
| 7  | --- | 0 VOLTS DC            |
| 8  | --- | 0 VOLTS DC            |
| 9  | --- | 0 VOLTS DC            |
| 10 | --- | 0 VOLTS DC            |
| 11 | --- | 0 VOLTS DC            |
| 12 | --- | 0 VOLTS DC            |
| 13 | --- | +16 VOLTS UNREGULATED |
| 14 | --- | NOT USED              |
| 15 | --- | -16 VOLTS UNREGULATED |

CR/LF TO START PROGRAM AGAIN - FN/TAB TO RETURN TO MENUE?

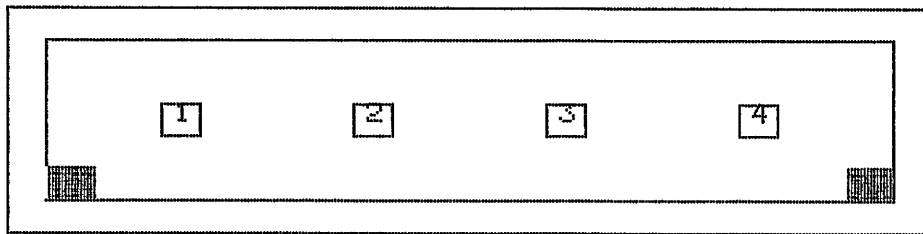
8396 BOARD  
CONNECTOR J-3

|   |     |  |
|---|-----|--|
| 1 | --- | +5V REGULATED                                |
| 2 | --- | +16V UNREGULATED - (INPUT TO +12V REGULATOR) |
| 3 | --- | +5V REGULATED                                |
| 4 | --- | -16V UNREGULATED - (INPUT TO -12V REGULATOR) |
| 5 | --- | 0 VOLTS DC                                   |
| 6 | --- | 0 VOLTS DC                                   |

CR/LF TO RESTART -- FN/TAB TO RETURN TO MENUE?



J-3 VOLTAGE CONNECTOR



PIN #1 = +12V DC

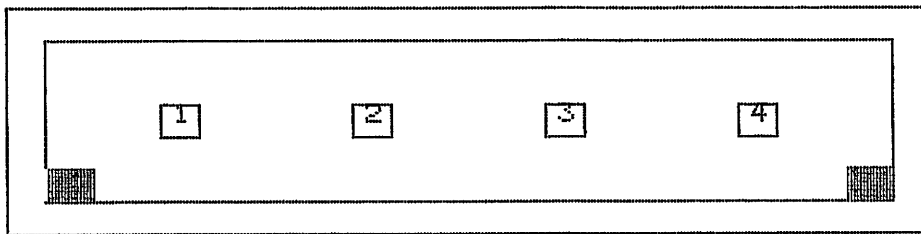
PIN #2 = +12V RETURN

PIN #3 = +5V RETURN

PIN #4 = +5V DC

CR/LF TO CONTINUE?

J-2 VOLTAGE CONNECTOR



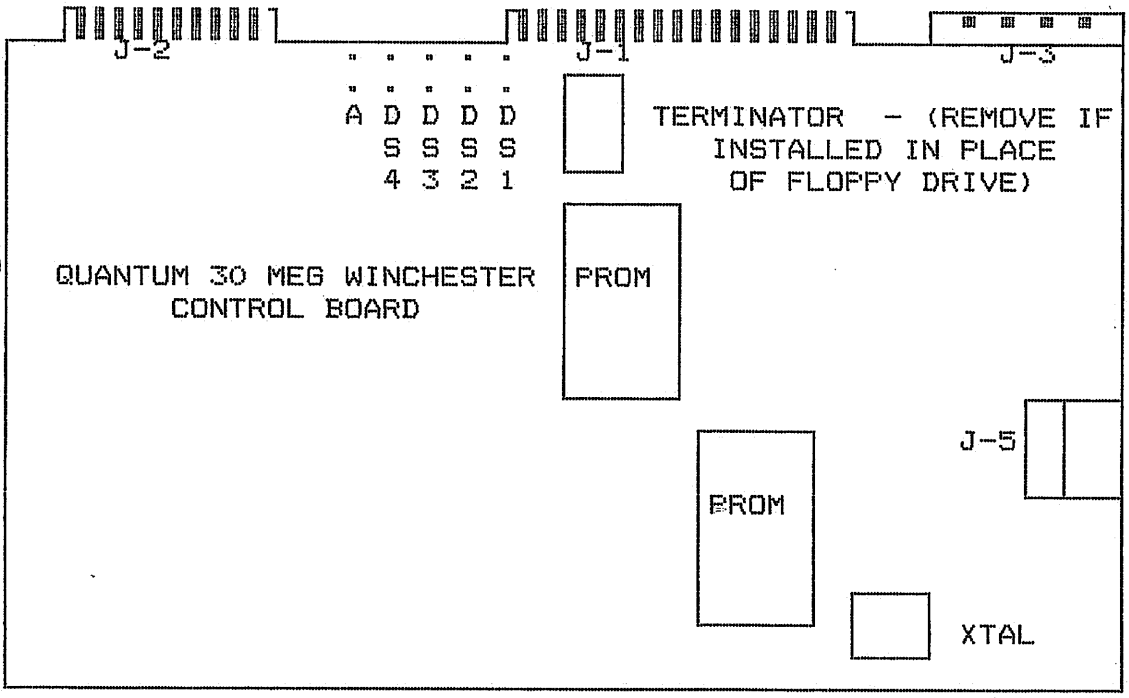
PIN #1 = +12V DC

PIN #2 = +12V RETURN

PIN #3 = +5V RETURN

PIN #4 = +5V DC

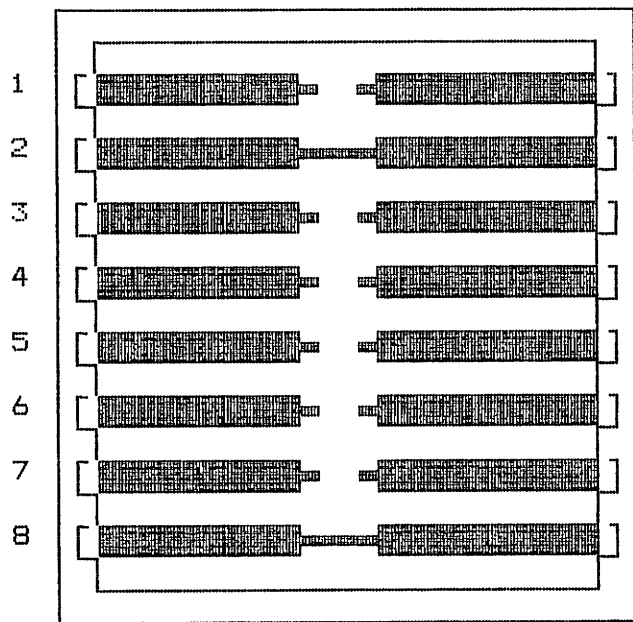
CR/LF TO CONTINUE?



NOTE:  
ALL CONNECTORS  
ARE KEYED.

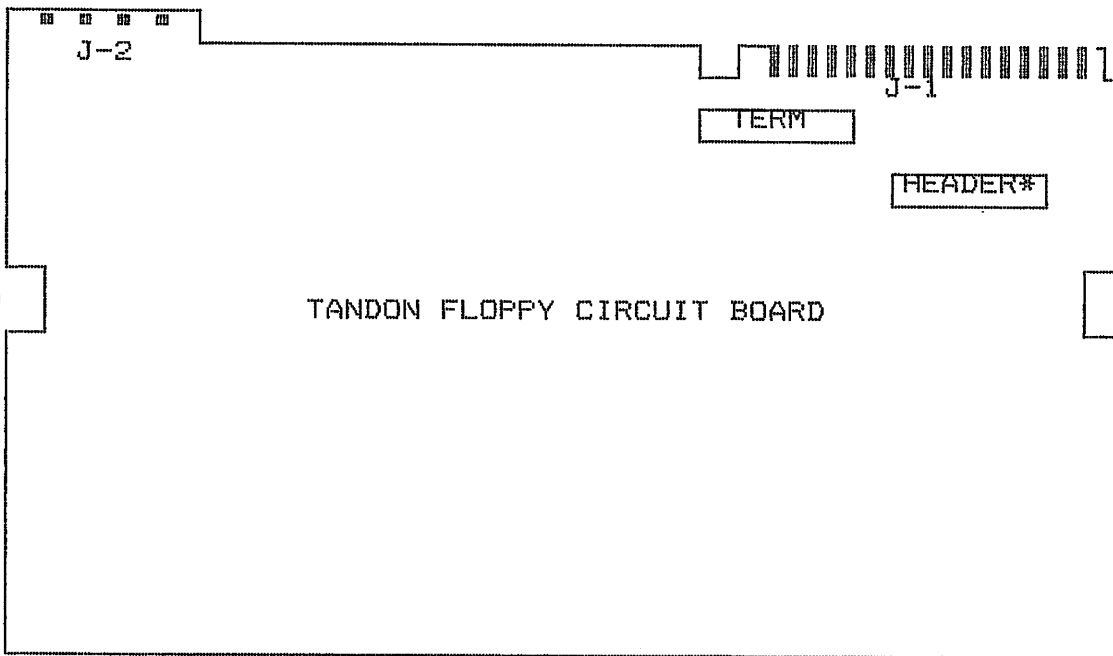
CR/LF TO  
CONTINUE  
?

HEADER FOR TANDON 5.25'' FLOPPY



- 16 \*\* HEAD SOLONOID WITH DRIVE SELECT
- 15 \*\* DRIVE SELECT #1
- 14 \*\* DRIVE SELECT #2
- 13 \*\* DRIVE SELECT #3
- 12 \*\* DRIVE SELECT #4
- 11 \*\* MUX
- 10 \*\* NOT USED
- 9 \*\* HEAD SOLONOID WITH MOTOR ON

FN/TAB TO RETURN TO MENUE

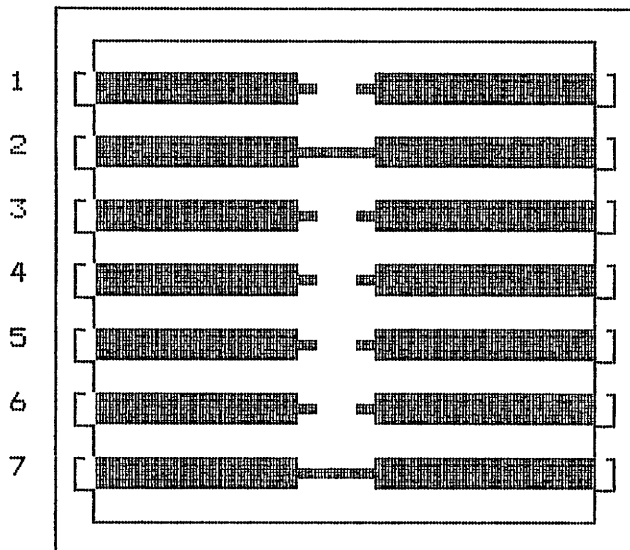


NOTE:  
ALL CONNECTORS  
ARE KEYED.

\* HEADER  
JUMPER 2-15  
AND 8-9

CR/LF TO  
CONTINUE  
?

HEADER FOR MPI 5.25'' FLOPPY



- 14 \*\* HEAD SOLONOID WITH DRIVE SELECT
- 13 \*\* DRIVE SELECT #1
- 12 \*\* DRIVE SELECT #2
- 11 \*\* DRIVE SELECT #3
- 10 \*\* MUX
- 9 \*\* DRIVE SELECT #4
- 8 \*\* HEAD SOLONOID WITH MOTOR ON

FN/TAB TO RETURN TO MENUE

?

5.25'' FLOPPY DRIVE P1/J1 I/O SIGNAL CONNECTOR

|    |    |      |   |
|----|----|------|---|
| 1  | 2  | ---- | PIN 2 = NOT USED                              |
| 3  | 4  | ---- | PIN 4 = MAY BE USED AS DOOR LOCK OR INDICATOR |
| 5  | 6  | ---- | PIN 6 = DRIVE SELECT #4                       |
| 7  | 8  | ---- | PIN 8 = INDEX                                 |
| 9  | 10 | ---- | PIN 10 = DRIVE SELECT #1                      |
| 11 | 12 | ---- | PIN 12 = DRIVE SELECT #2                      |
| 13 | 14 | ---- | PIN 14 = DRIVESelect #3                       |
| 15 | 16 | ---- | PIN 16 = MOTOR ON                             |
| 17 | 18 | ---- | PIN 18 = DIRECTION SELECT                     |
| 19 | 20 | ---- | PIN 20 = STEP                                 |
| 21 | 22 | ---- | PIN 22 = WRITE DATA                           |
| 23 | 24 | ---- | PIN 24 = WRITE GATE                           |
| 25 | 26 | ---- | PIN 26 = TRACK 00                             |
| 27 | 28 | ---- | PIN 28 = WRITE PROTECT                        |
| 29 | 30 | ---- | PIN 30 = READ DATA                            |
| 31 | 32 | ---- | PIN 32 = SIDE SELECT                          |
| 33 | 34 | ---- | PIN 34 = NOT USED                             |

FN/TAB TO RETURN  
TO MENUE?

NOTE: ALL ODD NUMBERED PINS ARE 0 VOLT DC RETURN LINES

10 MEG WINCHESTER DRIVE P1/J1 I/O SIGNAL CONNECTOR

|    |    |       |                           |
|----|----|-------|---------------------------|
| 1  | 2  | ----- | PIN 2 = RESERVED          |
| 3  | 4  | ----- | PIN 4 = HEAD SELECT 2     |
| 5  | 6  | ----- | PIN 6 = WRITE GATE        |
| 7  | 8  | ----- | PIN 8 = SEEK COMPLETE     |
| 9  | 10 | ----- | PIN 10 = TRACK 00         |
| 11 | 12 | ----- | PIN 12 = WRITE FAULT      |
| 13 | 14 | ----- | PIN 14 = HEAD SELECT 0    |
| 15 | 16 | ----- | PIN 16 = RESERVED         |
| 17 | 18 | ----- | PIN 18 = HEAD SELECT 1    |
| 19 | 20 | ----- | PIN 20 = INDEX            |
| 21 | 22 | ----- | PIN 22 = READY            |
| 23 | 24 | ----- | PIN 24 = STEP             |
| 25 | 26 | ----- | PIN 26 = DRIVE SELECT #1  |
| 27 | 28 | ----- | PIN 28 = DRIVE SELECT #2  |
| 29 | 30 | ----- | PIN 30 = DRIVE SELECT #3  |
| 31 | 32 | ----- | PIN 32 = DRIVE SELECT #4  |
| 33 | 34 | ----- | PIN 34 = DIRECTION SELECT |

FN/TAB TO RETURN  
TO MENU?

NOTE: ALL ODD NUMBERED PINS ARE 0 VOLT DC RETURN LINES



DRIVE SELECT JUMPERS



\*\* DRIVE SELECT #1

\*\* DRIVE SELECT #2

\*\* DRIVE SELECT #3

\*\* DRIVE SELECT #4

\*\* ALWAYS SELECTED

FN/TAB TO RETURN TO MENUE

?

M-E-M-O-R-A-N-D-U-M

TO: Gail Stanwyck M/S 1369  
FROM: Paul J. Hossfeld  
DEPARTMENT: Diagnostic Software Support M/S 8239(1)  
DATE: September 14, 1984  
SUBJECT: 2275 BIT

-----

The 2275 BIT Documentation Part Number: 760-1213  
Software Release: 1.0  
Prom Part Number: 379-2000  
can be released.

I have made the following change to the documentation in order to clarify a situation that occurred during testing. The enclosed diskette contains the correction.

Procedure 5.2 (Test Descriptions), the following note was added;

If the heads are ON track zero and they can't step off track,  
the BIT will not sense this as an error.

Dave Netzel has agreed to make the following change to the error indication on the next rev. of the firmware. The LED's remain ON if the controller board fails and, they blink if one or both drives fail.

This is for world distribution.

*HIT RESET to continue.  
Ailing drive cannot be accessed.*

Thank You

*Paul J. Hossfeld*  
Paul J. Hossfeld

cc

George Morgan  
Dave Netzel M/S 1369  
Harvy Worthington M/S 0125

## 1.0 PROJECT RESPONSIBILITY

|                             |                                |
|-----------------------------|--------------------------------|
| 1.1 Diagnostic Development  | Dave Netzel<br>DICE            |
| 1.2 Hardware Project Leader | Paul Congo                     |
| 1.3 Hardware Design         | Dan Messuri                    |
| 1.4 Firmware Design         | Ken Same1                      |
| 1.5 Software Design         | Bruce Patterson                |
| 1.6 Customer Engineering    | Scott Maxwell<br>Paul Hossfeld |

## 2.0 HARDWARE

- 2.1 The 2200 MVP 5 1/4" Disk Peripheral is a small stand-alone, add-on storage device for the 2200 MVP System. The disk processing unit will consist of a 5 1/4" Winchester, a 5 1/4" Floppy or two 5 1/4" Winchesters. The initial offering will consist of a 360K 48TPI floppy and a 5Mb Winchester disk. Potential options include a 720K 96TPI floppy and a 10Mb Winchester. The 2200 MVP 5 1/4" Disk Peripheral will connect to the 2200 MVP via a Triple Controller Board, and will contain a Z80 based Controller board, Power Supply, and the disk drive configuration of 1 Winchester & 1 Floppy or 2 Winchesters.
- 2.2 The Disk Controller board contains the following hardware:
- 1 - Z80A CPU 4MHZ
  - 2 - Z80A CTC 4MHZ
  - 1 - AMD9517 DMA Controller
  - 1 - uPD765 Floppy Disk Controller
  - 64k of Memory (8k of PROM, 56k of usable RAM)
  - Discrete logic Winchester Disk Controller
  - 2200 Interface Logic

## 3.0 DIAGNOSTIC PACKAGES

### 3.1 Built In Test (Z80 Assembly Language)

- 3.1.1 The Built In Test is designed to operate from power-up and will test as much of the logic available as possible within a restricted time frame. The traditionally untestable areas are the 2200 interface logic and the disk interface logic. Actual PROM space available to diagnostics amounts to approximately 1k.
- 3.1.2 User Interface - LED's on the Disk Drives will indicate failure via flashing on and off.
- 3.1.3 Diagnostic control user input may be provided via switch settings which enable two modes of operation, Mode 1 = Run self test and jump to firmware when completed, (Normal operating mode). Mode 2 = Loop on self test for manufacturing subassembly run-in. Mode 1 is the only mode currently available in the preliminary release of the BIT for Beta sites.

## 3.1 Built In Test (Z80 Assembly Language) Continued

3.1.3 Tests within the Built In Test are described below:

1. Since the last 30 PROM addresses are used for memory mapped I/O, no PROM Checksum Test will be run. The first test will be the Push/Pop Memory test designed to detect timing problems as well as detect cell failures.
2. Bad Parity Detect & Parity Generator Test: This test checks that NMI's can be detected using the write/read bad parity circuitry. Then the parity generator is presented with all 256 possible data patterns to insure no erroneous parity errors will occur.
3. CTC Addressing Test: This test checks the I/O addressing of the CTC's. It also checks that the data lines to and from the CTC's.
4. CTC Downcounter Timer Mode Test: This test checks the downcounter function of the CTC's timer mode, and their ability to decrement properly down to a zero value. Counter Mode testing is not done.
5. CTC Interrupt Test: This test checks that each channel of the two CTC's will provide vectored interrupts to the Z80A CPU.
6. DMA MASTER CLEAR & Data Bus Test: This test checks the "master clear" function of the DMA as well as the data bus, utilizing the temporary and status registers of the DMA.
7. DMA I/O Addressing Test: This test checks the I/O addressing to the DMA utilizing the Current Address registers and Word Count registers for all channels.
8. DMA Current Address and Word Count Registers Data Test: This test checks the Current Address and Word Count Registers for all channels of the DMA using incrementing and decrementing 256 byte data patterns to insure all DMA data holding capabilities are intact.

Why  
this is a  
problem.

3.1.4 Additional tests which will check the disks will be developed. Exact specifications and tests are not available at this writing. Ken Samel will provide the means of performing these tests utilizing firmware subroutines. A revision to the DEP will be developed and distributed when these additional tests have been defined.

## 3.2 Board Repair (DICE Systems, Inc.)

- 3.2.1 Board Repair diagnostics are provided to aid repair technicians in isolating faults to the chip level when possible and to the circuit level otherwise. DICE Systems, Inc. have been contracted to perform the development work for this level of diagnostic. The functional description of this diagnostic prior to starting program development has been provided to Diagnostic Engineering by DICE. A copy of this Specification is attached.

## 3.3 Functional Test (2200 BASIC II)

- 3.3.1 The functional test is normally used in a field environment. In the case of a disk controller it generally is used to exercise the drives and controller to detect unit failures. If this disk controller is the only one available, then isolation of the field replaceable unit is determined by the Built In Test because the operating system must utilize the disk drive in order to be initialized. "MultiDisk" and "GenEx" will be upgraded to handle these new drives.

## 3.4 Manufacturing Run In (2200 BASIC II)

- 3.4.1 The Run In diagnostic testing is used in manufacturing to weed out infant mortality failures as well as provide reliability verification. It is desirable to run in as many units as possible in a single test bed which typically utilizes a BASIC monitor, the MVP with a 9 slot I/O backplane, a 2236DE terminal, a terminal controller, a 2270A disk controller, and the remaining slots set aside for 3 Triple controllers for testing the Disk Controller and Disk units. Exactly how manufacturing intends to run in these units will be solicited.

DOCUMENT: 23001  
DATE: AUGUST 24, 1983  
CHARGE NUMBER: P.O. LOW-070-W077094

REVISION 0.0 OF

DIAGNOSTIC ENGINEERING FUNCTIONAL SPECIFICATION FOR

2275 WINCHESTER DISK CONTROLLER

ISSUED BY:

-----  
Project Leader

-----  
Supervisor

APPROVED BY:

-----  
-----

REVIEWED BY:

-----  
-----  
-----  
-----

REVISION HISTORY:

|              |                |                               |
|--------------|----------------|-------------------------------|
| Revision 0.0 | 24 August 1983 | V.F. Husovsky<br>Dice Systems |
| Revision 0.1 | 29 August 1983 | V.F. Husovsky<br>Dice Systems |

WANG LABORATORIES  
LOWELL, MASSACHUSETTS

CONTENTS

|                                    | Page  |
|------------------------------------|-------|
|                                    | ----- |
| 1.0 OVERVIEW OF DIAGNOSTIC PRODUCT | 3     |
| 2.0 PRODUCT GOALS                  | 4     |
| 3.0 REQUIREMENTS                   | 5     |
| 4.0 FUNCTIONAL DESCRIPTION         | 6     |
| 5.0 BIBLIOGRAPHY                   | 13    |

## 1.0 OVERVIEW

### 1.1 Product Description

The 2275 Disk Controller Diagnostic is designed to provide Wang manufacturing with an intensive exerciser routine which will test for correct operation of the 5 1/4 inch Disk Controller Board. The program is written in Z80 assembly language and will reside in the 2764 PROM. The PROM will replace existing controller firmware during testing. The program will perform power-up tests before entering a communications mode. When in the communications mode, the program establishes a link with the 2200 CPU before proceeding to further 2275 Controller tests. This communication link allows the test program to receive commands which are used in performing the remaining tests. The tests are menu driven from the Basic Monitor Workstation at the Host System. The updates to the Host BASIC code will be performed as per DICE proposal number 24101.

### 1.2 Product Users and Uses

The Test is designed to begin operation at power-up, and will aid repair technicians in locating faults at the circuit level and at the chip level when possible. The board level diagnostic will require a Basic II monitor. Inclusion of the monitor will enable multiple test selection, and loop on error.

#### NOTE

This diagnostic may be used in conjunction with the ZBUG Debugger Utility. Use of the utility will allow the operator to examine program register information, including expected and actual data patterns.



## 2.0 PRODUCT GOALS

### 2.1 Performance Goals

The 2275 Controller Board diagnostic test sequence will provide fast isolation of hard failures. A successful run of the diagnostic will indicate with a high degree of confidence that all major system components are working properly. A message will be displayed on the Basic Monitor console confirming successful completion of each test phase. Test runtime will be kept to a minimum.

### 2.2 Compatibility Goals

The 2275 Disk Controller test program will be written in Z80 assembly language. Tests will be written in a modular fashion and contained within a 2764 8K PROM. Existing Z80 assembly language diagnostics, Basic 2 Monitors, and Disk Exercisers will be used to implement project development.

### 3.0 REQUIREMENTS

#### 3.1 Hardware Description

##### 2275 Disk Controller Board (Part #8396)

Consisting of:

- 1 - Z80 Central Processing Unit
- 2 - Z80 Counter Timing Circuits
- 1 - AMD 9517 DMA Controller
- 1 - NEC 765 Floppy Disk Controller
- 1 - WD1100 (4 Chip set Winchester Controller)
- 1 - 2764 PROM (Firmware)
- 1 - 2732A PROM (Micro-Sequencer)
- 64k RAM (Disk Buffer)
- 2200 Interface Logic

#### 3.2 System Configuration

The equipment required for use with this repair diagnostic will be a MVP 2200 System with 2270A Disk Drive and 2236 DE Monitor, a Triple Controller Interface, a 2275 Disk Controller and the 'Zbug' Z80 Debugger. Both Floppy and Winchester 5 1/4 inch Drives are to be connected to the Disk's Controller.

## 4.0 POWER-UP TESTS

### 4.1 Processor Tests

The Z80A processor tests will begin with a check of basic control instructions. This test procedure will determine the processor's ability to execute an unconditional jump instruction, and then proceed to verify operation of the accumulator and conditional flag instructions. Subsequently, 8 and 16-bit register operations will be performed. The ability to set all register bits will be verified, along with correct flag status during rotate instructions. Operation of the built-in dynamic RAM refresh register is also tested.

### 4.2 Memory Tests

Memory tests are performed on the Disk Buffer 64K Byte Dynamic RAM. Both data and addressing tests are performed. A further test will check for parity errors. Initial Memory test failure is reported by the ZBUG Debugger. Any errors will display the failing address and the expected and actual data received.

A checksum test is performed to ascertain that PROM contents are correct.

### 4.3 Counter Timer Circuit Tests

Z80 CTC tests begin with an initialize condition status check. The internal 8 bit Channel Control Registers are used to verify Z80 CPU access to both CTC chips. The Internal 8 bit Time Constant Register will be loaded from the CPU, and the CTC's Timer Mode will be enabled and checked. This test sequence includes the use of the 8 bit Prescaler Register which is capable of dividing the system clock by either 16 or 256. This facility is designed for use by the Down Counter during Timer Mode operations.

#### 4.4 DMA Controller Tests

The 9517 DMA Controller tests begin with a check of the basic power-up conditions of the chip. The register addressing logic is exercised to ensure that each register can be accessed, and that the 344 bits of internal memory are functional. Tests are performed on the 16 bit Current Address Registers which are used during DMA transfers. Also, the 9517's Single Transfer Mode operation is checked by performing byte transfers to and from memory.

#### 4.5 Floppy Disk Controller Tests

Initially the 765 Floppy Controller tests verify chip status after a power-up or reset. Tests are performed on the 8 bit internal Data Register. A command sequence is then executed, and status register information is used to check for proper 765 Controller operation.

#### 4.6 WD1100 Winchester Controller Tests

A power-up status check is performed. A command sequence is generated to validate operation of the micro-sequencer firmware.

## 5.0 2200 COMMUNICATIONS TESTS

Tests are performed to verify the handshaking signals. These signals are essential element in communications with the 2200 MVP System. Status checks are completed, these test the Reset Signal, and the CPB Ready/Busy Signals. Upon successful completion of these tests, the controller awaits proper input from the 2200 before continuing with the menu selectable tests. The following tests can be run by command from the Monitor Workstation. Error reporting will consist of English Messages. Messages are displayed along with any available test results.

## 6.0 MONITOR OPERATED TESTS

### 6.1 Push-Pop RAM Test

A comprehensive Memory test is performed. This test is designed to discover any unique memory failures that might have escaped initial power-up memory testing. Error reporting is done by the 2200. The expected data, actual data read, and the address of the failure will be displayed on the screen.

### 6.2 CTC - 2200 I/O Tests

Tests are performed to check the I/O interrupt path to the Z80 CPU thru the Counter Timer Circuit (CTC) chips. Signals tested include the remaining 2200 interface lines; START and OBS, the 765 Controller's FLOPINT signal, the Winchester Controller's DONE and INDEX signals, and the 9517 DMA Controller's EOP signal.

### 6.3 DMA - 2200 I/O Tests

The ability of the 9517 to perform block transfers to and from the 2200 CPU is tested. The DMA chip is programmed to get 256 bytes from the 2200. When it has done this it is instructed to send the same 256 bytes back again.

The failure of the first part of this test is determined by the Z80. Any failure in the second part of the test must be determined by the Basic Monitor.

### 6.4 System Configuration Test

SW1 switch settings serve as input to the Z80 CPU, and the system's drive configuration is displayed using the 2200 Basic Monitor. Output messages will specify the peripherals which should be connected to the 2275 Controller in order to perform further tests. The Winchester and Floppy Drive combination is required to test many features of the 2275 Controller's hardware.

### 6.5 Disk Initialize Tests

After a select operation is performed, ready status for both drives is verified. Status checks are performed on both the fixed and removeable disk drives.

### 6.6 Floppy Disk Write Protect and Media Type Test

This test reads the 765 disk status register to determine if it can correctly detect the Floppy write protect tab. The sector size is checked to ascertain the media type. The 5 1/4 inch Floppy diskette media used contains either 256 byte sectors with 16 sectors per track, or 512 byte sectors with 9 sectors per track.

### 6.7 Floppy Disk Format Routine

This sequence formats the diskette in the removeable drive using the appropriate type of format. A special staggered sector map is used to facilitate the verify operation.

### 6.8 Floppy Disk Verify Test

This test reads each sector sequentially and checks for CRC or ID field errors. If no errors are found, it seeks the next track and repeats the test.

### 6.9 Floppy Disk Head Select Test

Verifies that a write operation uses the head specified. A sector containing the head number is written with each head and then each sector is read back to make sure its head number is correct.

#### 6.10 Floppy Write/Read Test

This test writes a worst case data pattern onto a sector on the inner tracks of the recording surface. These sectors are then read back to verify correct data. This test is performed to check that the data separator circuit is working properly.

#### 6.11 Floppy Reliability Test

Selection alternates between high and low tracks, a write operation and a read is performed for sector one on each. Any discrepancy between the expected and actual data is reported as an error.

#### 6.12 Winchester Write Protect Test

The 2200 CPU uses a reserved cylinder to maintain write protect status for the Winchester Drive. Upon power-up this reserve cylinder is read to determine whether write protect was enabled. A test is performed to check for correct operation of this function.

#### 6.13 Winchester Disk Format Routine

The Winchester Disk is formatted to initialize the sector headers.

#### 6.14 Winchester Disk Verify Test

Each sector is read sequentially and checked for CRC or ID field errors.

#### 6.15 Winchester Head Select Test

Check to see that when a particular head is specified, the data is really written to that head. A sector containing head number is written with each head and then each sector is read back to



make sure it's head number is correct.

#### 6.16 Winchester Write/Read Test

This test writes a worst case pattern onto a sector on the inner tracks of the recording surface. These sectors are then read back to verify correct data.

#### 6.17 Winchester Reliability Test

Alternately seeks a high track then a low track writing and reading sector 1 on each track as it proceeds.

1.0 BIBLIOGRAPHY

1. Wang 2275 5 1/4 inch Disks Controller Hardware Specification  
Revision-Preliminary 07/29/83
2. Wang 2200 SVP 7890 DPU Board Repair Diagnostic  
Revision-01 08/06/81
3. AMD-9517 DMA Data Sheet
4. NEC-765 FDC Data Sheet
5. Z80 CPU/CTC Data Sheets
6. Western Digital WD1100 Data Sheets

End of Document

NOTES ON 2275 TESTING 02/08/84

- 1) IF FLOPPY IS SELECTED AND DISKETTE IS NOT INSTALLED, THE SYSTEM WILL HANG.
- 2) AFTER INITIALIZATION BY MULTIDISK, THE 10 MEG WINCHESTER CAN BE FORMATTED SCRATCHED AND VERIFIED OK. PROBLEM IS THAT WHEN DISK CATALOG IS LISTED IT SHOWS SECTORS=00000.
  - 1) PROBLEM SHOWS UP ON WINCHESTER ONLY.
  - 2) TO SCRATCH WINCHESTER IN THIS CONDITION TURN POWER OFF AND BACK ON.
  - 3) FLOPPY ACTS NORMALLY AFTER MULTIDISK IS RUN.
- 3) INTERMITTANT I-98 ERRORS THE FIRST TIME THE FLOPPY IS SELECTED AFTER AN OPERATION ON ANOTHER DRIVE. (LIST DCT WILL FAIL AS AN EXAMPLE).
- 4) IF FLOPPY DISKETTE IS INSTALLED INCORRECTLY, DISKETTE IS SENSED AS INSTALLED BY SWITCH AND SYSTEM WILL HANG WAITING FOR DISK INDEX HOLE TO BE SENSED.
- 5) FLOPPY IS NOT RECOGNIZED BY MULTIDISK AND RECORDED ON DISK READY CHART. FLOPPY HAS TO BE ENTERED MANUALLY.

*Customer always need to have a blank diskette and floppy.  
Bring power up*

MEMORANDUM



RECEIVED

AUG 16 1984

MATT ZABOY  
Product Line Manager

TO : Matt Zaboy  
FROM: Michael Riley  
DATE: August 16, 1984  
SUBJ: 2275 Problems

During the past several months, I have had the opportunity to speak with several Branch Manager's and 2200 Customer Engineer's regarding problems that they are experiencing with the 2200 Product Line.

One of the problems is the lack of written support on the 2275 Disk Unit. I have yet to see a Field Service Maintenance Manual to support this product. Our Field Personnel are complaining since, they are suppose to install and maintain this unit but, they cannot get any written material on it. I feel that this is a major issue that must be resolved in order to support the field with the tools they need. This unit started to ship almost a year ago, and to-date there is over 2000 in the field.

Another issue is that, the 2275 is slated to be taught by Video Tape at Branch Level. This should be reconsidered due to the volume that these units are being sold. I recommend that the 2275 be part of the 2200 Formal Training Program, and be taught to all new Customer Engineer's since, they are the ones who will most likely install the units.

If I can be of any assistance regarding this matter, please contact me on extension (1-26) 60316.

Regards,

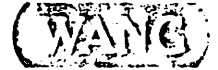
*Michael Riley*  
Michael Riley

MR/smr

CC: Gerry Crawford  
Earl Emerick  
Harvey Worthington

*Handwritten notes and signatures:*  
8/17  
Crawford's copy  
Gerry  
Earl  
Harvey  
M

*FU 8/27*



M-E-M-O-R-A-N-D-U-M

TO: Dave Netzel M/S 1369  
Richard Racicot M/S 1489

FROM: Paul J. Hossfeld

DEPARTMENT: Diagnostic Software Support M/S 8239(1)

DATE: August 31, 1984

SUBJECT: 2275 Firmware/BIT

-----

I have been reviewing the 2275 and have found the following problems;

With the floppy heads positioned at track zero and the head stepping motor disabled, no error is detected.

If one of the two drives has failed the BIT (LED indicating an error) and the second drive is accessed, there is no response and the system waits until it is reset. One bad drive shouldn't make the unit inoperable.

*Press Reset*

The 2275 I am testing has an R2 PROM, 30 MEG winchester and a floppy. The winchester has the address D21 and D22 the floppy address is D20. While testing the drives I found that they also respond to addresses D61, D62, and D60. The 60 series addresses are for the third drive on a three drive controller.

Thank You

Paul J. Hossfeld

cc

D. Logan M/S 1439  
G. Morgan  
M. Riley M/S 0122



MEMORANDUM

To: Roy Briscoe  
From: Harvey Worthington  
Subject: 2275 Floppy Alignment  
Date: August 3, 1984

---

Here is the copy of Don Logan memo on Reading the Alternate Sector Map, Performing the Radial Head Alignment Test and the Winchester and Floppy Caches. If you have any other questions on these topics get back to me. Please distribute this information to the domestic and international FSC's.

Sincerely

A handwritten signature in cursive script, appearing to read "Haw", written over a horizontal line.

Harvey Worthington

cc. Glen Hoffherr  
Mick Davis Eurotac

hw/hw

When a sector is written to the disk, the controller checks the cache identifiers to determine if that sector is in the cache. If it is, then the entire cache is voided. The cache is also voided during power-up and any time the controller is reset.

There are eight Winchester caches, each with enough memory for 16, 256-byte sectors. These caches are divided differently, depending upon the system configuration. All eight caches are assigned to a single drive in the -10 model, four caches are assigned to each drive for the -20 and -30 models (the controller treats a 30-Meg drive as two drives), and each of the four drives in the -60 model is assigned two caches.

These caches are controlled in much the same manner as the floppy cache. If a sector is requested that is not in any of the caches, the least recently used cache is assigned to receive the data. When a sector is written to the disk, all caches assigned to that disk are checked to see if they contain the sector just written. Any cache containing that sector is voided.

A single write cache is shared by all the drives. This cache is the same size as the floppy read cache. During multi-sector writes, the controller will receive data into this cache until either an end-multi command is received or the cache is full. At this time, the controller writes all sectors in the cache onto the disk in a single pass. Separate caches also exist for the alternate sector map, read after write, verify, ECC correction, and format.

Maximum Absolute Sector Addresses:

|                      |       |                         |
|----------------------|-------|-------------------------|
| Floppy (2200 Format) | 1279  |                         |
| Floppy (PC Format)   | 1439  |                         |
| Winchester (10-Meg)  | 38911 |                         |
| Winchester (30-Meg)  | 65023 | (130,046 sectors/drive) |

Distribution

Jerry Sevigny  
Dave Barrett

John Deutsch  
Niel Aronson  
Gene Mantoni

Mike Riley  
Harvey Worthington *11/5 0125*

Loren

Albright



Performing the Radial Head Alignment Test: As with reading the alternate sector map, turn off power to the board, and flip switch number three to the off position. Attach the scope probes to the appropriate test points on the drive, and turn the power back on. Perform a read operation on any sector of your choosing that is on the track and surface you desire the head to remain over. For example, to perform an index-to-data test on track 01, head 00, read sector 35. To turn on head 01, read sector 51. For radial-track alignment, sector 515 is on track 16, head 00, and sector 531 is on track 16, head 01.

When you attempt to read a sector, the controller will step the heads to the requested track, enable the requested head, and then issue a read command to the NEC floppy controller chip. When the NEC chip has sensed the index hole twice without finding the desired sector, it will terminate the command and return control to the Z80A. The Z80A will then read the operation result bytes, and, without interpreting these bytes, will re-issue the read command to the NEC chip. This whole operation takes place in far less time than the head-unload time, and the selected head will therefore continuously output signals from the diskette.

Needless to say, this operation hangs up the controller. In order to step the head to a different track or enable a different head, it is necessary to first reset the controller and then issue a new read command. A program can easily be written to take the thinking out of this task. A menu would allow you to select the track and head without having to worry about the sector numbers. After pressing RESET, it would only be necessary to hit RUN then RETURN, and then select the desired track and head from the menu again.

When through aligning the drive, power down the board, and return switch three to the on position. DO NOT FORGET TO RETURN SWITCH THREE TO THE ON POSITION !!!

Winchester and Floppy Caches: There is a single floppy cache with enough memory to hold 16, 256-byte sectors (2200 format) or nine, 512-byte sectors (PC format). The first two bytes in the cache indicate the absolute sector address of the first sector in the cache, and the next two bytes indicate the absolute sector address of the last sector in the cache. If no sectors are in the cache, all four of these bytes are set to FFh to indicate that condition.

When a floppy read request is received, the controller will first check the cache identifier bytes to see if the requested sector is in the cache. If the sector is in the cache, the controller will send the data to the 2200 without going to the disk. If the sector is not in the cache, the controller will read the sector plus the next 15 contiguous sectors into the cache. (It will read the sector plus the next 17 contiguous sectors if the diskette is formatted PC-style). These sectors are read based on the assumption that the 2200 is probably going to request consecutively higher contiguous sectors.

To: Distribution  
From: Don Logan  
Date: April 27, 1984  
Subject: Status of 2275 Microcode

Everything appears to be running smoothly. Only one problem has been reported to me from the field, and that problem has been taken care of. The code to allow the radial head alignment test has been added and tested. I have spent four days beating on the -60 and -30 models with Dave Barrett's latest disk demoralizer. Only two errors occurred on the -60 model with over a half a million disk accesses, and similarly only two errors occurred on the -30 model with over three quarters of a million disk accesses. Dave has reported similar results on the -20 model. I have started the paperwork for the ECO, and if nothing new crops up we'll be releasing this code as soon as possible.

The rest of this memo concerns the boring details of some of the features of this code. If you don't care about the details, you can throw this memo away without reading any further.

Reading the Alternate Sector Map: With the board powered off, flip switch number three to the off position. Power up the board. Perform a DATA LOAD BA operation on sectors 0, 32, 64, and 96. These sectors contain the error maps for heads 00, 01, 02, and 03 respectively. The data should be interpreted as follows: The first two hex digits indicate the number of sectors in the map. After these first two digits, data is organized into eight-digit segments. Digits one and two indicate the low-order byte of the cylinder with the bad sector, digits three and four indicate the high-order byte, digits five and six indicate which sector is bad, and digits seven and eight indicate which sector on track zero has been assigned as the alternate sector.

For example, assume that sector 64 is read and the data stored there reads 03500007015000080250000603. This data indicates that on head 02, three sectors have been mapped out. All three sectors are on cylinder 0050h (cylinder 80). These sectors are 07, 08, and 06, and they have been assigned alternate sectors 01, 02, and 03 respectively on cylinder 00, head 02.

The alternate sectors may also be read if desired. When through reading these maps, turn off power to the board, and return switch three to the on position. DO NOT FORGET TO FLIP SWITCH NUMBER THREE BACK TO THE ON POSITION, as disastrous results may ensue. This switch prevents the controller from adding the cylinder zero offset to the absolute sector address. If you write data to the disk with the switch on, you will not be writing to the sector you are intending to write to, and you might end up wiping out somebody's payroll records.

To: Distribution  
From: Don Logan  
Date: April 18, 1984  
Subject: Present Status of the 2275 Microcode

I have created enough room on the PROM to include the following features:

1. PC diskette write capability.
2. A status message that gives PROM rev #, indicates whether the system is a -10, -20, -30, or -60, and indicates the highest addressable sector on both the fixed and removeable drives.
3. Read alternate sector map capability. This feature uses a switch to indicate to the controller whether or not to add the cylinder zero offset. Although a switch is not the most desirable way to perform this function, it takes the least amount of memory. At any rate, this is not the type of function that a user needs to have access to.
4. A user program will now abort when a parity error occurs. I have noticed that the error message returned by the system depends upon the type of operation being performed at the time the error occurs. The error message is not that important, however, since the flashing lights on the drive indicate the nature of the problem. If no operation is in progress when the error occurs, the lights are flashed and no error message is sent.

In addition, the problem of the push with NOPs was fixed. A memory contention existed due to the fact that the Winchester hardware was not shut off before firmware attempted to find an alternate sector. Now the bad news:

1. The super verify function is dead. We're far too short of room to add it.
2. The super format function will not fit. Although it is a simple matter to add a \$GIO command that will not erase the alternate sector map, other things are not as simple as they first appeared. When reformatting a disk, it is possible that a sector mapped out in a previous format operation will not show up with an error in the current format operation. The header bytes of this sector and its neighbors will not be screwed up, and these previously bad sectors will no longer be mapped out. Unfortunately, these sectors will still be listed in the alternate sector map. It is not acceptable to have two sectors with the same address on a single drive. Code would therefore have to be added to read

the alternate sector map prior to reformatting the disk. Before each track is formatted, the cylinder and head would have to be checked against the alternate sector map to ensure that all sectors previously mapped out remain mapped out. Needless to say, this would take more bytes of code than we have available.

3. Bad news for radial head alignment. Before the controller can step the heads on the floppy, it has to figure out which track to step out to based on the absolute sector address. In order to know how many tracks to step out, the controller has to know whether it is dealing with a PC diskette or a 2200 diskette. It figures out which diskette it has by reading the first ID field it comes to on the track the heads are currently over. If the drive contains a blank diskette, the controller gets confused and refuses to go anywhere. We would have to add a separate subroutine and another \$GIO command in order to step the heads with a blank diskette in the drive. At this time, the only way to step the heads out to a given track is to use a formatted diskette.

I have burned a new set of PROMs with these latest updates. Anybody interested in a new set of PROMs should give me a call. I have been testing the 30 Meg drives with the new PROMs and Dave Barrett's disk exerciser and have encountered no problems. The PROMs that went out for Beta site testing have some 30 Meg flakes that are not present in the latest PROM. Since the problem of the push with NOPs was not fixed in the last release, I would suggest that any more PROMs released for Beta site testing should be from this latest batch.

#### Distribution

Jerry Sevigny  
Dave Barrett

John Deutsch  
Neil Aronson  
Gene Mantoni

Mike Riley  
Harvey Worthington *M/S 0125*

Loren Albright (a.k.a. "The Boss")

| QTY.        | REF. DES. | WANG PART NO. | VALUE/TYPE | DESCRIPTION                                   | DRAWING NO. | QTY. | ORIGIN |
|-------------|-----------|---------------|------------|---|-------------|------|--------|
| L44         |           |               |            |   |             |      |        |
| L7          | 376-0574- | 74LS163A      |            | IC BITIARY SYNCHRONOUS CLEAR 4-BIT COUNTERS   |             | 1    | ORIGIN |
| L120A       | 376-8006- | DEL LINE      |            | DIGITAL IC DELAY LINE ONE TAP 10NS/TAP        |             | 1    | ORIGIN |
| L49         | 376-9003- | SKT 24        |            | IC SOCKET 24 PIN DIL PC MOUNT                 |             | 1    | ORIGIN |
| @17 - @18   | 376-9008- | SKT 16        |            | IC SOCKET 16 PIN ANTI-WICKING SPACER          |             | 2    | ORIGIN |
| L98         | 376-9011- | SKT 40        |            | SOCKET 40 PIN DIL PC MOUNT                    |             | 1    | ORIGIN |
| L100        | 376-9015- | SKT 28        |            | IC SOCKET 28 PIN DIL MOUNT                    |             | 3    | ORIGIN |
| L124 - L125 |           |               |            |   |             |      |        |
| L74         | 376-9020- | SKT 20        |            | IC SOCKET 20 PIN DIL PC MOUNT                 |             | 4    | ORIGIN |
| L89         |           |               |            |   |             |      |        |
| L96         |           |               |            |   |             |      |        |
| L110        |           |               |            |   |             |      |        |
| L99         | 377-0411- | 9517A-4       |            | IC 9517A-4 MULTIMODE DMA CONTROLLER           | ECO 39901   | 1    | ORIGIN |
| L53         | 377-0426- | 765A          |            | IC UPD765AC FLOPPY DSK CONT 40 PIN            | ECO 39901   | 1    | ORIGIN |
| L9 - L17    | 377-0466- | 4164          |            | IC 64KX1 DRAM 200NS REF REQUIRE 2MS/128 ROW   |             | 9    | ORIGIN |
| D1 - D3     | 380-1012- | 1N914A        |            | DIO SIG 75V 250MA 4NS DO-35                   |             | 3    | ORIGIN |
| @1 - @2     | 449-0597- | BUTTON        |            | BUTTON PC GUIDES                              |             | 2    | ORIGIN |
| @32         | 458-1278- | SUPPORT       |            | SUPPORT, CONNECTOR                            | ECO 28389D  | 1    | ORIGIN |
| @29         | 458-3310- | GROUND        |            | GROUND, STATIC                                | ECO 28939D  | 1    | ORIGIN |
| @27 - @28   | 462-0426- | STH11004      |            | SPCR THRD 10-32 .25L .25HX ALUM               | ECO 28389D  | 2    | ORIGIN |
| @24 - @25   | 462-0453- | SPACER        |            | SPACER (.81)                                  | ECO 28389D  | 2    | ORIGIN |
| @21         | 510-8396- | PCB           |            |   |             | 1    | ORIGIN |
| @4 - @5     | 650-2128- | SCR30406      |            | SCR 4-40 3/8L PAN SLT NYLON                   | ECO 28389D  | 2    | ORIGIN |
| @6          | 650-4120- | SCR20806      |            | SCR 8-32 3/8L PAN PHL SEMS SST                | ECO 28389D  | 2    | ORIGIN |
| @9          | 652-0029- | NUT008        |            | NUT 8-32 KEPS STL .34HEX .11THK .38WSHR OD ZN | ECO 28389D  | 2    | ORIGIN |
| @13         | 652-2001- | NUT           |            | NYLON NUT                                     |             | 2    | ORIGIN |
| @19 - @20   | 653-4000- | FLT208        |            | WSHR FLAT 8 .174 .375 .016THK SST             | ECO 28389D  | 2    | ORIGIN |
| @14         |           |               |            |   |             |      |        |
| @16         |           |               |            |   |             |      |        |
| @30 - @31   | 653-4004- | FLT308        |            | WSHR FLAT 8 .187 .375 .032THK NYLON           | ECO 28389D  | 2    | ORIGIN |

|          |   |   |                |
|----------|---|---|----------------|
|          |   | WANG LABORATORIES, INC.<br>LOWELL, MA, U.S.A. |                |
| MATERIAL | MODEL NO  | BY  | DATE           |
|          | SEE ENGRG SPECIFICATIONS  | DWN   | E ENGR         |
| FINISH   | TOL EX AS NOTED<br>XR ± .010 FRAC ± 1/64<br>RLX ± .003 ANG ± 1°30' FINISH V | CHK   | M ENGR         |
|          | SCALE   | TITLE   |                |
|          | SMT 2 OF 3  | C.NTR   |                |
|          |   | WANG PART NUMBER                              | DATE           |
|          |   | 210-8396 C                                    | 8396           |
|          |   | SIZE  | DRAWING NUMBER |
|          |   |   | 8396           |
|          |   |   | REV            |
|          |   |   | 6              |

WANG

ECO

ECO NO. 45575

SHEET 1 OF 6

|            |                           |             |                                |      |          |
|------------|---------------------------|-------------|--------------------------------|------|----------|
| ORIGINATOR | Gilles Carrier/Royer Kirk | M/S         | 01439U/DL489U EXT. 74478/77624 | DATE | 07/22/87 |
| WRITTEN BY | Valerie Donahoe           | M/S         | 012-188 EXT. 74313             | DATE | 08/17/87 |
| PART NO.   | 209-8396/210-8396-A       | DESCRIPTION | 2275 MPA/C                     |      |          |
| DWG NO.    | 8396                      | PEP #       |                                |      |          |
| MODEL NO.  | 2275                      |             |                                |      |          |
| CLASS      | I II III                  |             |                                |      |          |

**DESCRIPTION OF CHANGE**

NOTE 1: Engineering has decided that the artwork will not be modified at this time, it is not cost justifiable.

Change schematic, sample board and parts list 210-8396-A per attached prints and as follows:

On circuit side:

Cut etch leading to L58 pin 1.

On component side:

Tie L68 pin 12 to L40 pin 15.

Tie L68 pin 13 to L57 pin 5.

Tie L68 pin 11 to L58 pin 1.

Remove wire between L116 pin 5 and L126 pin 13.

Tie L126 pin 13 and L126 pin 12.

Change sample board and parts list as follows:

|      |             |      |             |
|------|-------------|------|-------------|
| L100 | 379-2000-R4 | TO   | 379-2000-R5 |
|      |             | FROM |             |

continued on next page

**REASON/SYMPOTM FOR CHANGE**

- To stop Buss contention while reading drive status.
- Eliminate potential Ready/Busy timing problem through Multiplexer.
- Allow format of diskettes containing an 'all ones' test data pattern.
- Reduce the time required to format a diskette

**DOCUMENTS**

|                  | FROM | TO |
|------------------|------|----|
| HISTORY SHT. 510 |      |    |
| HISTORY SHT. 210 | 8    | 9  |
| ARTWORK          |      |    |
| E-REV.           | 5    | 6  |
| ASSY. DWG.       |      |    |
| DRILL DWG.       |      |    |
| SCHEM DWG.       |      |    |
| MECH. DWG.       |      |    |
| CBL DWG.         |      |    |
| S.P.I.           |      |    |
| SPECIFICATION    |      |    |

| CONFORMING AREA | CF | REMG. | DIST. | FINAL ASSY AREA | SUB ASSY AREA | NEXT ORDER | INFO ONLY |
|-----------------|----|-------|-------|-----------------|---------------|------------|-----------|
|                 | X  | X     | X     | X               | X             | X          |           |

CONFORMANCE DATE 9-15-87

**APPROVALS**

|                 |                    |      |  |
|-----------------|--------------------|------|--|
| ECO CHAIRPERSON | <i>[Signature]</i> | DATE |  |
| DESIGNER        | <i>[Signature]</i> |      |  |
| CUST. ENGRG.    | <i>[Signature]</i> |      |  |
| MFG.            | <i>[Signature]</i> |      |  |
| MTO             |                    |      |  |
| PP&M            |                    |      |  |
| F.C.C.          | <i>[Signature]</i> |      |  |
| PROD. SAFETY    | <i>[Signature]</i> |      |  |
| SECURE SYS.     |                    |      |  |
| ORIGINATOR      |                    |      |  |
| OTHER           |                    |      |  |



**ENGINEERING CHANGE ORDER  
CONTINUATION SHEET**

|              |         |         |
|--------------|---------|---------|
| DOCUMENT NO. | OLD REV | NEW REV |
| ECO NO.      | SHT     | OF      |
| 45575        | 2       | 6       |

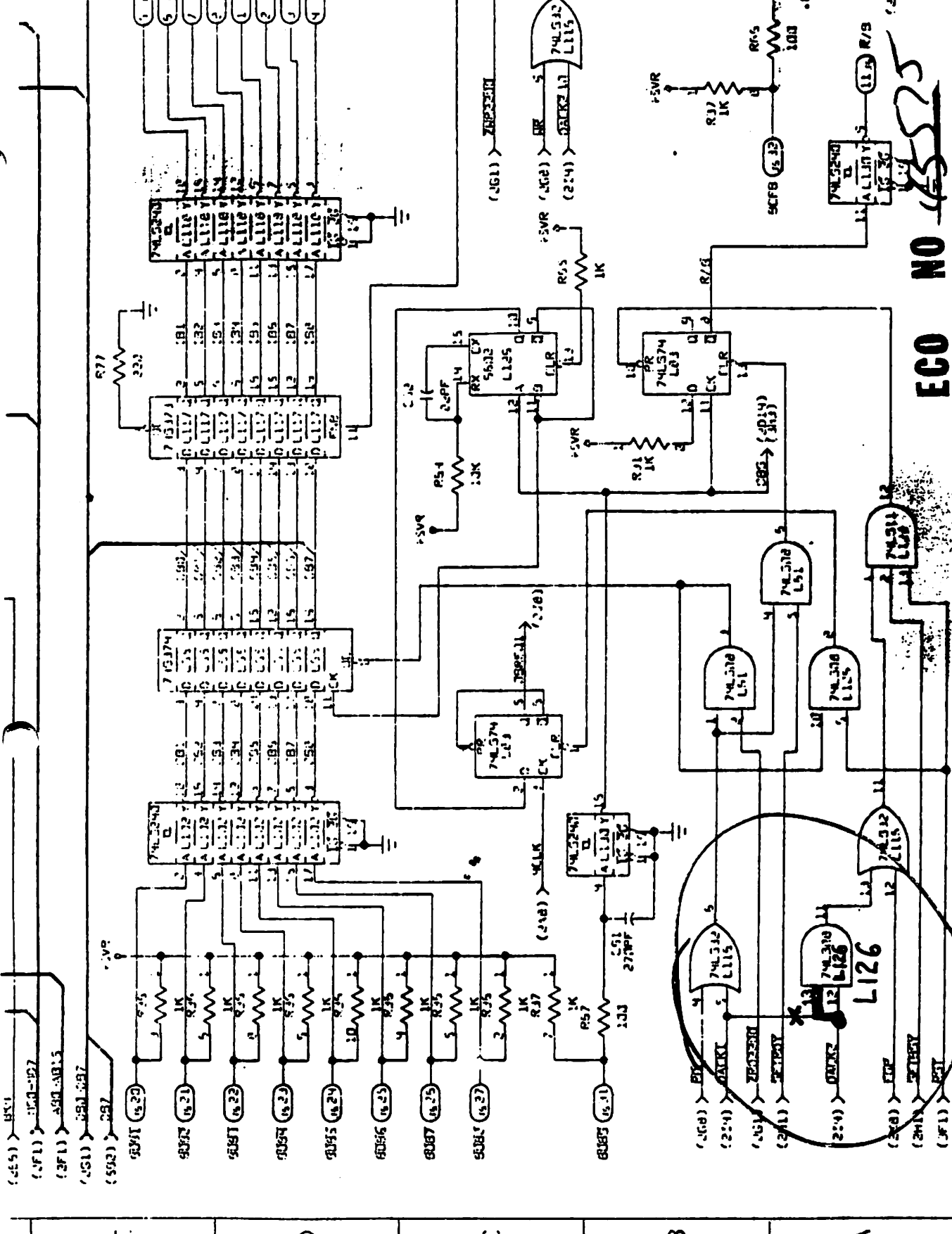
DOCUMENT TITLE: THIS ECO SHT, WHEN ATTACHED TO DOCUMENT OF PREVIOUS REV CONSTITUTES THE LATEST DOC.

**DESCRIPTION OF CHANGE:**

Change BOM 210-8396-A as follows:

| WLI#                | DESCRIPTION            | UM | COMP<br>TYPE | QTY<br>TYPE | QTY<br>TYPE |
|---------------------|------------------------|----|--------------|-------------|-------------|
| DELETE: 379-2000-R4 | 2275 DISK CONT PROM #2 | EA | 5 P          | 1           | 1           |
| ADD: 379-2000-R5    | 2275 DISK CONT PROM #2 | EA | 5 P          | 1           | 1           |

Delete the Product Structures and Part Numbers from the Data Base for the following prom:  
379-2000-R4



8396

ECO NO 65525

SHT 2 OF 6

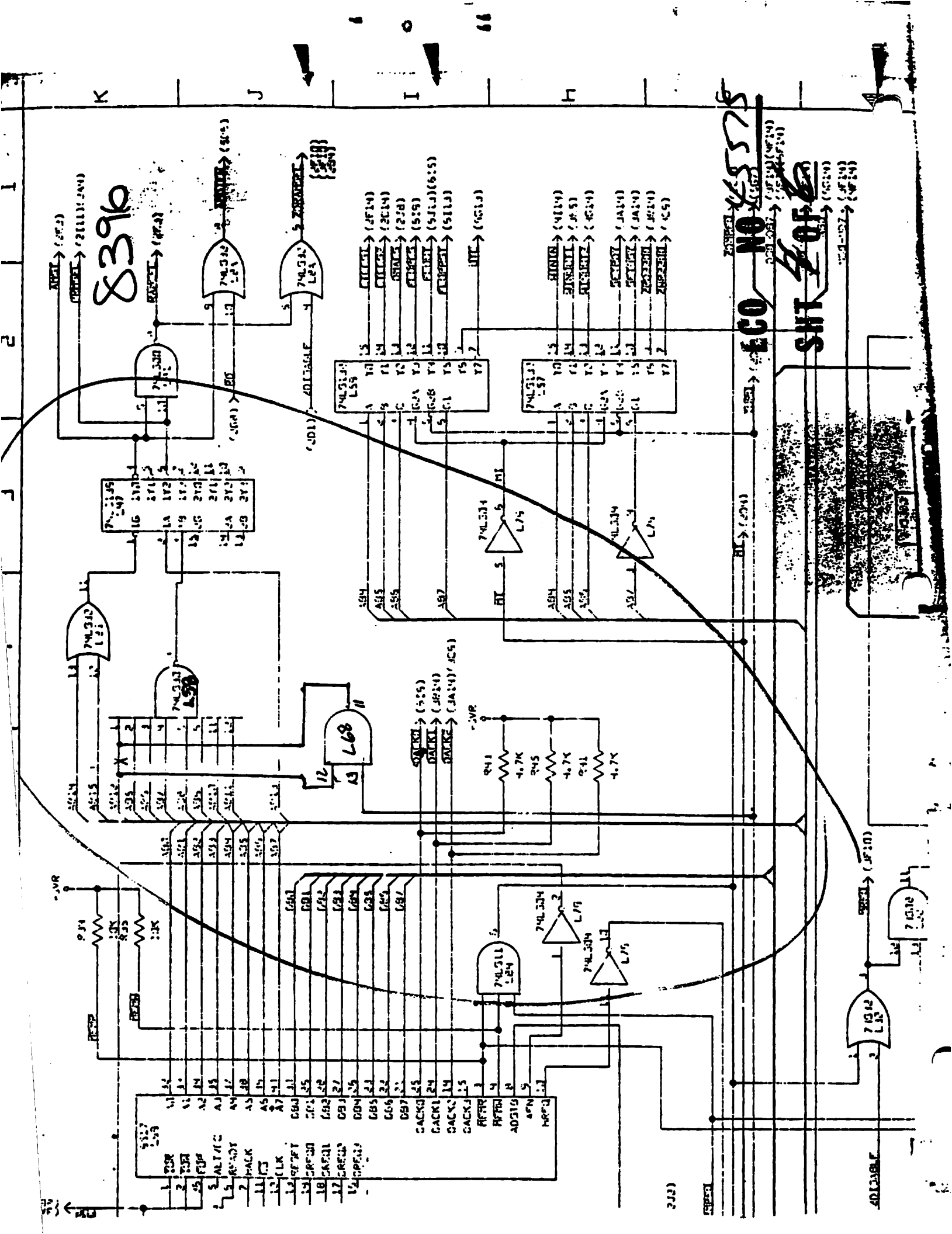
a

8.5"

11"

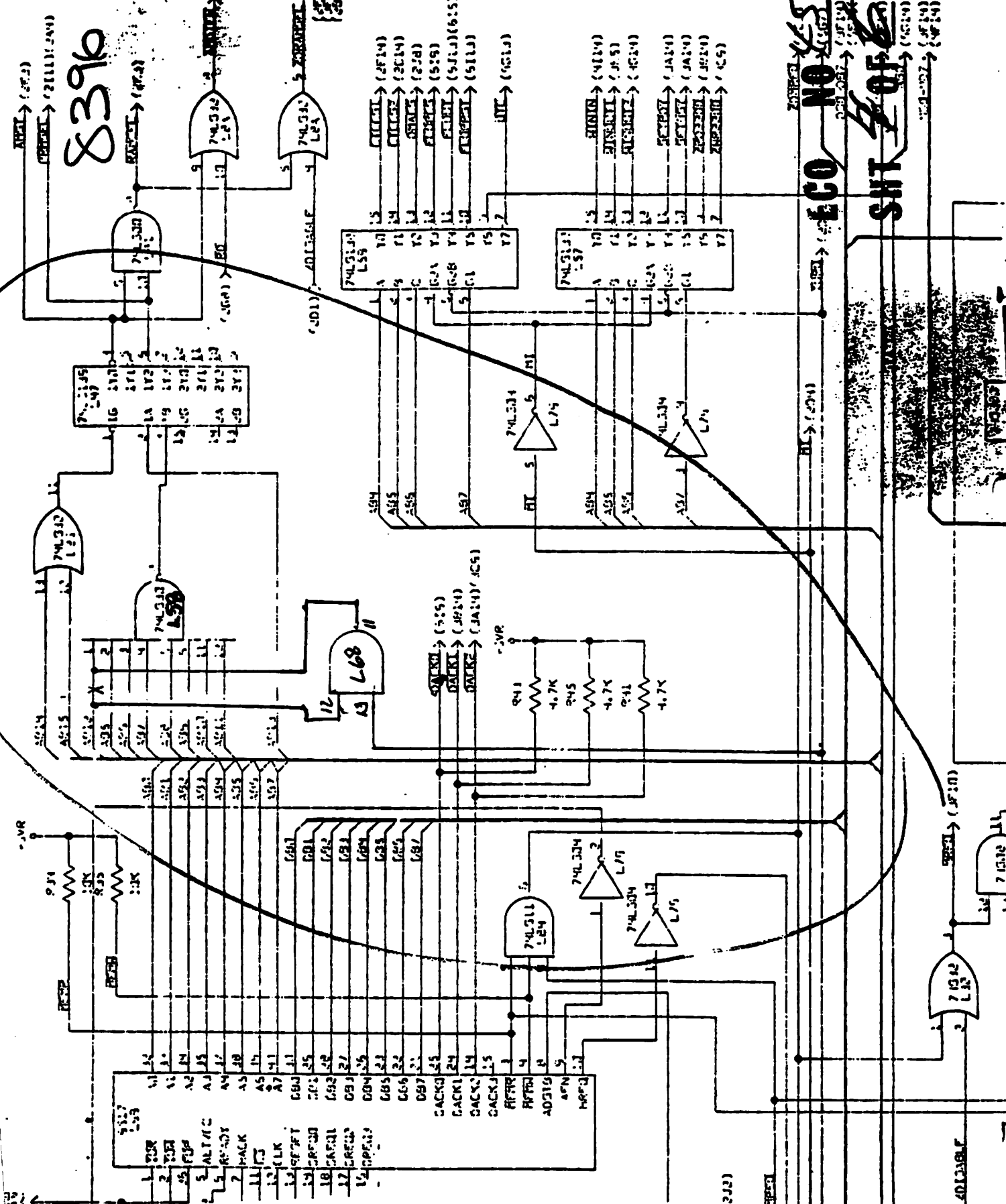
17"





8396

NO 4555  
SMT 2016



322

AD12345

**WANG**

# ENGINEERING CHANGE ORDER CUSTOMER ENGINEERING IMPACT SHEET

ECO NO. 45575  
SHEET      OF     

|                                  |                                     |
|----------------------------------|-------------------------------------|
| ALL UNITS                        | <input type="checkbox"/>            |
| PROB ONLY                        | <input checked="" type="checkbox"/> |
| INFO                             | <input type="checkbox"/>            |
| FCO REQUIRED                     | <input type="checkbox"/>            |
| IMMED                            | <input type="checkbox"/>            |
|                                  | NEXT CALL <input type="checkbox"/>  |
| IS A MUB REQUIRED FOR FSC REWORK | <input checked="" type="checkbox"/> |

**IMPACT COMMENTS**

*Normal Repair Cycle*

*Surge*

|                | DOMESTIC | INTER-NATIONAL |
|----------------|----------|----------------|
| EST. UNIT POP  | 10308    | 4123           |
| EST. SPARE POP | 411      | 164            |
| TOTAL          | 10719    | 4287           |

| EST. COST IMPACT       | APPROVALS                      | DATE    |
|------------------------|--------------------------------|---------|
| MATERIAL \$ 36,012.10  | TECH OPS                       |         |
| LABOR \$ 255,946.00    | LOGISTICS <i>Di. Murphy</i>    | 8/10/87 |
| TOTAL \$ 291,958.00    | FSC SUPPORT <i>to Williams</i> | 9/9     |
| IMPLEMENTATION PERIOD  | FINAL <i>Williams</i>          | 9/9/87  |
| ANNUAL COST \$ 1627.00 | OTHER                          |         |

**GENERAL COMMENTS** *TSB for file.*



# ENGINEERING CHANGE ORDER MANUFACTURING IMPACT SHEET

ECO NO. 45575  
SHEET \_\_\_\_\_ OF \_\_\_\_\_

|   |                 |                    |             |
|---|-----------------|--------------------|-------------|
| PART NO./ASSY NO.                             |                 | <b>DISPOSITION</b> |             |
| <b>MATERIAL DISPOSITION</b>                   | <b>QUANTITY</b> | <b>DISP</b>        | <b>COST</b> |
| PARTS ON HAND                                 |                 |                    |             |
| PARTS ON ORDER                                |                 |                    |             |
| ASSEMBLIES IN PROCESS                         |                 |                    |             |
| FINISHED SUB ASSEMBLIES                       |                 |                    |             |
| ASSEMBLIES IN UNITS                           |                 |                    |             |
| PREPARATION, IMPLEMENTATION COSTS             |                 |                    |             |
| <b>COST OF INCORPORATION</b>                  |                 |                    |             |
| PRODUCT COST CHANGE PER UNIT                  |                 |                    |             |
| PRODUCTION QUANTITY FROM MPP IN WKS _____ WKS |                 |                    |             |
| PRODUCT COST CHANGE (EXTENDED)                |                 |                    |             |
| TOTAL COST (OR COST SAVINGS) OF ECO           |                 |                    |             |
| <b>REMARKS</b>                                |                 |                    |             |
| Q1 Sch. 51 beds                               |                 |                    |             |
| WIP 132 (210's)                               |                 |                    |             |
| INV. LEVEL 16                                 |                 |                    |             |
| NSWO 17/87                                    |                 |                    |             |
| SMS EFFECTIVITY DATE <u>9-8-87</u>            |                 |                    |             |
| DOCUMENTATION ONLY <input type="checkbox"/>   |                 |                    |             |

### AFFECTED SITES

- |                                  |                               |                               |
|----------------------------------|-------------------------------|-------------------------------|
| TEWKS <input type="checkbox"/>   | BOS <input type="checkbox"/>  | HONG <input type="checkbox"/> |
| PKWD <input type="checkbox"/>    | IR <input type="checkbox"/>   | MEX <input type="checkbox"/>  |
| METH <input type="checkbox"/>    | PR <input type="checkbox"/>   |                               |
| LOW <input type="checkbox"/>     | SCOT <input type="checkbox"/> |                               |
| HLOK <input type="checkbox"/>    | AUST <input type="checkbox"/> |                               |
| PT BLVD <input type="checkbox"/> | TW <input type="checkbox"/>   |                               |

### APPROVALS

ECO ADMIN Wol/kslg

MFG ENG Sam 9/2/87

QUALITY

MATERIALS

PROD. CONTROL Dave Sows agh

FINANCE

RE-MFG

OTHER

**WANG**

**ECO**

**ECO NO. 42907**  
SHEET 1 OF 4

ORIGINATOR Gilles Carrier  
WRITTEN BY Valerie Goguen

M/S 014390  
M/S 012-18B

EXTRA 478  
EXTRA 313

DATE 2/12/86  
DATE 2/12/86

PART NO. 209-8396

DESCRIPTION  
5 1/4 Disk Contrl

**DOCUMENTS**

|                  | FROM | TO |
|------------------|------|----|
| HISTORY SHT. 510 |      |    |
| HISTORY SHT. 210 | 7    | 8  |
| ARTWORK          |      |    |
| E-REV.           | 4    | 5  |
| ASSY. DWG.       |      |    |
| DRILL DWG.       |      |    |
| SCHEM DWG.       |      |    |
| MECH. DWG.       |      |    |
| CBL DWG.         |      |    |
| S.P.I.           |      |    |
| SPECIFICATION    |      |    |

DWG NO. 8396

PEP #

CONFORMING AREA

MODEL NO. 2275 2200

REMG.

CE

CLASS (I) (II) (III)

CONFORMANCE DATE

DIST.

**DESCRIPTION OF CHANGE**

CONFORMING AREA

FINAL ASSY. AREA

NOTE 1: Engineering has decided that the artwork will not be modified at this time, it is not cost justifiable.

CONFORMING AREA

FINAL ASSY. AREA

Change schematic and sample board per attached print and as follows:

CONFORMING AREA

FINAL ASSY. AREA

Cut etch at L118 pin 19. (Zone 3D9) Comp Size  
The L118 pin 19 to (GND) (Zone 3D9) L118 Pin 10 (GND).  
L118 pins 1 & 19 will remain tied together.

CONFORMING AREA

FINAL ASSY. AREA

**REASON/SYMPOM FOR CHANGE**  
(512, 513, 2514)

CONFORMING AREA

FINAL ASSY. AREA

**COMPANY CONFIDENTIAL**

CONFORMING AREA

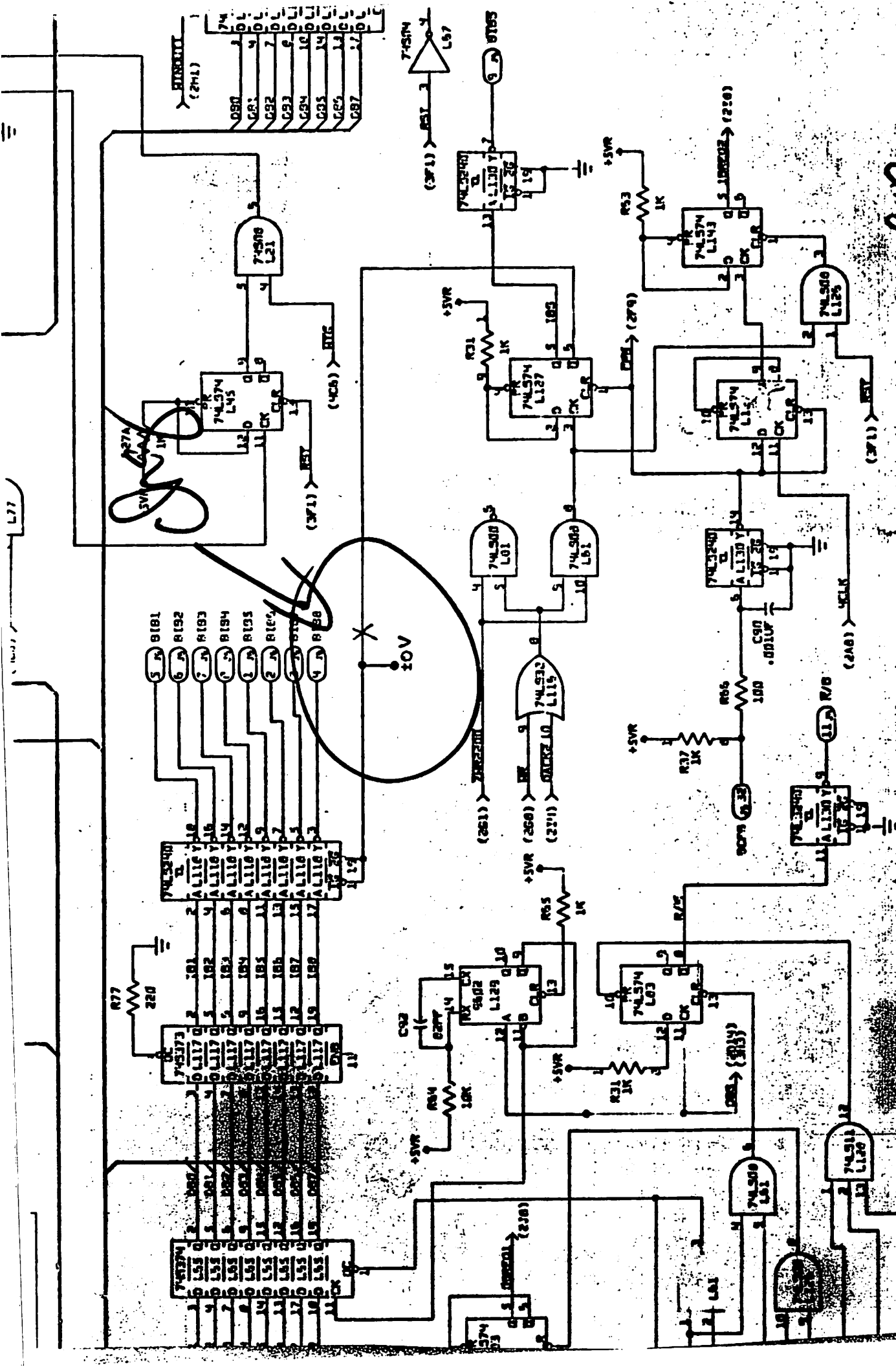
FINAL ASSY. AREA

To stop intermittent disk errors on 2275/ when may occur when used with the 210-7342 Dual Controllers.

CONFORMING AREA

FINAL ASSY. AREA

| APPROVALS                                    | DATE |
|--|------|
| ECO CHAIRPERSON                              |      |
| DES. ENGRG. <i>Attilio Carrier 12/17/86</i>  |      |
| CUST. ENGRG.                                 |      |
| MFG.   |      |
| MTO  |      |
| PP&M   |      |
| F.C.C. <i>Michael Busto 12/27/86</i>         |      |
| PROD. SAFETY <i>Attilio Carrier 12/27/86</i> |      |
| SECURE SYS.                                  |      |
| ORIGINATOR <i>Attilio Carrier 12/17/86</i>   |      |
| OTHER  |      |



8396 Sht 3 of 5  
 100 10 42907 5  
 SHT 4 OF 4

8396 Sht 3 of 5  
 Schematic Rev 15



# ECO

## ECO NO. 40541

SHEET 1 OF 5

|  |                                     |               |                  |
|--|-------------------------------------|---------------|------------------|
| ORIGINATOR<br>Sidney Robinson  | M/S<br>1482                         | EXT.<br>77386 | DATE<br>04/14/86 |
| WRITTEN BY<br>Jeannine Roy   | M/S<br>12188                        | EXT.<br>76930 | DATE<br>04/14/86 |
| PART NO.<br>210-8396-A   | DESCRIPTION<br>5 1/4 Disk Cntrl M/L |               |                  |
| DWG NO.<br>8396  |                                     |               |                  |
| MODEL NO.<br>2200 MPA/C  | PEP #<br>H0197A                     |               |                  |
| CLASS<br>I (II) III  |                                     |               |                  |
| <b>DESCRIPTION OF CHANGE</b>   |                                     |               |                  |
| Change 210-8396-A parts list and sample board as follows:<br><b>MAY 29 1986</b>  |                                     |               |                  |
| Change BOM 210-8396-A as follows:  |                                     |               |                  |
|  | FROM                                | TO            | PRINT ROOM       |
|  | L100                                | 379-2000-R3   | 379-2000-R4      |
| WL I#  | DESCRIPTION                         | UM            | COMP             |
| DELETE 379-2000-R3   | 2275 Disk Cont Prom #2              | EA            | 5P               |
| ADD 379-2000-R4  | 2275 Disk Cont Prom #2              | EA            | 5P               |
| Delete the Product Structure and Part Number from the Data Base for the following prom:<br>379-2000-R3   |                                     |               |                  |
| <b>REASON/SYMPOM FOR CHANGE</b>  |                                     |               |                  |
| This release of the 2275 microcode fixes all known bugs, improves response time for multiselector operations, and incorporates support for multiplexed environments. |                                     |               |                  |
| Note: ECO #36892 and #39995 must be installed as a prerequisite.   |                                     |               |                  |

### COMPANY CONFIDENTIAL

#### DOCUMENTS

|                  | REVISIONS |    |
|------------------|-----------|----|
|                  | FROM      | TO |
| HISTORY SHT. 510 |           |    |
| HISTORY SHT. 210 | 5         | 6  |
| ARTWORK          |           |    |
| E-REV.           |           |    |
| ASSY. DWG.       |           |    |
| DRILL DWG.       |           |    |
| SCHEM DWG.       |           |    |
| MECH. DWG.       |           |    |
| CBL DWG.         |           |    |
| SPI.             |           |    |
| SPECIFICATION    |           |    |

| CONFORMING AREA | FR | RMFG | DIST | FINAL ASSY AREA | ASSY AREA | ORDER | INFO ONLY |
|-----------------|----|------|------|-----------------|-----------|-------|-----------|
|                 |    |      |      |                 |           |       |           |

#### APPROVALS

|                 | DATE                           |
|-----------------|--------------------------------|
| ECO CHAIRPERSON | <i>J. Mulvaney</i> 5/28        |
| DES. ENGRG.     | <i>L. McManis</i> 4/24/86      |
| CUST. ENGRG.    | <i>Spurke</i> 5/28/86          |
| MFG             |                                |
| MTO             | <i>John Robinson</i> 5/28/86   |
| PP&M            |                                |
| F.C.C.          | <i>Michael Buehler</i> 4/25/86 |
| PROD. SAFETY    | <i>See Brumby</i> 5/2/86       |
| SECURE SYS.     |                                |
| ORIGINATOR      | <i>Sidney Robinson</i>         |
| OTHER           |                                |



# ENGINEERING CHANGE ORDER MANUFACTURING IMPACT SHEET

ECO NO. 40541  
SHEET 02 OF 05

|  |                 |             |             |
|--|-----------------|-------------|-------------|
| <b>PART NO./ASSY NO.</b>   |                 |             |             |
| <b>MATERIAL DISPOSITION</b>  | <b>QUANTITY</b> | <b>DISP</b> | <b>COST</b> |
| PARTS ON HAND  |                 |             |             |
| PARTS ON ORDER   |                 |             |             |
| ASSEMBLIES IN PROCESS  |                 |             |             |
| FINISHED SUB ASSEMBLIES  |                 |             |             |
| ASSEMBLIES IN UNITS  |                 |             |             |
| <b>PREPARATION IMPLEMENTATION COSTS</b>  |                 |             |             |
| <b>COST OF INCORPORATION</b>   |                 |             |             |
| PRODUCT COST CHANGE PER UNIT   |                 |             |             |
| PRODUCTION QUANTITY FROM MFP IN WKS _____ WKS  |                 |             |             |
| PRODUCT COST CHANGE (EXTENDED)   |                 |             |             |
| TOTAL COST (OR COST SAVINGS) OF ECO  |                 |             |             |
| <b>REMARKS</b>   |                 |             |             |
| <p><i>P.O. 24 in WIP      QY BUILD - 433</i></p> <p><i>Kit 100 in process      210 WIP - 425</i></p> <p><i>57 pcs distribution      NEXT KIT RELEASE - 6/5/86</i></p> <p><i>CE space shipped after 6/1/86</i></p> <p><i>will conform</i></p> |                 |             |             |
| SMS EFFECTIVITY DATE <u>6/4/86</u>   |                 |             |             |
| DOCUMENTATION ONLY <input type="checkbox"/>  |                 |             |             |

**DISPOSITION**

1. USE AS IS
2. REWORK
3. SCRAP/SALVAGE
4. NEXT ORDER
5. SEE REMARKS

**AFFECTED SITES**

|   |                               |                               |
|---|-------------------------------|-------------------------------|
| TEWKS <input checked="" type="checkbox"/>   | BOS <input type="checkbox"/>  | HONG <input type="checkbox"/> |
| PKWD <input type="checkbox"/>               | IR <input type="checkbox"/>   | MEX <input type="checkbox"/>  |
| METH <input type="checkbox"/>               | PR <input type="checkbox"/>   |                               |
| LOW <input type="checkbox"/>                | SCOT <input type="checkbox"/> |                               |
| HLOK <input type="checkbox"/>               | AUST <input type="checkbox"/> |                               |
| PT BLYD <input checked="" type="checkbox"/> | TW <input type="checkbox"/>   |                               |

**APPROVALS**

|               |                         |                |
|---------------|-------------------------|----------------|
| ECO ADMIN     | <i>Andrew Ross</i>      | <i>5/29/86</i> |
| MFG ENG       | <i>David McQueen</i>    | <i>5/28/86</i> |
| QUALITY       | <i>David Chapman</i>    | <i>5/28/86</i> |
| MATERIALS     | <i>CP Haley</i>         |                |
| PROD. CONTROL | <i>Paul Coffey</i>      |                |
| FINANCE       |                         |                |
| RE-MFG        | <i>D. Stewart (DES)</i> |                |
| OTHER         |                         |                |

# ENGINEERING CHANGE ORDER CUSTOMER ENGINEERING IMPACT SHEET

ECONOMY  
SHEET **3** OF **5**  
40541



|                                  |                                     |                                     |
|----------------------------------|-------------------------------------|-------------------------------------|
| ALL UNITS                        | <input type="checkbox"/>            |                                     |
| PROB ONLY                        | <input checked="" type="checkbox"/> |                                     |
| INFO                             | <input type="checkbox"/>            |                                     |
| FCO REQUIRED                     | <input checked="" type="checkbox"/> |                                     |
| IMMED <input type="checkbox"/>   | NEXT CALL                           | <input checked="" type="checkbox"/> |
| IS A MUB REQUIRED FOR FSC REWORK | <input checked="" type="checkbox"/> |                                     |

**IMPACT COMMENTS**

Rework during repair.  
FCO for field.  
Purge stock.

|                | DOMESTIC | INTER-NATIONAL |
|----------------|----------|----------------|
| EST. UNIT POP  | 2711     | 178            |
| EST. SPARE POP | 531      | 212            |
| TOTAL          | 3242     | 390            |

| EST. COST IMPACT      | APPROVALS  | TECH OPS           | LOGISTICS         | FSC SUPPORT            | FINAL              | OTHER | DATE    |
|-----------------------|------------|--------------------|-------------------|------------------------|--------------------|-------|---------|
| MATERIAL              | —          |                    |                   |                        |                    |       |         |
| LABOR                 | \$ 4514.00 | <i>R. Erickson</i> | <i>Paul Elmal</i> |                        |                    |       | 5/27    |
| TOTAL                 | \$ 4514.00 |                    |                   | <i>Elb's &amp; Co.</i> |                    |       | 5/27/86 |
| IMPLEMENTATION PERIOD | 5.4        |                    |                   |                        |                    |       |         |
| ANNUAL COST           | \$ 1340.00 |                    |                   |                        | <i>W. Lawrence</i> |       | 5/28    |

**GENERAL COMMENTS**

FCO 1111 A will be ~~replaced~~ replaced.



# SSD RELEASE MEMORANDUM

## SUMMARY DATA

Release Memo #: 212  
Release Coordinator: Sidney Robinson M/S 1489  
Date: April 7, 1986  
Product Line: 2200  
Probe Component: N/A  
Product Name: 2275 Disk Controller  
Version Number: 04  
Maximum Memory Requirement: N/A  
Release Type: Customer  
Package Number(s): 379-2000-R04  
PEP Number: N/A  
Number of Proms: (1)  
Copyright Notice Standards: (X) Meets requirements  
( ) Does not meet requirements

ECO NO 40541  
SHT 4 OF 5

## GENERAL DESCRIPTION

This release of the 2275 microcode fixes all known bugs, improves response time for multisector operations, and incorporates support for multiplexed environments.

## PREREQUISITE HARDWARE

A 2275 with ECO numbers 36892 and 39995 installed.

## PREREQUISITE SOFTWARE

None.

## TECHNICAL DOCUMENTATION

### 1 )MARKETING REQUIREMENTS SPECIFICATION:

MVP-10 Rev. 4 Prom for 2275 Disk Unit

### 2 )FUNCTIONAL SPECIFICATION:

MVP-08 2275 Disk Unit Firmware Release 4 Functional Spec.

### 3 )DESIGN SPECIFICATION:

MVP-09 2275 Disk Unit Firmware Release 4 Design Spec.

WHERE TO OBTAIN THIS RELEASE

Via corporate WISE network, 8th Floor Alliance System "SWLIB", Tower 1/11 Lab or Tower 11 Resource Room.

Software Please see Release Engineering for a 2275 Disk Controller Prom.

Release Memorandum Library: rmlib  
ID: 212

Technical Documentation Library: intl  
ID: 68 (MVP-08)  
ID: 69 (MVP-09)

Rev. 4 Prom for 2275 Disk Unit Marketing Requirements Spec. (MVP-10) is available in hard copy only and can be obtained from the MVP Binder located in the Resource Room.

ECO NO 44541  
SHT 5 OF 5

RESTRICTIONS

The prerequisite ECOs MUST be installed for proper operations to occur, see listed ECO #'s in Prerequisite Hardware section of this memo.

SPECIAL CONSIDERATIONS

None.

ENHANCEMENTS

- o Read and write speeds have been increased for multisector operations.
- o Support for multiplexed environments was added.

PROBLEMS CORRECTED

The Winchester format routine now fully decodes platter addresses to verify their correctness.

KNOWN ANOMALIES

None.

MEDIA

1 - 2275 Disk Controller Prom Diskette which includes the chip image file 92000R04.

This Prom (379-2000-R04) will be ECO'd unto the 2275 DPU board (#8396) at location L100.

# ECO

# CHANGE

36892

OF 6 SHEET

ORIGINATOR Sau Cai M/S 1439 EXT.77332 DATE 05/21/85

WRITTEN BY Elly Gilks M/S 1218B EXT.73230 DATE 05/21/85

| PART NO.  | DWG NO.     | DESCRIPTION        | REVISIONS                         |                                   |
|-----------|-------------|--------------------|-----------------------------------|-----------------------------------|
|           |             |                    | F                                 | T                                 |
| 510 -8396 |             | 5 1/4 DISK CONTROL |                                   |                                   |
| 8396      |             |                    |                                   |                                   |
| MODEL NO. | 2200MP/2275 | PEP # H0197A       |                                   |                                   |
| CLASS     | I           | TYPE               | <input type="checkbox"/> HARDWARE | <input type="checkbox"/> SOFTWARE |

### DESCRIPTION OF CHANGE

Change artwork, assembly drawing, fabrication drawing, schematic, parts list and sample board per attached prints and as follows:

- Tie J6 pin-12 to L60 pin-9.
- At L60 tie (330-3011) 1K ohm resistor 1/4W 5% between pin-14 +5VR to pin-9.
- Tie L60 pin-8 to L63 pin-17. (See schem., zone 3F8)
- Tie L60 pin-10 to L60 pin-13.

Change BOM 209-8396 as follows:

| WLI#     | DESCRIPTION         | UM | EA | EA | COMP | QTY    | TYPE |
|----------|---------------------|----|----|----|------|--------|------|
| 330-3011 | 1K OHM RES. 1/4W 5% | EA | EA | EA | I    | 21     | I    |
|          |                     |    |    |    | I    | To: 22 | I    |

Change schematic parts list as follows:

- Change from (21) (330-3011) 1K OHM RES. 1/4W 5% to (22) (330-3011) 1K OHM RES. 1/4W 5%.

NOTE TO EDD: CREATE A 510 HISTORY SHEET

### REASON/SYMPOTM FOR CHANGE

To correct the drive selection.

NOTE: This ECO must be done in conjunction with ECO 37694.

RECEIVED  
AUG 24 1985  
PRINT ROOM

16

### DOCUMENTS

| DOCUMENTS       | REVISIONS |
|-----------------|-----------|
| BOM             |           |
| ARTWORK         |           |
| E-REV           | 2         |
| SAMPLE BD       | 3         |
| ASSY. DWG.      | 3         |
| DRILL DWG.      |           |
| SCHEM. DWG.     |           |
| MECH. DWG.      |           |
| CBL ASSY. DWG.  |           |
| S.P.I.          |           |
| MECH ASSY. DWG. |           |
| COMPONENT SPEC  |           |

### APPROVALS

| APPROVALS                             | DATE    |
|---------------------------------------|---------|
| ECO MGR. <i>J. Gilks</i>              | 8/28    |
| DES. ENGRG. <i>Louis V. Bonaro</i>    | 5/22/85 |
| CUST. ENGRG. <i>Sau Cai</i>           | 8/28    |
| MFG. ENGRG. <i>Velody M. Quinetti</i> | 8/21/85 |
| ORIGINATOR <i>Sau Cai</i>             | 5/22    |
| <i>Prop. John F. ...</i>              |         |
| <i>F.C.C. Arthur B. Holden</i>        | 5/22/85 |



# ECO

# ECO NO. 391955

SHEET 1 OF 1

|  |                                      |                     |                  |
|--|--------------------------------------|---------------------|------------------|
| ORIGINATOR<br>Gary Cardone/Beth Fioessel | M/S<br>1439                          | EXT.<br>75916/76124 | DATE<br>02/24/86 |
| WRITTEN BY<br>Elly Gilks                 | M/S<br>1218B                         | EXT.<br>73230       | DATE<br>02/24/86 |
| PART NO.<br>209-8396                     | DESCRIPTION<br>WINCHESTER DISK CNTRL |                     |                  |
| DWG NO.<br>8396                          | PEP # H0197A                         |                     |                  |
| MODEL NO.<br>2275                        | PEP # H0197A                         |                     |                  |
| CLASS<br>I II III                        | PEP # H0197A                         |                     |                  |

### DESCRIPTION OF CHANGE

NOTE 1: Engineering has decided that the artwork will not be modified at this time, it is not cost justifiable.

Change schematic and sample per attached print and as follows:

- Cut etch at L116 pin 13. (see schem. zone A314 component side and see attached artwork sheet)
- Tie L126 pin 11 to L116 pin 13. (see schem. zone A314)
- Tie L126 pin 12 to L116 pin 10. (see schem. zone A314)
- Tie L126 pin 13 to L116 pin 5. (see schem. zone A314)

NOTE TO EDD: Change History sheet over to assembly drawing.

## REASON/SYMPOTM FOR CHANGE COMPANY CONFIDENTIAL

To correct potential time out problem.

80

### DOCUMENTS

|                  | FROM | TO |
|------------------|------|----|
| HISTORY SHT. 510 |      |    |
| HISTORY SHT. 210 | 4    | 5  |
| ARTWORK          |      |    |
| E-REV.           | 3    | 4  |
| ASSY. DWG.       |      |    |
| DRILL DWG.       |      |    |
| SCHEM DWG.       |      |    |
| MECH. DWG.       |      |    |
| CBL DWG.         |      |    |
| SPI.             |      |    |
| SPECIFICATION    |      |    |

| CONFORMING AREA          | CF  | REMG | DST | FINAL ASSY AREA | SUB ASSY AREA | ASSY AREA | NEXT ORDER | INFO ONLY |
|--------------------------|-----|------|-----|-----------------|---------------|-----------|------------|-----------|
|                          | XIX | XIX  |     | XIX             | XIX           | XIX       |            |           |
| CONFORMANCE DATE 4/21/86 |     |      |     |                 |               |           |            |           |

### APPROVALS

| ECO CHAIRPERSON                    | DATE    |
|------------------------------------|---------|
| <i>J. Fitch</i>                    | 4/9     |
| DES. ENGRG. <i>Ray C. Cardone</i>  | 5/24/86 |
| CUST. ENGRG. <i>Ray C. Cardone</i> | 4/19/86 |
| MFG. <i>Ray C. Cardone</i>         | 4/19/86 |
| MTO <i>John Walmsley</i>           | 4/19/86 |
| PP&M                               |         |
| F.C.C.                             |         |
| PROD. SAFETY <i>Geo Bruner</i>     | 3/13/86 |
| SECURE SYS.                        |         |
| ORIGINATOR                         |         |
| OTHER                              |         |



ECO NO. 4054

SHEET 1 OF 5

ORIGINATOR Sidney Robinson EXT. 77386 DATE 04/14/86

WRITTEN BY Jeannine Roy EXT. 76930 DATE 04/14/86

PART NO. 21U-8396-A

DWG NO. 8396

MODEL NO. 2200 MVPA/C

DESCRIPTION 5 1/4 Disk Cntrl M/L

PEP # PEP# H0197A

CLASS I (II) III

**DESCRIPTION OF CHANGE**

Change 210-8396-A parts list and sample board as follows:

Change BOM 210-8396-A as follows:

| WI. I#             | DESCRIPTION            | UM | COMP TYPE | QTY | QTY TYPE |
|--------------------|------------------------|----|-----------|-----|----------|
| DELETE 379-2000-R3 | 2275 Disk Cont Prom #2 | EA | 5P        | 1   | 1        |
| ADD 379-2000-R4    | 2275 Disk Cont Prom #2 | EA | 5P        | 1   | 1        |

Delete the Product Structure and Part Number from the Data Base for the following prom:  
379-2000-R3

**COMPANY CONFIDENTIAL**

**REASON/SYMPOTM FOR CHANGE**

This release of the 2275 microcode fixes all known bugs, improves response time for multiselector operations, and incorporates support for multiplexed environments.

Note: ECO #36892 and #39995 must be installed as a prerequisite.

**DOCUMENTS**

|                  | FROM | TO |
|------------------|------|----|
| HISTORY SHT. 510 |      |    |
| HISTORY SHT. 210 | 5    | 6  |
| ARTWORK          |      |    |
| E-REV.           |      |    |
| ASSY. DWG.       |      |    |
| DRILL DWG.       |      |    |
| SCHEM DWG.       |      |    |
| MECH. DWG.       |      |    |
| CBL DWG.         |      |    |
| S.P.I.           |      |    |
| SPECIFICATION    |      |    |

| CONFORMING AREA | CF | REMG | DIST | FINAL ASSY AREA | SUB ASSY AREA | NEXT ORDER | INFO ONLY |
|-----------------|----|------|------|-----------------|---------------|------------|-----------|
|                 |    |      |      |                 |               |            |           |

**APPROVALS**

| ECO CHAIRPERSON                   | DATE           |
|-----------------------------------|----------------|
| DES. ENGRG. <u>L.H. Conrad</u>    | <u>4/24/86</u> |
| CUST. ENGRG.                      |                |
| MFG.                              |                |
| MTO                               |                |
| PP&M                              |                |
| F.C.C.                            |                |
| PROD. SAFETY                      |                |
| SECURE SYS.                       |                |
| ORIGINATOR <u>Sidney Robinson</u> |                |
| OTHER                             |                |

# SSD RELEASE MEMORANDUM

## SUMMARY DATA

Release Memo #: 212  
Release Coordinator: Sidney Robinson M/S 1489  
Date: April 7, 1986  
Product Line: 2200  
Probe Component: N/A  
Product Name: 2275 Disk Controller  
Version Number: 04  
Maximum Memory Requirement: N/A  
Release Type: Customer  
Package Number(s): 379-2000-R04  
PEP Number: N/A  
Number of Proms: (1)  
Copyright Notice Standards: (X) Meets requirements  
( ) Does not meet requirements

ECO NO 40541  
ON CD  
SHT 4 OF 5

## GENERAL DESCRIPTION

This release of the 2275 microcode fixes all known bugs, improves response time for multisector operations, and incorporates support for multiplexed environments.

## PREREQUISITE HARDWARE

A 2275 with ECO numbers 36892 and 39995 installed.

## PREREQUISITE SOFTWARE

None.

## TECHNICAL DOCUMENTATION

### 1 )MARKETING REQUIREMENTS SPECIFICATION:

MVP-10 Rev. 4 Prom for 2275 Disk Unit

### 2 )FUNCTIONAL SPECIFICATION:

MVP-08 2275 Disk Unit Firmware Release 4 Functional Spec.

### 3 )DESIGN SPECIFICATION:

MVP-09 2275 Disk Unit Firmware Release 4 Design Spec.

WHERE TO OBTAIN THIS RELEASE

Via corporate WISE network, 8th Floor Alliance System "SWLIB", Tower I/II Lab or Tower II Resource Room.

Software Please see Release Engineering for a 2275 Disk Controller Prom.

Release Memorandum Library: rmlib  
ID: 212

Technical Documentation Library: intl  
ID: 68 (MVP-08)  
ID: 69 (MVP-09)

Rev. 4 Prom for 2275 Disk Unit Marketing Requirements Spec. (MVP-10) is available in hard copy only and can be obtained from the MVP Binder located in the Resource Room.

ECO NO 40541  
SHT 5 OF 5

RESTRICTIONS

The prerequisite ECOs MUST be installed for proper operations to occur, see listed ECO #'s in Prerequisite Hardware section of this memo.

SPECIAL CONSIDERATIONS

None.

ENHANCEMENTS

- o Read and write speeds have been increased for multisector operations.
- o Support for multiplexed environments was added.

PROBLEMS CORRECTED

The Winchester format routine now fully decodes platter addresses to verify their correctness.

KNOWN ANOMALIES

None.

MEDIA

1 - 2275 Disk Controller Prom Diskette which includes the chip image file 92000R04.

This Prom (379-2000-R04) will be ECO'd unto the 2275 DPU board (#8396) at location L100.

**WANG**

# FIELD CHANGE ORDER

|         |
|---------|
| FCO NO. |
| 1111    |

Equipment Affected 2275-10, 20, 30 Disc Peripheral

Class All Units FCO Kit # 728-0129 Page 1 of 5

Org. Code 3110 FCO Doc. # 729-1531 Approval Date:

Est. Install. Time 15 minutes Ref. ECO # 33512 AUG 30 1984

THIS FCO VOIDS FCO 1100

SEE MISCELLANEOUS FOR INFORMATION RELATED TO FCO 1100

1. REASON FOR CHANGE

This release of the 2275 Disk Processing Unit Firmware obsoletes the R1 EPROM and corrects the following:

- A. The 2200 operating system issues a D81 error message to the screen when a user attempts to save a modified version of a file over the original version and there is not enough disk space in the original version. Due to a bug in the operating system there is a failure to issue an end-multi-sector-write command to the 2275 disk controller. Subsequent commands to the 2275 are misinterpreted because the 2275's multi-sector write flags are still set. This version of the EPROM contains a mechanism to detect this condition and reset the multi-sector write flags when the condition occurs.
- B. At power-up or after reset firmware loses track of which cylinder the heads of the removeable drive are over. This makes a retry necessary the next time the removeable drive is accessed. This bug causes the manufacturing diagnostics to fail since a special GIO command sequence in the diagnostics disables retries.

2. DESCRIPTION OF CHANGE

The EPROM at L100 is changed from a 379-2000-R1 to a 379-2000-R2 on the 210-8396-A PCA.

3. DOCUMENTATION AFFECTED

N/A

4. PREREQUISITE

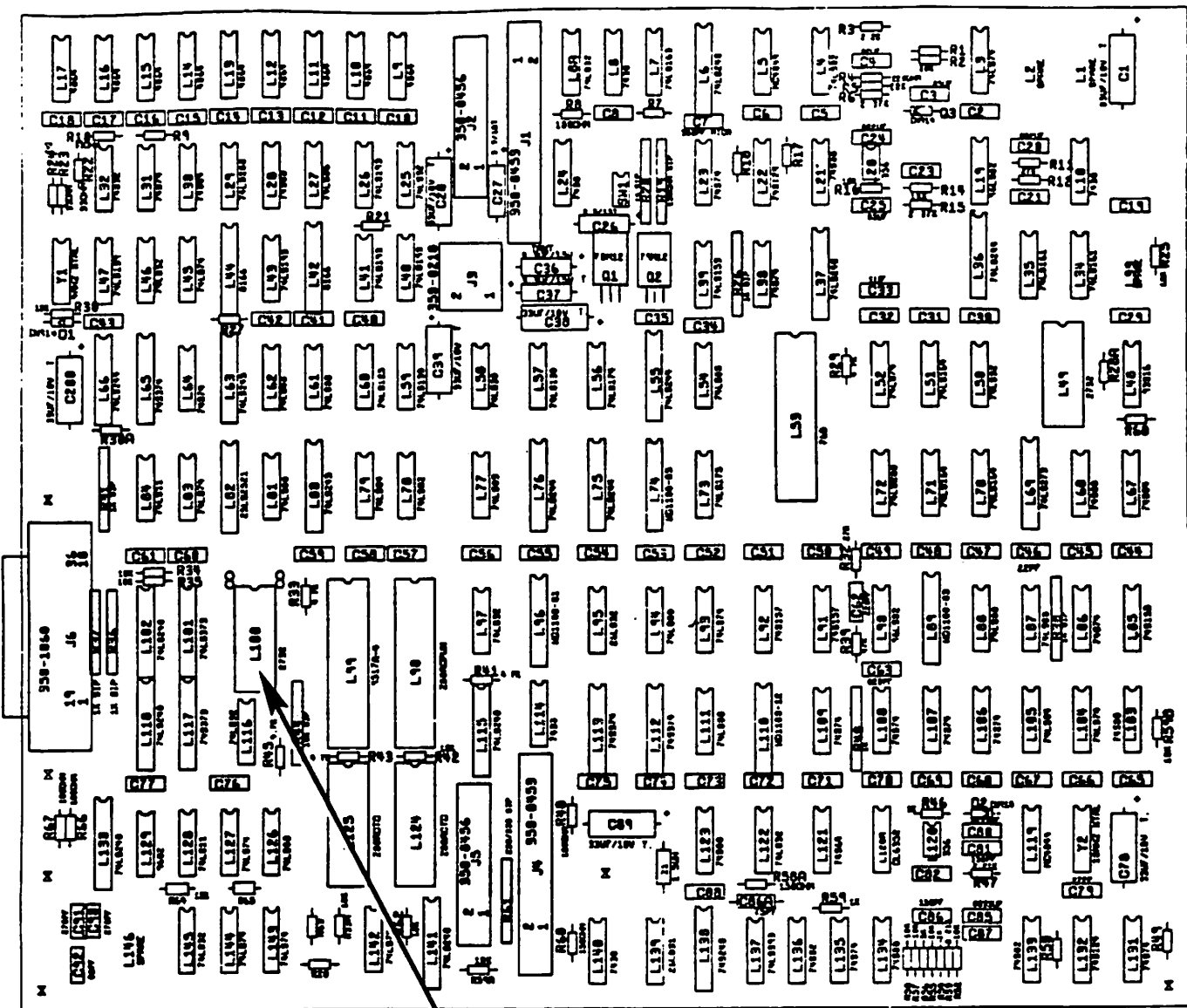
N/A

|                        |  |  |   |
|------------------------|--|--|---|
| Tech Ops<br><i>Hau</i> | Logistics<br>8-29-84<br><i>Phil Murphy</i> | Originator<br>8/24/84<br><i>Mary Keady</i> | FCO Coordinator<br><i>John Prodic</i> 8/29/84 |
|------------------------|--|--|---|



5. INSTALLATION PROCEDURE

- A. Power down unit.
- B. Take out and retain four screws at back of unit. Remove chassis from unit.
- C. Access EPROM at L100 on the 210-8396-A PCA thru the top of the unit between the fan and the floppy drive. Change the EPROM at L100 from a 379-2000-R1 to a 379-2000-R2 as shown in Figure 1.
- D. Reassemble unit by reversing the procedures in Step 5.B. above.
- E. Document installation of the FCO by completing a Call Report or Activity Report.



CHANGE EPROM AT L100  
TO 379-2000-R2

FIGURE 1 210-8396-A PCA

6. CHECK-OUT PROCEDURE

- A. Power up. Insure customer data is properly backed up.
- B. Run Magnetic Media Diagnostics in 2200 Diagnostic Package:

Software Package # 195-2956-0

| <u>Disk Type</u> | <u>Part Number</u> | <u>Revision</u> |
|------------------|--------------------|-----------------|
| 8" SSSD          | 702-0292           | 6436            |
| 5 1/4" DSDD      | 732-0049           | 6436            |

NOTE: If Software Package #195-2956-0 is unavailable, run 2200 Multi Disk Exerciser, #702-0146 (SSSD) or 732-0013 (DSDD) Revision 16B4. (This diagnostic does not recognize the 2275 model.)

7. FCO KIT PARTS LISTING

FCO Kit # 728-0129

| <u>Item</u> | <u>Qty.</u> | <u>Description</u> |
|-------------|-------------|--------------------|
| 729-1531    | 1           | FCO Document 1111  |
| 379-2000-R2 | 1           | EPROM              |

8. FCO KIT AVAILABILITY DATE

FCO Kit #728-0129 will be available September 10, 1984. To obtain it, place a routine order through the Logistics Order Processing System.

9. REMOVED PARTS DISPOSITION

Recycle removed EPROM through your FSC.

10. MISCELLANEOUS

FCO Kit #728-0118 (referenced in FCO 1100) has been replaced by FCO Kit #728-0129 (referenced in FCO 1111). The updated EPROM's contained in FCO Kit #728-0129 are designed to fix the problems cited in both FCO 1100 and 1111.

FCO 1100, Section 1, "Reason for Change," lists the following:

- A. To correct all known bugs in the system:
  - 1. System hangs if 210-8396-A PCA is powered up with no floppy diskette in the drive.

2. System hangs if a LIST DT command is issued when there is no media in the drive.
  3. Alternate sector mapping function does not work.
  4. Winchester hardware is not disabled when the Z80 attempts to access the alternate sector map, creating a memory contention.
  5. Parity error hangs the system without returning an error message.
  6. Cacheing problem causes invalid data to be returned to the 2200.
  7. System status message does not properly identify the system configuration.
- B. To provide the following enhancements:
1. Firmware now supports 30 Megabyte Quantum Winchester drive.
  2. PC diskettes can be read, written and formatted by the 2275.
  3. Winchester format is now a one pass operation that writes a DB6, B6D, 6DB pattern onto the disk to help locate marginal sectors. ECC is disabled during format, and only two retries are allowed for header errors. In addition to mapping out a bad sector, the sectors immediately preceding and following the bad sector are mapped out.
  4. A hook is provided so that C.E. can perform radial-track and index-to-data head alignment.
  5. A hook is provided to allow C.E. to read the alternate sector map.

**WANG****FIELD CHANGE ORDER**

FCO NO.

1100A

Equipment Affected 2275-10, 20, 30 Disc Peripheral

Class All Units FCO Kit # 728-0118 Page 1 of 4

Org. Code 3110 \* FCO Doc. # 729-1517A Approval Date: AUG 30 1984

Est. Install. Time 15 minutes Ref. ECO # 32608

\*THIS FCO VOIDS FCO 1100. REFER TO FCO 1111.

1. REASON FOR CHANGE

## A. To correct all known bugs in the system:

1. System hangs if 210-8396-A PCA is powered up with no floppy diskette in the drive.
2. System hangs if a LIST DT command is issued when there is no media in the drive.
3. Alternate sector mapping function does not work.
4. Winchester hardware is not disabled when the Z80 attempts to access the alternate sector map, creating a memory contention.
5. Parity error hangs the system without returning an error message.
6. Cacheing problem causes invalid data to be returned to the 2200.
7. System status message does not properly identify the system configuration.

## B. To provide the following enhancements:

1. Firmware now supports 30 Megabyte Quantum Winchester drive.
2. PC diskettes can be read, written and formatted by the 2275.
3. Winchester format is now a one pass operation that writes a DB6, B6D, 6DB pattern onto the disk to help locate marginal sectors. ECC is disabled during format, and only two retries are allowed for header errors. In addition to mapping out a bad sector, the sectors immediately preceding and following the bad sector are mapped out.

Tech Ops

*Hau*

Logistics

8-29-84

*Phil Murphy*

Originator 8/24/84

*Mary Keady*

FCO Coordinator

*John Presler 8/29/84*

4. A hook is provided so that C.E. can perform radial-track and index-to-data head alignment.

5. A hook is provided to allow C.E. to read the alternate sector map.

2. DESCRIPTION OF CHANGE

The PROM at L100 is changed from a 379-2000 to a 379-2000-R1 on the 210-8396-A PCA.

3. DOCUMENTATION AFFECTED

N/A

4. PREREQUISITE

N/A

5. INSTALLATION PROCEDURE

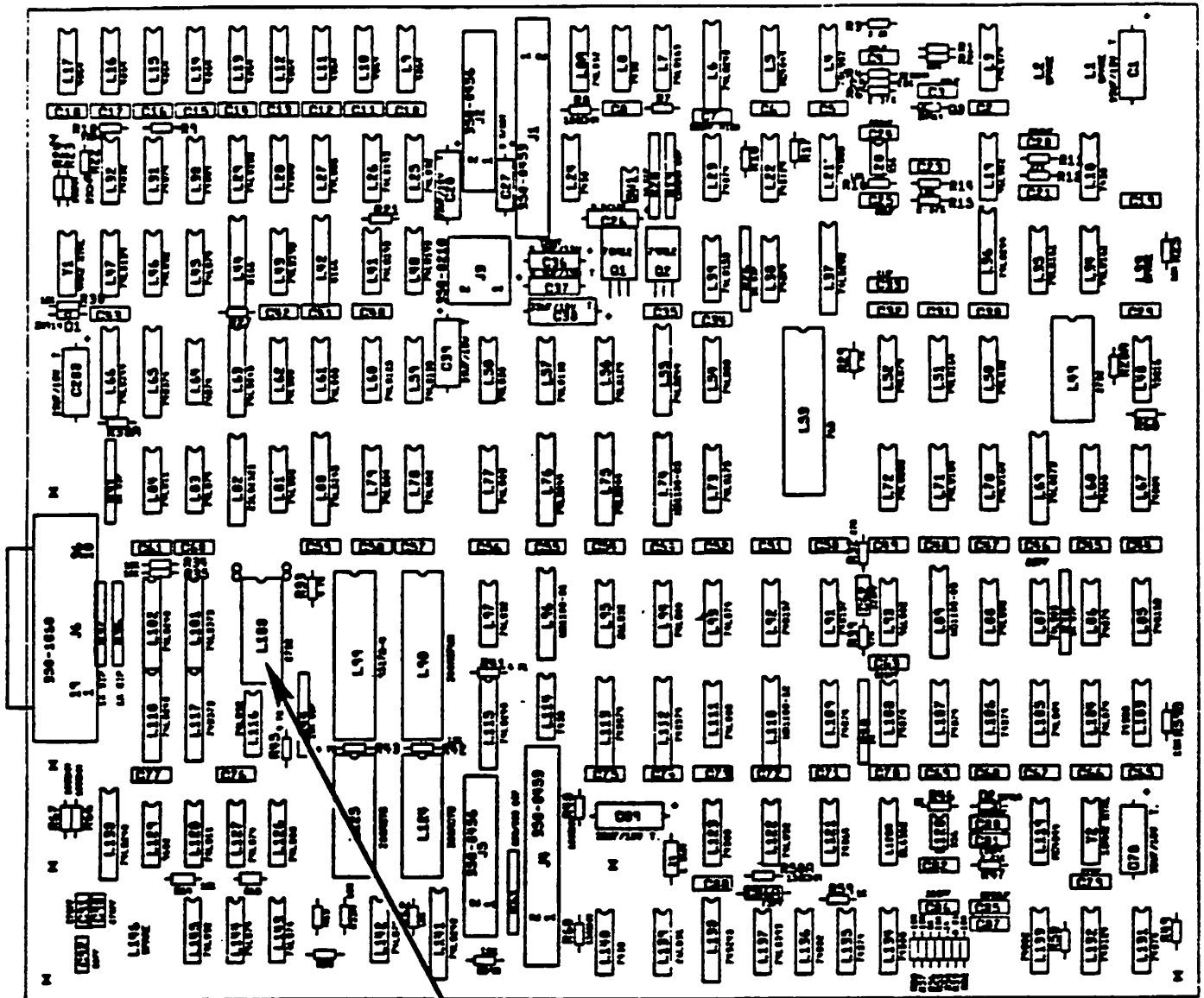
A. Power down unit.

B. Take out and retain four screws at back of unit. Remove chassis from unit.

C. Access PROM at L100 on the 210-8396-A PCA thru the top of the unit between the fan and the floppy drive. Change the PROM at L100 from a 379-2000 to a 379-2000-R1 as shown in Figure 1.

D. Reassemble the unit by reversing the procedures in Step 5.B. above.

E. Document installation of the FOD by completing a Call Report or Activity Report.



CHANGE FROM AT L100  
TO 378-2000-R1

FIGURE 1 210-8396-A PCA

6. CHECK-OUT PROCEDURE

- A. Power up. Insure customer data is properly backed up.
- B. Run Magnetic Media diagnostics in 2200 Diagnostic Package:

Software Package # 195-2956-0

| <u>Disk Type</u> | <u>Part Number</u> | <u>Revision</u> |
|------------------|--------------------|-----------------|
| 8" SSSD          | 702-0292           | 6436            |
| 5 1/4" DSDD      | 732-0049           | 6436            |

NOTE: If Software Package #195-2956-0 is unavailable, run 2200 Multi Disk Exerciser, #702-0146 (SSSD) or 732-0013 (DSDD) Revision 16B4. (This diagnostic does not recognize the 2275 model.)

7. FOO KIT PARTS LISTING

FOO Kit # 728-0118

| <u>Item</u> | <u>Qty.</u> | <u>Description</u> |
|-------------|-------------|--------------------|
| 729-1517    | 1           | FOO Document 1100  |
| 379-2000-R1 | 1           | FROM               |

\* 8. FOO KIT AVAILABILITY DATE

FOO Kit #728-0118 is no longer available effective September 10, 1984. It is replaced by FOO Kit #728-0129 (referenced in FOO 1111). FOO Kit #728-0129 will be available September 10, 1984. To obtain it, place a routine order through the Logistics Order Processing System.

9. REMOVED PARTS DISPOSITION

Recycle removed FROM through your FSC.

10. MISCELLANEOUS

N/A



**WANG**

# FIELD CHANGE ORDER

|         |
|---------|
| FCO NO. |
| 1100    |

Equipment Affected 2275-10, 20, 30 Disc Peripheral

Class All Units FCO Kit # 728-0118 Page 1 of 4

Org. Code 3110 FCO Doc. # 729-1517 Approval Date: **JUN 20 1984**

Est. Install. Time 15 minutes Ref. ECO # 32608

1. REASON FOR CHANGE

A. To correct all known bugs in the system:

1. System hangs if 210-8396-A PCA is powered up with no floppy diskette in the drive.
2. System hangs if a LIST DT command is issued when there is no media in the drive.
3. Alternate sector mapping function does not work.
4. Winchester hardware is not disabled when the Z80 attempts to access the alternate sector map, creating a memory contention.
5. Parity error hangs the system without returning an error message.
6. Cacheing problem causes invalid data to be returned to the 2200.
7. System status message does not properly identify the system configuration.

B. To provide the following enhancements:

1. Firmware now supports 30 Megabyte Quantum Winchester drive.
2. PC diskettes can be read, written and formatted by the 2275.
3. Winchester format is now a one pass operation that writes a DB6, B6D, 6DB pattern onto the disk to help locate marginal sectors. ECC is disabled during format, and only two retries are allowed for header errors. In addition to mapping out a bad sector, the sectors immediately preceding and following the bad sector are mapped out.
4. A hook is provided so that C.E. can perform radial-track and index-to-data head alignment.

|   |  |  |  |
|---|--|--|--|
| Tech Ops<br><i>Haw</i><br><u>06/19/84</u> | Logistics <u>6-20-84</u><br><i>Phil Murphy</i> | Originator <u>6/12/84</u><br><i>Mary Keady</i> | FCO Coordinator<br><i>John Rowley</i> <u>6/20/84</u> |
|---|--|--|--|

5. A hook is provided to allow C.E. to read the alternate sector map.

2. DESCRIPTION OF CHANGE

The PROM at L100 is changed from a 379-2000 to a 379-2000-R1 on the 210-8396-A PCA.

3. DOCUMENTATION AFFECTED

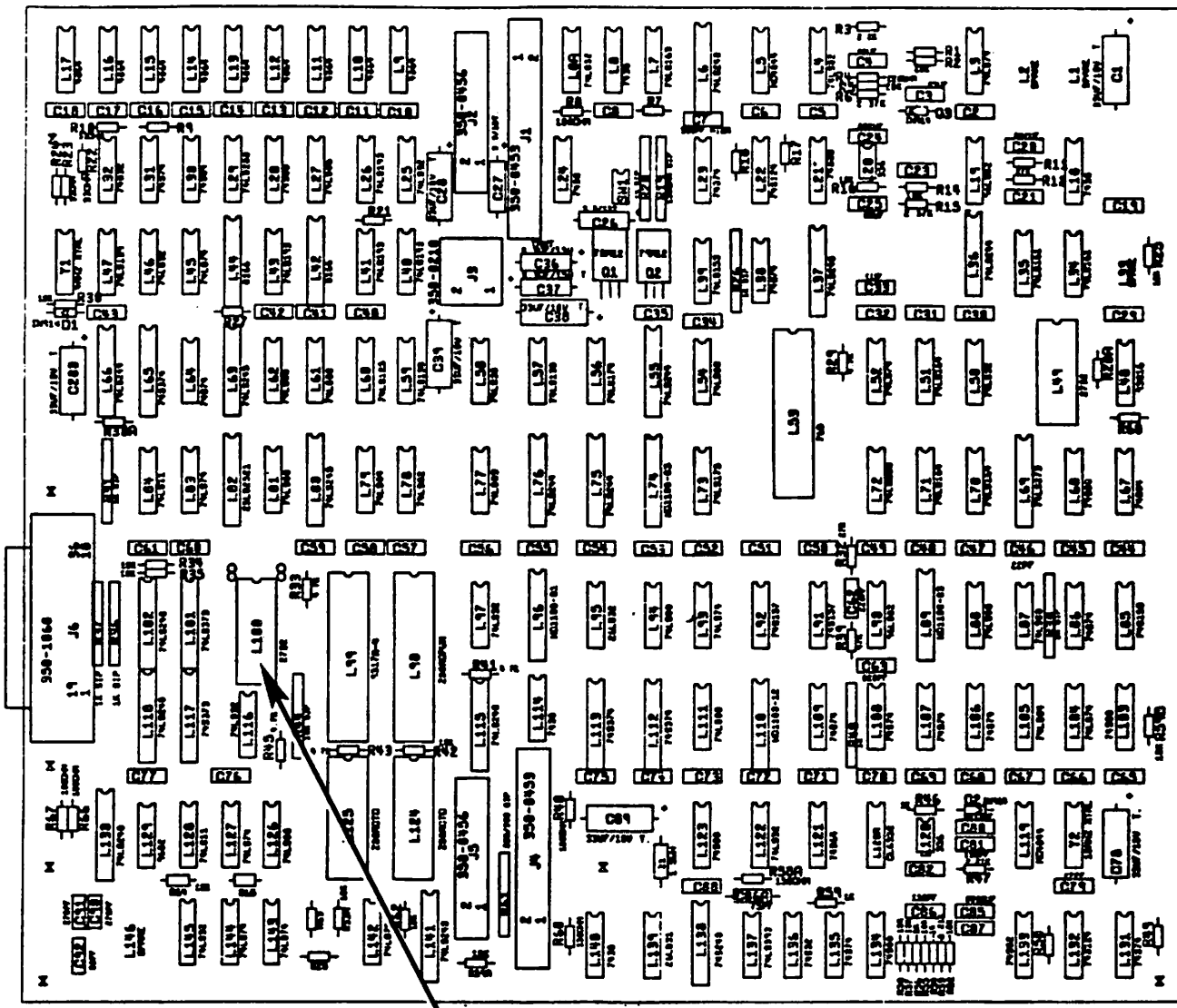
N/A

4. PREREQUISITE

N/A

5. INSTALLATION PROCEDURE

- A. Power down unit.
- B. Take out and retain four screws at back of unit. Remove chassis from unit.
- C. Access PROM at L100 on the 210-8396-A PCA thru the top of the unit between the fan and the floppy drive. Change the PROM at L100 from a 379-2000 to a 379-2000-R1 as shown in Figure 1.
- D. Reassemble the unit by reversing the procedures in Step 5.B. above.
- E. Document installation of the FCO by completing a Call Report or Activity Report.



CHANGE PROM AT L100  
TO 379-2000-R1

FIGURE 1 210-8396-A PCA

6. CHECK-OUT PROCEDURE

- A. Power up. Insure customer data is properly backed up.
- B. Run Magnetic Media diagnostics in 2200 Diagnostic Package:

Software Package # 195-2956-0

| <u>Disk Type</u> | <u>Part Number</u> | <u>Revision</u> |
|------------------|--------------------|-----------------|
| 8" SSSD          | 702-0292           | 6436            |
| 5 1/4" DSDD      | 732-0049           | 6436            |

NOTE: If Software Package #195-2956-0 is unavailable, run 2200 Multi Disk Exerciser, #702-0146 (SSSD) or 732-0013 (DSDD) Revision 16B4. (This diagnostic does not recognize the 2275 model.)

7. FCO KIT PARTS LISTING

FCO Kit # 728-0118

| <u>Item</u> | <u>Qty.</u> | <u>Description</u> |
|-------------|-------------|--------------------|
| 729-1517    | 1           | FCO Document 1100  |
| 379-2000-R1 | 1           | PROM               |

8. FCO KIT AVAILABILITY DATE

FCO Kit #728-0118 will be available July 2, 1984. To obtain it, place a routine order through the Logistics Order Processing System.

9. REMOVED PARTS DISPOSITION

Recycle removed PROM through your FSC.

10. MISCELLANEOUS

N/A



**ECO NO. 32638**  
SHEET 1 OF 4

ORIGINATOR: Don Logan/Al Floyd  
WRITTEN BY: Valerie Goguen  
PART NO.: 210-8396-A  
DWG NO.: 8396  
MODEL NO.: 2200MVPA/C  
CLASS: I (II) III

EXT. 76302/77468  
EXT. 4313  
DATE 05/07/84  
DATE 05/07/84

| DOCUMENTS       | REVISIONS |   |
|-----------------|-----------|---|
|                 | F         | T |
| BOM             |           |   |
| ARTWORK         |           |   |
| E-REV           |           |   |
| SAMPLE BD       |           |   |
| ASSY. DWG.      |           |   |
| DRILL DWG.      |           |   |
| SCHEM. DWG.     | 3         | 4 |
| MECH. DWG.      |           |   |
| CBL ASSY. DWG.  |           |   |
| S.P.I.          |           |   |
| MECH ASSY. DWG. |           |   |
| COMPONENT SPEC  |           |   |

| DESCRIPTION   | PEP #       | TYPE   | QTY | TYPE |
|---|-------------|--|-----|------|
| 5 1/4 Disk Contr 1 M/L  | PEP# H0197A | <input checked="" type="checkbox"/> HARDWARE <input type="checkbox"/> SOFTWARE | 1   | 1    |
| <b>DESCRIPTION OF CHANGE</b>  |             |  |     |      |
| Change schematic, software loading chart and sample board as follows:<br>FROM 379-2000<br>L100 379-2000<br>TO 379-2000-R1 |             |  |     |      |
| Change BOM 210-8396-A as follows:   |             |  |     |      |
| WL I#   | DESCRIPTION | UM   | QTY | TYPE |
| DELETE: 379-2000  | Prom        | EA   | 5   | P    |
| ADD: 379-2000-R1  | Prom        | EA   | 5   | P    |
| Delete the Product Structure and Part Number from the Data Base for the following prom:<br>379-2000                       |             |  |     |      |

RECEIVED 1  
JUN 5 1984  
PRINT ROOM

REASON/SYMPATOM FOR CHANGE

SEE ATTACHED SHEET.

Blank DM 377-0522 90

| EFFECTIVITY                | R F | CF | DT | TN | TA | TA | TA | TA |
|----------------------------|-----|----|----|----|----|----|----|----|
| TO CONFORM                 |     |    |    |    |    |    |    |    |
| USE AS IS TO PREVIOUS REV. |     |    |    |    |    |    |    |    |

| APPROVALS                        | DATE    |
|----------------------------------|---------|
| ECO MGR <i>John Floyd</i>        | 5/30/84 |
| DES. ENGRG. <i>John Floyd</i>    | 5-9-84  |
| CUST. ENGRG. <i>John Floyd</i>   | 5/30/84 |
| MFG. ENGRG. <i>John Floyd</i>    | 5-9-84  |
| ORIGINATOR <i>John Floyd</i>     | 5-9-84  |
| F.C.C. <i>Michael G. Beecher</i> | 5/14/84 |

This general release of the 2275 Disk Processing Unit firmware obsoletes the original production version. This release corrects the following problems:

-System hangs if board is powered up with no floppy diskette in the drive.

System hangs if a LIST DT command is issued when there is no media in the drive.

Alternate sector mapping function does not work.

Winchester hardware is not disabled when the Z80 attempts to access the alternate sector map, creating a memory contention.

Parity error hangs the system without returning an error message.

Cacheing problem causes invalid data to be returned to the 2200.

System status message does not properly identify the system configuration.

Additions have been made to the firmware as follows:

Firmware now supports 30 M-byte Quantum Winchester drives.

PC diskettes can be read, written, and formatted by the 2275.

Winchester format is now a one pass operation that writes a DB6, B6D, 6DB pattern onto the disk to help locate marginal sectors. ECC is disabled during format, and only two retries are allowed for header errors. In addition to mapping out a bad sector, the sectors immediately preceding and following the bad sector are mapped out.

A hook is provided so that Customer Engineering can perform radial-track and index-to-data head alignment.

A hook is provided to allow Customer Engineering to read the alternate sector map.

32608  
SMT 2 4

**WANG**

**ENGINEERING CHANGE ORDER  
MANUFACTURING EFFECTIVITY AND DISPOSITION**

ECO #

32608

SHEET

3 OF 4

**MATERIAL DISPOSITION**

IN STOCK  VENDOR

SCRAP

REWORK

USE AS IS

NEXT BUY

**SPECIAL INSTRUCTIONS**

*Sub assay and final test will conform upon receipt of final ECO and Skunkette.  
Master PROM was tested and approved at 1st test run.  
No change in blank PROM*

DOCUMENTATION ONLY

EFFECTIVITY: MATERIAL AVAILABILITY 5/25/84

IMPLEMENTATION 6-4-84

DATE 5/25/84

**APPROVALS**

COMMITTEE CHAIRPERSON

*John W. Johnson 5/25/84*

DISTRIBUTION

RE-MANUFACTURING

SITE MFG ENGINEERING

COMPONENT ENGINEER

CENTRAL QUALITY ENGRG. R.G. Thompson 5/30/84

SITE MATERIALS

OTHER

DISTRIBUTION

ALL UNITS ON OR BEFORE

RETURN TO MFG. PRODUCT LINE FOR REWORK

NO IMPACT

SPECIAL INSTRUCTIONS



**ENGINEERING CHANGE ORDER  
CUSTOMER ENGINEERING EFFECTIVITY AND DISPOSITION**

ECO 32608

SHEET 4 OF 4

|   |   |   |  |
|---|---|---|--|
| ALL UNITS <input checked="" type="checkbox"/><br>PROB. ONLY <input type="checkbox"/><br>INFO <input type="checkbox"/><br>FCO REQUIRED <input checked="" type="checkbox"/><br>EXP. _____<br>FSC REWORK <input checked="" type="checkbox"/><br>EXP. _____ | EFFECTIVITY COMMENTS:<br><i>Burge</i><br><i>MUB for Repair</i><br><i>FCO for field</i> <del>118</del> <sup>118</sup><br><i>10/18/84</i> | DOMESTIC<br>EST. UNIT POP. <u>777</u><br>EST. SPARE POP. <u>115</u><br>TOTAL <u>892</u> | INTERNATIONAL<br><u>522</u><br><u>95</u><br><u>617</u> |
|---|---|---|--|

| APPROVALS                    | DATE           | PROJECTED COST IMPACT |       |       |
|------------------------------|----------------|-----------------------|-------|-------|
|                              |                | MATERIAL              | LABOR | TOTAL |
| TECH OPS                     |                | \$ 1,369.00           |       |       |
| LOGISTICS <i>Dick D'Neil</i> | <i>5/17/84</i> | \$ 14,980.00          |       |       |
| FINAL <i>W. Ranno</i>        | <i>5/17/84</i> | \$ 16,349.00          |       |       |
| OTHER                        |                |                       |       |       |
| TOTAL                        |                |                       | 1     | 5.27  |

GENERAL COMMENTS: *See newsletter to field.*







ENGINEERING CHANGE ORDER  
CONTINUATION SHEET

DOCUMENT NO.

OLD REV

NEW REV

THIS ECO SHT, WHEN ATTACHED TO DOCUMENT OF  
PREVIOUS REV CONSTITUTES THE LATEST DOC.

ECO NO.

SHT

OF

33513

2

1

DOCUMENT TITLE:

Reason Symptom For Change:

Reason for hardware change:

During Winchester operations, the Z80 is out off from memory to allow the Winchester hardware to access memory. When a hard-wired reset is received by the 2275, hardware allows the Z80 immediate access to memory. If the user happens to reset the system during a Winchester operation, a memory contention occurs since no mechanism is provided to shut off the Winchester circuitry. This contention results in a parity error that ends up hanging the drive in the power-up diagnostics. The only way out of this condition is to power down the board and power it back up again.

This change shuts off the Winchester circuitry when a reset is received, provided that a disk write operation is not in progress. If a disk write operation is in progress, this change will delay the reset until the current sector is written. Delaying the reset signal during a Winchester write prevents the Winchester hardware from placing a write splice in the middle of a data field and eliminates ECC errors.





| COMPONENT  | TYPE   | WANG PART NO.   | QTY  |
|--|--|---|--|
| C1, 23   | .05UF +80-20% 16V  | 300-1938  | 2  |
| C91  | 270PF 500V   | 300-1279  | 1  |
| C92, 86A   | 82PF 500V  | 300-1082  | 2  |
| C79  | 27PF 500V  | 300-1027  | 1  |
| C46  | 22PF 500V  | 300-1022  | 1  |
| C81, 88  | 150PF 500V   | 300-1150  | 2  |
| C62  | 220PF 500V   | 300-1220  | 1  |
| C63  | 820PF 500V   | 300-1020  | 1  |
| C4   | .02UF 25V  | 300-1904  | 1  |
| C24, 20  | .002UF 500V  | 300-1913  | 2  |
| C10-C18  | .1UF 50V   | 300-1930  | 9  |
| C80, 85  | .0033UF 500V   | 300-1909  | 2  |
| C3, 5, 6, 8, 19, 21,<br>23, 24, 25, 26, 27,<br>28, 29, 30, 31, 32, 33,<br>34, 35, 36, 37, 38,<br>39, 40, 41, 42, 43, 44,<br>45, 46, 47, 48, 49,<br>50, 51, 52, 53, 54,<br>55, 56, 57, 58, 59, 60,<br>61, 62, 63, 64, 65, 66, 67, 68,<br>69, 70, 71, 72, 73, 74,<br>75, 76, 77, 78, 79, 80,<br>81, 82, 83, 84, 85, 86,<br>87, 88, 89, 90, 91, 92,<br>93, 94, 95, 96, 97, 98,<br>99, 100                   | .047UF 50V   | 300-1966  | 51   |
| C26, 37  | 3.3UF 16V (T)  | 300-4016  | 2  |
| C1, 23, 24, 25, 26, 27,<br>28, 29, 30, 31, 32, 33,<br>34, 35, 36, 37, 38,<br>39, 40, 41, 42, 43, 44,<br>45, 46, 47, 48, 49,<br>50, 51, 52, 53, 54,<br>55, 56, 57, 58, 59, 60,<br>61, 62, 63, 64, 65, 66,<br>67, 68, 69, 70, 71, 72,<br>73, 74, 75, 76, 77, 78,<br>79, 80, 81, 82, 83, 84,<br>85, 86, 87, 88, 89, 90,<br>91, 92, 93, 94, 95, 96,<br>97, 98, 99, 100                                       | 33UF 10V (T)   | 300-4024  | 7  |
| C7   | 300PF 500V (M)   | 300-5042  | 1  |
| C36, 27  | 5.8UF 35V (T)  | 300-4028  | 2  |
| C90  | .001UF CER.  | 300-1906  | 1  |
| R48, 56, 57, 8   | 100 1/4W 5%<br>200 1/4W 5%   | 330-2011  | 4  |
| R50, 58A   | 150 1/4W 5%  | 330-2016  | 2  |
| R4, 70, 71, 72, 73,<br>74, 75, 76, 77, 78,<br>79, 80, 81, 82, 83,<br>84, 85, 86, 87, 88,<br>89, 90, 91, 92, 93,<br>94, 95, 96, 97, 98,<br>99, 100  | 220 1/4W 5%  | 330-2023  | 9  |
| R19  | 150 91P/9 PACK   | 333-0854  | 1  |
| R10, 23, 22  | 33 1/4W 5%   | 330-1074  | 3  |
| R44  | 10K 91P  | 333-0809  | 1  |
| R20, 26, 31, 38,<br>40, 30, 33   | 1K 91P   | 333-0837  | 7  |
| R7   | 2.2K 1/4W 5%   | 330-3023  | 1  |
| R47, 53  | 2.21K 1/8W 1%  | 333-0183  | 2  |
| R1, 7, 9, 12, 17,<br>18, 21, 22, 23, 24,<br>25, 26, 27, 28, 29,<br>30, 31, 32, 33, 34,<br>35, 36, 37, 38, 39,<br>40, 41, 42, 43, 44,<br>45, 46, 47, 48, 49,<br>50, 51, 52, 53, 54,<br>55, 56, 57, 58, 59,<br>60, 61, 62, 63, 64,<br>65, 66, 67, 68, 69,<br>70, 71, 72, 73, 74,<br>75, 76, 77, 78, 79,<br>80, 81, 82, 83, 84,<br>85, 86, 87, 88, 89,<br>90, 91, 92, 93, 94,<br>95, 96, 97, 98, 99,<br>100 | 1K 1/4W 5%   | 330-3011  | 20   |
| R29, 33, 41, 43,<br>45, 76   | 4.7K 1/4W 5%   | 330-3040  | 6  |
| R1, 72   | 27K 1/4W 5%  | 330-4020  | 2  |
| R39  | 47K 1/4W 5%  | 330-4040  | 1  |
| R56  | 4.99K 1/8W 1%  | 333-0202  | 1  |
| R33A, 25, 30, 34,<br>35, 42, 54A, 54B,<br>62, 64   | 10K 1/4W 5%  | 330-4011  | 10   |
| R6, 15   | 2.37K 1/8W 1%  | 333-0093  | 2  |
| R2, 5  | 20K 1/8W 1%  | 333-3110  | 2  |
| R61  | 220/330 91P  | 333-0807  | 1  |
| Y1   | 4 MHz XTAL   | 321-1004  | 1  |
| Y2   | 10MHz XTAL   | 321-1010  | 1  |
| D1, 2, 3   | 1N914  | 300-1012  | 3  |
| Z1   | 1.5UH COIL   | 320-0713  | 1  |
| PCF  | 91L PAD  | 375-9034  | 2  |
| Q1   | 75M12  | 374-0014  | 1  |
| Q2   | 75M12  | 374-0019  | 1  |
| J1, 4  | 34 PCS CONN  | 350-0453  | 2  |
| J2, 5  | 20 PCS CONN  | 350-0456  | 2  |
| J3   | 5 PCS CONN   | 350-0218  | 1  |
| J6   | 36 PCS CONN  | 350-1060-M  | 1  |
| SW1  | 4 BANK SPST<br>BUTTON<br>SPACER<br>SPACER (B1)<br>SCREW<br>NUT<br>#8 FLAT WASHER<br>NYLON WASHER<br>NYLON SCREW<br>NYLON NUT<br>SUPPORT CONN.<br>GROUND STATIC | 325-1504<br>449-0597<br>462-0426<br>462-0433<br>650-4120<br>652-0029<br>653-4000<br>653-4004<br>650-2120<br>652-2001<br>458-1278-XA<br>458-3310 | 1<br>2<br>2<br>2<br>2<br>2<br>2<br>2<br>2<br>2<br>1<br>1 |
| R52, 55, 14, 16,<br>57, 58, 64   | 10K 1/8W 1%  | 333-0090  | 7  |

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| IC LOCATION                                       | TYPE       | HANG PART NO. | QTY |
|---|------------|---------------|-----|
| L1.45, 52, 93, 104, 83, 143, 144, 127, 142        | 74574      | 376-0155      | 10  |
| L4, 70  | 74502      | 376-0200      | 2   |
| L5, 119   | 4044       | 376-0264      | 2   |
| L6, 37, 102, 115, 118, 130, 141                   | 745240     | 376-0297      | 7   |
| L7  | 745163     | 376-0574      | 1   |
| L8, 18, 24, 114, 140                              | 7470       | 376-0120      | 5   |
| L8A, 122, 97, 50, 46, 115, 25, 145                | 74572      | 376-0211      | 8   |
| L9-17   | 4164       | 377-0466      | 9   |
| L90, 129  | 961502     | 376-0502      | 2   |
| L20, 120  | 756        | 376-0547      | 2   |
| L21, 28, 66, 103, 123, 134                        | 74508      | 376-0200      | 6   |
| L22, 132  | 745124     | 376-0273      | 2   |
| L23, 18, 86, 84, 71, 111, 135, 109, 106, 107, 108 | 74574      | 376-0202      | 11  |
| L26, 40, 41, 43                                   | 745193     | 376-0220      | 4   |
| L27   | 74586      | 376-0231      | 1   |
| L29, 72   | 74522      | 376-0275      | 2   |
| L30, 67   | 74504      | 376-0197      | 2   |
| L32   | 74572      | 376-0205      | 1   |
| L34, 35   | 745161     | 376-0233      | 2   |
| L36, 55, 66, 75, 76                               | 745244     | 376-0200      | 5   |
| L39   | 745157     | 376-0156      | 1   |
| L42, 44   | 8166       | 376-0553      | 2   |
| L47   | 745139     | 376-0226      | 1   |
| L48   | 745161     | 376-0270      | 1   |
| L49   | 2732A      | 376-9045      | 1   |
| L53   | 765A       | 377-0426      | 1   |
| L54, 81, 94                                       | 74500      | 376-0207      | 3   |
| L56   | 745174     | 376-0159      | 1   |
| L57, 59   | 745130     | 376-0294      | 2   |
| L58   | 74570      | 376-0249      | 1   |
| L60   | 745125     | 376-0406      | 1   |
| L61, 92, 111, 87, 88, 126                         | 74508      | 376-0153      | 6   |
| L63, 80   | 745245     | 376-0205      | 2   |
| L65, 145, 113                                     | 74574      | 376-0305      | 2   |
| L69 <i>L112</i>                                   | 745273     | 376-0302      | 1   |
| L70, 71, 51                                       | 745164     | 376-0236      | 3   |
| L73   | 745175     | 376-0160      | 1   |
| L74   | 401100-05  | 377-0450      | 1   |
| L77   | 74503      | 376-0224      | 1   |
| L79, 105  | 74504      | 376-0180      | 2   |
| L82   | 25152521   | 376-0317      | 1   |
| L84, 120  | 745111     | 376-0225      | 2   |
| L85   | 745153     | 376-0215      | 1   |
| L89   | 401100-03  | 377-0457      | 1   |
| L91, 92   | 745157     | 376-0217      | 2   |
| L95   | 261572     | 376-0471      | 1   |
| L96   | 401100-01  | 377-0459      | 1   |
| L98   | Z8FACPU    | 377-0360      | 1   |
| L99   | 9517-4     | 377-0411      | 1   |
| L101  | 745373     | 376-0310      | 1   |
| L110  | 401100-12  | 377-0456      | 1   |
| L117  | 745373     | 376-0306      | 1   |
| L121  | 564        | 376-0201      | 1   |
| L124, 125   | Z80ACTC    | 377-0371      | 2   |
| L133, 135   | 74502      | 376-0199      | 2   |
| L137  | 745793     | 376-0307      | 1   |
| L138  | 745240     | 376-0334      | 1   |
| L139  | 261571     | 376-0470      | 1   |
| L120A   | CL5752     | 376-8006      | 1   |
| L9-17   | SKT        | 376-9002      | 9   |
| L49   | SKT        | 376-9003      | 1   |
| L53, 98, 99                                       | SKT        | 376-9011      | 3   |
| L124, 125, 100                                    | SKT        | 376-9015      | 3   |
| L74, 89, 96, 110                                  | SKT        | 376-9020      | 4   |
| V1, 72  | INSTR. PAD | 376-9000      | 2   |
| L100  | 2764-2     | 379-2000      | 1   |

ECO# \_\_\_\_\_

PRODUCT SUPPORT CHECKLIST  
AND IMPACT REVIEW

SPECIFIC MODELS AFFECTED: 2275

EFFECTIVITY: ALL UNITS \_\_\_\_\_ PROB X INFO \_\_\_\_\_  
(Field Impact) (Field Impact)

REASON FOR CHOOSING EFFECTIVITY? Some customers will have this problem even after R2 programs

ESTIMATED PERCENTAGE OF UNITS TO EXHIBIT PROBLEM: 15%  
(Only for ECO's with "Problem Only" effectivity)

IS FIELD REWORK REQUIRED (FCO)? YES X NO \_\_\_\_\_

ESTIMATED INSTALLATION TIME 30 min

IS A "TAC NEWSLETTER" REQUIRED? YES X NO \_\_\_\_\_

IS FSC REWORK REQUIRED (MUB)? YES X NO \_\_\_\_\_

IS A "PURGE OF STOCK" REQUIRED? YES X NO \_\_\_\_\_

DOES ECO IMPACT LOGISTICS? YES X NO \_\_\_\_\_

IS REASON FOR CHANGE CLEAR, ACCURATE AND TECHNICALLY CORRECT? YES X NO \_\_\_\_\_

DOES ECO IMPACT:

GENERAL TECHNICAL SUPPORT, UNIQUE TOOLS, REPAIR TECHNIQUE, TECHNICAL DOCUMENTATION, ETC.? YES \_\_\_\_\_ NO \_\_\_\_\_

REVIEWER SIGNATURE [Signature] DATE: 8/7/84

COMMENTS ON THE ABOVE STATEMENTS:  
Should be done in conjunction with 33512

ME-02-24



# ECO

3/27

ECO NO. 30135

SHEET 1 OF 4

ORIGINATOR **MARK J. NELSON** M/S 6312 EXT. 365 DATE 03/20/84

WRITTEN BY M/S EXT.

| PART NO.  | DESCRIPTION | DOCUMENTS |   | REVISIONS |   |
|-----------|-------------|-----------|---|-----------|---|
|           |             | F         | T | F         | T |
| DWG NO.   | SEE BELOW   |           |   |           |   |
| MODEL NO. | 2275-10/20  |           |   |           |   |
| CLASS     | I (II) III  |           |   |           |   |

| WLI#             | DESCRIPTION             | UM | COMP TYPE | QTY.   | TYPE |
|------------------|-------------------------|----|-----------|--------|------|
| 167/187-3505     | 2275-10 DISK PERIPHERAL |    |           |        |      |
| 167/187-3506     | 2275-20 DISK PERIPHERAL |    |           |        |      |
| DELETE: 685-0728 | SACK FLAT CUSH 8.5x12   | EA | I         | 1.0000 | I    |
| ADD: 290-0134    | 2275-10/20 PKG ASSY.    | EA | I         | 1.0000 | I    |
| ADD: 615-1719    | LBL UL LST MRK          | EA | I         | 1.0000 | I    |

**DESCRIPTION OF CHANGE**

1. CHANGE THE FOLLOWING BOM'S:

RECEIVED  
APR 27 1984  
PRINT ROOM

**REASON/SYMPOTM FOR CHANGE**

1. TO INCLUDE THE PACKAGING ASSEMBLY AND UL LABEL ON THE 227-10/20 BOM'S.  
 2. WLI# 685-0728 IS NOT THE PROPER SIZE BAG FOR USE IN THE ABOVE MENTIONED SYSTEMS, IS NOT CURRENTLY BEING USED IN PRODUCTION AND IS BEING RETURNED TO THE STOCKROOM. WLI# 690-0312 IS BEING USED INSTEAD OF WLI# 685-0728.

| DOCUMENTS       | REVISIONS |
|-----------------|-----------|
| BOM             |           |
| ARTWORK         |           |
| E-REV           |           |
| SAMPLE BD       |           |
| ASSY. DWG.      |           |
| DRILL DWG.      |           |
| SCHEM. DWG.     |           |
| MECH. DWG.      |           |
| CBL ASSY. DWG.  |           |
| S.P.I.          |           |
| MECH ASSY. DWG. |           |
| COMPONENT SPEC  |           |

| EFFECTIVITY                | RF MFG | C.E. | DIST. | FINAL ASSY AREA | SUB ASSY AREA | FUTR MFG |
|----------------------------|--------|------|-------|-----------------|---------------|----------|
| TO CONFORM                 |        |      |       |                 |               | X        |
| USE AS IS TO PREVIOUS REV. | X      | X    | X     | X               |               |          |

| APPROVALS                        | DATE     |
|----------------------------------|----------|
| ECO MGR. <i>G. J. J. J.</i>      | 4/18     |
| DES. ENGRG.                      |          |
| CUST. ENGRG.                     | 4/18/84  |
| MFG. ENGRG. <i>John J. J. J.</i> | 4/17/84  |
| ORIGINATOR <i>hand of Nelson</i> | 22MAR-84 |
| F.C.C.                           |          |



**WANG**

ENGINEERING CHANGE ORDER  
CONTINUATION SHEET

|                  |          |         |
|------------------|----------|---------|
| DOCUMENT NO.     | OLD REV  | NEW REV |
| ECO NO.<br>32135 | SHT<br>2 | OF<br>4 |

THIS ECO SHT, WHEN ATTACHED TO DOCUMENT OF PREVIOUS REV CONSTITUTES THE LATEST DOC.

DOCUMENT TITLE:

DESCRIPTION OF CHANGE:

2. CHANGE THE FOLLOWING BOM:

| <u>MLI#</u>      | <u>DESCRIPTION</u>                  | <u>UM</u> | <u>TYPE</u> | <u>QTY.</u> | <u>TYPE</u> |
|------------------|-------------------------------------|-----------|-------------|-------------|-------------|
| 290-0098         | SHPG PKG BOM: MINI ARCHIVING-TAP-DR |           |             |             |             |
| DELETE: 685-0728 | SACK FLAT CUSH 8.5x12 EA            | 1         | EA          | 1.0000      | 1           |

# ENGINEERING CHANGE ORDER MANUFACTURING EFFECTIVITY AND DISPOSITION

**WANG**

ECO # 32135

SHEET 3 OF 4

## MATERIAL DISPOSITION

IN STOCK VENDOR

- SCRAP
- REWORK
- USE AS IS
- NEXT BUY

SPECIAL INSTRUCTIONS

DOCUMENTATION ONLY

EFFECTIVITY: MATERIAL AVAILABILITY IMMEDIATE DATE IMMEDIATE

IMPLEMENTATION 4-27-84

## APPROVALS

COMMITTEE CHAIRPERSON *John DeLorenzo 4/17/84*

DISTRIBUTION

RE-MANUFACTURING

SITE MFG ENGINEERING *13 MAR 84*

COMPONENT ENGINEER

CENTRAL QUALITY ENGRG. *4-17-84*

R & D

SITE MATERIALS *4/17/84*

OTHER *4/17/84*

DISTRIBUTION

ALL UNITS ON OR BEFORE

RETURN TO MFG. PRODUCT LINE FOR REWORK

NO IMPACT

SPECIAL INSTRUCTIONS



**ENGINEERING CHANGE ORDER  
CUSTOMER ENGINEERING EFFECTIVITY AND DISPOSITION**

ECO 32135

SHEET 4 OF 4

| <input type="checkbox"/> ALL UNITS<br><input type="checkbox"/> PROB. ONLY<br><input checked="" type="checkbox"/> INFO<br><br><input type="checkbox"/> FCO REQUIRED<br>EXP. _____<br><br><input type="checkbox"/> FSC REWORK<br>EXP. _____   | EFFECTIVITY COMMENTS:<br><br><div style="text-align: center; font-size: 2em; font-family: cursive;"> <i>Document to be reviewed</i> </div> | <table style="width:100%; border-collapse: collapse;"> <tr> <td style="width:50%; text-align: center;">DOMESTIC</td> <td style="width:50%; text-align: center;">INTERNATIONAL</td> </tr> <tr> <td style="text-align: center;">EST. UNIT POP. _____</td> <td style="text-align: center;">_____</td> </tr> <tr> <td style="text-align: center;">EST. SPARE POP. _____</td> <td style="text-align: center;">_____</td> </tr> <tr> <td style="text-align: center;">TOTAL _____</td> <td style="text-align: center;">_____</td> </tr> </table> | DOMESTIC | INTERNATIONAL | EST. UNIT POP. _____ | _____ | EST. SPARE POP. _____ | _____ | TOTAL _____ | _____ |  |  |  |       |  |  |                   |
|---|--|---|----------|---------------|----------------------|-------|-----------------------|-------|-------------|-------|--|--|--|-------|--|--|-------------------|
| DOMESTIC  | INTERNATIONAL  |   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |
| EST. UNIT POP. _____  | _____  |   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |
| EST. SPARE POP. _____   | _____  |   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |
| TOTAL _____   | _____  |   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |
| APPROVALS _____<br><br>TECH OPS _____<br><br>LOGISTICS <i>Jack O'Neil</i><br><br>FINAL <i>W. Harris</i><br><br>OTHER _____  | DATE _____<br><br>_____<br>_____<br>_____  | PROJECTED COST IMPACT<br><br>MATERIAL _____<br>LABOR _____<br>TOTAL _____   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |
| PROJECTED PART REQUIREMENT<br><br><table style="width:100%; border-collapse: collapse;"> <thead> <tr> <th style="width:60%;">PART #</th> <th style="width:15%;">QTY</th> <th style="width:25%;">EXT. COST</th> </tr> </thead> <tbody> <tr> <td> </td> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> <td> </td> </tr> <tr> <td> </td> <td> </td> <td> </td> </tr> <tr> <td style="text-align: center;">TOTAL</td> <td> </td> <td> </td> </tr> </tbody> </table> |  | PART #  | QTY      | EXT. COST     |                      |       |                       |       |             |       |  |  |  | TOTAL |  |  | GENERAL COMMENTS: |
| PART #  | QTY  | EXT. COST   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |
|   |  |   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |
|   |  |   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |
|   |  |   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |
| TOTAL   |  |   |          |               |                      |       |                       |       |             |       |  |  |  |       |  |  |                   |



# ECO

# ECO NO. 276-13

SHEET 1 OF 5

ORIGINATOR: Don Paradis  
 WRITTEN BY: Elly Gilks  
 PART NO.: 300-3141  
 DWG NO.: N/A  
 MODEL NO.: 525 ADD-ON DISK DR.  
 CLASS: I II III

EXT. 4117  
 EXT. 3230  
 DATE 04/13/83  
 DATE 04/13/83

| DOCUMENTS       | REVISIONS |   |
|-----------------|-----------|---|
|                 | F         | T |
| BOM             |           |   |
| ARTWORK         |           |   |
| E-REV           |           |   |
| SAMPLE BD       |           |   |
| ASSY. DWG.      | 2         | 3 |
| DRILL DWG.      |           |   |
| SCHEM. DWG.     | 2         | 3 |
| MECH. DWG.      |           |   |
| CBL ASSY. DWG.  |           |   |
| S.P.I.          |           |   |
| MECH ASSY. DWG. |           |   |
| COMPONENT SPEC  |           |   |

|             |  |
|-------------|--|
| DESCRIPTION | SEE BELOW  |
| PEP #       | PEP# H0100A  |
| TYPE        | <input checked="" type="checkbox"/> HARDWARE <input type="checkbox"/> SOFTWARE |

**DESCRIPTION OF CHANGE**  
 Change Item Master description as follows:  
 WLI# 300-3141  
 FROM: CAP 2200UF 15V+ 20% ALUM ELEC  
 TO: CAP 2200UF 16V+ 20% ALUM ELEC

Change schematic and assembly drawing per attached prints.

**RECEIVED**  
 JUN 16 1983  
 PRINT ROOM

**REASON/SYMPOTM FOR CHANGE**  
 To correct voltage cited in Item Master to agree with parts to be ordered from vender.

|                            |          |    |      |           |               |           |
|----------------------------|----------|----|------|-----------|---------------|-----------|
| EFFECTIVITY                | R F MFG. | CF | DST. | FINL AREA | SUB ASSY AREA | FUTR MFG. |
| TO CONFORM                 |          |    |      |           |               |           |
| USE AS IS TO PREVIOUS REV. |          |    |      |           |               |           |

| APPROVALS                      | DATE    |
|--------------------------------|---------|
| ECO MGR. <i>Don Paradis</i>    | 5/27    |
| DES. ENGRG. <i>Don Paradis</i> | 4/14/83 |
| CUST. ENGRG. J. PROULX         | 4/27/83 |
| MFG. ENGRG. J. TYNAN           | 5-25-83 |
| ORIGINATOR                     |         |
| F.C.C. <i>Elly Gilks</i>       | 5/27/83 |



TECHNICAL SERVICE BULLETIN  
 SECTION: HardWare Technical

NUMBER: HWT 5012 REPLACES: \_\_\_\_\_ DATE: 01/22/85 PAGE 1 OF 1

MATRIX ID. 3110 PRODUCT/RELEASE# 2275

TITLE: 2275 General Information

PURPOSE:

To inform field of undocumented switch settings as well as additional information on configurations and addressing.

EXPLANATION:

Wang is now offering four (4) versions of the 2275, dependent on the disk drives. The switch bank on the 210-8396 Disk Controller Board should be set as follows:

| VERSION | FIXED  | ADDRESS | LAST SECTOR                    | REMOVABLE | ADDRESS | LAST SECTOR                    | SW1 | SW2 | SW3 | SW4 |   |
|---------|--------|---------|--------------------------------|-----------|---------|--------------------------------|-----|-----|-----|-----|---|
| -10     | 10 MEG | D11     | 38911                          | FLOPPY    | D10     | 1279                           | ON  | ON  | ON  | ON  | F |
| -20     | 10 MEG | D11     | 38911                          | 10 MEG    | D10     | 38911                          | ON  | ON  | ON  | OFF | 7 |
| -30     | 30 MEG | D11/D12 | <sup>5</sup> <del>6</del> A023 | FLOPPY    | D10     | 1279                           | OFF | ON  | ON  | ON  | E |
| -60     | 30 MEG | D11/D12 | <sup>5</sup> <del>6</del> A023 | 30 MEG    | D10/D13 | <sup>5</sup> <del>6</del> A023 | OFF | OFF | ON  | OFF | 4 |
|         | 30 MEG | D11/D12 | 65023                          | 10 MEG    | D10     | 65023                          | OFF | ON  | ON  | OFF | 6 |

At this time the only manufacturer for 30 Meg drives that we are using is Quantum, model #5040, and this is the only 5 1/4" model we are using from them. This means if you have a 5 1/4" fixed drive and it is a Quantum, then it is a 30 Meg, and if it is not a Quantum, it is a 10 Meg.

ONLY 1ST <sup>WINC</sup> ~~WINT~~ TERMINATED (FIXED LEFT) D11 TERMINATOR 726-1882  
 DS1 SELECTED ON BOTH WINCHESTERS  
 FLOPPY IS DS1 + IS TERMINATED

★ 220-3324 DAISY CHAIN CABLE NEEDED WHEN USING 2 Winc's. D11 IS 1<sup>ST</sup> DRIVE ON CABLE.  
 ALSO NEEDED B CABLE FOR 2<sup>ND</sup> DRIVE - 220-3313.  
 210-7342 DUAL CONTROLLER PROBLEM - NEED 8396 B20, E-REV 6. FIX: LIFT PIN 6 OF L127  
 TIE L118 PIN 1 TO L118 PIN 10  
 ADD 57 Ω RESISTOR FROM L118 PIN 10 TO GND  
 GROUP: Technical Assistance Center P.C. Group MAIL STOP: 0126

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.

## PERIPHERALS - DISK DRIVES - 5 1/4 "DISK DRIVES

TOPIC: 2275 General Information

Wang is now offering four (4) versions of the 2275 dependent of the disk drives. The switch bank on the #210-8396 Disk Controller Board should be set as follows:

| VERSION | FIXED  | ADDRESS | LAST<br>SECTOR | REMOVABLE | ADDRESS | LAST<br>SECTOR | SW1 | SW2 | SW3 | SW4 |
|---------|--------|---------|----------------|-----------|---------|----------------|-----|-----|-----|-----|
| -10     | 10 MEG | D11     | 38911          | FLOPPY    | D10     | 1279           | ON  | ON  | ON  | ON  |
| -20     | 10 MEG | D11     | 38911          | 10 MEG    | D10     | 38911          | ON  | ON  | ON  |     |
| -30     | 30 MEG | D11/D12 | 64023          | FLOPPY    | D10     | 1279           |     | ON  | ON  | ON  |
| -60     | 30 MEG | D11/D12 | 64023          | 30 MEG    | D10/D13 | 64023          |     |     | ON  |     |

At this time, the only manufacturer for 30 MEG drives that we are using is Quantum, Model #5040, and this is the only 5 1/4" model we are using from them. This means if you have a 5 1/4" fixed drive and it is a Quantum, then it is a 30 MEG, and if it is not a Quantum, it is a 10 MEG.

---

Mike Bahia  
PSE X60256

MB/smr

| PORT ADDRESS | DPU SYSTEM STATUS REGISTER  |
|--------------|---|
| XXE0         | DB0 = 1 2200 Computer is Ready to Communicate with the DPU<br>DB1 = 1 Floppy Disk Drive Door was Opened<br>DB2 = 0 Winchester Drive is in Process of Writing Data Field during a Format Operation<br>DB3 = 1 Floppy Disk Drive Index Pulse (may be used by diagnostic to time Floppy Spindle Speed) |

| PORT ADDRESS   | SWITCH FUNCTIONS - OPEN = 1 CLOSE = 0  |                |     |                             |               |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
|----------------|--|----------------|-----|-----------------------------|---------------|-----------------------------|--|-----|-----|-----|-----|-----------|---------------|-----|-----|-----|-----|--|--|---|---|---|---|-----------|--------|---|---|---|---|-----------|--------|---|---|---|---|-----------|--|---|---|---|---|-----------|-----------|---|---|---|---|-----------|-----------|---|---|---|---|-----------|--|---|---|---|---|-----------|-----------|
| XXE0           | <table border="1"> <thead> <tr> <th colspan="4">Switch Setting</th> <th colspan="2">Drive Description &amp; Address</th> </tr> <tr> <th>DB7</th> <th>DB6</th> <th>DB5</th> <th>DB4</th> <th>Fixed (F)</th> <th>Removable (R)</th> </tr> <tr> <th>SW4</th> <th>SW3</th> <th>SW2</th> <th>SW1</th> <th></th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>10meg WIN</td> <td>FLOPPY</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>30meg WIN</td> <td>FLOPPY</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>Undefined</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>10meg WIN</td> <td>10meg WIN</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>30meg WIN</td> <td>10meg WIN</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>0</td> <td>Undefined</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>1</td> <td>30meg WIN</td> <td>30meg WIN</td> </tr> </tbody> </table> | Switch Setting |     |                             |               | Drive Description & Address |  | DB7 | DB6 | DB5 | DB4 | Fixed (F) | Removable (R) | SW4 | SW3 | SW2 | SW1 |  |  | 0 | 0 | 0 | 0 | 10meg WIN | FLOPPY | 0 | 0 | 0 | 1 | 30meg WIN | FLOPPY | 0 | 0 | 1 | 0 | Undefined |  | 1 | 0 | 0 | 0 | 10meg WIN | 10meg WIN | 1 | 0 | 0 | 1 | 30meg WIN | 10meg WIN | 1 | 0 | 1 | 0 | Undefined |  | 1 | 0 | 1 | 1 | 30meg WIN | 30meg WIN |
| Switch Setting |  |                |     | Drive Description & Address |               |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
| DB7            | DB6  | DB5            | DB4 | Fixed (F)                   | Removable (R) |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
| SW4            | SW3  | SW2            | SW1 |                             |               |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
| 0              | 0  | 0              | 0   | 10meg WIN                   | FLOPPY        |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
| 0              | 0  | 0              | 1   | 30meg WIN                   | FLOPPY        |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
| 0              | 0  | 1              | 0   | Undefined                   |               |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
| 1              | 0  | 0              | 0   | 10meg WIN                   | 10meg WIN     |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
| 1              | 0  | 0              | 1   | 30meg WIN                   | 10meg WIN     |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
| 1              | 0  | 1              | 0   | Undefined                   |               |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |
| 1              | 0  | 1              | 1   | 30meg WIN                   | 30meg WIN     |                             |  |     |     |     |     |           |               |     |     |     |     |  |  |   |   |   |   |           |        |   |   |   |   |           |        |   |   |   |   |           |  |   |   |   |   |           |           |   |   |   |   |           |           |   |   |   |   |           |  |   |   |   |   |           |           |

2275

X = ON

8396 BOARD

SWITCH SETTINGS

| F      | R      | SW 1 | SW 2 | SW 3 | SW 4 |     |
|--------|--------|------|------|------|------|-----|
| 10 MEG | FLOP   | X    | X    | X    | X    | -10 |
| 10 MEG | 10 MEG | X    | X    | X    |      | -20 |
| 30 MEG | FLOP   |      | X    | X    | X    | -30 |
| 30 MEG | 10 MEG |      | X    | X    |      |     |
| 30 MEG | 30 MEG |      |      | X    |      | -60 |

ONLY FIRST WINCHESTER TERMINATED (D11)

DS1 SELECTED ON BOTH WINCHESTER.

DS1 ON FLOPPY ALWAYS, FLOPPY ALWAYS TERMINATED



## 2275 DISK UNIT

## General Information

The 2275 was recently released to the field and comes in 2 models, the -10 (A 10MB 5 1/4" Winchester and a 320 KB floppy) and the -20 (2 Winchester drives).

Along with 2 drives there are also 2 boards in this unit, a regulator and a controller board. The part numbers are as follows:

|                |  |  |
|----------------|--|--|
|                | 210-8397   | Power Supply Regulator Board                                       |
|                | 210-8396   | Disk Controller Board  |
|                | 278-4030   | 10 MB Winchester (same as PC) SEAGATE ST412/NEC DS124              |
|                | 278-4034   | 30 MB QUANTUM MDL Q5040 (SAME AS DS)                               |
|                | 278-4026   | 320 KB Floppy (same as PC)   |
|                | 220-3312   | FLOPPY + SINGLE WINC DRIVE CABLES                                  |
|                | 220-2013   | Internal Cable - POWER HARNESS                                     |
|                | 220-3324   | INTERNAL DAISY CHAIN CABLE FOR 2 WINC DRIVES                       |
|                | 220-0105-4   | I/O Cable (220-0364/0365) BAD CONNECTORS, REVERSING CABLE          |
|                | 220-3313   | WINC B CABLE <span style="float: right;">SOMETIMES CORRECTS</span> |
| I/O Controller | 210-6541 rev 3   | Disk Controller (in CPU) or  |
|                | 210-3012   | MVP Triple Controller  |
|                | THERE WERE PROBLEMS EARLY ON W/ THE PRINTER/DISK CONTROLLER, OK NOW. |  |
|                | MVP 2.4 or higher is required.                                       |  |

## Switch Settings:

8396 Board - SW 1, 2, 3, 4 closed (Winc. and Floppy) SW 1, 2, 3 closed, 4 open (2 Winc. ) 2 30 MEG SW 3 CLOSED SW 1, 2, 4 OPEN  
 30 MEG F/10 MEG R SW 2, 3 CLOSED SW 1, 4 OPEN  
 30 MEG F/FLOPPY SW 2, 3, 4 CLOSED SW 1 OPEN

278-4030 - If an IMI Winchester - SW 1 on only (no switches on other drives)

## Voltages

|                  |                       |                          |
|------------------|-----------------------|--------------------------|
| -12V regulated   | 8396 brd, base of Q2  | Not adjustable           |
| +12V regulated   | 8396 brd, base of Q1  | Not adjustable           |
| +5V regulated    | 8397 brd, see picture | Pot on 8397, see picture |
| +12V regulated   | 8397 brd, see picture | Pot on 8397, see picture |
| -16V unregulated | 8397 brd, see picture | Not adjustable           |
| +16V unregulated | 8397 brd, see picture | Not adjustable           |
| +0V              | 8397 brd, see picture |                          |

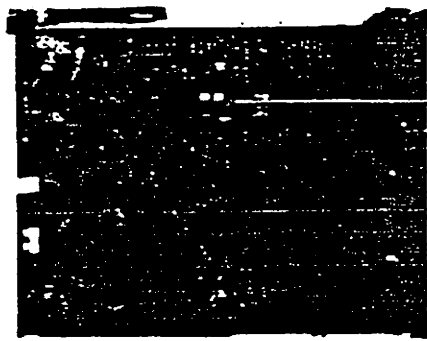
## WINCHESTER ADDRESSING

WINC. 1 D10 D13 OR FLOPPY D10

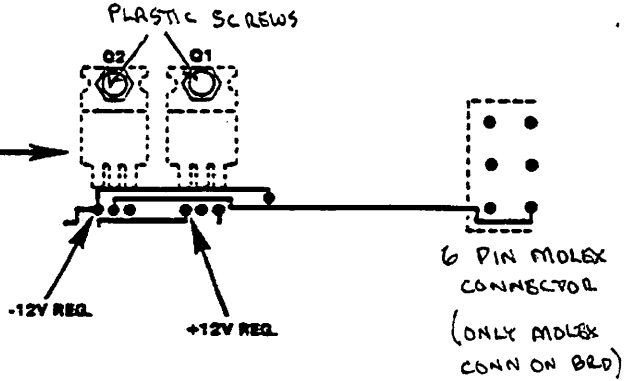
WINC. 2 D11 D12

## LAST SECTOR

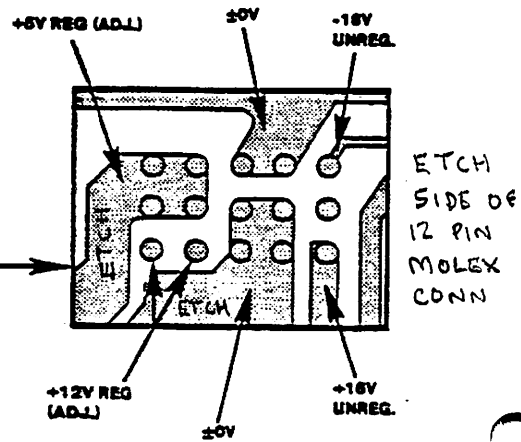
FLOPPY 1279 10MEG 38911 30MEG 64023 (2 SURFACES)



8396 CONTROLLER BOARD



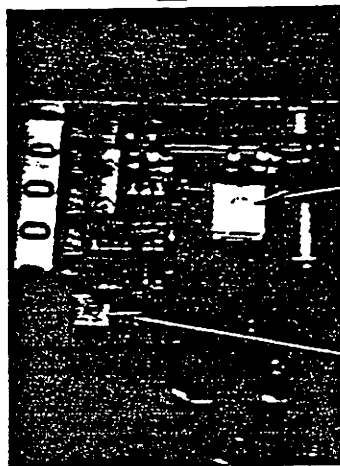
8397 REGULATOR BOARD



Voltage Test Points



RIGHT SIDE  
IN FRONT  
OF FAN



+12V ADJUSTMENT  
CENTER OF RT SIDE, 1" IN FROM EDGE

+5V ADJUSTMENT  
NEAR FRONT EDGE OF BOARD TO RIGHT  
OF 12 PIN MOLEX CONN

WANG

TECHNICAL SERVICE BULLETIN  
SECTION: HardWare Technical

NUMBER: HWT 6291 REPLACES: \_\_\_\_\_ DATE: 12/02/86 PAGE 1 OF 1

MATRIX ID. 3110 PRODUCT/RELEASE # 2275

TITLE: 2275 I/O CABLE PROBLEM

PURPOSE:

To inform the field of a possible poor mating connection problem between the I/O (WLN 220-0105-4) cable and the I/O port connector on the board (WLN 210-8396A).

EXPLANATION:

Manufacturing has used some standoffs on the 2275 port connector that prevents the I/O cable from making a good electronic contact with the 210-8396A port connector on the board, causing I-92 errors.

The circumventions are:

- Reinsert the I/O cable into the port of the 2275 unit.
- Try a different I/O cable.

Boards with the wrong standoff can be identified by observing the I/O cable connector sitting too high on the 210-8396 port connector.

To correct this problem order the correct standoff, WLN 462-0452, from stock.

GROUP: Desktop Systems/Peripherals Group MAIL STOP: 001-250

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.

TECHNICAL SERVICE BULLETIN  
SECTION: HARDWARE TECHNICAL

NUMBER: HWT 6257 REPLACES: N/A DATE: 10/28/86 PAGE 1 OF 1  
MATRIX ID. 3107 PRODUCT/RELEASE# 2275  
TITLE: PCB 210-8396 REV. 4 GIVING I-92 ERROR

PURPOSE:

To inform the field of I-92 errors on the 2275 when running customer applications.

EXPLANATION:

In the last 16 weeks Manufacturing had built the 210-8396 Rev. 4 with the wrong memory chips at locations L9, L10, L11, L12, L13, L14, L15, L16 and L17. The wrong memory chips are from Siemens - SHY B4164 / P2 LF and are out of specifications.

Boards with these memory chips are causing I-92 errors. The correct WLN for the 200ns, 64K memory chips (Motorola or TI) is 377-0466.

Boards with the incorrect memory chips can be corrected in the field by replacing the Siemens memory chips with the above.

Manufacturing processed a Purge Notice to correct their stock. CE Logistics and Repair Centers were notified of this problem, and will purge stock and correct boards as they are returned.

GROUP: Desktop Systems/Peripherals Group MAIL STOP: 0114

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.

**WANG**

TECHNICAL SERVICE BULLETIN  
SECTION: HardWare Technical

NUMBER: HWT 5337 REPLACES: N/A DATE: 01/14/86 PAGE 1 OF 1  
MATRIX ID. 3110 PRODUCT/RELEASE# Half-Height Floppy Disk Drive  
TITLE: Half-Height Floppy Disk Drive Problems

PURPOSE:

To inform the field of a potential problem with the 360 KB half-height floppy disk drive (WLI P/N 278-4033).

EXPLANATION:

The vendor supplying this floppy drive recently switched over to a newer version using VLSI and surface mount technology. These newer version drives can be identified by the Model No. JU455-5 on the rear of the frame, and the drive door handle does not have a hole in it. A problem with this new model drive has been identified as causing alteration or loss of data.

CORRECTIVE ACTIONS:

All drives that have been corrected have been identified in the following manner:

- A 22uf capacitor has been added between Pins 8 and 9 of J6 connector on the component side of the PCB with the plus end attached to Pin 9. The physical location of the added cap is where D1 and D2 are silkscreened on the PCB.

Any drive found to be exhibiting this problem should be checked for this identification, and should it be missing, the drive should be replaced. This problem only affects the JU455-5 model and not the SA455-3 model.

GROUP: Peripheral Hardware Support Group MAIL STOP: 0125

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.

TECHNICAL SERVICE BULLETIN  
SECTION: HardWare Technical

NUMBER: HWT 5238 REPLACES: \_\_\_\_\_ DATE: 10/22/85 PAGE 1 OF 1  
MATRIX ID. 3110 PRODUCT/RELEASE# 5 1/4 Disk Drive  
TITLE: FCO 1111A, 2275-10, 20, 30 Disk Peripheral

PURPOSE:

To inform the field that FCO 1111A has been released. R3 Proms

EXPLANATION:

FCO 1111A, released October 1, 1985, documents ECO 37694 and replaces FCO 1111. One EPROM on the 210-8396-A Disk Controller PCB is changed. The reason for the change is to correct the following problems.

1. The '40' bit of the drive address is not checked. The 2275 responds to 350 as if it were 310, 360 as if 320, 370 as if 330.
2. An "I92" error occurs when the '\$GIO' "Read Prom Rev Level" command is given.
3. The power-up diagnostic does not flag floppy drive stepper motor failures.
4. Formatting a drive does not reset the read/write caches.
5. In the Winchester back-up subroutine, the 2275 does not recognize an unformatted diskette and hangs the system.
6. The diagnostic gets lost if there is an error on the Winchester.
7. Will not report the number of sectors available.

FCO 1175 must be done in conjunction with FCO 1111A. (An "I91" error may occur if FCO 1175 is not installed.)

FCO kit #728-0129A is available and can be obtained by placing a routine order through the Logistics order processing system.

GROUP: ECO Support Group

MAIL STOP: 0139

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.

WANG

TECHNICAL SERVICE BULLETIN  
SECTION: HardWare Technical

NUMBER: HWT 5239 REPLACES: \_\_\_\_\_ DATE: 10/22/85 PAGE 1 OF 1  
MATRIX ID. 3110 PRODUCT/RELEASE# 5 1/4 Disk Drive  
TITLE: FCO 1175, 2275-10, 20, 30 Disk Peripheral

PURPOSE:

To inform the field that FCO 1175 has been released.

EXPLANATION:

FCO 1175, released October 1, 1985, documents ECO 36892. Three jumper wires and one resistor are added to the 210-8396A Disk Controller PCB. The reason for the change is to support the R3 EPROM revision. Without this change an "I91" error may occur when the R3 EPROM is installed.

FCO kit #728-0191 is available and can be obtained by placing a routine order through the Logistics order processing system.

GROUP: ECO Support Group

MAIL STOP: 0139

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.



TECHNICAL SERVICE BULLETIN  
 SECTION: HardWare Technical

NUMBER: HWT 5012 REPLACES: \_\_\_\_\_ DATE: 01/22/85 PAGE 1 OF 1

MATRIX ID. 3110 PRODUCT/RELEASE# 2275

TITLE: 2275 General Information

PURPOSE:

To inform field of undocumented switch settings as well as additional information on configurations and addressing.

EXPLANATION:

Wang is now offering four (4) versions of the 2275, dependent on the disk drives. The switch bank on the 210-8396 Disk Controller Board should be set as follows:

| VERSION | FIXED  | ADDRESS | LAST<br>SECTOR                    | REMOVABLE | ADDRESS | LAST<br>SECTOR                    | SW1 | SW2 | SW3 | SW4 |   |
|---------|--------|---------|-----------------------------------|-----------|---------|-----------------------------------|-----|-----|-----|-----|---|
| -10     | 10 MEG | D11     | 38911                             | FLOPPY    | D10     | 1279                              | ON  | ON  | ON  | ON  | F |
| -20     | 10 MEG | D11     | 38911                             | 10 MEG    | D10     | 38911                             | ON  | ON  | ON  | OFF | 7 |
| -30     | 30 MEG | D11/D12 | <sup>5</sup><br><del>6</del> A023 | FLOPPY    | D10     | 1279                              | OFF | ON  | ON  | ON  | E |
| -60     | 30 MEG | D11/D12 | <sup>5</sup><br><del>6</del> A023 | 30 MEG    | D10/D13 | <sup>5</sup><br><del>6</del> A023 | OFF | OFF | ON  | OFF | 4 |
|         | 30 MEG | D11/D12 | 65023                             | 10 MEG    | D10     | 65023                             | OFF | ON  | ON  | OFF | 6 |

At this time the only manufacturer for 30 Meg drives that we are using is Quantum, model #5040, and this is the only 5 1/4" model we are using from them. This means if you have a 5 1/4" fixed drive and it is a Quantum, then it is a 30 Meg, and if it is not a Quantum, it is a 10 Meg.

ONLY 1ST <sup>WINC</sup> ~~SWITCH~~ TERMINATED (FIXED LEFT) D11 TERMINATE 726-1882  
 DS1 SELECTED ON BOTH WINCHESTER  
 FLOPPY IS DS1 + IS TERMINATED

★ 220-3324 DAISSY CHAIN CABLE NEEDED WHEN USING 2 Winc's. D11 IS 1<sup>ST</sup> DRIVE ON CABLE.  
 ALSO NEEDED CABLE FOR 2<sup>ND</sup> DRIVE - 220-3313. FIX: LIFT PIN 6 OF L127  
 210-7342 DUAL CONTROLLER PROBLEM - NEEDED 8396 B20, E-REV 6. TIE L118 PIN 1 TO L118 PIN 10  
 ADD 57 Ω RESISTOR FROM L118 PIN 10 TO GND  
 MAIL STOP: 0126

GROUP: Technical Assistance Center P.C. Group

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.



NEC D5124  
10-MEG 278-4030

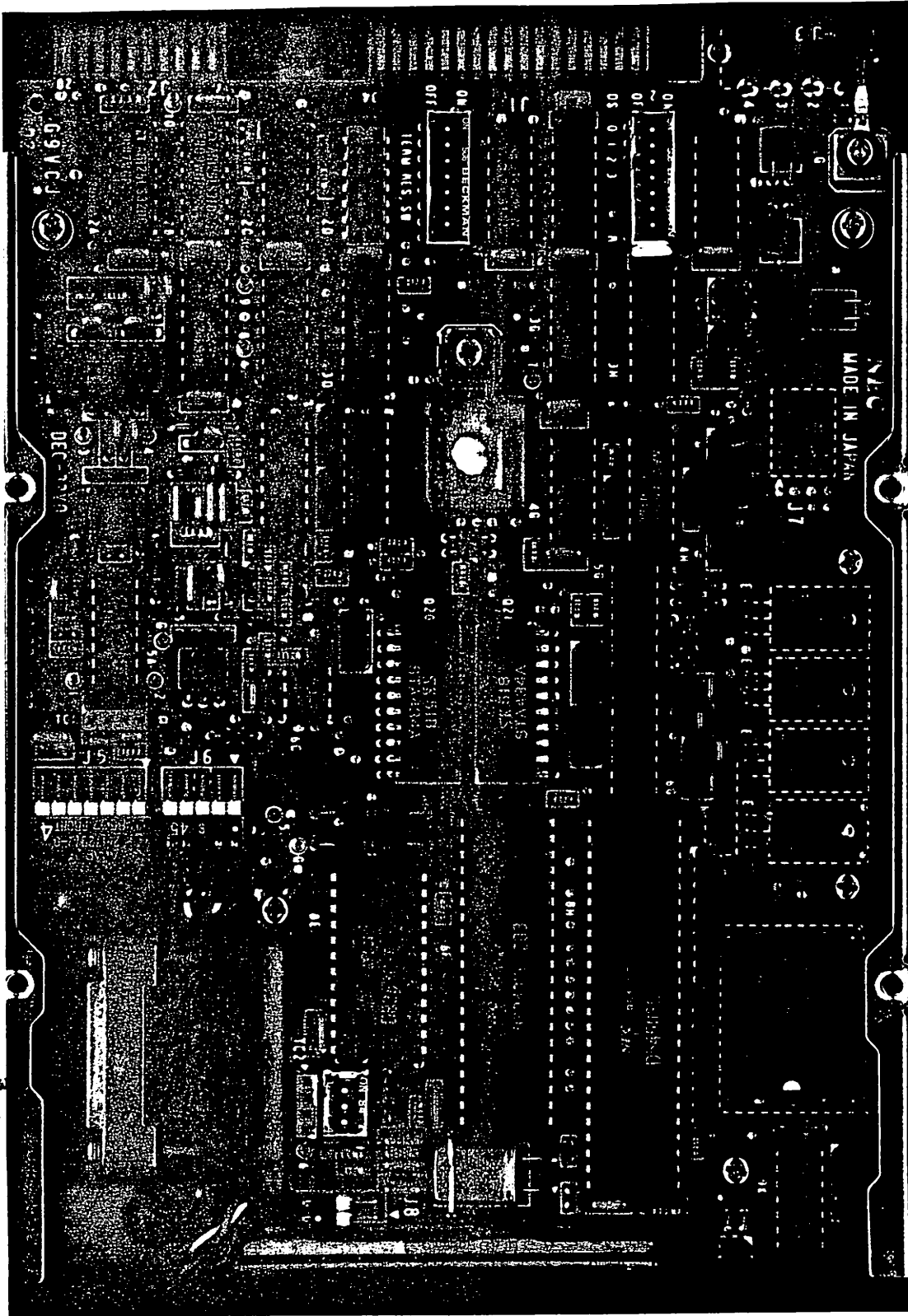
-2275-

DS0 = DS1 = SW 1 ON

NO JUMPERS  
ON THIS DRIVE

TERMINATION

DS0 1 2 3



4 BANKS  
A: →  
ALL ON

2275 PROBLEM UPDATE

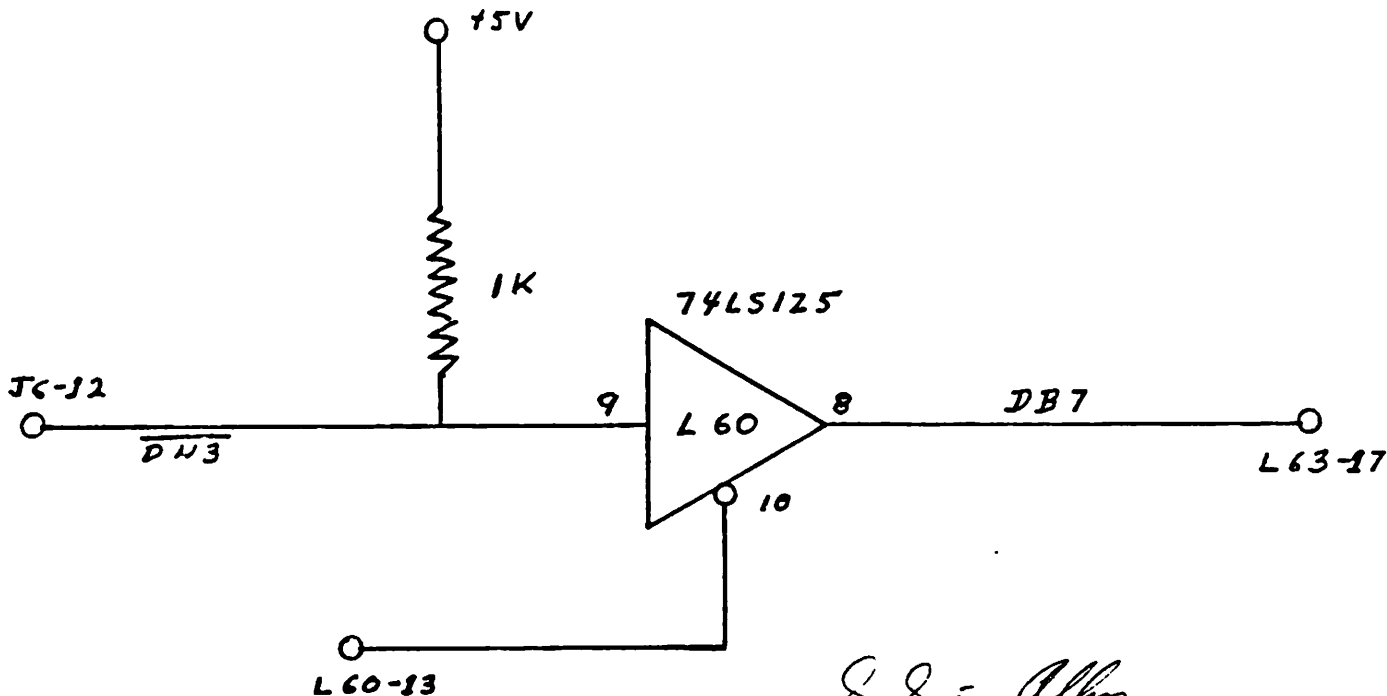
PROMS

PRE-RELEASE R-56 PROMS ARE BEING BETA TESTED. IF NO PROBLEMS ARE ENCOUNTERED, THESE PROMS WILL BE RELEASED AS R-3 PROMS.

210-8396A CIRCUIT BOARD

A CIRCUIT REVISION TO THIS BOARD HAS BEEN COMPLETED. (AN ECO NUMBER HAS NOT BEEN ASSIGNED AS OF THIS TIME). THE CHANGE USES THE HIGH ORDER 40 ADDRESS BIT FROM THE CONTROLLER (NOT DN3), (0100 0000), AND PUTS IT ON THE DATA BUS (DB-7) FOR INTERROGATION BY THE MICROCODE. THIS ALLOWS THE 2275 TO DISCRIMINATE BETWEEN ADDRESSES 10 AND 50, 20 AND 60, 30 AND 70. PREVIOUSLY A 2275 WITH AN ADDRESS OF 20 WOULD RESPOND INCORRECTLY TO AN ADDRESS OF 60.

DIAGRAM BELOW IS CHANGE TO THE 8396A BOARD. IT SHOULD BE NOTED THAT THE MICROCODE MUST BE AT REV 3 FOR THIS CHANGE TO BE EFFECTIVE.



*Skip Allen*  
-----  
SKIP ALLEN, 2200/VS/PC  
TECHNICAL ASSISTANCE CENTER

2275 Disk Unit

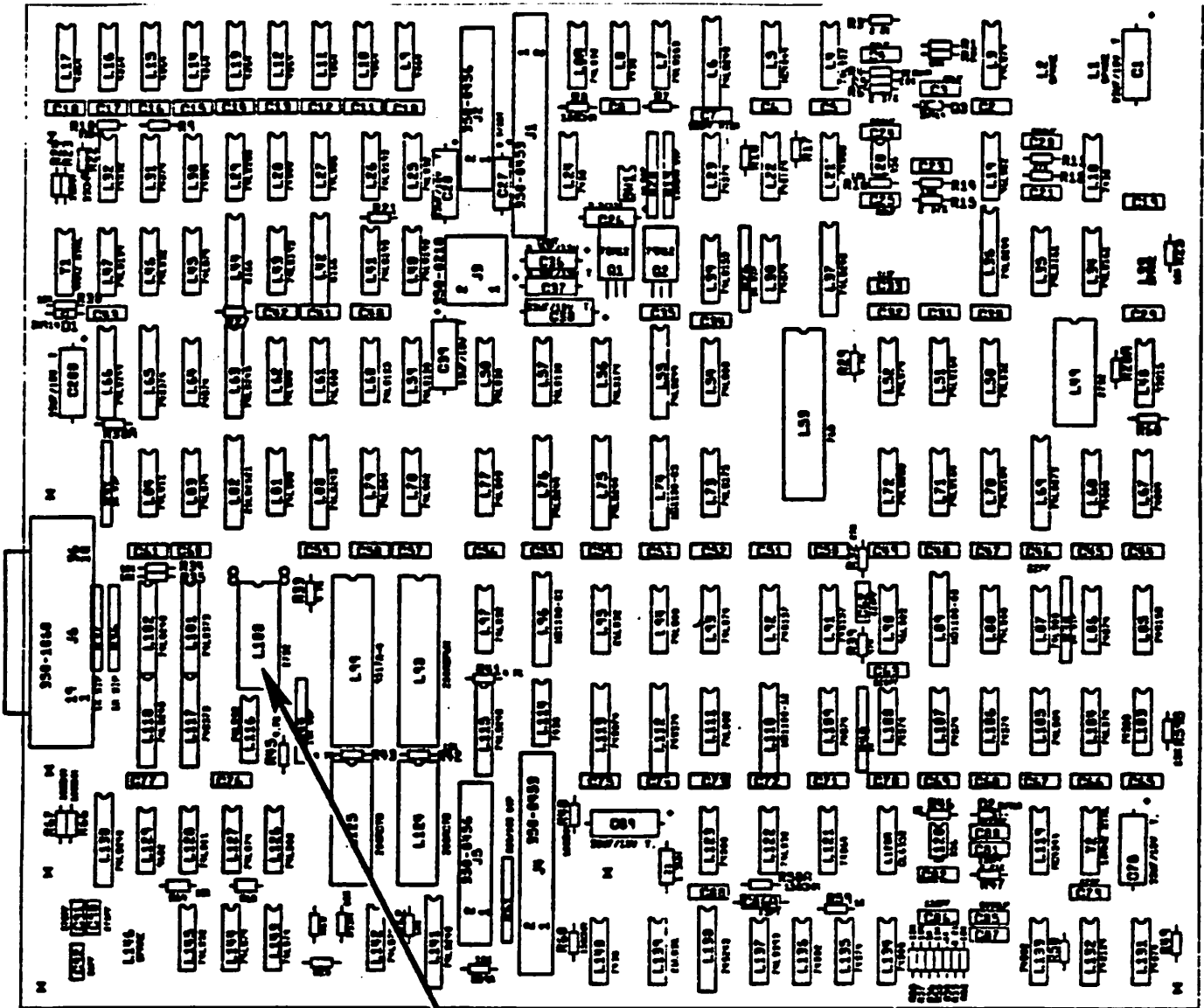
R2 Prom

The R2 Prom is available and should correct some of the hanging problems as well as D81 and D88 errors. If experiencing these problems order the prom by the FC0 kit. The ECO number is 33512. The prom is located at L100 of the 210-8396A board.

FC0 Kit 1111  
Prom

728-0129  
379-2000 R2

An R3 Prom is expected in the near future.



CHANGE EPROM AT L100  
TO 379-2000-R2



TECHNICAL SERVICE BULLETIN  
SECTION: HardWare Technical

NUMBER: HWT 7243 REPLACES: \_\_\_\_\_ DATE: 11/10/87 PAGE 1 OF 1  
MATRIX ID. 3110 PRODUCT/RELEASE# 2275  
TITLE: FCO 1207A, 2275

PURPOSE:

To inform the field that FCO 1207A has been released, documenting ECO 45575.

EXPLANATION:

This FCO voids FCO 1207. Originally, it documented ECO# 40541 which changed an EPROM. In addition, FCO 1175A and FCO 1210 had to be done in conjunction with this change.

With the release of ECO# 45575, the rework now required to fully upgrade the 210-8396 PCB is considered to be excessive for field installation. In the future, if problems referenced in Section 10 are encountered, the 210-8396 should be sent to your local Field Repair Center (FSC) for rework.

NUMBER: HWT 7242 REPLACES: \_\_\_\_\_ DATE: 11/10/87 PAGE 1 OF 1  
MATRIX ID. 3110 PRODUCT/RELEASE# 2275  
TITLE: FCO 1175B, 2275

PURPOSE:

To inform the field that FCO 1175B has been released, documenting ECO 45575.

EXPLANATION:

This FCO voids FCO 1175A. Originally, it documented ECO# 36892 which modified certain sections of circuitry and incremented the E-Rev to 3. In addition, FCO 1207 and FCO 1210 had to be done in conjunction with this change.

With the release of ECO# 45575, the rework now required to fully upgrade the 210-8396 PCB is considered to be excessive for field installation. In the future, if problems referenced in Section 10 are encountered, the 210-8396 should be sent to your local Field Repair Center (FSC) for rework.

TECHNICAL SERVICE BULLETIN  
SECTION: HardWare Technical

NUMBER: HWT 7244 REPLACES: \_\_\_\_\_ DATE: 11/10/87 PAGE 1 OF 1  
MATRIX ID. 3110 PRODUCT/RELEASE# 2275  
TITLE: FCO 1210A, 2275

PURPOSE:

To inform the field that FCO 1210A has been released, documenting ECO 45575.

EXPLANATION:

This FCO voids FCO 1210. Originally, it documented ECO# 39995 which modified certain sections of circuitry and incremented the E-Rev to 4. In addition, FCO 1175A and FCO 1207 had to be done in conjunction with this change.

With the release of ECO# 45575, the rework now required to fully upgrade the 210-8396 PCB is considered to be excessive for field installation. In the future, if problems referenced in Section 10 are encountered, the 210-8396 should be sent to your local Field Repair Center (FSC) for rework.

GROUP: ECO Group

MAIL STOP: 012-18B

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.

5 1/4" PANASONIC FLOPPY

WANG

TECHNICAL SERVICE BULLETIN  
SECTION: HardWare Technical

NUMBER: HWT 6193 REPLACES: \_\_\_\_\_ DATE: 12/02/86 PAGE 1 OF 1

MATRIX ID. 3101 PRODUCT/RELEASE# SA 455 (VLSI) WLN 278-4033

TITLE: DESCRIPTION OF THE TEST POINTS ON VLSI BOARD

## PURPOSE:

To inform the field of test point functionality.

## EXPLANATION:

The VLSI board on the Half High floppy (WLN 278-4033) uses different test points from the regular TTL board. The following information is needed to verify drive alignments when using an oscilloscope.

Description of the Test Points

|              |   |                                      |
|--------------|---|--------------------------------------|
| TP 1 and 2   | : | Differential analog read data signal |
| TP 7 (wire)  | : | Index                                |
| TP 8         | : | Track Zero                           |
| TP 12 (wire) | : | Step                                 |
| TP 6 (wire)  | : | Digital read data                    |
| TP 5, 10     | : | Ground                               |

Index is located at connector J1 pin #8.

Step is located at connector J1 pin #20.

GROUP: Desktop Systems/Peripherals Group MAIL STOP: 001-250

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.

5 1/4" PANASONIC FLOPPY



TECHNICAL SERVICE BULLETIN  
SECTION: HardWare Technical

NUMBER: HWT 6192 REPLACES: N/A DATE: 08/19/86 PAGE 1 OF 1  
MATRIX ID. 3101 PRODUCT/RELEASE# SA 455 (VLSI)  
TITLE: Jumper Configuration

PURPOSE:

To inform the field of the jumper configuration for the SA 455 with the VLSI board.

EXPLANATION:

The Panasonic floppy drive (Wang Part No. 278-4033) using the VLSI board uses the following jumpers. A drive configured with these options will work on the Wang Office Assistant, PC, 2275, PIC, and OIS 50/60.

| PLUG JUMPER | DESCRIPTION                            | OPEN | SHORT |
|-------------|--|------|-------|
| DS1         | DRIVE SELECT 1                         |      | X     |
| DS2,3,4     | DRIVE SELECT 2,3,4                     | X    |       |
| WP          | WRITE PROTECT                          |      | X     |
| MM          | ENABLES DRIVE MOTOR WITH MOTOR ON      |      | X     |
| DS          | ENABLES DRIVE SELECT IN A MULTI SYSTEM |      | X     |
| MX          | CONSTAN DR SELECT FOR SINGLE DR        | X    |       |
| MS          | ENABLES DR MOTOR WITH DRIVE SELECT     | X    |       |
| DR          | ENABLES DR READY WITH DR SELECT        | X    |       |
| RR          | READY ENABLE FROM +READY OR SW         |      | X     |
| SW          | DOOR SWITCH                            |      | X     |
| RD          | ENABLES TRUE READY                     | X    |       |
| RY          | READY SIGNAL                           |      | X     |

Termination for each input line is accommodated by a 150 OHM resistor pack installed in dip socket located on the logic board.

The hardwired jumpers configuration of this board should not be modified.

GROUP: Peripheral Hardware Support Group MAIL STOP: 0125

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.

TECHNICAL SERVICE BULLETIN  
SECTION: HARDWARE TECHNICAL

NUMBER: HWT6257      REPLACES: N/A      DATE: OCT 20/86      PAGE 1 OF 1  
MATRIX ID. 3107      PRODUCT RELEASE# 2275  
TITLE: PCB 210-8396 REV. 4 GIVING I-92 ERROR

Purpose:

To inform the field on the model 2275 giving I-92 error running customer applications.

Explanation:

In the last 16 weeks manufacturing built the 210-8396 Rev. 4 with the wrong memory chips at locations L9, L10, L11, L12, L13, L14, L15, L16 and L17. The wrong memory chips are from Siemens - SHY B4164 / P2 LF and are out of specifications.

Boards with these memory chips are causing I-92 errors. The correct WLN for the memory chips is 377-0466.

Boards with the incorrect memory chips can be corrected in the field by replacing the Siemens memory chips.

Manufacturing processed a Purge Notice to correct their stock. CE Logistics and Repair Centers were notified of this problem and will correct boards as they are returned.



**WANG**

TECHNICAL SERVICE BULLETIN  
SECTION: HardWare Technical

NUMBER: HWT 5033 REPLACES: N/A DATE: 02/26/85 PAGE 01 OF 01  
MATRIX ID. 3110 PRODUCT/RELEASE# 2275  
TITLE: 2275 Problems

PURPOSE:

To inform the field of the problems that have been identified and will be resolved on the 2275.

1. The '40' bit of the drive address is not checked. The 2275 responds to 350 as if it were 310, 360 as if 320, and 370 as if 330.
2. The \$GIO "read PROM Rev. level" command does not work.
3. The non-sequential multi-sector write problem is from an incomplete implementation of multi-sector write as implemented in the Phoenix and the SVP/LVP.
4. The head alignment routine requires changes to the read routine.
5. The power-up diagnostic does not flag floppy drive stepper motor failures.
6. Formatting a drive does not reset the read/write caches.  
NOTE: Notify all customers to use the reset key in the keyboard after formatting the drive as a circumvention.
7. In the Winchester back-up subroutine the 2275 does not recognize unformatted diskette and hangs the operation.  
NOTE: Notify all customers to use formatted diskettes only as a circumvention.
8. The diagnostic gets lost if it gets an error on the Winchester.

All these problems will be corrected in the R3 PROM. Estimated completion date for the PROM is the end of April.

GROUP: Peripheral Hardware Support Group MAIL STOP: 0125

COMPANY CONFIDENTIAL

WANG Laboratories, Inc.

CUSTOMER ENGINEERING  
TECHNICAL ASSISTANCE CENTER  
NEWSLETTER

#40724

3110

PERIPHERALS-DISK DRIVES-5 1/4 DISK DRIVES

TOPIC: FCO 1100

FCO 1100, which has the new R1 PROM for the model 2275-10 and 2275-20, will be replaced by FCO 1107 due to D81 and D88 errors. R&D is planning to release the R2 PROM by the end of this month. The R2 PROM will take care of the D81 and D88 errors. Sixty R2 pre-release PROMS will be distributed to the Domestic Areas and ten to Europe for Beta site support on July 18. FCO 1107 will be available in August.

#40<sup>703</sup>~~724~~

3110

PERIPHERALS-DISK DRIVES-5 1/4 DISK DRIVE

TOPIC: FCO 1100, 2275-10, 20, 30 DISK PERIPHERAL

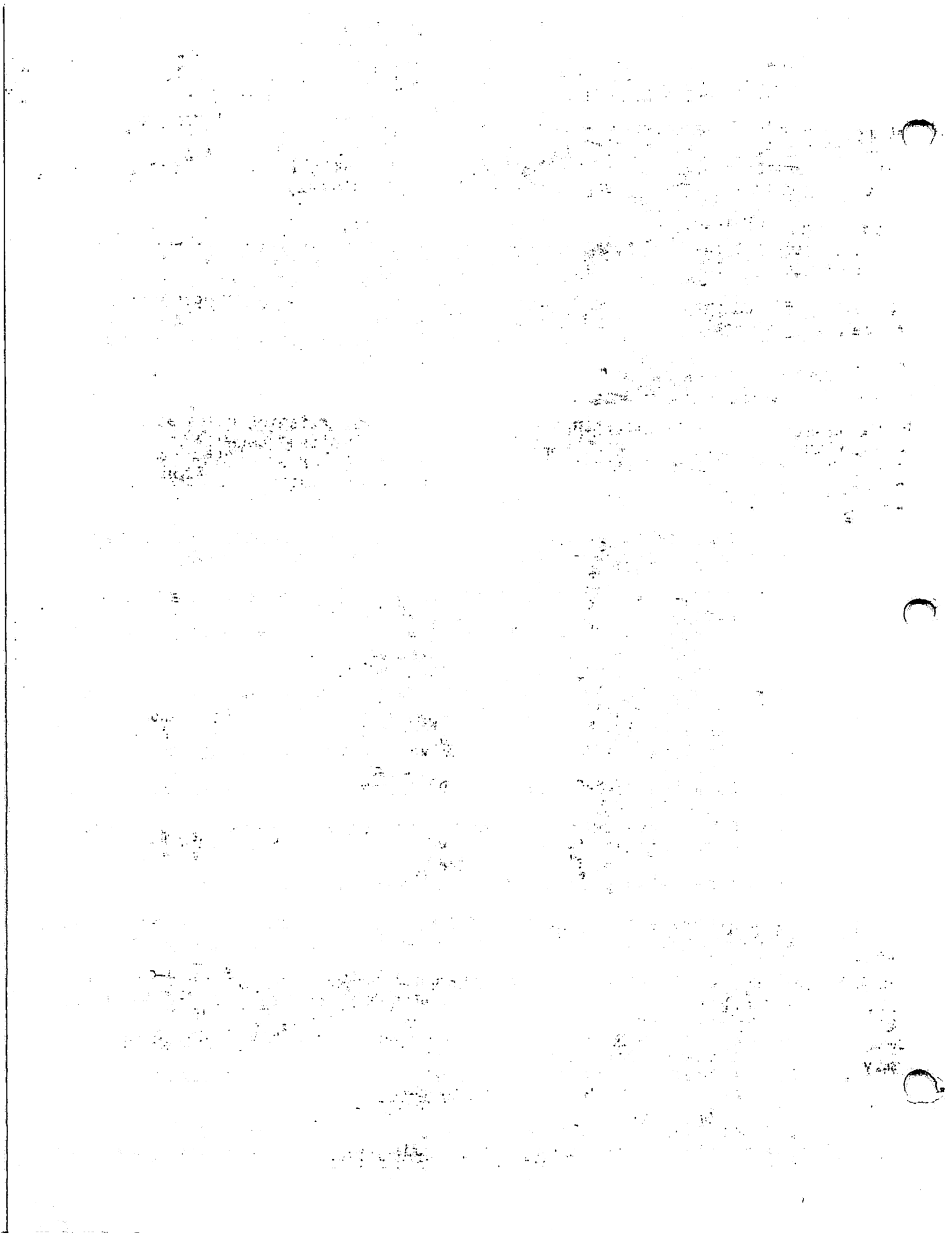
FCO 1100, released June 20, 1984, documents ECO 32608. A PROM change on the 210-8396-A PCA corrects the following known bugs:

- 1) System hangs when 210-8396-A PCA is powered up with no floppy diskette in the drive.
- 2) System hangs when a LIST DT command is issued when there is no media in the drive.
- 3) Alternate sector mapping does not work.
- 4) Winchester hardware is not disabled when the Z80 attempts to access the alternate sector map, creating a memory contention.
- 5) Parity error hangs the system without returning an error message.
- 6) Cacheing problem causes invalid data to be returned to the the 2200.
- 7) System status message does not properly identify the system configuration.

The change also provides the following enhancements:

- 1) Firmware now supports 30 Megabyte Quantum Winchester drive.
- 2) PC diskettes can be read, written, and formatted by the 2275.
- 3) Winchester format is now a one pass operation that writes DB6, B6D, 6DB pattern onto the disk to help locate marginal sectors.
- 4) A hook is provided so that CE can perform radial track and index-to-data head alignment.
- 5) A hook is provided to allow CE to read the alternate sector map.

FCO Kit #728-0118 will be available July 2, 1984. To obtain it, place a routine order through the Logistics Order Processing System.



# ANNOUNCING THE NEW FAMILY OF 2200 SMALL BUSINESS COMPUTER SYSTEMS

Hang Laboratories is pleased to announce a new series of 2200 system packages including the latest in 5 1/4" disk storage technology. Combined with aggressive pricing and increased flexibility in hardware configurations, the 2200 family sets a tough, new standard in price/performance.

This announcement fulfills the promise made by John Cunningham in his November 15, 1982 statement on 2200 product line direction, to offer a complete 2200 system for under \$12,000 U.S. list.

The family of 2200 products now includes three new MVP packaged configurations as well as a standalone 5 1/4" disk storage peripheral.

## New 2200 System Configurations

These packaged configurations are aimed at new customers, existing users as add-on equipment and large corporations buying multiple units. Because of their low entry price and expandability, they are viable as a competitor against a wide range of low-end minicomputers, personal computers and other high-end micros.

- MVP-P1 . MVP Processor with 8 Available I/O Slots
  - 64KB Memory
  - 22C32 Triple Controller
  - 5 1/4" Disk Storage Device with 10MB Fixed Storage and 320KB Removable Floppy Drive
  
- MVP-P2 . MVP Processor with 8 Available I/O Slots
  - 128KB Memory
  - 22C32 Triple Controller
  - 5 1/4" Disk Storage Device with 10MB Fixed Storage and 320KB Removable Floppy Drive
  
- MVP-P3 . MVP Processor with 8 Available I/O Slots
  - 256KB Memory
  - 22C32 Triple Controller
  - 5 1/4" Disk Storage Device with 10MB Fixed Storage and 320KB Removable Floppy Drive

## New 5 1/4" Disk Storage Technology

This 5 1/4" unit is a new 2200 peripheral aimed at existing users as add-on equipment as well as a component of the three new MVP packages outlined above. The unit can be used as an add-on to VP, LVP, LVPC, MVP and MVPC systems. When configured as an add-on, a 22C03, 22C11, or a 22C32 Controller may be used.

- 2275-10 . 10MB 5 1/4" Winchester drive
  - 320KB Floppy Drive
  
- 2275-20 . Dual 10MB 5 1/4" Winchester drives

## 2275 IPL PROBLEMS

---

WHEN POWERING UP THE 2275 IT WILL START INTERNAL DIAGNOSTICS. IF THE WORKSTATION RESET KEY IS PRESSED DURING THIS TIME, THE LIGHT ON THE WINCHESTER WILL GO OUT AND A RANDOM ERROR MAY OCCUR. ERRORS D85, 195 OR LIGHTS FLASHING ON THE FLOPPY AND WINCHESTER ARE COMMON. TO PREVENT THIS FROM HAPPENING, WAIT UNTIL THE WINCHESTER LIGHT IS EXTINGUISHED BEFORE PRESSING THE RESET KEY.

REGARDS,

SKIP

0/31/85

MEMORANDUM

WANG

TO : Joe Scaglione MS/001-260  
FROM : Harvey A. Worthington *HW*  
SUBJECT: Floppy Media For the 2275 (WPN 177-0080)  
DATE : April 15, 1987

---

PROBLEM- Field escalated the inability to format new diskettes from Wang Direct on the Wang model 2275.

The diskettes that you gave me are from Sentinel. This vendor by mistake shipped approximately 20000 diskettes (2000 boxes) to the supply division. Wang Direct has none of these left in stock at this time. This vendor error was corrected and new procedures have been implemented at Wang Direct to include a verification of erasure at incoming.

The reason why the 2275 failed to format the diskettes is that the media was tested by the vendor, at the end of the test the vendor had all one's pattern on all tracks on both sides. Usually after this test we force the vendor to degauss the media.

Recommendations-

1. The 2275 should format any 177-0080 diskette without problems with left over data, different format or testing information. In order to prevent future media problems I recommend to have the Software group in R&D verify their format routine and see if they can correct this difficulty.
2. You can recommend the field to use another Wang System (i.e. PC), once you format the diskettes they will be able to format the diskettes in the 2275.

cc. Robert Beaudette MS/014-490  
Ray Peltzman MS/001-140  
Kim Thompson MS/001-140

TAC

CUSTOMER ALERT

CONTROL NUMBER 05275031

CONTACT NAME RAY BERRY POSITION CE  
RDB # 3523 TDX # PHONE # 919 665 8930 EXT #

SYSTEM TYPE 2200MVP DEVICE TYPE 2275-10  
UTILITY NAME SOFTWARE LEVEL

METHOD OF CALL P T = TELEX, P = PHONE, M = MEMO, E = EMS  
HAS THE AREA OR DISTRICT BEEN CONTACTED  
N A = AREA, D = DISTRICT, B = BOTH, N = NONE  
IS THIS INQUIRY PERTAINING TO A NATIONAL ACCOUNT ?  
U Y = YES, N = NO, U = UNKNOWN

USE THE FOLLOWING AREA TO DESCRIBE THE SITE THAT CREATED THIS REQUEST  
CUST/OFFICE NAME PHONE #  
ADDRESS 3D CITY STATE  
ON SITE CONTACT NAME

PROBLEM (\*) SOLUTION (+)

\*\*ON BOOT IN THE MORNING THEY GET AN ERROR "D85" WHEN IT  
\*TRIES TO DO THE BOOT CUSTOMER RECYCLES POWER TO THE  
\*2275 UNIT AND IT WORKS BUT ON A FIRST TRY EVERY  
\*MORNING IT GIVE THE ERROR MESSAGE D85  
\*HAS REPLACED ALL POSSIBLE PROBLEM PARTS  
10/02/85:

I CALLED THE CR:D-85 IS CATALOG INDEX FULL-THERE IS  
NO MORE ROOM IN THE CATALOG INDEX FOR A NEW NAME.  
FIX IS TO SCRATCH ANY UNWANTED FILES AND COMPRESS  
THE CATALOG USING A MOVE STATEMENT,OR MOUNT A NEW  
PLATTER AND CREATE A NEW CATALOG.THE SYSTEM MUST BE  
POWERED DOWN TWICE IN THE MORNING AND THEN IT LOADS  
CORRECTLY.THE CE WILL ORDER EOM 1111A THE NEW REV 3  
PROM FOR THE 2275 DISK BOARD.THE SYSTEM IS UNIQUE IN  
THE CES TERRITORY,IN AS MUCH AS IT IS THE ONLY 2200  
THAT COMES UP OFF THE 2275 FOR THE OPERATING SYSTEM.  
2.6.2.

WJ.

10/02/85:

I GAVE THE CE THE FOLLOWING TWO FCO PART #S:  
(728-0129A) FOR A 379-2000: REV-3 PROM ON THE 2275  
DISK BD.AND A (722-0191) A WIRE CHANGE ON THE 2275.

WJ.

NEW 2275 FCO 1111A

TAC

INFORMATION CALL

CONTROL NUMBER P7069001

CONTACT NAME BENNETT CHL POSITION  
RCB # 9508 TDX # PHONE # 111 111 1111 EXT # 25

SYSTEM TYPE 2200 DEVICE TYPE 2275  
UTILITY NAME SOFTWARE LEVEL

METHOD OF CALL P T = TELEX, P = PHONE, M = MEMO, E = EMS  
HAS THE AREA OR DISTRICT BEEN CONTACTED  
N A = AREA, D = DISTRICT, B = BOTH, N = NONE  
IS THIS INQUIRY PERTAINING TO A NATIONAL ACCOUNT ?  
L Y = YES, N = NO, L = UNKNOWN

USE THE FOLLOWING AREA TO DESCRIBE THE SITE THAT CREATED THIS REQUEST  
CUST/OFFICE NAME TAIWAN CSC PHONE #  
ADDRESS (3DIG) CITY TAIWAN STATE 05  
ON SITE CONTACT NAME 3 ESCALATED TO TSO

QUESTION (\*) / ANSWER (+)

\*SYS CONFIG: IPC, 30MB DRIVE (278-4069)  
\*S/W: NIL  
\*THE NEW 30MB DRIVE (278-4069) IS USED WITH IPC WITHOUT ANY  
\*PROBLEM. PLS ADVISE IF IT CAN BE USED ON 2275 TO REPLACE  
\*THE OLD QUANTUM DRIVE (278-4024) AS PROBLEM OCCURED, OR  
\*ANY NECESSARY MODIFICATION IN F/W OR S/W REQUIRED.  
1F/09MAR87: ACK TLX SENT TO TAIWAN. RCVD PHONE CALL FROM  
L.S. SUN TO REQUEST INFO ON DRIVES.  
AREA ASSIGNED CONTROL NO. IS P7069001.  
SPECIALIST ASSIGNED CALL IS PETER WONG. (KYW)  
2F/10MAR87: INITIAL TACNET TO H.C. FOR ASSISTANCE:-  
& PLS ADVISE WHETHER THE 30MB MICROPCDIS DISK  
& DRIVE CAN REPLACE THE QUANTUM DRIVE IN 2275  
& OR NOT. (PETER)  
3F/12/87: THE 30 MEG MICROPCDIS DISK DRIVE IS NOT COMPATIBLE  
& WITH THE 2200. WITH THE PC SW SETTINGS ARE CHANGED  
& TO IDENTIFY THE MICROPCDIS DRIVE. MUST USE THE  
& QUANTUM ON THE 2200. MIKEB  
& UPDATE CLEUED TO HOME OFFICE  
!!CALL SUCCESSFULLY SENT TO FIELD SYSTEM  
3F/13MAR87: THANKS FOR UPDATE. CALL CLOSED WITH H.C.  
\$ REPLY FAX TO TAIWAN CSC. (PETER)  
+CALL CLOSED /FIELD.

3/16/87

MIKEB



TAC

Information Call

Control Number 08322011

Contact Name KEVIN WRIGHT Position CE  
Rdb # 3429 Tdx # Phone # 302 322 3115 Ext #

System Type 2200 Device Type 2275-10  
Utility Name Software Level

Method of Call P T = Telex, P = Phone, M = Memo, E = Ems  
Has the Area or District been contacted  
N A = Area, D = District, B = Both, N = None  
Is this inquiry pertaining to a National Account ?  
U Y = Yes, N = No, U = Unknown

Use the following area to describe the site that created this request

Cust/Office Name Phone #  
Address 3D01 City State  
On Site Contact Name

Question (\*) / Answer (+)

\*EMP#23728

\*DSP#N/A DIGITAL BEEPER 800-802-2201

\*NEED INFO. ON THE POWER SUPPLY

\*ONSITE# 302-436-8688

11/16/88: REGULATOR PROB IT APPEARS. IF PLUGS ANYTHING INTO  
REGULATOR 5V GOES WAY DOWN. CE TO GET REG & 8396  
BRD. (10MIN) MIKEB

12/28/88: LEFT MESSAGE AT OFFICE TO CALL. (5MIN) MIKEB

1/17/89: LEFT MESSAGE W/ BM FOR CE TO CALL. (10MIN) MIKEB  
>WAYNE OSBORNE CALLED IN. WILL HAVE KEVIN CALL.  
(5MIN) MIKEB

+LOOSE WIRE TO BRIDGE RECTIFIER. CORRECTED & NO PROB SINCE.  
(5MIN) MIKEB

# REDSHAW®

Redshaw, Inc.  
Foster Plaza Ten  
680 Andersen Drive  
Pittsburgh, PA 15220  
412/937-3661

Gene Schulz  
Wang Laboratories  
One Industrial Avenue  
Lowell, Massachusetts 01851

November 15, 1989

Dear Gene:

There are indications of a problem with the current PROM update for Wang 2275 drives.

Redshaw has received reports from customer sites that upgrades to 2275-10/-30 drives are being installed with PROMs of revision level R5. This PROM is not operating properly, and has been causing compatibility problems at our customer sites. Redshaw has been substituting R3 or R4 level PROMs in place of the R5 chips provided by the Wang, and these (R3 and R4 PROMs) have been operating successfully.

From conversations with Mike Bahia, I understand that one of the changes implemented was a correction to eliminate bus contention during a request for drive status. Redshaw programs utilize the values provided from the drive status (as defined in the Wang technical documentation); should the R5 PROM revise the layout of the status values, Redshaw software could be negatively affected.

Could you please provide information on the R5 PROM, such as details on the changes that were made, what are the differences from the R4 PROM, exactly when was R5 made available to Redshaw customers, and can Wang supply Redshaw users with R3 or R4 PROMs until this issue is resolved? Since this is affecting the operational capability of our users' systems, Redshaw is considering this an urgent item.

Please feel free to contact me if you need any additional information or clarification.

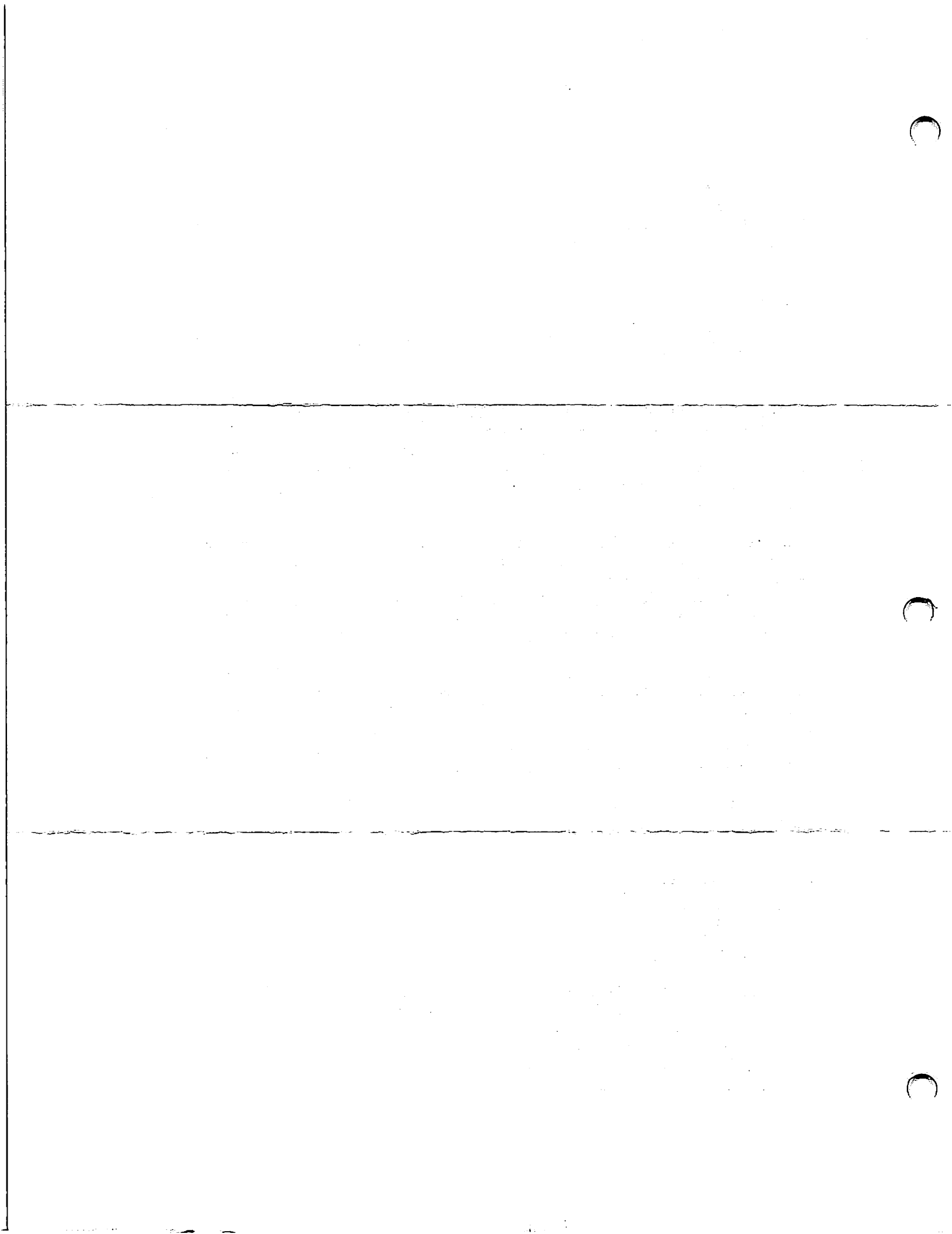
Sincerely yours,



Mark Guzan

cc: Gary Bromley - Redshaw  
John Deutsch - Redshaw  
Dorene Dinncenzo - Redshaw  
Joe Heuler - Redshaw  
Angie Nofsinger - Redshaw  
Jo Roberts - Redshaw

Mike Bahia - Wang ✓  
Mike Riley - Wang  
Ed Whitney - Wang



To:  
Subject: 2275 Rev 5

Distribution:

None, this item is In Progress

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To: Mike Bahia  
Subject: 2275 Rev 5

From: Eugene S. Schulz  
Date Sent: 11/15/89

Does any such animal exist? Redshaw called and asked.

----- Reply -----

Gene,

This has been the hot topic of the day. Yes there is a Rev 5 prom & it has been out for 2 years. Appears Redshaw is looking at some specific bytes in the prom code which probably were moved with the rev 5 prom. This appears to be the case from my conversation with Mark Guzan of Redshaw. Have given all related info to Ed Whitney, the Account Manager & Mike Riley. If you have further questions please let me know.

Regards,  
Mike

CC: Mike Bahia MS0126/LOWELL  
From: ED WHITNEY  
Subject: REDSHAW 2275 PROM ISSUE Date: 11/27/89

Distribution:

Not Requested

---

Gene,

I just received my copy of the letter that Mark Guzan sent you on Nov. 15th.. I would like to add some additional info that may be of some value to you, Mike Bahia, or Mike Riley.

The Prom in question is located on a 210-8396-A PCB ( Control Bd. ) in location L100. Redshaw escalated one customer situation to me on 11/14 for a client of theirs by the name of Fritz Baehr located in Broomfield Co.. It was discovered that the backup routine did not function after upgrading software. There is no error message, the screen prompt simply changes with no system activity having occurred. Redshaw ( Dorene Dinncenzo) told me that they had seen the same thing at two other accounts and it was corrected with the install of a REV 4 Prom. I was able to coordinate the shipment of one for Baehr and it did correct the problem there also.

I don't believe that our technical people nor Redshaw's have sufficient data to determine if it is a Wang or a Redshaw problem. I made an agreement with Redshaw last week to exchange a down rev board for a Rev 5 one in Pittsburgh so they could do some testing. I called Mark Guzan this morning to find out if he was still interested since no one had as of yet called me for it. This caught him by surprise, and I was able to make arrangements with him for the exchange of boards. He will have a Rev 5 board tomorrow morning.

It is essential that Wang follow through promptly and provide the detail Mark asked for in his memo on the what the change did for REV 5. I spoke with Bahia and he was not aware of any other customer reporting problems with the REV 5, and it has been out there for a long time. It looks like this is a Redshaw specific since no other VAR or regular commercial customer has reported the same problem.

The other thing I learned in seeking out a REV 4 board for Baehr is that very few exist in the field. In fact a two hour search of all major stocking locations in the Central and Western regions came up with only one board. This factor illustrates the urgency in which we need to respond.

Please call if you have any questions... 708-250-4635  
Regards, ED

# REDSHAW<sup>®</sup>

Redshaw, Inc.  
Foster Plaza Ten  
680 Andersen Drive  
Pittsburgh, PA 15220  
412/937-3661

X.C. Mike Rely  
Mike Baker

4 Return

RVI

Ed 2/23

Ed Whitney  
Wang Laboratories  
Suite 400  
300 Park Boulevard  
Itasca, Illinois 60143-2661

February 16, 1990

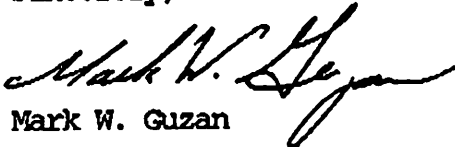
Dear Ed:

In response to your February 15 letter, this is the status of Redshaw's efforts with the 2275 R5 PROM. Redshaw has performed testing on the R5 PROM, specifically a "same level" update from our Release 8.5 to 8.5, and no problems occurred. Today, Redshaw is testing R5 operation for a Release 8.0 to 8.5 update, and a Release 8.0 backup.

We have performed technical testing on codes that the PROM returns in response to programmed status requests (\$GIO commands). The PROM has responded correctly (provided PROM level and drive type) to this command.

Based on the results of today's tests, Redshaw Customer Support will certify if agencies with Redshaw Release 8.5 software updates can proceed, even with the R5 PROM installed. In the meantime, Redshaw will provide a test utility to help agencies determine their 2275 PROM level.

Sincerely,

  
Mark W. Guzan

cc: Gary Bromley  
John Deutsch  
Dot Foote  
Joe Heuler  
Judy Miller  
Jo Roberts